PROCEEDINGS OF SCIENCE

Irradiations on DEPFET-like test structures

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For the upgrade of the Belle detector at KEK DEPFET pixels (Depleted p-channel field effect transistor) are foreseen for the two innermost layers of the vertex detector. As a MOS device, the DEPFET is susceptible to ionizing radiation, which will be created near the interaction point. Ionizing radiation damages the silicon dioxide and alters the operating characteristics of the transistor. The DEPFET exhibits two gate contacts (gate and clear gate) and the final sensor may have a relatively complex pixel layout. In this layout several potential configurations for the clear gate contact exist. As the radiation damage depends not only on the dose, but also on the electric field in the gate oxide, several test structures, which correspond to different clear gate designs, have been irradiated with x-rays.
This paper presents measurements and results from irradiation campaigns and show the influence of a variable silicon nitride layer deposited on top of the silicon dioxide.

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1. Introduction

The planned upgrade of the Belle detector at KEK, Japan will have to cope with several requirements. One issue is the higher luminosity in the detector, another the required vertex tracking performance, resulting in high granularity tracking detectors. In order to achieve high vertex resolution, the detectors should be placed as close as possible to the beam pipe. To prevent multiple scattering, the sensors should be made very thin and still have a good signal-to-noise ratio. In order to reduce multiple scattering further, one would also like to have a low heat dissipation from the detector. This allows to avoid extensive cooling equipment for the sensors, which would add to the radiation length, thereby reducing the benefit from thin sensors.
Given the above requirements, the two innermost layers of the vertex detector of the Belle II experiment [1] will consist of DEPFET pixels (Depleted p-channel field effect transistor, explanation in section 2). They will have a total thickness of 75 μm of silicon in the sensitive area and can be cooled via end flanges and air stream.
The planned SuperKEKB accelerator provides e^+/e^- collisions. Although NIEL (non-ionizing energy loss) damage is expected from these collisions and from several background processes, this will not be covered in this paper.
Another important issue is the damage resulting from ionizing radiation. Although the dose rate is still not precisely known, an exposure rate of few $\frac{Mrad}{yr}$ has to be taken into account. Ionizing radiation changes transistor characteristics (see section 3 for details) and this effect needs to be known prior to the experiment and production of the final detectors.
As the electric field along the gate oxide has a major impact, a pixel layout with relevant voltages is presented in section 4.1.Then, according to these relevant voltages, several measurements (see section 5) have been conducted with special test structures. These have been irradiated with x-rays and analyzed.

2. DEPFET

The DEPFET is a semiconductor radiation detector, and was first published in [2]. The detector consists in principle of two MOSFETs, a schematic of this device is shown in figure 1. Via the backside implantation the device can be fully depleted. The n doping directly below the channel, together with an appropriate backside voltage, creates a potential minimum for electrons.
The charge created by a traversing particle is divided. Holes drift to the negative backside contact, whereas electrons drift to the internal gate. The charge stored in this internal gate increases the source-drain current I_{DS}. The drain current is then read-out, leaving the stored charge unchanged.
To be sensitive for further measurements, the charge has to be removed. This is done via the second MOSFET by applying a positive voltage on the clear contact. A punch-through to the internal gate is established and the stored charge moves to the clear contact. The drain current is then read-out again, taking the difference of the two measurements as a signal equivalent quantity. This read-out process, *sample-clear-sample*, is known as correlated double sampling (CDS).
However, timing requirements in Belle II are tight (measuring time for CDS $t_{CDS} \approx 120\ ns$ [3]), so that the process had to be adapted slightly. Instead of CDS a single sampling (*sample-clear*) is

performed, subtracting cached values of the pedestal current digitally.
As the clear contact itself is highly n-doped a barrier is needed to prevent electron movement to this contact or, depending on the voltage, avoid back injection of electrons from the clear contact into the bulk. This is done via the clear gate and a deep p-doping.
Further explanations of this device can be found e. g. in [4].

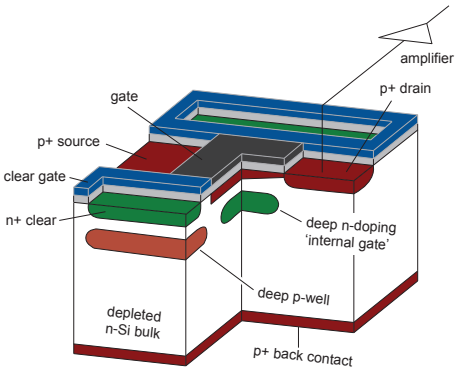

Figure 1: Schematic view of a DEPFET pixel. Electrons generated from ionization travel to the internal gate, whereas holes are removed via the back contact.

3. Ionizing radiation damage

As a MOS device the DEPFET is susceptible to ionizing radiation. Two important defect types are located in the silicon dioxide of the device in correspondence of the gate structures. These are trapped oxide charges and interface traps. Interface traps create basically additional noise for the detector, whereas trapped oxide charges changes the operation point of the transistor. Since a proper operation point is crucial for the operation of the DEPFET and therefore for the Belle II experiment, trapped oxide charges will be briefly explained. A comprehensive overview about radiation damage in MOS devices is given in [5].

3.1 Trapped oxide charge

At the interface between silicon and silicon dioxide, the chemical bindings between these two materials are stressed. Ionizing radiation creates electron/hole pairs in the silicon dioxide. Due to their high mobility, electrons are swiftly swept out of the oxide in the order of *ps*. Holes, however, exhibit a much lower mobility and are likely to get trapped at the interface. This happens at oxygen vacancies where a binding between two SiO_2 tetrahedrons is formed from one silicon atom to another.
These oxygen vacancies occur mostly at the interface between SiO_2 and Si. The two different materials lead to a narrow sheet of crystal defects, making this region attractive for diffusing charge carriers, especially for holes with their low mobility.
The trapped oxide charge is located directly at the interface, hereby shifting the control voltage of

the gate (with an oxide capacitance of C_{ox}) by

$$V_{shift} = \frac{\Delta Q_{ox}}{C_{ox}}, \tag{3.1}$$

which leads to a shift of the threshold voltage V_{th} of the same amount and opposite sign.

3.2 Influence of Gate Voltage on Radiation Damage

The amount of trapped charge depends not only on the dose, but also on the electric field within the gate oxide. Depending on the particle, a more or less dense column of electron/hole pairs are formed along the trajectory of the traversing particle.
If there is no electric field present in the gate oxide, recombination of a vast amount of the created charge is possible. Therefore only a small number of holes remain in the oxide, which can then be trapped.
The scenario changes in the presence of an electric field. This hinders recombination, increases therefore the charge yield of holes and electrons by separating them. Thereby leading to a higher shift in the threshold voltage. The highest threshold shift is achieved, if there is a positive voltage at the gate contact. Not only recombination is suppressed, but in addition the created holes are forced to the trap precursors which are located at the Si/SiO_2 interface.
A detailed explanation can be found in [6].

4. Pixel Layout and Voltage Dependencies

4.1 Pixel Layout

Figure 2 shows a schematic pixel layout of four DEPFETs. The internal gate is located between source and drain; it is realized by the *n* implantation below the channel (not visible in figure 2; the internal gate is positioned below the external Gate). Also depicted are the typical voltages during operation. As mentioned in section 2 the DEPFET has two gates which need to be adjusted for the voltage shift due to radiation damage. These are the normal (external) gate and the clear gate.
The clear gate is more critical, because it has a large cross section to the drift region. A potential difference of 5.5 V is established by the typical voltage $V_{ClearGate} = -2.5\ V$ and $V_{Drift} = -8\ V$.
As explained in section 3.2 a higher positive potential leads to more trapped oxide charge. Therefore, we expect at this region a higher threshold voltage shift than e. g. at the region from clear gate to source or clear gate to drain.
This could lead to lowering of the barrier between clear and clear gate (see also section 2) thereby emitting electrons from the clear contact into the bulk region. These electrons would then drift to the internal gate and would be treated as signal electrons or in the worst case flood the internal gate.
The pixel detector for the Belle II experiment will be divided in sectors along the beam pipe axis. Since only one clear gate voltage for a whole DEPFET sector will be available, we need to know the response of our devices to ionizing radiation with the voltage at gate contacts as a parameter.
It is planned to adapt the clear gate voltage to the shift due to trapped charge in the insulator, ensuring a continued normal operation. However, different amount of trapped charge in one pixel (at

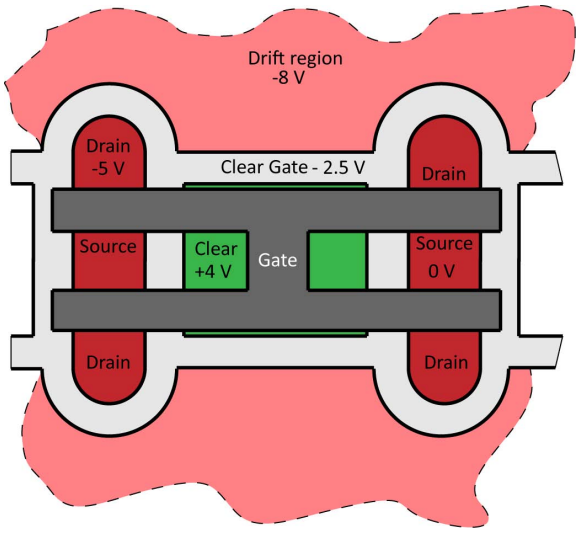

Figure 2: Potential pixel layout of four DEPFETs. As the typical pixel size is larger than a DEPFET structure, the pixel area is realized by an additional drift region surrounding the DEPFET. Gate voltages vary between $+2\ V$ for the off-state and $-3\ V$ for the on-state. The critical region is between the clear gate to the drift area.

the different clear gate cross sections) makes it difficult to find a common operation point.

4.2 DEPFET-like test devices

In order to have a large variety of parameters, special test structures have been developed and produced. Each structure consists of 14 MOSFETs with a gate controlled diode or a MOS capacitor. All the structures have the same oxide thickness and a variable silicon nitride (Si_3N_4) thickness deposited on top. The transistors have different gate lengths and the dopings are similar to the ones used in a DEPFET clear gate.

4.3 Silicon nitride

Silicon nitride is typically deposited above the oxide. Besides its property as a diffusion barrier [7], it has the advantage that metal-nitride-oxide-semiconductor (MNOS) structures are more radiation tolerant than ordinary MOS devices ([8], [9]). By varying the nitride layer thickness it should be possible to achieve a layer structure where holes are trapped in the oxide and electrons are trapped in Si_3N_4, resulting in a minimal net charge. In [10] a minimal shift of the mid gap voltage V_{mg} of $-2.5\ V$ could be achieved between the two different gate voltages of $+6\ V$ and $-6\ V$ with a nitride layer thickness of 20 nm and a dose of 1 $Mrad$.

5. Measurement and Results

5.1 Measurement

The test structure were bonded on a 40 pin ceramic carrier, so that an easy access via a PCB could be established. Irradiations were performed with an x-ray tube of type FK 60-04 W 2000W

Kurz-Anode, with point focus $0.4x0.8\ mm^2$ from AEG at the Institute for Experimental Nuclear Physics (IEKP) at KIT [1]. The x-ray source was operated at 60 kV and had a tungsten anode.
The test structure were fully biased (e. g. $V_{DS} = -5\ V$) and then irradiated at room temperature with a dose rate of 571 $krad/h$. After each irradiation step, the input characteristic $I_{DS}(V_G)$ of the devices were measured with a Keithley 4200. Only a couple of minutes went by between irradiation and measurement. After the last irradiation step to 5 $Mrad$ some hours of annealing passed by, leading to a little decrease in the shift of the threshold voltage (visible e. g. in DUT (device under test) 1, figure 3a).
The threshold voltage was extracted via fitting a polynomial of first order to a $\sqrt{I_{DS}}(V_G)$ plot in the threshold region and taking the intersection point with the voltage axis as the threshold voltage V_{th} [11].

Figure 3a to 3d show the threshold voltage shift results of four DUTs with thick nitride which were irradiated with different gate biases. A selection of the same data (limited to high doses) is depicted in figure 4b with the threshold voltage shift as a function of gate bias voltage during irradiation. Figure 4a shows the results from another measurement, which was taken for this study, with five DUTs exhibiting a thinner nitride layer.

5.2 Conclusions

Comparing figure 4a for a thin nitride layer with figure 4b for a thicker one, it is clear that to achieve a minimal voltage shift the thicker nitride layer is preferred. A maximum threshold shift of 9.4 V at a dose of 5 $Mrad$ stands against the shift of 13.8 V already at 3 $Mrad$ with the thinner nitride sample (see figure 4a).
Concerning the homogeneity of the shift with different potentials during irradiation as a parameter, a difference between the two nitride layers is not visible.
The presented irradiations deal with a specific problem of the DEPFET, the voltage dependent damage of the clear gate. For the gate contact the situation is different, measurements indicate that a thin nitride layer performs better, since the threshold voltage shift is minimal for minimal nitride layer thickness [12].

6. Summary and Outlook

We have shown irradiation results performed with special test structures, which are equivalent to the clear gate region of the DEPFET. The irradiation was done with an x-ray tube to simulate the ionizing damage in the Belle II experiment. Two parameters have been varied, first the voltages on the gate contact of the test structure to simulate different regions of the clear gate and secondly the nitride layer thickness in order to investigate technological possibilities to improve radiation hardness.
As a result, we can say that a thicker nitride layer has performed better and future investigations will focus on additional nitride variations.

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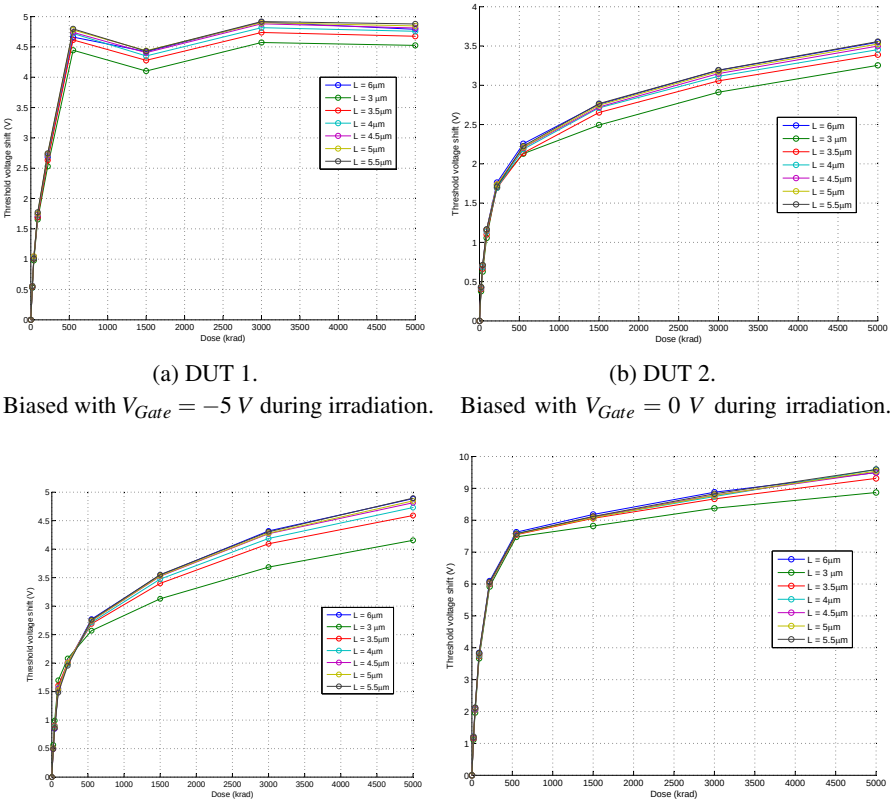


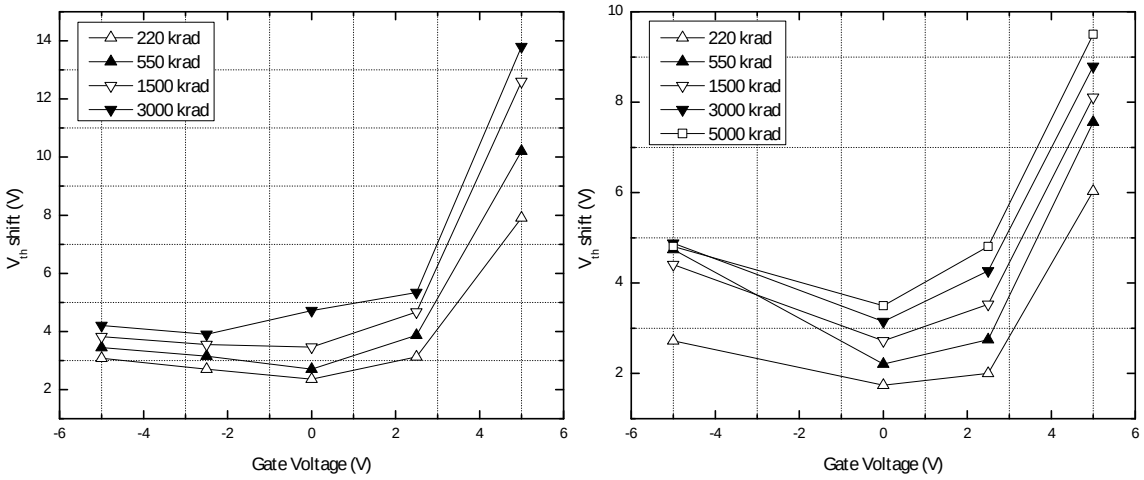
(a) DUT 1. Biased with $V_{Gate} = -5\ V$ during irradiation.

(b) DUT 2. Biased with $V_{Gate} = 0\ V$ during irradiation.

(c) DUT 3. Biased with $V_{Gate} = +2.5\ V$ during irradiation.

(d) DUT 4. Biased with $V_{Gate} = +5\ V$ during irradiation.

Figure 3: Measurement results from four identical test structures, each one irradiated with a different gate bias voltage. The parameter for the curves in each plot is the gate length L.



(a) Thin nitride layer samples.

(b) Thick nitride layer samples.

Figure 4: Threshold voltage shift as a function of gate voltages during irradiation. Comparison between two nitride layer thicknesses, all data points are referred to a gate length of $L = 4.5\ \mu m$.

Intra pixel variations are hard to tackle and can maybe solved with a different pixel layout, resolving the high electric field issue between clear gate and the drift region.

7. Acknowledgement

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