FRONT-END ELECTRONICS FOR PARTICLE DETECTION AND DATA COMMUNICATION

F.Giannini, E.Limiti, G.Orengo
Department of Electronic Engineering – University of Roma "Tor Vergata"
email: giannini@elettra.eln.uniroma2.it

Abstract

A family of GaAs monolithic front-end amplifiers, to be used in a large number of applications in present and future radiation detection experimental apparatus, is described in this paper. Design, realization and measurements are presented for MMICs especially designed for front-end circuits in particle detectors as RPC or solid-state detectors, including discriminators, charge amplifiers and logarithmic amplifiers, or front-end receivers in high-speed data communication link as optical front-end amplifiers and cable equalizers.

1. INTRODUCTION

In the future experiments in the field of high energy physics, such as the planned experiments of the Large Hadron Collider (LHC) at CERN, the increasing flux of ionizing particles and the large number of detectors in a small volume will end up being a large flux of data to be processed. The detecting apparatus will require low power, high gain-bandwidth product front-end electronics, easy to serialize, possibly in a custom version, to keep the cost of a large number of channels very low. On the other hand, the communication network that will be handling high transmission rates coming from different sources will require large bandwidths in receiving subsystems. Moreover, this electronics should exhibit low sensitivity to radiation [1].

Beyond the fact that a monolithic approach is necessary to guarantee high yield and repeatibility in a large scale production, these requirements are today not completely fulfilled by traditional silicon technology, both in terms of reception and transmission speed, gain performance and power budget [1,2].

In the next sections, different MMIC front-end amplifiers for particle physics readout electronics will be presented, and their design, realisation and experimental tests will be described. The types of circuits investigated and realised can be grouped into two main categories: front-ends for particle detectors and optical or cable front-ends for data communications. The circuits have been designed by the Group operating at the University of Roma Tor Vergata and at the National Institute of Nuclear Physics (INFN).

2. PARTICLE DETECTOR FRONT-ENDS

2.2 An 8-Channels Discriminator Front-end

Both for RPC (resistive plate chamber) and solid-state detectors, the pick-up system can be treated as a delay line, when the collection charge time is lower than the propagation time in the pick-up system. A voltage amplifier must be adopted as front-end stage, possibly matched to the low source impedance of the system. As an example, an RPC operating in avalanche mode typically produces a single signal of 5 ns FWHM (Full Width Half Maximum) and 1.5 ns time jitter, while the pick-up propagation time is 15 ns, in a 25 Ω impedance environment [3].

An 8-ch front-end discriminators for application in readout electronics of RPC particle detectors, composed of a high-gain pulse amplifier integrated with a variable threshold comparator and an ECL buffer, have been designed. The chip turns out to be very stable, featuring high voltage gain (>1000), gain-bandwidth product (10^{11}) and sensitivity (~50μV), fast rise time (1.5ns), high trigger time resolution (1ns), and 25mW per channel of power consumption .

The input stage of the front-end is a voltage amplifier; the good time performance of the RPC detectors, utilized for the bunch crossing identification, imposes an amplifier rise time of the order of the RPC jitter time (~1.5ns), because the large fluctuations in signal amplitude of the detector (100μV to 0.5 V) generate a jitter time at the threshold crossing of the order of the pulse rise time. The amplifier frequency response is optimized for typical time structure of the avalanche signal according to the following conditions: 1) same risetime for the amplifier and input signals, which is nearly 1.5 ns; 2) minimum return-to-zero time for the output signal. The resulting frequency response has a maximum at 100 MHz and a 3dB bandwidth of 160 MHz. The amplifier output shows a bipolar shape, as plotted in Fig.1, giving zero integrated charge, thus avoiding a possible dependance of steady ouput voltage on the counting rate.

The high input impedance R_I of the amplifier has been matched to the low impedance R_S of the pick-up strip teaming the amplifier with a transformer input coupling by means of coaxial air-coupled spiral inductances, since ferrite materials cannot be used in the high intensity magnetic fields of the high energy physics experimental apparatuses.

A comparator is cascaded to the amplifying section to generate a standard positive or negative squared pulse from a bipolar one, with less than 2 ns rise and fall time, as schematized in Fig.1. The threshold value can be regulated to give adequate immunity respect to the noise. The minimum comparator threshold combined with the amplifier gain fixes the minimum detectable signal amplitude. A block diagram of the whole front-end discriminator is shown in Fig.2.

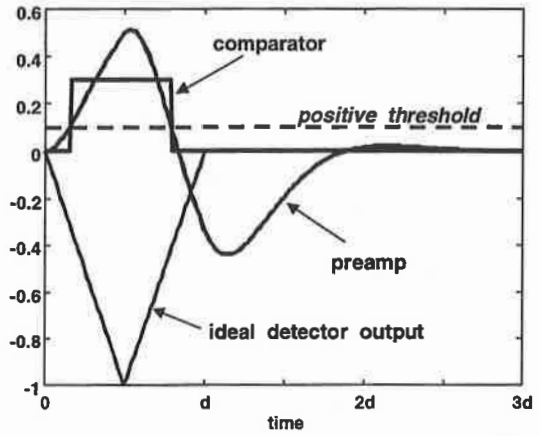

Fig.1. Front-end response to a triangular-shaped detector output.

From the technological point of view, 20GHz cutoff frequency MESFETs have been chosen for their intrinsic high gain-bandwidth product. Moreover, the GaAs MESFET features the minimum serial-parallel noise at the given frequency band, which is above the 1/f corner. The chip size resulted 1.5x2.3 mm^2.

A summary of channel characterization is presented in Figg.3-5. All measurements were performed on an 8-channels full-custom test board by means of a TEK_TDS684B digital oscilloscope. Finally, the measured power consumption per channel is lower than 25mW.

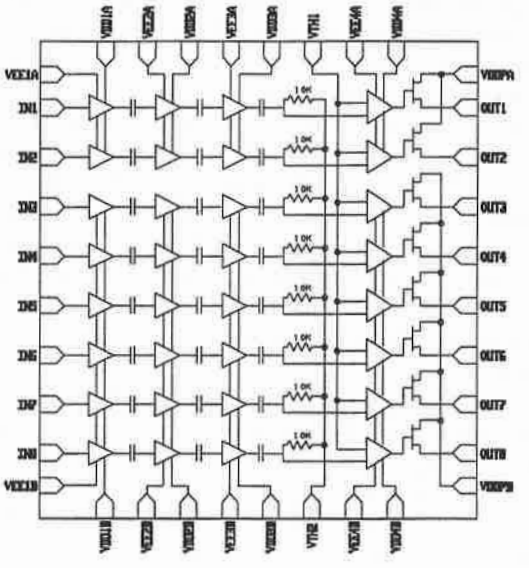

Fig.2. Block diagram of the 8-channel front-end.

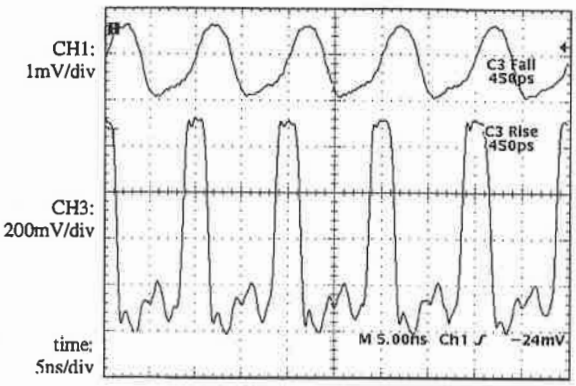

Fig.3. Max. rate performance (100 MHz).

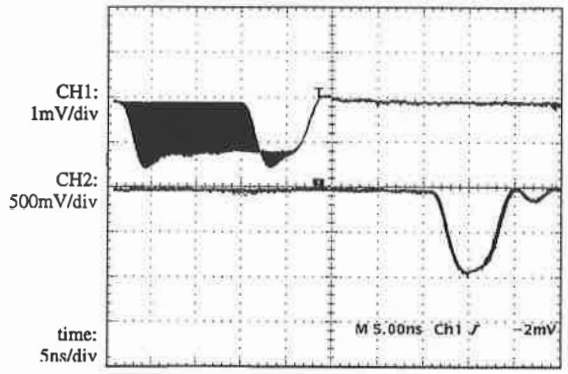

Fig.4. Output shaping for input pulse variation in width (6-20ns).

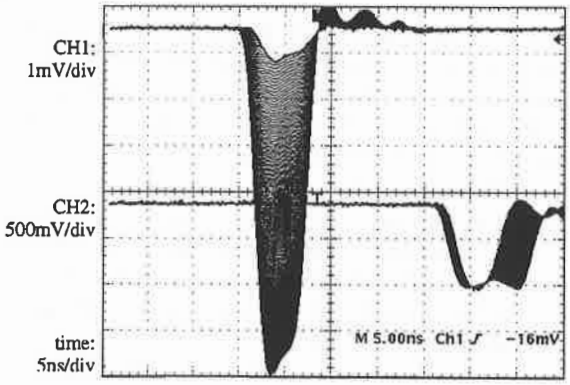

Fig.5. Output jitter time (on the fall) *vs* input pulse amplitude (0.5-7 mV).

2.2 *Charge Amplifying Front-ends*

An 0.3μm HEMT-based charge amplifier is presented. The amplifier has been manufactured by the ALENIA Foundry. The function blocks of the amplifier are shown in Fig.6. The input charge preamplifier is followed by an RC-CR filter with two interstage buffers, which assure a better linearity with respect to the single transistor buffer version. Dry etching techniques have been adopted both to increase the feedback resistance of

the charge amplifier up to 100kΩ, so improving the thermal noise, and to change the front-end HEMT device gate length from 1 to 0.2 μm, in order to enable the amplifier to match the 1-10 pF input detector capacitance. Despite of the increased circuit complexity, the chip size is only 2.3x1.5mm^2, while the total expected power dissipation is less than 5mW. The simulated performances of the front-end are shown in Fig.7, where the frequency behaviour of the open loop voltage gain of the charge preamplifier is plotted, and in Fig.8, where are reported the responses to a voltage step, applied to an input capacitance simulating the detector, of the preamplifier and the RC-CR shaping buffer stages, respectively.

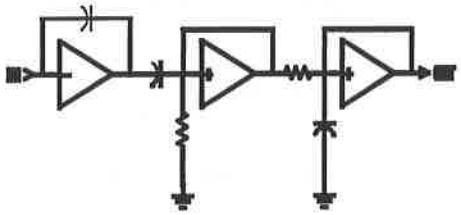

Fig.6. Block diagram of the charge amp.+ RC-CR shaper

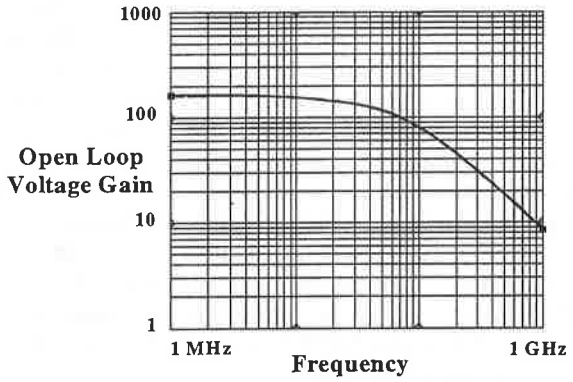

Fig.7. Simulated open loop voltage gain of the preamplifier.

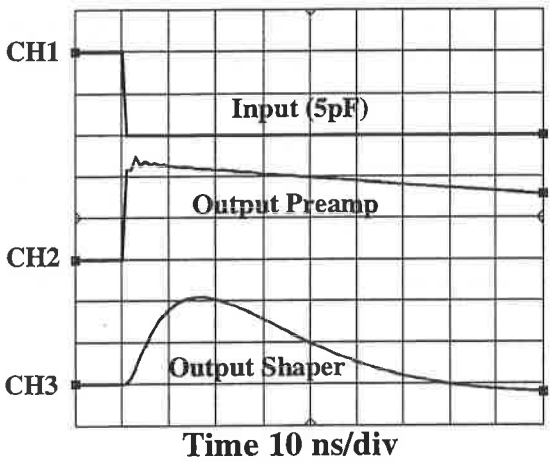

Fig.8. Simulated response of the preamp. (CH2) and of the shaper (CH3) to an input voltage step (CH1) (Cdet=5pF).

2.3 A High-Speed Logarithmic Amplifier

The design methodology is based on a parabolic approximation of the ideal logarithic characteristic yielding a major reduction of the logarithmic error. The amplifier, realised in GaAs 0.5μm MESFET monolithic low-noise technology, features ultra-broadband performance from 0.3 GHz to 5 GHz. A three chips amplifier was assembled utilising a modular strategy, allowing the fulfillment of design goals simply increasing the number of cascaded stages [4].

The circuit has been fabricated entirely in monolithic 0.5 μm MESFET low-noise technology by ALENIA, on a 120μm-thick GaAs substrate. A photograph of the realised chip is reported in Fig.9. The chip dimensions are 2x2 mm^2.

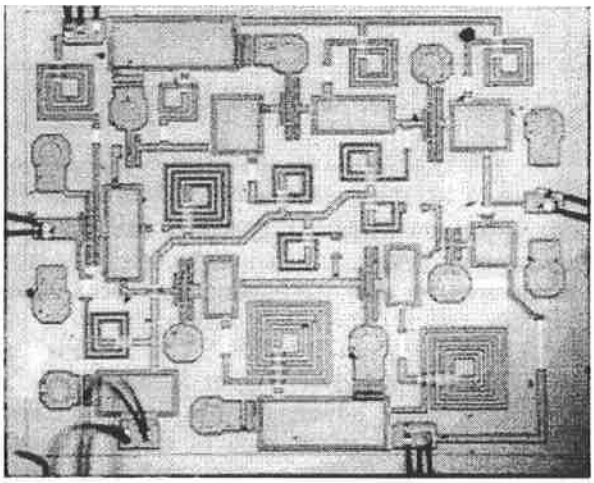

Fig.9. Photograph of the realised MMIC chip

In Fig.10 the simulated and measured input-output voltage characteristic for a single stage, at two different frequencies (2 and 0.5 GHz), are reported. Finally, three stages were cascaded and measured. The resulting input/output voltage characteristic is plotted in Fig.11, demonstrating the very good behavior of the "parabolic shaped" true log-amp.

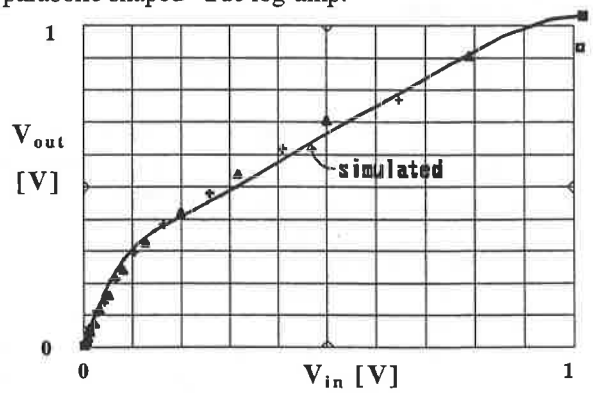

Fig.10.Single-stage simulated (solid line) and measured input-output voltage characteristics at 0.5 GHz (triangles) and at 2 GHz (crosses)

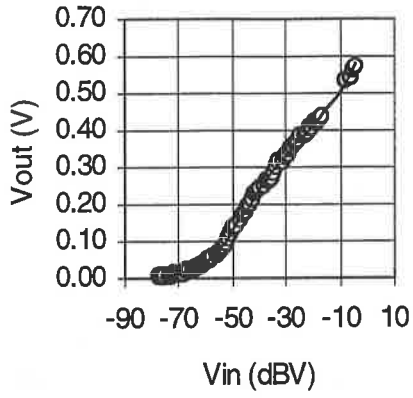

Fig.11. Measured input-output characteristics of the cascade of three stages at 2 GHz

3. DATA LINK FRONT-ENDS

In a high energy physics experimental apparatus, such as the LHC (Large Hadron Collider) at the CERN of Ginevra, the communication system is characterized by start-stop transmission on a star link topology, connecting different sources, each transmitting at a speed between 0.5 Gbit/s and 1 Gbit/s. Data stream should be 1000 Gbit/s (1000 optical link at 1 Gbit/s). This communication system can be implemented both on fiber or cable links. Fibers show clear advantages for data transmission respect to electrical cables such as lower attenuation, larger distance-bandwidth product, combined with an intrinsic electromagnetic coupling immunity. Despite of the high fabrication, installation and maintenance costs, fibers seems to be the most suitable link for long distances (200 mt at least). On the other hand, the possibility of digital data transmission on coaxial cables at high rates (1 Gbit/s) along distances beyond 100m has been successfully attempted, and suggested the development of an MMIC equaliser-amplifier chip, matching different needs with a simple unique technological solution.

3.1 A 1 Gbit/s Optical Front-end

This section reports a MMIC GaAs transimpedance amplifier for optical systems, carried out in collaboration with the Brazilian Telecomm (Telebrás). Operating bandwidth in excess of 2.2 GHz, without the input photodiode parasitic, and a transimpedance gain of 65 dBΩ were achieved; a complete receiver module has been realised and tested with an optical signal in the STM-4 hierarchy at 622.08 MHz [5]. The receiver consists in a first stage for optoelectronic conversion, realised with a PIN diode, and a transimpedance amplifier to obtain a voltage signal from the current generated in the photodiode. After optoelectronic conversion, the signal is fed to a low-pass filter, to eliminate out-of-band thermal and shot noise, and to a limiting amplifier; the last one guarantees a constant output level, indipendently from the signal variation in the dynamic range of the transimpedance amplifier, drives the decision circuit and the clock recovery circuit. Both outputs are sent to a demultiplexer (1:4) to obtain the STM-1 signal (155 MHz). The block composition of the system is shown in Fig.12.

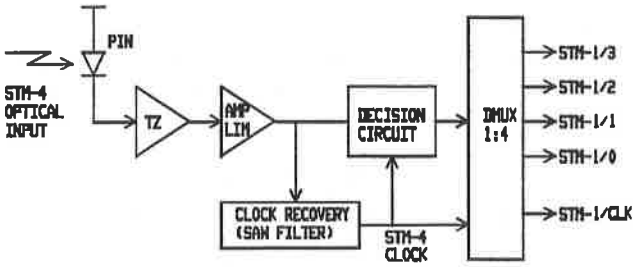

Fig.12 : Block diagram of the receiver.

The clock recovery in high rate transmission systems can be realized using non linear circuit as PLL, or, as in our case, band-pass filters employing the SAW technology. The clock recovery block employs a transition detector, acting as a frequency doubler, and a SAW band-pass filter at 622 MHz, producing a sinusoidal signal at the same frequency at the output. The clock signal is introduced together with data signal in the decision circuit. Its topology is basically a D-type Flip-Flop Master/Slave, and its main function is to synchronize data and clock signals to be fed to the demultiplexer. This one can operate alternatively as 1:4 at 622 Mbit/s or 1:16 at 2.5 Gbit/s, compatible with SDH/STM-4 or SDH/STM-16 respectively, and providing 155 Mbit/s output channels.

The eye diagram at the output of the transimpedance amplifier (190 mV_{pp}) is plotted in Fig.13, for an optical signal in the STM-4 hierarchy at 622 MHz NRZ, while Fig.14 shows the signal of an output channel of the demultiplexer at 155Mb/s and 800mV_{pp}, together with the eye diagram demonstrating a low bit error rate.

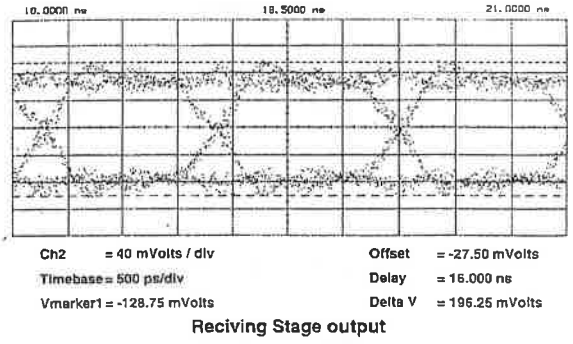

Fig.13: (a) Eye diagram at the output of the optical preamplifier (622 MHz, 190 mV_{PP})

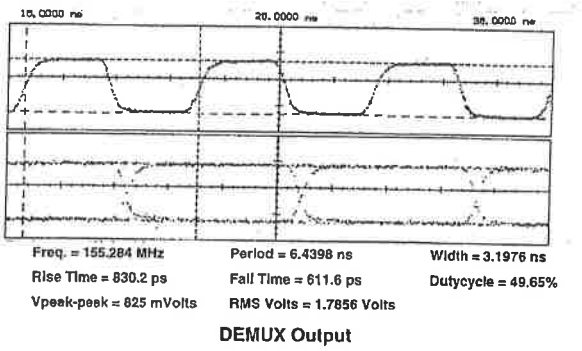

Fig.14: An output channel of the demultiplexer and the corresponding eye diagram (155 Mb/s, 800 mV_{PP}).

3.2 Cable Equalizers

The performance of a coaxial cable depends on its length, and for a distance larger than 10m the most used cables exhibit a disequalised attenuation, which could make the output digital pulses to be "misunderstood" by a threshold device. A simple equalising technique could be based on a receiving device with an opposite gain slope. To behave properly with different cables of different lengths, this solution is required to perform different equalisations.

In order to achieve this features, a new GaAs integrated equalizer-amplifier was designed to match different cable types and lengths by means of a voltage-controlled equalisation procedure [6]. The chip has been fabricated by the Alenia foundry and performs a maximum gain of 24 dB at 1 GHz, while the slope can be varied from 3 dB/dec to 16 dB/dec in the 100÷1000 MHz band. The effect of the equaliser-amplifier insertion on a cable transmission link in the worst conditions has been reported in Fig.15. The original bit sequence has been recovered, although inverted, and complementary bit recognition is still allowed.

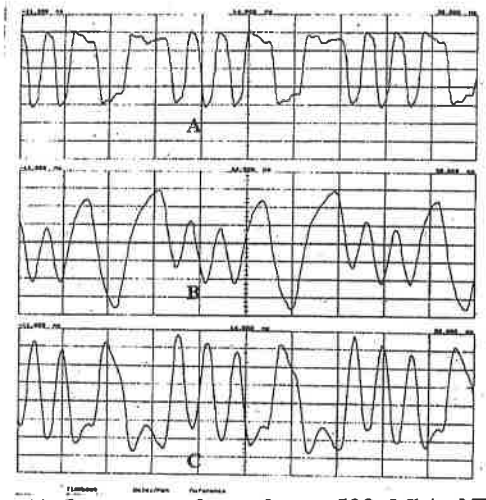

Fig.15. A) Input waveform for a 500 Mb/s NRZ bit stream. B) Output waveform after 100m of C-0-12 SAT plus 42 m of RG58 coaxial cables. C) Output wafeform after the equaliser-amplifier.

CONCLUSIONS

The reported results, extracted from the ones related to more than thirty different MMICs designed at the University of Roma Tor Vergata, demonstrated the effectiveness of the approach and the success of the particular effort, devoted to the establishment of a design and testing capability in the field of very high frequency integrated microelectronics.

Moreover, the feasibility of the GaAs monolithic integrated solution as an effective way to solve some of the many problems arising from the new high energy physics experiments, was also demonstrated.

REFERENCES

[1] F.Giannini, E.Limiti, G.Orengo, R.Cardarelli, "GaAs MMIC front-end electronics for high-energy physics", Aracne, Roma, 1998.

[2] M.Massani, A.Cetronio, "Alenia Foundry activities in the field of GaAs detector and electronics for high energy physics", *Proceedings of the 25th European Microwave Conference*, pp.9-16, Bologna, Italy, September 1995.

[3] G.Aielli, P.Camarri, R.Cardarelli, V.Chiostri, A. Di Ciaccio, L.Di Stante, G.Orengo, R.Santonico, "RPC front-end electronics for the ATLAS LVL1 trigger detector", *Nuclear Instruments and Methods*, June 1998.

[4] G.Acciari, F.Giannini, E.Limiti, "Theory and performance of parabolic true logarithmic amplifier" , *IEE Proceedings - Circuits Devices & Systems*, Vol. 144, No. 4, August 1997.

[5] F.Giannini, E.Limiti, G.Orengo, C.Finardi, "Design and Fabrication of GaAs IC's Receiver Modules for High Speed Optical Communication Systems", *Asia Pacific Microwave Conference APMC'96*, Vol.III, sec. E8-1,pp.875-878, New Delhi, December 1996.

[6] R.Cardarelli, G.Orengo, G.Piccinelli, "1 Gbit/s Data Transmission On Coaxial Cable up to 200 meters", *Proceedings of the 3rd International Workshop on Gallium Arsenide and Related Compounds*, pp.204-208, S.Miniato (PI), March 1995.