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Design and Testing of a radiation tolerant Clock, Control and Monitor (CCM) Module For the CMS HCAL Electronics

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***Abstract*-- A Clock, Control and Monitoring (CCM) Module is being designed for the Hadron Calorimeter subsystem of the CMS Detector. The CMS detector has been designed to detect cleanly the diverse signatures of new physics at the Large Hadron Collider.**

This CCM module will be responsible for low skew clock and beam crossing marker distribution, monitoring of voltages and temperatures and as the interface between the main control system and the Front End Modules. The CCM module will reside in the HCAL Readout Box that will be mounted on the HCAL detector. Due to this physical location the CCM module will need to work within a radiation environment with minimal access over a ten-year period. The electronics are expected to see a total neutron fluence of $1.3x10^{11}$ n/cm^2 and a total ionizing dose of 330 rads over the 10 year running period. This paper will detail the design of the CCM Module including the selecting and testing of devices that will operate within the radiation field.

I. Introduction

The Clock, Control and Monitoring (CCM) Module is being designed for the Hadron Calorimeter subsystem of the CMS Detector[1]. The CCM is an integral part of the Front End Readout electronics and operates in conjunction with twelve Front End (FE) Readout cards[2] that condition and digitize data from the Calorimeter. The CCM and the FE cards plug into a custom backplane that resides in a custom crate called a Readout Box (RBX). The backplane, besides distributing power, is used to provide a serial communication path between the CCM and four groups of three FE cards.

The CCM module operates in a radiation environment and component selection was a critical factor in the design. Components were chosen that were not susceptible to a Total Ionizing Damage (TID) of less than 330 rads and were also Single Event Effects (SEE) tolerant. Access to the CCM will be minimal and the other FE boards will have limited functionality without a proper operating CCM.

The CCM performs three functions: 1). Receive and distribute a low skew 40 MHz. Clock along with a beam-crossing marker to the FE cards. 2). Monitor the temperature at the FE cards and also the power supply voltages that are present on the backplane. 3). Provide a means for a Main Control system to communicate with the ASICs located on the FE cards and also provide a method to download parameters to those ASICs during a global reset.

The CCM module consists of three printed circuit boards that reside within a custom chassis. The chassis plugs into the middle location on the backplane located within the HCAL Readout Box. The three printed circuit boards each perform one of the above functions.

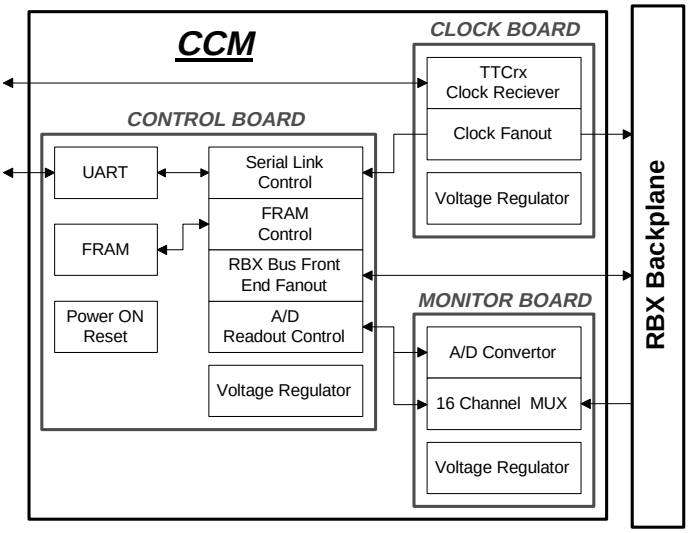

Fig. 1. CCM Module Block diagram showing the three printed circuit boards: Clock, Control and Monitor.

II. Board Design

The three 6 layer printed circuit boards are all based on a design, which allows four signal layers, a split power plane and a ground plane. All three boards will be physically located in a custom Aluminum chassis, which will provide a cooling path to

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allow heat transfer away from the boards. The boards interconnect with short ribbon cables (cables will be replaced with stackable connectors) and a RG174 cable to transfer the clock signal to the Control board. The size constraints of the RBX required the three boards to be 8cm tall and 12cm long with a board spacing of 1.6cm. The Monitor board length was reduced to 5cm to allow for a mezzanine board that holds a Clock receiver circuit to be mounted on the backside of the Clock board.

The CCM module is electrically isolated from both the Main Control system and the TTC clock system using optical isolation devices. Power to the module comes from the RBX backplane in the form of two voltages, +6.5v and +5.0v. Radiation Hardened voltage regulators LHC4913 are used on each of the three boards to reduce the voltages to +5.0v and +3.3v along with +2.5v on the Control board.

A. Clock Board

The Clock board receives timing and control information through the Timing, Trigger and Control (TTC)[3] system. The TTCrx a custom IC that was developed by the CERN MICROELECTRONICS GROUP receives the timing information. The TTCrx along with its associated components such as the photodiode+preamp reside on a mezzanine card. The mezzanine card mounts onto the back of the Clock Board. A 40.08 MHz bunch –crossing reference clock signal along with a Beam-Zero marker are extracted from the custom IC. The clock signal is distributed onto the backplane to the FE cards using an ON-Semiconductor MC100LVEP111 differential LVPECL clock driver. The Beam-Zero marker is distributed onto the backplane using an ON-Semiconductor MC100LVELT22 differential LVPECL translator. A copy of the clock signal is also forwarded to the Control Board to use as a master clock to operate the FPGA.

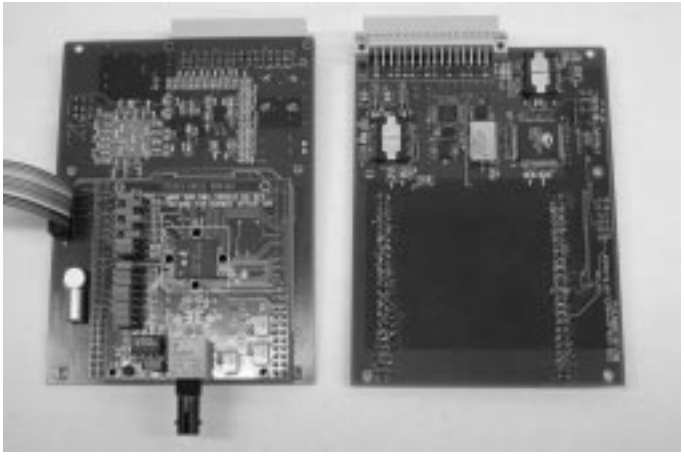

Fig. 2. Clock Board showing both sides with the mezzanine board attached.

The jitter of the raw 40.08 MHz clock output of the TTCrx is too high to effectively operate the high-speed serializers on the FE boards. A VCXO/PLL ASIC is being developed by the CERN Microelectronics Group for use as a jitter filter. The QPLL is expected to have a peak-peak output jitter of less than 50 ps.

B. Control Board

The Control board performs a number of functions including interfacing with the Main control system, distributing control signals to the FE boards and controlling the Clock and Monitor boards. An Actel Antifuse A54SX72A FPGA along with associated drivers and receivers provide the serial communication link between the FE card's ASICs and the CMS HCAL main control system. The FPGA acts as a slave to the Main Control system and as a master to the FE cards.

Fig. 3. Control Board with ribbon cables that attach to the Clock and Monitor boards.

An optically isolated serial path allows communication between a UART core within the FPGA and the Main Control system using National Semiconductor's DS36276 RS485 transceivers and Agilent 6N134 opto-couplers. A four pair Category 5 cable is used for the serial link with a separate transmit and receive pair along with a power and ground pair. The FPGA receives the information from the Main Control system and distributes it onto one of four serial communication paths labeled the RBXbus across the backplane. Each of the four RBXbus consists of a data line and differential LVPECL clock line. Each RBXbus on the backplane connects to three FE boards grouped together to form a readout module. A Ramtron FM18L08 Ferro-Electric RAM is used on the Control board to hold preset parameters that are downloaded on a global reset to all FE cards using the same four RBXbus on the back plane.

The Main control system is also able to send various controls or reset signals via the FPGA to the FE boards using On-Semiconductor MC100LVELT22 differential LVPECL translators.

Fig. 4. Monitor Board.

C. *Monitor Board*

An Analog Devices AD590 Temperature Transducer produces a current representing the temperature of each readout module. The current is converted to a voltage and is sent via the backplane to the Monitor Board. These temperatures along with the power supply voltages are converted to a digital word using the Analog Devices AD670 Bipolar 8-Bit Analog to Digital converter and the ADG706 Analog Mulitplexer. The temperature and voltage readings can be accessed by the Main Control system through the Control Board of the CCM.

III. Component Selection and Radiation Testing

After an initial investigation into radiation hard devices it was determined that commercial off the shelf (COTS) components would need to be used to fit within the budget constraints of the project. Components were chosen first on their ability to avoid a destructive failure such as Single Event Latchup and secondly on there susceptibility to Single Event Upsets. Whenever possible Bipolar or PECL parts were chosen or components that had previously been used and tested in a radiation environment.

Individual components and a prototype CCM unit were tested at the Cyclotron Facility (200MeV beam) at Indiana University. Components were tested for Total Ionizing Dose (TID, Single Event Latchup (SEL) and Single Event Upsets (SEU) where applicable. Test boards were produced that contained a quantity of the same type device. These test boards were than subjected to radiation levels that allowed us to generate statistics that would provide a failure rate for a ten-year operating period. Results of the tests showed that all components and the prototype CCM will operate beyond the ten year dose of 330 rads with a neutron fluence of 1.3×10^{11} n/cm^2. The SEL tests showed that for all the components on the CCM there exists the possibly of less than one failure for every four years.

Single Event Upsets are possible within the Actel FPGA. Tests were performed on the FPGA using a 2012 bit shift register and also with a 670-bit shift register that implemented Triple Modular Redundancy (TMR). The TMR design recorded zero upsets while the 2012 bit design provided the statistic of one SEU every other day for the 130 CCM units in operation. The CCM's FPGA design will implement half of the design using TMR. Links to the radiation tests can be found in the references [4],[5],[6],[7],[8],[9],[10].

TABLE I
INTEGRATED CIRCUITS USED ON THE CCM

Part #	**Manufacturer**	**Description**	**Qty**	**Tested**
DS36276M	National Semiconductor	RS485 Transceiver	2	Oct. 02'
A54SX72A	Actel	Antifuse FPGA	1	Oct. 02'
P82B715	Philips	I2C Buffer	4	Oct. 02'
AD670JN	Analog Devices	8-Bit A/D Converter	1	Oct. 02'
AD590KH	Analog Devices	Temperature Sensor	1	May 01'
ADG706BRU	Analog Devices	Analog Multiplexer	1	Sept. 01'
MC100LVELT22D	ON-Semiconductor	TTL-LVPECL Clock Translator	8	Sept. 01'
MC100LVELT23D	ON-Semiconductor	LVPECL-TTL Clock Translator	8	Sept. 01'
MC100LVEP111FA	ON-Semiconductor	LVPECL 1:10 Clock Fanout	8	Sept. 01'
TTCrx	CERN Microelectronics	Timing ASIC	1	CERN
LHC4913	CERN Microelectronics	Voltage Regulator	7	CERN
OP184ES	Analog Devices	Op-Amp	1	
PZT2222A	Philips	NPN-Transistor	1	
HFBR-2316T	Agilent	Fiber Optic Receiver	1	CERN
6N134	Agilent	Opto-Coupler	2	HP
FM18L08	RAMTRON	FRAM Memory	1	JPL
QPLL	CERN Microelectronics	Quartz Crystal PLL	1	CERN

IV. Serial Communication Protocol

The CCM module incorporates a general purpose UART core in the Actel FPGA. The UART will communicate with the Main Control system using a custom control package[11] being developed at CERN. The initial software has been developed including a simulator and a debugging tool. The UART core operates in an asynchronous mode with a start bit followed by 8-bits of data an even parity bit and then a stop bit. The baud rate is expected to be 115,200 Hz. and will be dip-switch selectable on the Controller board. The custom software will send a command with the following format XXYYYYYY. Where the XX is the command itself and the YYYYYY is the operand. The operand specifies an address. The command can be of four types: 00 – ignore, 01 – read contents of the address specified by the operand, 10 – write single byte of information to the address specified by the operand, 11 – write an array of data to the CCM at the address specified by the operand. The CCM will respond to the read command with a status byte followed by the 8-bit data byte. With the write commands the data follows in the next 8-bit bytes. The CCM will respond to write commands with a status byte. The status byte will report parity errors, framing errors and the operating mode of the CCM.

V. Conclusion

A prototype of the CCM module has been built and was used in a Test Beam at CERN in July of 2002. The CCM was able to successfully communicate with the Main Control system using the custom control software. Communication with all the FE boards within a RBX was successful along with monitoring of the temperature and voltages. For the prototype CCM an Actel ProAsic reprogrammable FPGA was used to allow for any changes in the design specification. Following the Test Beam an Actel Antifuse 54SX72A part has been programmed and installed on another prototype CCM and works in a manner similar to the ProAsic part. The final Antifuse design will incorporate the Triple Module Redundancy design techniques to reduce the possibility of SEU effects.

Incorporating TMR reduces the amount of cells available for logic within a design. The CCM design uses about 50 percent of the A54SX72A cells without TMR. Particular sections of the design that are critical to operation like the serial communication link will receive TMR other sections such as the Analog to Digital converter controller will operate without the feature.

There will be approximately 130 CCM modules installed in the CMS HCAL experiment that will need to operate for a ten year period. Installation is expected to begin in the fall of 2003.

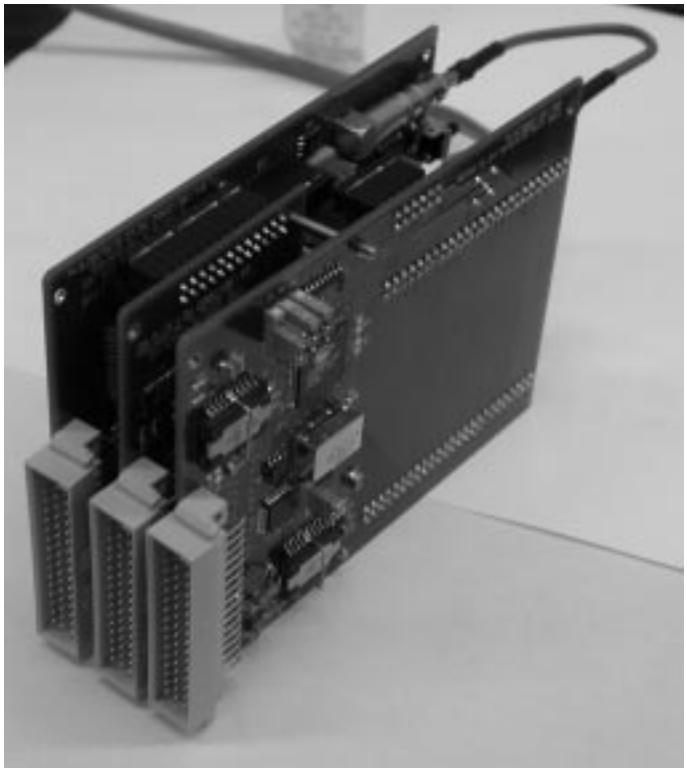

Fig. 5. Prototype Clock, Control and Monitor Module.

VI. References

[1] CMS, The Hadron Calorimeter Technical Design Report, CERN/LHCC 97-31, June 20, 1997.

[2] T. Shaw, “The CMS Hadron Calorimeter Front-End Module,” Fermi National Accelerator Laboratory, Batavia, Illinois, Oct. 2002.

[3] J. Christiansen, A. Marchioro, P. Moreira, and T. Toifil, "A Timing, Trigger and Control Receiver ASIC for LHC Detectors," CERN – EP/MIC, Geneva, Switzerland, Oct. 1999.

[4] J. Whitmore, A. Baumbaugh, J.E. Elias, S. Holm,K. Knickerbocker, S. Los, C. Rivetta, A. Ronzhim, A. Shenai, R. Yarema, T. Zimmerman, "Radiation Validation for the CMS HCAL Front-End Electronics," Fermi National Accelerator Laboratory, Batavia, Illinois, Oct. 2002.

[5] S. Holm. (2002, Oct.). Actel Antifuse Radiation Tests. Fermi National Acceleratror Laboratory. Batavia, Illinois [Online] Available: http://www-ppd.fnal.gov/holm.myweb/cms_hcal/Actel_Antifuse_RAD_TEST.ppt

[6] J. Wang, et. al. “Radiation Tolerant Antifuse FPGA,” Actel Corporation. Sunnyvale, Ca.

[7] D.N. Nguyen, L.Z. Scheick, "TID Testing of Ferro-electric Nonvolatile RAM," Jet Propulsion Laboratory, California Institute of Technology, Pasadena, Ca.

[8] Leif Scheick, S. Guertin, D.N. Nguyen, "SEU Evaluation of FeRAM Memories for Space Applications," Jet Propulsion Laboratory, California Institute of Technology, Pasadena, Ca.

[9] K.A. Label, et al. "A Compendium of Recent Optocoupler Radiation Test Data," NASA/Goddard Space Flight Center, Ca.

[10] T. Toifil, P. Moreira, A. Marchioro, "Measurements of Radiation Effects on the Timing, Trigger and Control Receiver (TTCrx) ASIC," CERN – EP/MIC, Geneva, Switzerland.

[11] S. Surgueev. (2002, Sept.). HCAL DCS Status and Plans. CERN. Geneva, Switzerland [Online] Available: http://sergueev.home.cern.ch/sergueev/hcal/DCS_Sept2002.ppt