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The Compact Muon Solenoid Experiment

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Commissioning the CMS Silicon Strip Tracker prior to Operations with Cosmic Ray Muons

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Abstract

During autumn 2008, the Silicon Strip Tracker was operated with the full CMS experiment in a comprehensive test, in the presence of the 3.8 T magnetic field produced by the CMS superconducting solenoid. This note details the detector commissioning phase just prior to this data-taking exercise and the procedures used to optimise the performance of the Silicon Strip Tracker. The number of detector modules used during the test corresponds to 98.0% of the total system. The ten million channels of the SST readout system were calibrated and synchronised with cosmic ray muon data using automated procedures. Excellent hit and track reconstruction efficiencies were observed, which demonstrate the quality of the SST detector and the precision of the calibration procedures.

1 Introduction

The primary goal of the Compact Muon Solenoid (CMS) experiment [1] is to explore particle physics at the TeV energy scale exploiting the proton-proton collisions delivered by the Large Hadron Collider (LHC) [2]. The central tracking detector [1] built for the CMS experiment is a unique instrument, in both size and complexity. It comprises two systems based on silicon sensor technology: one employing silicon pixels and another using silicon microstrips. The Pixel Detector surrounds the beampipe and contains 66 million detector channels [3]. The Pixel system is, in turn, surrounded by the Silicon Strip Tracker (SST), which is the subject of this paper.

The SST consists of four main subsystems, shown in Fig. 1: the four-layer Tracker Inner Barrel (TIB), the six-layer Tracker Outer Barrel (TOB) and, on each side of the barrel region, the three-disk Tracker Inner Disks (TID), and the nine-disk Tracker End Caps (TEC). Each TID disk is made of three rings of modules, while TEC disks have seven rings. Overall, the tracker cylinder is 5.5 m long and 2.4 m in diameter, with a total active area of 198 m^2, consisting of 15 148 detector modules and comprising 9.3 million detector channels. Each detector module consists of a carbon or graphite fibre frame, which supports the silicon sensor and the associated front-end readout electronics. Four barrel layers and three rings in the end cap disks are equipped with double-sided modules, each of which is constructed from two single-sided modules mounted back-to-back with a stereo angle of 100 mrad between the strips. The silicon sensors are made up of single-sided p^+ strips on n-bulk sensors with two different thicknesses: 320 μm and 500 μm in the inner four and outer six layers of the barrel, respectively; 320 μm in the inner disks; and 320 μm and 500 μm in the inner four and outer three rings of the end cap disks, respectively. There are a total of fifteen different types of sensors in the SST, which vary in terms of strip length and pitch [4] to ensure that the single strip occupancy is low even at full LHC luminosity.

The first experience of the SST operation and detector performance study was gained in summer 2006, when a small fraction of the SST was inserted into the CMS detector. Cosmic ray

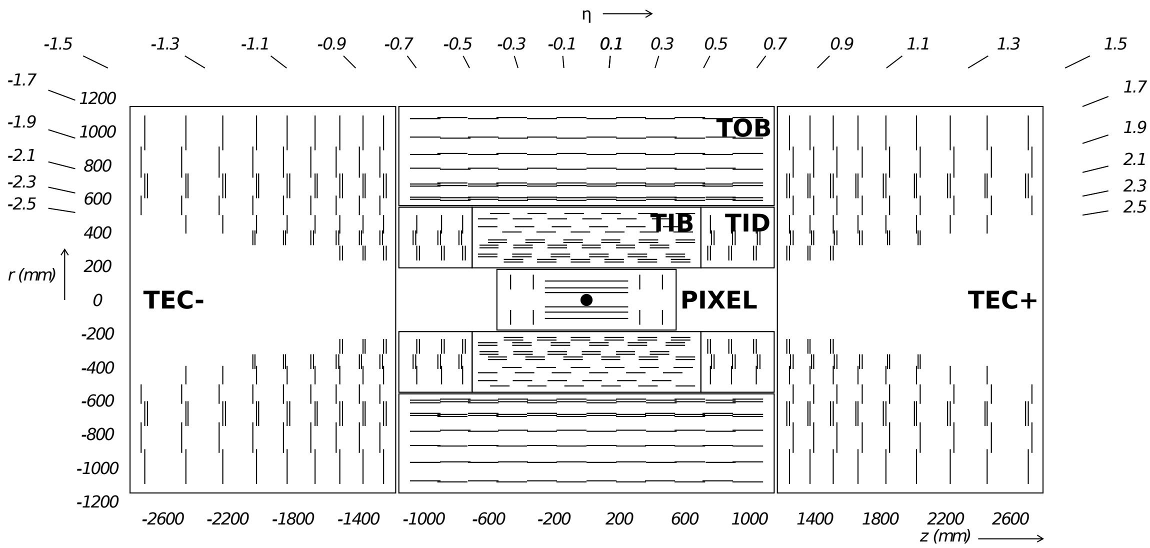

Figure 1: Schematic cross section of the CMS tracker. Each line represents a detector module. Double lines indicate double-sided modules which deliver stereo hits.

muon data were recorded in the presence of a solenoidal field up to the maximum design value of 4 T. The results from this period of data-taking are described elsewhere [5]. Construction of the full SST was completed in 2007 and 15% of the full SST was commissioned and operated for several months prior to installation in the underground CMS experimental hall. The results of this period of stand-alone operation, known as the Slice Test, are also described elsewhere [6, 7].

The installation of the SST within CMS was completed during 2008 and the system underwent its first round of *in situ* commissioning together with the other CMS sub-detectors during summer 2008. The first operation of the SST in a 3.8 T magnetic field took place during October-November 2008, when the CMS Collaboration conducted a month-long data-taking exercise known as the Cosmic Run At Four Tesla (CRAFT) [8]. This exercise provided valuable operational experience, as well as allowing, for the first time, a full study of the SST performance after installation and commissioning [9]. Results from detailed studies performed during the detector commissioning phase are presented here.

This note is laid out as follows. Section 2 describes the goals of the detector commissioning phase. Section 3 provides an overview of the SST control and readout systems. Section 4 summarises the checkout procedures used to determine the functional components of these systems. Sections 5-9 review the various commissioning procedures and their performances.

2 Goals of detector commissioning

In order to bring the SST detector into an operational state suitable for data-taking, several commissioning procedures are required to configure, calibrate, and synchronise the various hardware components of the control and readout systems. These procedures have been used to commission and evaluate aspects of the detector performance during the integration phase of the experiment. During the operational phase, the procedures will be performed periodically in order to ensure optimal detector performance during subsequent data-taking. Throughout the paper, a period of continuous data-taking during which the operating conditions are stable will be referred to as a run.

Each commissioning procedure is designed to tune the parameters used to configure the devices in the readout chain and determine calibration constants. The configuration parameters and calibration constants are stored in a database and are used for subsequent commissioning procedures or cosmic ray muons data taking.

The majority of the commissioning procedures are performed with the SST operating independently of the rest of the CMS experiment. These runs are performed using locally generated triggers and a local data acquisition system and computing cluster [10]. Only the procedures that concern synchronisation to an external trigger, described in Section 9, require reconstructed particle trajectories from cosmic ray muons or LHC pp collision data. In these cases, the SST is operated with other sub-detector systems of the CMS experiment. The SST subsystems (TIB/TID, TOB, TEC+, and TEC-[1]) are typically commissioned as individual partitions.

The commissioning of the SST aims to maximise the signal identification efficiency for in-time particles and minimise pileup due to out-of-time particles. The ultimate objective is to maximise the tracking efficiency while minimising the number of tracks caused by out-of-time signals from adjacent bunch crossings.

[1] The + and - labels refer to the position along the beam axis.

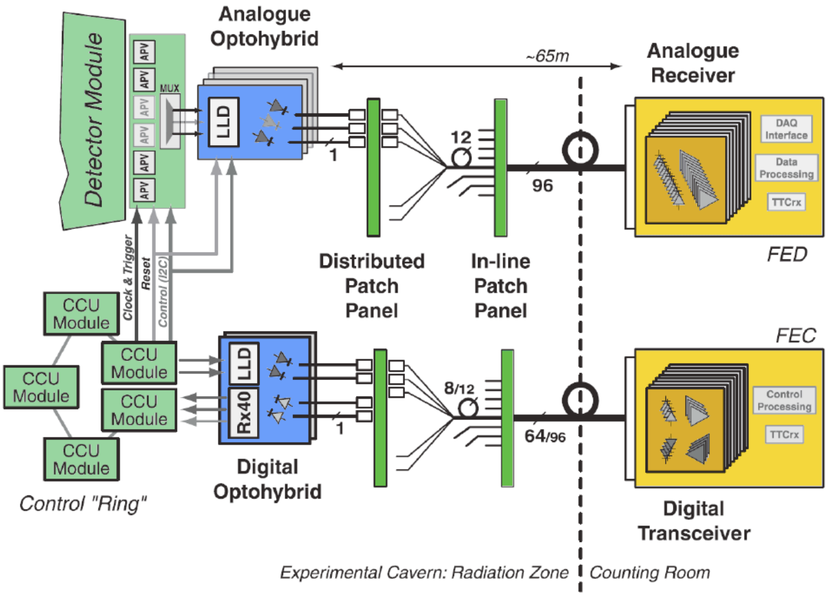

Figure 2: Schematic view of the readout and control system of the tracker.

3 The control and readout systems

Figure 2 shows a schematic of the control and readout systems for the SST, detailed descriptions of which can be found in Ref. [11].

The complete SST system is driven with the 40 MHz LHC clock provided by the Timing, Trigger, and Control system [12]. The CMS Level-1 hardware-based trigger, together with some fast control signals (reset, resynchronisation, calibration trigger) , is encoded in the clock signal.

The major components of the readout system are: 15 148 front-end hybrids on the detector modules that host 76 000 APV25 [13] readout chips, an analogue optical link system comprising 38 000 individual fibres [14], and 440 off-detector analogue receiver boards, known as Front-End Drivers (FED) [15], housed in VME crates.

In addition to the sensors, each detector module comprises: four or six APV25 chips; a Phase Locked Loop (PLL) chip [16] which is used to lock on and skew the 40 MHz clock signal; a MUX chip which multiplexes data from pairs of APV25 chips; and a Detector Control Unit (DCU) chip [17] which encodes a unique identifier and provides monitoring of voltages, currents, and temperature.

The SST control system [18] distributes the LHC 40 MHz clock, Level-1 triggers, and fast control signals to 368 *control rings* via digital optical links [14]. The control rings are driven by 46 off-detector digital transceiver boards, known as Front-End Controllers (FEC) [19], housed in VME crates. In each control ring a Digital Opto-Hybrid (DOH) module [14] converts the optical signals from a FEC and distributes electrical signals to multiple Communication and Control Units (CCU) [20] on the ring, which are connected in a redundant architecture in such a way that a single faulty CCU can be by-passed without preventing communication with the other elements on the ring. Each CCU distributes the clock, trigger, and fast control signals to groups of detector modules. The CCUs also use an I^2C bus [21] to transmit slow control signals to the detector modules and configure all front-end devices prior to a run. The complete system configuration requires 1.64 million parameters. The vast majority (93%) of these parameters are used to configure the operating modes and the bias of the APV25 chips. The complete set of parameters are stored in a versioned database to maintain a history of the tracker configuration.

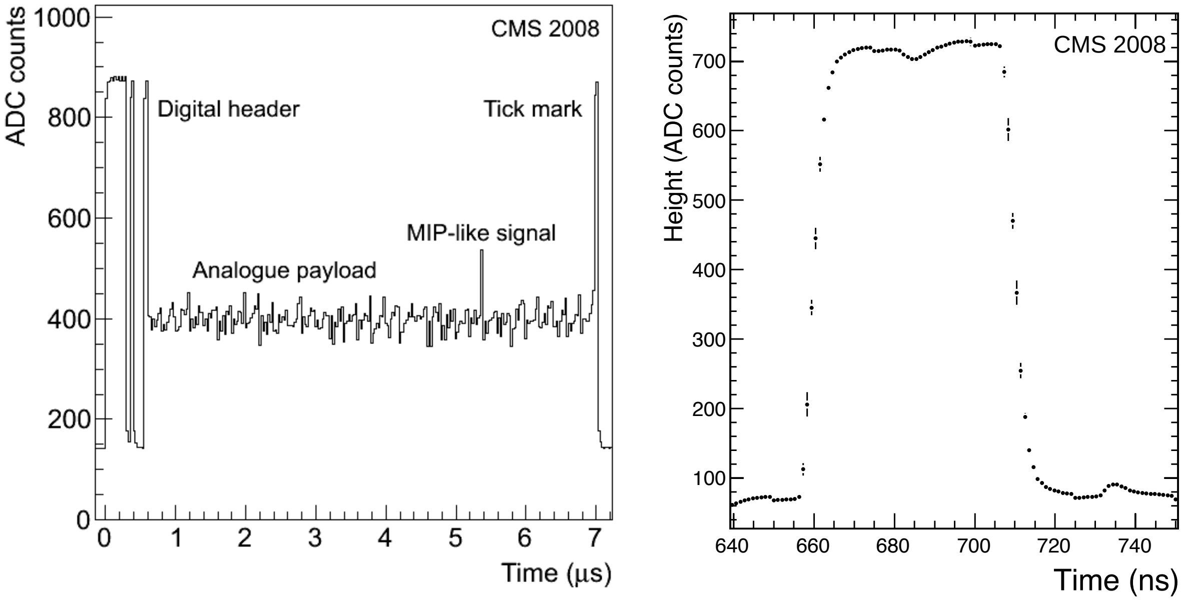

Figure 3: (left) Two APV25 data frames multiplexed, containing a time stamp and the sensor pulse height information. (right) A feature of the APV25 data stream, known as a tick mark, that is heavily used by the checkout and commissioning procedures. The left and right figures have sampling intervals of 25 ns and 1.04 ns, respectively.

The APV25 chip samples, amplifies, buffers, and processes signals from 128 detector channels at a frequency of 40 MHz. Fast pulse shaping is therefore required to provide bunch crossing identification and minimise pileup. The APV25 chip uses pre-amplifier and shaper stages to produce a CR-RC pulse shape with a relatively slow rise-time of 50 ns in an operating mode known as *peak*. An alternative mode, *deconvolution*, performs additional signal processing to constrain the signal to a single bunch crossing [22] at the expense of a reduced signal-to-noise ratio. Deconvolution is expected to be the standard mode of operation. Due to lack of time to complete a final timing adjustement needed for operation in deconvolution mode, the results presented in this paper are based on data accumulated with peak mode operation, unless stated otherwise.

On receipt of a Level-1 trigger, pulse height and bunch-crossing information from pairs of APV25 chips are generated and multiplexed onto a single line by the MUX chip. The data are converted to optical signals by the Analogue Opto-Hybrid (AOH) [23] and transmitted via optical links, driven by Linear Laser Driver (LLD) chips [24], to the off-detector FED boards. The FEDs digitise, compress, and format the pulse height data from up to 96 pairs of APV25 chips, before forwarding the resulting event fragments to the CMS data acquisition and high-level trigger systems [25]. These systems perform the tasks of event building, reconstruction, selection, and writing to storage.

Figure 3 (left) shows an example of the raw data captured at 40 MHz by a FED readout channel on receipt of a trigger. The data contain two frames multiplexed (interleaved) together from two APV25 chips. A single frame comprises 12 bits of binary information, known as the digital header, followed by analogue pulse height data from 128 sensor strips. A trailing *tick mark* identifies the end of the frame. The digital header encodes three header bits used to mark the beginning of a frame, eight address bits that provide a time stamp, and a single bit used to flag error conditions in the internal logic of the chip. The structure observed in the pulse height data across the 128 channels is due to static offsets, known as *pedestals*, which are unique to each detector channel. Small, time-varying *common mode* shifts in the levels of all 128 channels can be observed when operating. Figure 3 (left) shows the multiplexed frames of two APV25 chips and an example of a signal left by a minimum ionising particle. Signals are superimposed on the pedestal and common mode levels, which must be subtracted before the signal can be identified. In the absence of a trigger, no data frames are output by the chip and tick marks are produced every 70 clock cycles. Figure 3 (right) shows the pulse shape of multiplexed tick marks from two APV25 chips that are reconstructed with an effective sampling frequency of 960 MHz. This feature of the APV25 data stream is used heavily in the checkout and commissioning procedures detailed below.

The FEDs can format the pulse height data from the APV25 chips in different ways. The first is Scope Mode (SM), which is simply a capture of the raw data, as shown in Fig. 3 (left). The second is Virgin Raw (VR), which removes all of the binary information (digital header and tick marks) and simply provides the digitised pulse height data from the sensors. Both modes provide digital samples with a 10-bit range and are used when commissioning the SST system and for debugging. The third and nominal mode of operation is Zero Suppressed (ZS). This uses Field Programmable Gate Array (FPGA) chips to implement algorithms that perform pedestal subtraction, common mode subtraction, and identification of channels potentially containing signals above threshold. A threshold of five times the detector channel noise is used for single channels, but a threshold of only twice the channel noise is used for each of multiple contiguous channels. The zero-suppressed data are output with an 8-bit range.

4 Checkout of the detector components and connections

The first step of the checkout procedure is to establish which components in the control and readout systems, both on-detector and off-detector, respond to communication via the control system and VME bus. Automated hardware scans are used to perform basic functionality tests, such as checking for stuck register bits, and to identify unresponsive devices by cross-checking against the SST construction database. The registers of all devices are configured with default settings, as defined by design specifications or laboratory measurements, and are stored in a database.

Once active and functional devices have been identified, automated procedures are used to determine the cabling of both the readout electronics chain, from the detector modules to the off-detector FED boards, and the Low Voltage (LV) and High Voltage (HV) buses of the power supply system [26]. These procedures also map the detector modules to their geometrical position in the tracker superstructure. Automation is an important and necessary feature of the procedures, given the complexity of the SST control, readout, and power supply systems. The SST construction database is used as a reference and discrepancies indicate faulty components or incorrectly cabled devices.

The procedure that determines the cabling of the LV power supply system is a two-step process. Since both CCUs and detector modules can be uniquely identified through their DCU chip, they are powered sequentially and the detected DCU chips tagged the connected devices. First, the control rings, each hosting several CCU modules, are powered individually through their corresponding Power Supply Units (PSU). All CCU modules that respond to communication via the I^2C bus are then mapped to the PSU. Then, several detector modules known as a power group are mapped to a single PSU, again by powering individual PSUs and using an I^2C broadcast to identify the powered devices.

The procedure that establishes the cabling of the optical link readout system, which connects

Table 1: Statistics of functional modules and fibre connections after the checkout and commissioning procedures.

Partition	TEC+	TEC-	TOB	TIB/TID	SST
Modules in system	3200	3200	5208	3540	15148
Functional modules	3189 (99.7%)	3198 (99.9%)	5196 (99.8%)	3487 (98.5%)	15070 (99.5%)
Fibres expected	7528	7552	12087	9067	36234
Connected fibres	7524 (99.9%)	7543 (99.9%)	12066 (99.8%)	9053 (99.8%)	36186 (99.9%)
Modules used	3175 (99.2%)	3144 (98.3%)	5106 (98.1%)	3422 (96.7%)	14847 (98.0%)

pairs of APV25 chips to individual readout channels of the FED boards, requires operating both the control and readout systems. The connections are determined by scanning through the front-end LLD chips that drive the signals in the optical fibres and configuring each one to produce a unique pattern that is observed only in the data stream of the connected FED channel. The procedure verifies the configuration of the Analogue/Digital Converters (ADC) in the FEDs and, more importantly, identifies problems in the cabling of the optical link system, such as broken, poorly connected, or dirty fibres. Again, the SST construction database is used as a reference.

Finally, the connections of the HV power supplies are tested. This is achieved by measuring the noise of individual detector channels, as described in Section 8. Biasing the sensors decreases their strip capacitance, which should result in a reduced detector channel noise. Modules exhibiting high noise values were tagged and the corresponding HV power supplies checked.

Table 1 summarises the number of functional modules and connected optical fibres, as determined by the checkout procedures. The most significant losses were of a complete control ring in the TIB and TOB. In the TIB, it was due to a single faulty CCU. The remaining CCUs on this ring have since been recovered by taking advantage of the redundancy in the control ring. In the TOB, the faulty control ring was slightly under-powered which led to instabilities. Additionally, individual modules exhibiting abnormal or unstable behaviour, mainly due to problems in the LV and HV power supplies, were identified and removed from the configured system. Table 1 shows the final numbers of modules used in the CRAFT data-taking period. The total number of modules used corresponds to 98.0% of the total system. The fraction of operational modules was subsequently improved to 98.6% after data-taking, once problems identified during checkout were investigated more fully (mainly the TOB ring recovery).

5 Relative synchronisation of the front-end

Relative synchronisation involves adjusting the phase of the clock delivered to the front-end so that the sampling times of all APV25 chips in the system are synchronous. Additionally, the signal sampling time of the FED ADCs is appropriately adjusted. This procedure accounts for differences in signal propagation time in the control system due to differing cable lengths. The precision of the relative synchronisation procedure, described here, and the absolute synchronisation to an external trigger, as described in Section 9, is important because signal amplitude is attenuated by as much as 4% per nanosecond misalignment in time, due to the narrow pulse shape in deconvolution mode.

This procedure is the first of several that use the tick mark feature of the raw APV25 data stream. Using the FED boards in Scope Mode, measurements of the delays required to align the system in time are possible using the tick mark feature. The complete tick mark pulse shape is reconstructed with a 1.04 ns step width by varying the clock phase using the PLL chip on each detector module, as shown in Fig. 3 (right). The ideal sampling point is considered

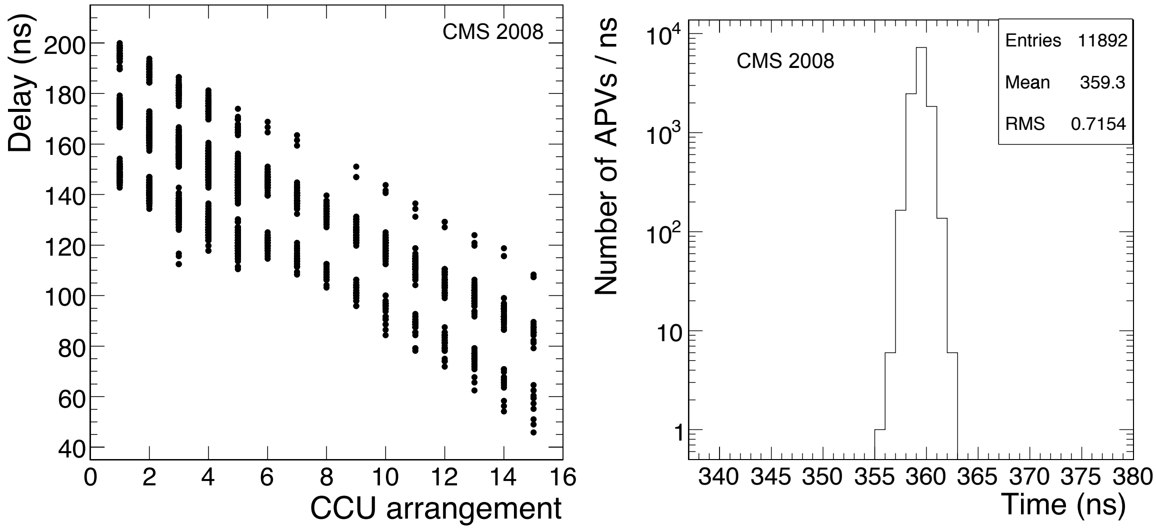

Figure 4: (left) Signal propagation times for each detector module in the TIB system as a function of its CCU position within the control ring. (right) Synchronisation of all modules in the TIB after the relative synchronisation procedure.

to be on the signal plateau, 15 ns after the rising edge of the tick mark. The required delays are thus inferred from the arrival times of the tick mark edges at the FED ADCs. The delay adjustments are applied at the level of a detector module and the precision of the procedure is typically better than a nanosecond. Differences in propagation times in the readout system are accounted for by using measurements from an optical time domain reflectometer to determine the required adjustment in the sampling times of the FED ADCs. This adjustment is made prior to synchronising the front-end.

Figure 4 (left) shows the signal propagation times for each detector module in the TIB system as a function of its CCU position within the control ring. The observed structure reflects the differences in signal propagation times in the control system: the three bands are due to three different fibre lengths used to connect the FECs to the TTC system; the gradient across the bins is due to the different positions of the CCUs within their control rings; and the spread for each group within a single bin is due to the different location of detector modules relative to their CCUs. Figure 4 (right) demonstrates the relative synchronisation of the TIB partition after performing the procedure; the RMS of the distribution is 0.72 ns and 99.9% of APV25 chips are synchronised to within 2 ns of the median value. The largest deviation is 4 ns, which corresponds to a maximum signal attenuation of $\sim$16%.

6 Calibration of the readout system gain

One of the largest contributions to gain variation in the readout system is the distribution of laser output efficiencies caused by the variation of laser-to-fibre alignment from sample to sample during production of the transmitters. In addition some loss may have been introduced at the three optical patch panels in the fibre system, despite careful cleaning of optical connectors during integration. Changes in the LV power supply or enviromental temperature can also significantly affect the gain at the level of a FED readout channel. The variations of laser output are comfortably within the link design specifications and there is ample provision for balancing gain in the system, such as on the LLD chips.

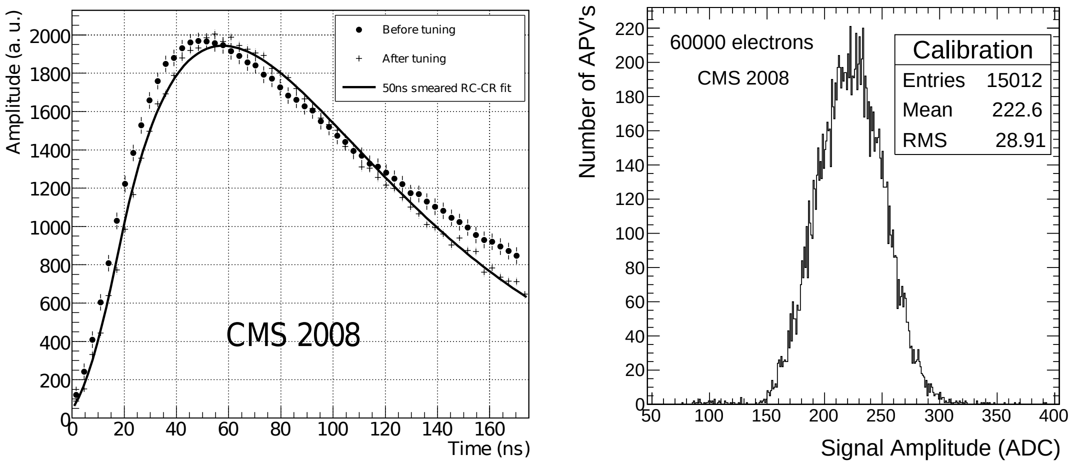

Figure 5: (Left) An example of the CR-RC pulse shape of a single APV25 chip, before and after the pulse shape tuning procedure. (Right) Pulse height measurements using the on-chip calibration circuitry of APV25 chips in the TEC+.

The procedure aims to optimise the use of the available dynamic range of the FED ADCs and also equalise the gain of the entire readout system. This is achieved by tuning the bias and gain register settings of the LLD chip for individual fibres. Four gain settings are possible. The amplitude of the tick mark, which is assumed to be roughly constant in time and across all APV25 chips within the system, is used to measure the gain of each readout channel. The setting that results in a tick mark amplitude closest to 640 ADC counts is chosen, as this amplitude corresponds to the expected design gain of 0.8. After tuning the system, a spread of $\pm 20\%$ is observed, which is expected due to the coarse granularity of the LLD gain settings (factors 1, 1.5, 2, and 2.5).

The response of all detector channels can be further equalised during offline reconstruction by correcting the signal magnitude by the normalisation factor $f = 640$ ADC counts $/a_{\mathrm{tickmark}}$, where a_{tickmark} is the tick mark amplitude in ADC counts. The tick mark amplitude is a good indicator of the maximum output of the APV25 chip, which corresponds to a charge deposit of 175 000 e^-. This method provides a calibration factor of 274 ± 14 e^-/ADC count, which permits the precise determination of signal and noise amplitudes in terms of electrons. The estimated systematic uncertainty is 5%, attributable to the sensitivity of the tick mark amplitude to variations in the LV power supply and environmental temperature [6].

This procedure was performed whenever there were significant changes in the tracker environmental temperature ($> 5^{\mathrm{o}}$) or in the hardware configuration. Signals from LHC pp collision data are expected to provide a more precise calibration and also account for the gain of the analogue stages of the APV25 circuitry [9].

7 Tuning of the APV25 front-end amplifier pulse shape

The shape of the CR-RC pulse from the APV25 pre-amplifier and shaper stages is dependent on the input capacitance, which depends on sensor geometry and will evolve with total radiation dose (and therefore integrated luminosity).

The tuning of the pulse shape uses dedicated on-chip calibration circuitry, which simulates a detector signal by injecting charge into the APV25 pre-amplifier stage. The injection time can be skewed in steps of 3.25 ns in order to reconstruct the full CR-RC pulse shape. Two registers are available to set the currents and bias voltages necessary to power the pre-amplifier and shaper stages, which change the shape.

By default, all APV25 chips are configured with pre-defined settings appropriate to the sensor geometry, based on laboratory measurements [27]. However, non-uniformities in the fabrication process result in a small natural spread in the pulse shape parameters, and the environmental temperature also affects the optimum parameter settings, so these defaults must be tuned. This is particularly important for performance in deconvolution mode, which is highly sensitive to the pulse shaping. In order to maximise the signal-to-noise ratio and confine the signal to a single bunch crossing interval, the rise time must be tuned to 50 ns and the signal amplitude at 125 ns after the signal maximum should be 36% of the maximum. By tuning the rise time, this reduces the timing uncertainties associated with the synchronisation procedures. Figure 5 (left) demonstrates how the pulse shape of an APV25 can be improved by the procedure. Two-dimensional scans through the register settings allow selection of optimal pulse shaping parameters.

The charge injection provided by the calibration circuit is known with a precision of 5%, which can be used to calibrate the detector signal amplitude. Figure 5 (right) shows the pulse height amplitude (in ADC counts) observed for a charge injection of 60000 e^- using the on-chip calibration circuitry. The charge was injected on all individual detector channels within the TEC+ partition. A mean signal of 223 ADC counts with a RMS of 29 ADC counts was observed, giving a calibration factor of $269 \pm 13\,e^-/\mathrm{ADC}$ counts. This measurement is compatible with the calibration based on tick mark amplitudes, described in Section 6, which yields $274 \pm 14\,e^-/\mathrm{ADC}$ counts.

8 Calibration of the detector channel pedestals and noise

The mean level of the pedestals for the 128 channels of a given APV25 chip, known as the *baseline* level, can be adjusted to optimise the signal linearity and the use of the available dynamic range of the APV25. The baseline level for each APV25 chip is adjusted to sit at approximately one third of the dynamic range.

Following this baseline adjustment, the pedestal and noise constants for each individual detector channel must be measured, as these values are used by the zero-suppression algorithms implemented in the logic of the FED FPGA chips.

Pedestals and noise are both measured using a random, low frequency trigger ($\sim$10 Hz) in the absence of signal. Pedestals are first calculated as the mean of the raw data in each detector channel from a large event sample. Once known, they are then subsequently subtracted from the raw data values for each event. Common mode offsets are evaluated for each APV25 chip per event by calculating the median of the residual (pedestal-subtracted) data levels. The median value is then subtracted from each channel. The noise for each detector channel is then defined to be the standard deviation of the residual data levels, which can be calibrated using the measurements described in Sections 6 and 7.

Figure 6 (left) shows a distribution of the mean noise measured per APV25 chip, for TOB single side layer 3. The outliers correspond to APV25 chips from modules with unbiased sensors, due to problems in the HV power supply.

Modules with different sensor geometries are studied separately to account for the different strip lengths and pitch adapter layouts that affect the input capacitance. The mean normalised noise measured for the different sensor geometries are summarised in Table 2. Fitting the mean

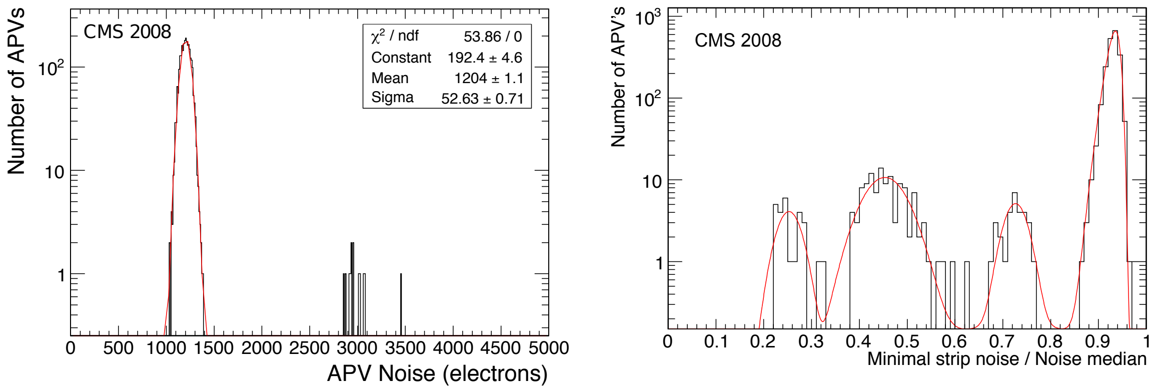

Figure 6: (Left) Mean calibrated noise for individual APV25 chips on modules in the TOB single side layer 3. (Right) The ratio of minimum noise to median noise per APV25 chip. The distinct populations reflect the different noise sources within a module.

Table 2: Summary of the mean normalised noise for each type of sensor geometry.

Partition	Strip length (cm)	Total noise (e^-)	Pitch adapter (e^-)	Bare APV (e^-)
TEC Ring 1	8.52	757	421	245
TEC Ring 2	8.82	791	434	265
TEC Ring 3	11.07	832	450	250
TEC Ring 4	11.52	843	437	257
TEC Ring 5	14.44	1024	461	265
TEC Ring 6	18.10	1097	513	270
TEC Ring 7	20.18	1146	510	258
TOB Layers 1-4	18.32	1184	583	254
TOB Layers 5-6	18.32	1205	538	261
TIB Layers 1-2	11.69	925	454	265
TIB Layers 3-4	11.69	851	445	256

noise versus silicon strip length, the following parameterisation is obtained:

$$noise(e^-) = (427 \pm 39) + (38.7 \pm 3.0) \times length(cm)$$

This is compatible with the measurement performed during the SST integration period, prior to installation [1].

The individual sources of noise on the detector module can be identified and measured by plotting the ratio of the minimum to the median noise value for each APV25, as shown in Fig. 6 (right). The ratio takes advantage of the fact that broken wire bonds on the detector modules effectively reduce the input capacitance to individual channels of the APV25 chips. Broken wire bonds can occur between (in ascending capacitance order): the APV25 and pitch adapter; the pitch adapter and silicon sensor; and sensors in two-sensor modules. Fitting to the first three populations, corresponding to the previous broken wire configurations, provides an estimate of different noise contributions. The fourth population corresponds to modules with no broken wires. The noise estimate for bare APV25 chips is compatible with the design specifications and laboratory measurements [1].

Complementary to the noise measurements above, non-Gaussian noise behaviour can be identified and the associated detector channels masked. For each individual detector channel, the residual data (after subtraction of the pedestal and common mode values) were accumulated and fitted with a Gaussian distribution. In addition to studying the χ^2 probability, a

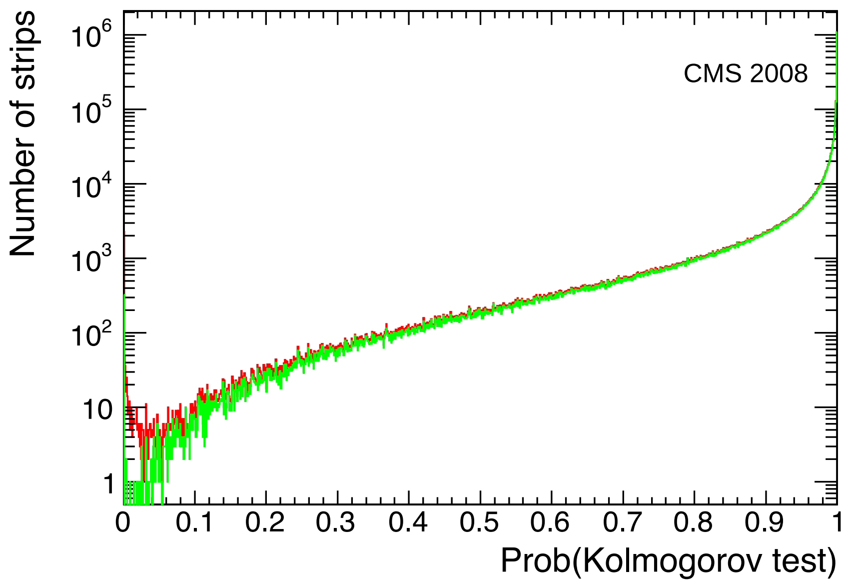

Figure 7: results for all detector channels (red) and channels where a Gaussian fit of the strip signal has a $Prob(\chi^2) \geq 0.1$ (green).

Kolmogorov-Smirnov test was performed on the positive tails of both the noise distribution and a Gaussian distribution with a central value and width equal to the measured mean and RMS of the data, respectively. Figure 7 shows the Kolmogorov probability for all detector channels. Very few detector channels ($\sim$0.1%) had a probability below 5 %, therefore failing the Kolmogorov-Smirnov test. Further studies revealed that most rejected channels belonged to a limited number of APV25 chips. Thus, a combined probability was constructed from the 20 channels exhibiting the least Gaussian-like behaviour per APV25 chip. A 2% cut on this combined probability was applied to reject entire APV25 chips. Using this method, an additional 29 APV25 chips were removed from the analysis.

9 Absolute synchronisation to an external trigger

The last two commissioning procedures concern the synchronisation of all modules in the SST with the Level-1 trigger of CMS. This was done using a dedicated technical trigger provided by the Muon Drift Tube sub-detector [28], based on a coincidence between centrally-located top and bottom chambers. The procedure requires track reconstruction and the analysis was performed offline [27]. Absolute synchronisation accounts for both the delays introduced by the hardware configuration and the effects due to the time-of-flight of particles.

The first of the two procedures is a coarse scan in time, in steps of 25 ns, by adjusting the latency between the trigger arrival and the sampling time of the APV25 chip. The mean signal of the channel with the largest signal amplitude (*leading strip*) in clusters associated to reconstructed tracks was extracted as a function of the latency. The signal magnitude was corrected for the track path length through the active sensor volume, inferred from the track angle. The measurement was performed for the tracker as a whole (rather than for individual partitions). Unfortunately, it was discovered after data-taking that an incorrect trigger cable length for the TOB was used in the calculation. This resulted in adjustments to the hardware configuration such that the detector modules in the TOB received an out-of-phase clock signal, shifted by 12.5 ns with respect to the other partitions. Since the statistics collected in the TOB dominated the measurement, the adjustments were done relative to the TOB results. TIB and TEC- were

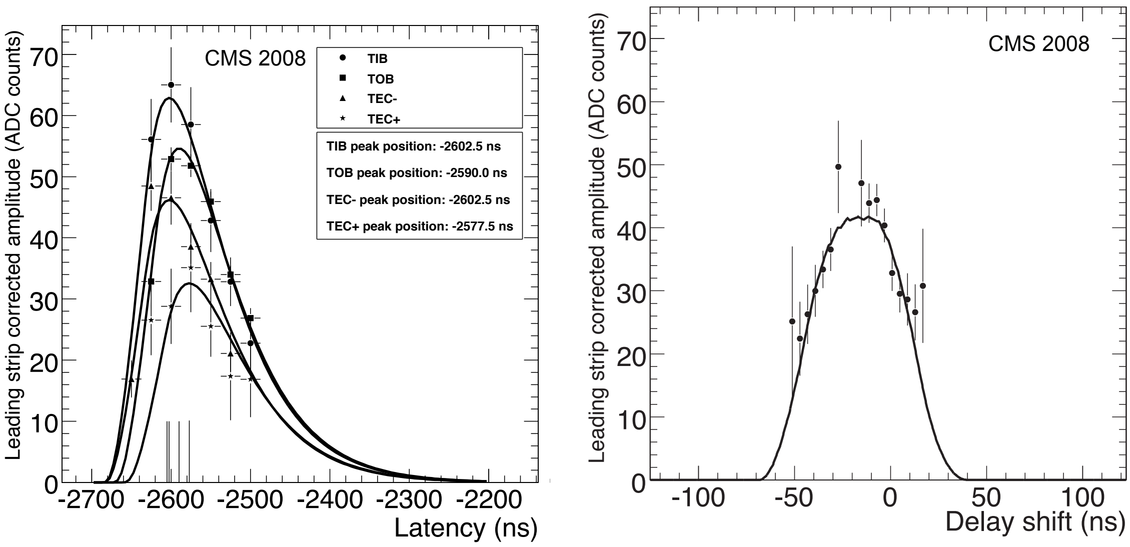

Figure 8: (Left) Mean signal of leading strip in clusters associated to tracks as a function of the latency (25 ns steps), for each of the four partitions. (Right) Fine delay scan for the TOB layer 3, in deconvolution. The mean position (-14.2 ns) is including the mean time-of-flight of particles from the muon system to the silicon sensors (12 ns).

Table 3: Signal amplitude correction factors for each partition to account for limitations in the synchronisation procedures used during CRAFT. The uncertainty accounts for a 3 ns resolution on the ideal sampling time and includes residual time-of-flight effects in the tracker volume.

Partition	Correction Factor
TIB/TID	$1.018^{+0.012}_{-0.009}$
TOB	$1.0013^{+0.0065}_{-0.0012}$
TEC+	$1.058^{+0.032}_{-0.023}$
TEC-	$1.018^{+0.012}_{-0.009}$

shifted by 12.5 ns and TEC+ by -12.5 ns, as shown by the fits in Fig. 8 (left). Time-of-flight is not taken into account in this procedure, since the variations expected across the detector ($\leq$10 ns with cosmic ray muons, 5 ns in collisions) are lower than the target precision of 25 ns.

The last procedure comprises a fine tuning of the synchronisation and was not performed until the very end of the CRAFT data-taking period. It involves skewing the clock delay in steps of 1 ns around the expected optimal value for all modules of a given test layer, with the configuration of all other modules in the SST unchanged with respect to the value obtained from the coarse latency scan. Clusters on the test layer compatible with a reconstructed track are used to reconstruct the pulse shape. Figure 8 (right) shows the resulting pulse shape from clusters found in modules of TOB layer 3, acquired in deconvolution mode. With collision data, the time-of-flight can be adjusted for each individual track, but this is not the case for cosmic ray muons, for which the jitter from the trigger cannot be subtracted. The 14 ns shift observed is consistent with the expected time-of-flight (12 ns) of cosmic ray muons from the Muon Drift Tube chambers to the TOB layer 3.

From the analysis of latency and fine delay scans, correction factors can be computed to compensate the residual mis-synchronisation of each partition. These factors are presented in Table 3. They correspond to the ratio of amplitude at the expected working point and at the maximum of the CR-RC curve, and have to be used to correct the cluster charge used in calibration and $\frac{dE}{dx}$ studies reported elsewhere [9].

10 Summary

The period of detector commissioning prior to the CRAFT data-taking exercise in summer 2008 was an important milestone for the SST towards final commissioning with colliding beam data.

The control, readout and power supply systems were successfully checked out using automated procedures. The total number of detector modules used during CRAFT corresponds to 98.0% of the total system.

The ten million channels of the SST readout system were synchronised relative to one another with a precision of better than 1 ns. The SST detector was then synchronised to the Level-1 Trigger with a precision of better than 25 ns, which was sufficient to provide efficient hit reconstruction for the mode of operation used during CRAFT. The gain and noise performance of the readout system was also measured, which was excellent and consistent with the original design specifications.

The SST was subsequently operated in global runs with all other detectors of the CMS experiment [8]. About 15 million events with a cosmic ray muon passing through the tracker were collected. The SST performance was excellent, with signal-to-noise ratios greater than 25 and 31 for thin and thick modules, respectively, and both hit and track reconstruction efficiencies were higher than 99% [9]. This demonstrates that the goal of the detector commissioning procedures, to provide efficient signal identification for in-time particles, was achieved.

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