The Development of Photo-Detector Module Electronics for the JEM- EUSO Experiment

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Abstract: The JEM-EUSO focal surface detector consists of about 300,000 photodetector channels that are organized into 137 building blocks called Photo-Detector Module (PDM). A PDM is composed of 36 64-ch MAPMTs, analog ASICs, and digital electronics. The digital electronics, called PDM board, is in charge of readout of 36 MAPMTs via ASICs, control of ASICs via JEM- EUSO central data acquisition system, Level-1 trigger with decision every JEM-EUSO time unit of 2.5 μ s, and buffering of a complete event of Extreme Energy Cosmic Rays typically lasting 200 μ s. On positive trigger, the data of 8 adjacent PDMs is transferred to Cluster Control Board where Level-2 trigger is processed to refine the selection of interesting events. We expect the rate of Level-1 trigger is designed to be 7 Hz with 2 kHz of input data. We present the development of the PDM board for the JEM-EUSO experiment.

Keywords: JEM-EUSO, Ultra High Energy Cosmic Rays (UHECR), Trigger

1 Introduction

The JEM-EUSO space mission is devoted to the detection of Extreme Energy Cosmic rays (EECRs) including neutrinos by looking downward from the International Space Station [1,2,3]. The JEM-EUSO telescope is based on double Fresnel lens optics with a large diameter (about 2.5m) and a wide (±30°) field of view (FoV). The focal surface system identifies the track of UV photons generated by UHECR with an angular resolution of 01. Degrees thanks to a fast (~μ s) and highly pixellated (~3x105 pixels) digital camera which works in single photon counting mode. Details of the optics are described elsewhere.

The focal surface (FS) of JEM-EUSO has a spherical shape with about 2.7 m curvature radius, covered with about 5,000 64-channel (8x8) multi-anode photomultiplier tubes (MAPMTs). The FS detector consists of Photo-Detector Modules (PDMs), each of which consists of nine Elementary Cells (ECs). The EC contains four units of the MAPMTs. The FS accommodates 137 PDMs. Details of the focal surface detector are described elsewhere [4]. The FS electronics system records the signals of UV photons generated by cosmic rays with high trigger efficiency and reasonable linearity in the range of 1019-1021 eV. Power consumption per channel is required to be less than 2.5mW to accommodate the 3x105 signal channels within the power budget of 1 kW.

Figure 1 shows an overview of JEM-EUSO readout, trigger and control architecture. Anode signals of the MAPMTs are counted and recorded in buffers for each GTU (Gate Time Unit~2.5 μ s) to wait for a trigger. The PDM (Photo-Detector Module) electronics receives digitized data from frontend ASIC [5] and transmits to CCB (Cluster Control Board) [6] on positive triggers. PDM is connected electrically to 9 EC boards each consisting of 4 MAPMTs. The FS system is built with 137 PDMs and

therefore 2304 MAPMT channels in total. On triggering from a PDM, 8 adjacent PDMs are subject to transfer the data kept in their buffers to a CCB through high speed data protocol. PDMs are independent each other, which implies that there is no communication between PDMs. Therefore, system clocks, configuration of ASIC, run control including overall data transfer, and housekeeping (HK) should be provided to each PDM by higher level systems of CPU through CCB, as shown in Figure 1. The required clocks [7] are 40 MHz for subsystems not only PDM electronics but also frontend ASIC and 400 kHz that is the clock of the JEM-EUSO GTU.

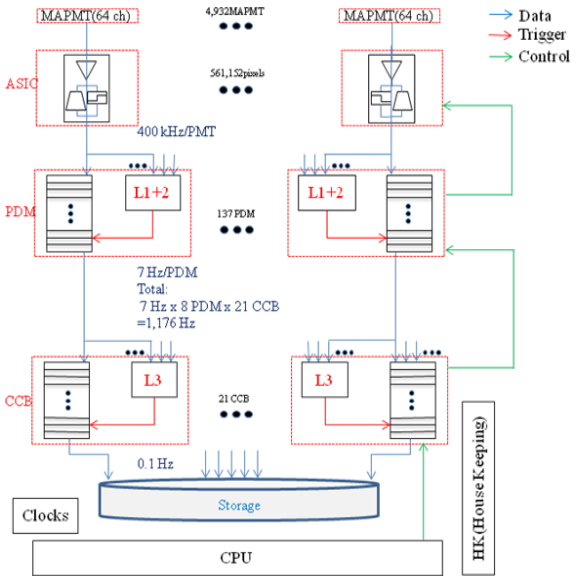

Figure 1. JEM-EUSO trigger, readout and control architecture.

In JEM-EUSO a hierarchical trigger [8] scheme has been investigated for effective reduction of raw data of ~10 GB/s down to 297 kbps, which meets the requirement of the limit in data transfer to the ground. The data reduction is made first at the PDM electronics with Level 1 (L1) trigger processor. Input rate is expected to be 400 kHz, while output is 7 Hz, so reduction of factor 6×104 is required from the trigger electronics of PDM. As shown in Figure 1, Level 2 (L2) trigger is carried out by the CCB, and described in [6]. The L1 trigger latency within PDM is expected to be only 1 GTU, 2.5 μ s, which means that the trigger decision will be made every GTU. The EECR trigger will be issued typically around its shower maximum, and thus the PDM needs data buffer of about 128 GTUs to hold the data of the entire shower profile, before and after, the decision of L1 trigger. Four L1 trigger modes are under development: a) Normal mode with a GTU of 2.5 μ s for routine data taking of EAS, b) Slow mode with a programmable GTU up to a few ms, for the study of meteorites and other atmospheric luminous phenomena, c) Detector calibration mode with a GTU value suitable for the calibration runs, and d) LIDAR mode with a GTU of 200 ns. Details of the FS electronics system are described in [9].

2 Requirements

The hardware of PDM electronics includes FPGA (Field Programmable Gate Array) chips and interfaces to ASIC and CCB, and thus a large number of connector pins is foreseen. Another major limitation in the design of PDM electronics comes from power consumption which is about 1.5 Watts per PDM. Therefore, the selection of FPGA chips is a non-trivial issue because power consumption, number of I/O pins enough for a large number of data transfer lines from ASICs and to CCB, space qualification for at least three years of operation in space, number of logic cells enough for of complex trigger algorithms, and cost of space grade chips must be taken into account all together.

Power consumption: Most power consumed device in the PDM electronic is FPGA. The most popular species are the ones of Xilinx, ALTERA, and ACTEL. The JEM-EUSO is considering one of ACTEL families because of its long space heritage, low power consumption. The limitation in memory size of ACTEL might be overcome with an external memory.

Clocks: The clocks, 40 MHz and 400 kHz, are received from CCB and distributed to ASICs as well. The 400 kHz clock is GTU clock and is necessary for data transfers among ASIC, PDM and CCB. The 40 MHz clock is used as an internal system clock for a various calculations and data handlings in PDMs.

Physical dimension of the PDM boards: As shown in Figure 2 (bottom right), the PDM electronics is built with 6 boards maximum, each 120mm×135mm in size where 100mm×115mm will be used for devices mount. Three boards are equipped with multi-pin connectors because the PDM needs a relatively large number of I/O pins, about 500 I/O, to connect to 9 EC boards and a CCB. The mass of 145 gram is allocated for a PDM electronics board.

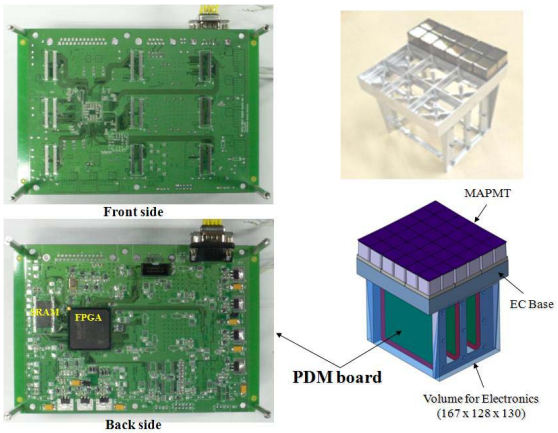

Figure 2. Fabricated PDM prototype board (left). PDM structure [10] and MAPMTs (upper right corner). PDM includes MAPMTs, EC boards and PDM board (bottom right corner).

Thermal: The required temperature for the operation of PDM is between -30°C and 50°C, so associated electronic parts should meet this standard. The PDM might be

turned off at the temperature out of range to protect itself against any possible damages.

Data rate: PDM has an input data from ASIC at the rate of 400 kHz. PDM is subject to lower the data rate down to 7 Hz that is output to CCB. So the factor of data reduction via Level 1 trigger is expected to be about 6×104.

Threshold tuning against backgrounds: As seen in Figure 3, backgrounds are different by about factor three in PDMs ranging from the center to the edge of the FS. Therefore, thresholds for trigger should be set differently depending on the location of PDMs. Those thresholds might be recalibrated and reset in space by uploading relevant parameters from ground and to take into account the varying conditions of the nightglow background.

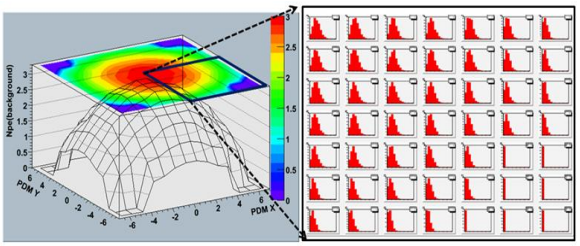

Figure 3. Simulation of background distribution in terms of number of photo-electrons/GTU/pixel (Npe) on FS (left) and for each PDM (right).

3 Design of the PDM board

The physical layout of PDM has been shown in Figure 2 (right), where the mechanical frame [10] is designed to hold 6 boards in total. Three boards are of a primary set of the PDM electronics, while the other three of a redundancy set. A board is dedicated for placing FPGAs. Connectors for cables interfacing to ASIC and CCB are mounted on the other two boards. The same power lines are connected to primary and redundancy boards, but only a set of boards are selected at a time by a switch. The redundancy boards might be switched to by issuing a special command from ground if necessary.

The schematic layout of the PDM board is shown in Figure 4 (left). The main functional blocks are as follows: ASIC for the reception of photon counting data from ASIC, KI for the reception of charge to time data from ASIC, PDM(FPGA) for logics of trigger, data readout and control, CCB for the transmission of triggered data to CCB, HK for the interface to HK for slow control monitoring [11], CPU for the interface to CPU that is the main control, PC interface for the interface to PC for standalone tests, POWER for the interface to JEM-EUSO PDM power supply, and PROM/JTAG for the download of FPGA codes.

Figure 4 (right) shows the functional blocks of the PDM FPGA which include trigger calculation unit, control of the PDM board and interfaces of ASIC, CCB, CPU and HK. Those units are briefly described as follows: SC (System Control) for the control of PDM system for operation, ABIU (ASIC Bus Interface Unit) for the interface between ASIC and PDM by customized communication, CBIU (CCB Bus Interface Unit) for the interface between PDM and CCB by customized or commercial communication, HIU (HK Interface Unit) for the interface between PDM and HK, CIU (CPU Interface Unit) for the interface between PDM and CPU, TU (Trigger Unit) for the decision of the best trigger from simultaneous trigger signals, DPU (Data Processing Unit) for the processing of PDM data, CRU (Calibration Run Unit) for the control of calibration run, RS (Run Summary) for creation of run summary.

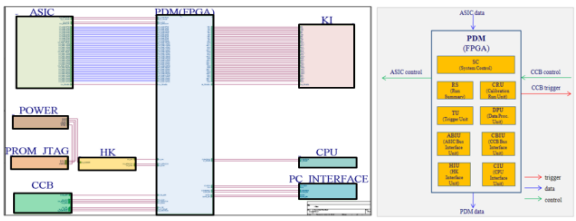

Figure 4. The schematic layout of the PDM board (left) and the functional blocks of the PDM FPGA (right).

4 PDM interfaces to ASIC and CCB

A PDM oversees 9 ECs, as shown in Figure 2 (right), and each EC board built with 4 ASICs supports 4 MAPMTs. As described earlier, two boards of PDM are equipped with connectors which receives data from ASIC, relays controls and powers to ASIC. At the beginning of power on, ASICs will be configured via a number of configuration control lines by PDM. The data from ASICs to PDM are two folds: one is photon counting data and the other KI data that is summed charge information of 8 MAPMT channels. On the other hand, each ASIC provides its prompt trigger signals which are useful for PDM to see any significance in photon counting and KI data in prior to waiting or collecting the data every GTU, which might save the power consumption of PDM. Such fast signals can be used for triggering of fast and/or large intensity event like TLEs and Cerenkov from neutrinos.

The PDM-CCB interface is similar to ASIC-PDM such that 8 PDMs are connected to a CCB as described in earlier. When any of 8 PDMs fires a Level-1 trigger, the PDM notifies the CCB which subsequently requests data transfer to the group of 8 PDMs physically neighboring each other. Although Level 1 trigger latency is 1 GTU, but the decision is made near the maximum of EECR shower, which implies that the data buffer of at least a full event is required in PDM, which is about 128 GTU, equivalently 320 μ s. Therefore, total data size per PDM to be transferred to CCB is about 2.7 Mbits (= 64 ch × 8 bit × 36 PMTs × 128 samples, plus 12% additional data from the analog part - KI). The trigger output is designed to be 7 Hz per PDM, so a CCB foresees 56 Hz of input from 8 PDMs. Assuming the transfer rate from PDM to CCB via 40 MHz, it takes about 0.07 s (2.7 Mbits / 40 MHz) or 27,000 GTU per line. However, the dead time fraction of data taking will be minimized by employing a double buffering method; a buffer for data taking and the other for data transfer to CCB.

5 The PDM prototype board

The prototype board has been built as shown in Figure 2 (left) and tested mainly for interfacing to ASIC and implementation of reduced version of trigger algorithms. The USB-8451(NI) is used for the control and data transfer via PC. The test is successful as expected from the design. The PDM sends 40 MHz and GTU clocks to ASIC, then ASIC issues a series of loading of 8 bit data to be transferred to PDM. Total 64 pixels photon counting data are received at PDM via 8 lines. A text file of the data is sent from ASIC to PDM, and opened at PC, where each of 8 lines receives 8 bits data. The next step is to test the transfer of data to CCB and to implement the full Level 1 trigger algorithm in FPGA.

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