SURVEY OF LLRF DEVELOPMENT FOR THE ILC*

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Abstract

The key to a successful LLRF design for the International Linear Collider (ILC) relies on a combined effort from the different laboratories involved in this global project. This paper covers the ILC LLRF design progress both long term and for current test facilities around the world. The SIMCON controller board, originally developed at DESY has been successfully used at FNAL to control superconducting capture cavity I and II. LLRF team leaders from DESY, KEK and FNAL have worked together toward a common design and costing estimate for the ILC LLRF. This paper gives a general overview of the LLRF development achieved through continuous collaboration and communication between the various labs involved in the ILC LLRF design process.

INTRODUCTION

The DESY effort at the Tesla Test Facility (TTF) has been underway for many years since the design proposal was first issued in 1992 [1]. Nowadays, the Free Electron Laser facility in Hamburg (FLASH) provides a lot of experience for driving a multi cavity cryomodule with a single klystron, and also serves as a pilot experiment for the future X-Ray laser project (XFEL). Simultaneously, the A0 test facility at Fermilab has been devoted to acquiring experience with superconducting cavities (Capture Cavity I or CCI). About a year ago, another superconducting cavity was installed at Fermilab (CCII) where high gradients (~31.5 MV/m) were achieved, for a flattop length of 800 μs. Recently, the Horizontal Test Stand (HTS) was assembled at FNAL to prove the working principle of gradient testing for ILC-type cavities. At KEK, the ILC R&D facility is the Superconducting RF Test Facility (STF). In STF-phase 1, a cryomodule with 8 cavities will be installed, as well as an RF gun. The cavities will be driven by a single high-power klystron (10 MW). In STF-phase 2, an additional two cryomodules will be added to the beam line.

An overview of the LLRF R&D progress achieved in each laboratory is presented in the following sections.

DESY OVERVIEW

To improve the latency and processing power of the LLRF system at FLASH, DESY started replacing the existing DSP based field controllers by new FPGA boards. This choice was motivated by recent breakthroughs of FPGA devices achieving comparable computing power and shorter latency than DSP processors. The R&D effort led by DESY in collaboration with the universities of technology at Warsaw and Lodz in Poland produced a multi purpose FPGA based controller, the SIMCON board [2]. It is based on a Virtex II Pro FPGA, has ten 14 bit ADCs and 4 DACS, external SRAM and multiple IO interface. In 2006, the SIMCON3.1 was successfully used to control the RF gun at FLASH. Replacing the DSP hardware with the SIMCON controller reduced the latency in the digital processing section of the signal chain, allowing for a maximum feedback gain around 3 [3]. The SIMCON3.1 board was also used to control an 8 cavity TESLA cryomodule (ACC1 at FLASH). Switching to the FPGA controller decreased the overall latency and increased the possible loop gain by a factor of 2 [3]. This allowed for adding new features to the control algorithm, such as beam load compensation and adaptive feed forward.

The next generation of digital controller improves the current SIMCON3.1 design by adding an on-board DSP processor to handle floating point operations and perform pulse to pulse algorithms. This will free up some space for the FPGA to handle fast loop controls and signal processing during the RF pulse. Controlling several cryomodules, summing up to 24 cavities per RF station will require the use of several SIMCON controllers. Future plans include distributing the algorithms to the different SIMCON boards. Communication between the distributed systems will be done using gigalink I/Os and using the SIMCON4.0 concentrator board [3] to distribute and gather data.

Similar to the ILC requirements, the operational goals of the European X-FEL require more than 90% uptime, which imposes an availability of more than 99% on the LLRF system. This high availability requirement presents both a hardware and software challenge. The choice was made at DESY to pursue the industrial standard solution of Advanced Telecom Computing Architecture (ATCA) and microTCA (μTCA) as attractive alternatives to the VME or VXI standards. Hence the next generation of SIMCON controller will follow the ATCA standard.

Ongoing effort at DESY is also targeted toward designing software that meets the high availability requirements [4]. This includes low latency algorithms, which is supported by the massive parallel processing in the FPGAs, exception handling and build-in diagnostics, beam based feedback, redundancy, and remote control ability. Due to the large number of cavities involved in this project, automation of operations and calibrations is another crucial point which is currently looked into. This applies to field vector measurements, but also loaded Q

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and cavity tuning, vector sum and cavity phase calibrations as well as klystron linearization.

The experience gained at FLASH gives a precious insight of the challenges inherent to designing a LLRF system for a high gradient, high precision, high availability, 20,000 cavity accelerator.

KEK OVERVIEW

This section provides an overview of the LLRF R&D effort at KEK. A detailed description of the LLRF system and its performance is presented in [5]. The LLRF system for STF is based on the JPARC linac LLRF system [6]. The targeted RF stability in amplitude and phase is 0.3% and 0.3° respectively [5]. This system consists of a master oscillator (MO) unit, an up and down converter, an FPGA board, a DSP mezzanine board and an I/O board. The MO provides the RF reference, the LO and the clock signals. The jitter is found to be 0.01° at 1310 MHz, integrated from 100 Hz to 1 MHz. The up and down converter unit has ten active mixers (AD8343) and two IQ modulators (AD8349) and converts to and from IF = 10 MHz. The 10 channel digital controller was developed by KEK and is based on a Xilinx Virtex II Pro FPGA. It has ten 16-bit ADCs from Linear Technology (LTC2204) and two Analog Devices 14-bits DACs (AD9764). The sampling rate of the ADCs is 40 MHz. A 4000-point FFT of the digital IF is shown in Fig.1. To evaluate the performance of the digital feedback system, cavity simulators including Lorentz force detuning and beam effects have been developed using commercial FPGA boards. First results using PI control show amplitude and phase noise of ± 0.05% and ± 0.03° respectively.

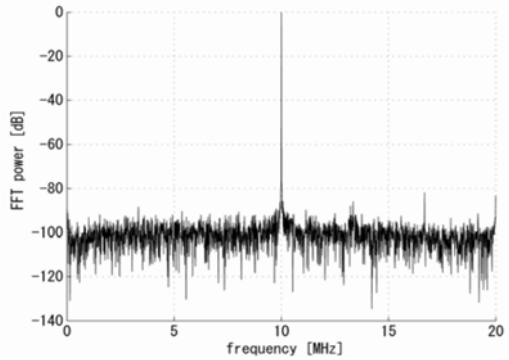

Figure 1: 4000-point FFT of the digital 10 MHz IF signal.

To deal with the large signal density issue, KEK is currently investigating a multi-intermediate frequency scheme [7]. This approach consists of down converting several RF signals to different IFs, and combining these IF signals before sending them to the FPGA controller. This scheme reduces the number of ADCs and traces on the main controller board. The combined IF signal is then digitized using a single ADC and the individual IF signals are reconstructed inside the FPGA. KEK is currently testing this scheme for a combination of two different IF signals defined as $IF_1 = f_s / N_1$ and $IF_2 = f_s / N_2$, where f_s is the ADC sampling rate. The combined IF sequence is then averaged on N_1 or N_2 consecutive samples to restore the individual signals. In-phase (I) and quadrature (Q) components are then obtained by multiplying the reconstructed signals by the corresponding cosine and sine functions, and averaging over N_1 (N_2, respectively) components. The total latency associated with this combined IF scheme is (N_1+N_2)/IF.

Future plans include extending this scheme to more than two signals. More work is needed to fully characterize the signal degradation and process overhead associated with reconstructing the signals. Down converting the RF signals to different intermediate frequencies also increases the complexity of the LLRF system.

FNAL OVERVIEW

Fermilab started off with using the DESY LLRF design based on the SIMCON controller card. A0 superconducting cavity (CCI) has been successfully controlled using the SIMCON board, version 2.1. The following generation of SIMCON board designed at DESY, the SIMCON version 3.1 has also been integrated to our system. Along with the hardware upgrade, development on the controls interface also took place. For development purposes, Fermilab started off from a MATLAB® based controls environment. In collaboration with DESY, a more robust controls interface based on DOOCS was developed at Fermilab and successfully used both at the CCI and CCII test areas.

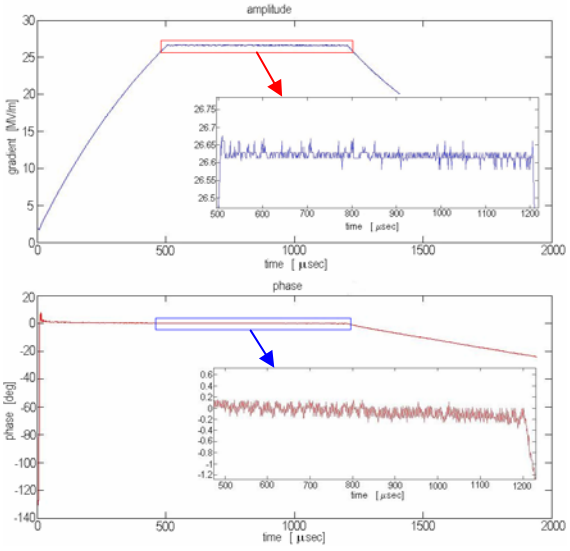

Figure 2: Amplitude and phase plots, obtained with the 13 MHz IF, at 26.6 MV/m with a feedback gain of 30.

To improve the signal to noise ratio characteristic of the LLRF system, the decision was made to move away from the 250 kHz Intermediate Frequency (IF) to a non IQ sampling scheme at a higher frequency. A 13 MHz IF receiver was designed at FNAL, down converting the cavity probe signal and a 1.3 GHz reference signal to the new IF [8]. This receiver was successfully used at CCII and additional units are to be used for other LLRF systems at Fermilab at the New Muon Laboratory (NML) or to control the 3.9 GHz copper cavity at A0. Moving to

a higher IF improved the noise performance on the digitized I and Q signals. This is illustrated in Fig.2, showing the amplitude and phase plots obtained at a flat top gradient of 26.6 MV/m with a feedback gain of 30. The zoomed windows show an RMS noise of 0.06% in amplitude and 0.07° in phase.

In an effort to further improve the system noise performance, Fermilab worked on a new layout for the SIMCON 3.1 board, migrating from a VME32 to a VME64 standard. The analog front end has been modified using dual channel 14 bit ADCs, optional DC coupling and replacing the input differential amplifiers with RF pulse transformers. The power distribution has been modified using a combination of DC-to-DC converters and regulators to minimize the noise, the main FPGA has been upgraded from a Xilinx Virtex II Pro to a Virtex IV and the clock distribution has been redesigned for lower jitter and better layout. The ADCs are sampling at 54.17 MHz using a differential LVPECL external clock. Preliminary results show a SNR of 79 dB and an ENOB of 13.1 bits, as illustrated in Fig.3, showing a 8K point FFT of a 50 MHz signal, sampled at f_s = 78.125 MHz.

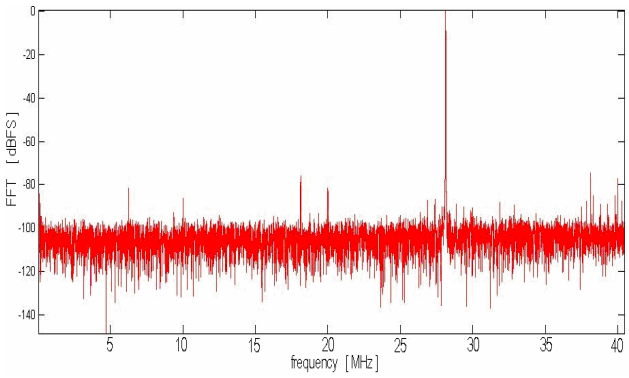

Figure 3: 8K point FFT of a 50 MHz signal

In a parallel effort, Fermilab aimed at integrating and modifying the SIMCON firmware originally developed at DESY, to accommodate for this higher IF scheme. The down conversion to base band is now performed by a Numerically Controlled Oscillator (NCO) followed by a CIC filter. A combination of Simulink® and Sysgen® tools has been successfully used to build off the original VHDL firmware and implement the additional features mentioned above.

In the current ILC design, one RF station serves three cryomodules, accommodating a total of 26 cavities. For each cavity, the RF station needs to control the forward power and monitor the reflected and the transmitted power signals. This sums up to 3×26 = 78 signals per RF station. Other LLRF signals include controls and read back signals for the fast piezoelectric tuner, klystron forward and reflected power, etc… To address this large signal density issue, a complementary effort was carried at FNAL aiming at developing a less expensive controller board, featuring a high channel count. The Multi Field Controller (MFC) [9] VXI board comprises 33 input channels (four octal 12-bits ADCs: AD9222, and one 14-bit fast ADC: AD6645 for a fast klystron feedback loop) and 4 outputs (two dual 14 bits DACs: ISL5927). It has a TigerSharc DSP and a Cyclone II FPGA. The goal of this multi channel board is to control 26 cavities with one board and to monitor the reflected and transmitted power signals with an additional two boards so that a set of 3 boards suffice for a complete RF station. Preliminary results on the MFC board show a SNR of -142 dBc/Hz and crosstalk isolation above 90 dB.

CONCLUSION

The ILC is an international project, requiring funding from numerous countries, but also involving combined R&D efforts coming from the three leading poles in the US, in Europe and in Asia. A successful LLRF design will only be possible through a productive collaboration between laboratories. Among the challenges associated with designing a LLRF control system for the ILC, one can cite the requirement for high availability and reliability, the need for a high and very stable accelerating gradient, the high channel count, and the need for automation. DESY, KEK and FNAL are looking into different approaches to achieve these goals. KEK-STF in Japan, FLASH and X-FEL in Germany, and CCII, HTS and NML in the USA are test facilities where LLRF systems are being developed and tested to achieve the ILC specifications and reveal the unforeseen challenges inherent to such a complex project.

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