Development of Fully-Integrated, Rad-Hard, Low-Noise, High-Speed Electronics for Particle Detection in the Superconducting Supercollider.

Dr. P. M. VanPeteghem

Dr. R. L. Geiger

Texas A&M University, Department of Electrical Engineering,

College Station, TX 77843

Tel.: (409) 845-8373

FAX: (409) 845-7161

In cooperation with:

Texas Instruments, Dallas, TX

Harris Semiconductor, Melbourne, FL

October 2, 1989

Project Summary

We propose here to develop reliable fully-integrated data acquisition electronics for warm-liquid calorimetry in the Superconducting Supercollider (SSC), using industrial radiation hardened IC technologies. These circuits will be placed inside the vessel, close to the detectors, to optimize speed and noise performance. A complete channel, including a low-noise charge preamplifier with less than 1,000 electrons input referred noise charge and speed of less than 100 nanoseconds, a noise shaper, a 16 sample analog memory, a trigger processor with 2,500 electrons input noise and 10 nanoseconds response time, and a 10 bit A-D converter, will all be integrated in one or two integrated circuits with a total power consumption of less than 150 mw. We expect that the production cost per detector channel will be below $30.00. Samples of these integrated circuits will be applied in experiments currently prepared by Dr. D. DiBitonto and co-workers at the University of Alabama at Tuscaloosa. During the first year of this project (FY '90) we will develop the front-end IC, i.e. the preamplifier with noise shaper and trigger processor.

For this development, the military-grade rad-hard dielectrically-isolated BiFET technologies of Texas Instruments and Harris have been selected for their excellent radiation hardness and high-frequency performance. These IC technologies are currently being evaluated; a first fully-integrated rad-hard, low-noise charge preamplifier has successfully been developed. To support design and testing, the VLSI laboratory at Texas A&M University has been enhanced for the design, modeling and evaluation of low-noise, high-speed, rad-hard integrated circuits.

The requested funding will also be applied as seed money to further expand this laboratory into a permanent center of expertise at Texas A&M University on the design of high-reliability integrated data acquisition circuitry for a radiation environment. This center will cooperate intimately with SSC, and with the industrial partners (Honeywell, Texas Instruments, Harris).

Table of Contents

1. Objectives of Proposed R&D and Relevance to SSC Experiments

In high-energy physics calorimetry experiments, elementary particles that have scattered from a proton-proton collision are traced by detecting the pairs of negative and positive charges that are left in the medium through which these particles propagate. These charges are collected by applying a strong DC bias to a parallel-plate detector capacitor so that positive and negative charges drift to opposite plates. The charge on this detector is traditionally read out by a charge preamplifier. This preamplifier is typically followed by a noise shaper, an analog memory bank and A/D conversion. In parallel with this signal processing path, there is a trigger processor which detects the presence of an induced charge, larger than some preset level.

High-energy experiments can only be conducted in a meaningful way if these charge measurements in large detector arrays are accurate, repeatable and reliable. As such, the most important specifications are sensitivity (expressed in mV/pC), noise performance (expressed in electrons RMS), and useful lifetime.

Traditionally, data acquisition circuits for particle detection were discrete designs, or hybrid designs with discrete low-noise transistors, connected to the detectors through long cables [1,2,3]. Input transistors were typically FET's for low-capacitance detectors, or bipolar transistors for high-capacitance detectors. The cost of selecting discrete matched components and of manufacturing hybrid circuits is very high, and also power consumption per channel can be excessive.

These classical designs will not be suitable for implementation in the new Superconducting Supercollider, because the imposed limitations and requirements lead to completely different design trade-offs [4]. E.g.: the exposure of the data acquisition circuitry to high radiation levels eliminates certain choices in technology or circuit design [5]. Only limited design experience is available in the area of rad-hard, low-noise, high-speed analog I.C. design. Hence, it can be expected that the development of reliable data acquisition electronics might become one of the major roadblocks on the way to a successful construction of the SSC [4].

In particular, the design of data acquisition circuitry for particle detection electronics for the SSC must conform to the following set of very challenging requirements:

a) The noise floor must be reduced to the absolute minimum, i.e. less than 1,000 electrons [1-3]. Lower noise levels are not compatible with other requirements such as power consumption, response time, and size.
b) High collision repetition rates (60 MHz) dictate that device speed must be maximized [3]. A response time of less than 100 nanoseconds seems appropriate. This speed can only be achieved if long coaxial cables can be avoided. This implies that, unlike previous designs, the front-end data acquisition circuitry be mounted on or close to the detectors.
c) Many hundreds of thousands of data acquisition channels must be installed (in principle: one channel per detector capacitance). Hence, heat management and electrical power management considerations dictate that power consumption per channel is limited to a few hundred milliwatts maximum [4]. The physical size of the electronics must, for the same reasons, be kept to a minimum [4].
d) Performance must be maintained over prolonged periods of time. First of all, it is very costly to interrupt experiments. Also, front-end electronics can be virtually inaccessible (inside the vessel). And finally, recalibration of detector electronics is in general a painful and time-consuming task. Slow build-up of radiation damage is the primary cause for noise performance degradation [5,6] over time. It is estimated that most of the front-end electronics must be resistant to 2 MegaRads of Gamma radiation and 2×10^{13} neutrons/cm^2; in this way, a useful life time of about two years can be guaranteed.
e) The capacitive nature of the detectors demands low-noise FET input stages [1] in the charge preamplifiers, in order to minimize noise levels. Bipolar transistors are not useful as input devices, since radiation damage reduces the current gain h_{FE} to about 30 to 40, even in very hard IC technologies. As a result, noise would increase to unacceptable levels.
f) A major issue is to produce these several hundreds of thousands of channels of precision detector electronics in a reliable and economical way, using standard industrial processes and manufacturing techniques.

It is clear that the only way to fulfill all these requirements is to integrate the data acquisition electronics using Integrated Circuit (IC) design techniques. Due to the high total radiation doses that can be accumulated over a few years, only a few military-grade IC technologies, such as Bipolar of BiFET technologies, are suitable [7]. CMOS, although inexpensive and widely available, is unsuitable in any environment where total Gamma

doses exceed a few hundred kiloRads [8]. In the group of acceptable industrial IC technologies, we have selected those technologies that are backed up by a strong experience in the design of analog integrated circuits. Two of the most important companies that meet these requirements are:

a) Texas Instruments in Dallas, Texas.

b) Harris Semiconductor in Melbourne, Florida.

Both companies have a complete range of radiation-hardened analog IC processes, with each having as top of the line a dielectrically isolated BiFET process.

An excellent cooperation has been set up with both companies over the past two years on the design of fully-integrated rad-hard low-noise analog integrated circuits for particle detection in the SSC. Next to their obvious experience in device modeling and circuit design for rad-hard analog design, these groups have another competitive edge over other semiconductor manufacturing companies. Over the past decade, they have been very active not only in the development of dedicated radiation-hardened analog IC's, but also in the development of the electronic systems in which these IC's are used (both military and space applications [9,10]. Therefore, they are familiar with producing small series of high-performance, highly customized analog IC's, and with tailoring the specifications of an IC to the required performance of a dedicated system. Most other IC manufacturers only are interested in the design of standard integrated circuits with a production of over a million samples a year.

We will now briefly summarize the results of some studies on rad-hard analog IC design and device modeling, conducted over the last year. These investigations were an intrinsic part of a pilot study, sponsored by DOE.

a) Modeling of radiation damage in devices for low-noise analog IC design.

As has been said, speed and noise requirements [2,11] in the SSC dictate that the most sensitive portion of the electronics be mounted on the electrodes [12], where the level of radiation obviously is highest [6]. A systematic study has been conducted on testing and characterizing the degradation of device performance after radiation in rad-hard IC technologies. The most important observations are listed here:

1°: JFETS (being majority-carrier devices) tend to be unaffected by neutrons, and are only moderately affected by Gamma radiation. In a dielectrically-isolated BiFET process V_P and I_{DSS} variations are less than a few percent. However, JFET's in all industrial rad-hard IC processes show a strong degradation in low-frequency noise and junction leakage after Gamma doses of over 500 kRads. The increase in leakage current and flicker noise can be several orders of magnitude.

2°: The only parameter in bipolar transistors which is significantly degraded in rad-hard technologies is the current gain factor h_{FE}. This gain can "sag" after radiation to values as low as 20 to 30 in NPN's and as low as 5 in PNP's. Also, the range for collector current where h_{FE} is acceptable shifts to higher I_C, and narrows down considerably. This can result in severe bias problems in analog IC design.

3°: Enhanced MESFET and HIGFET devices in GaAs technology have been characterized in cooperation with Honeywell in Minneapolis, MN. It has been observed that these devices are extremely hard (no threshold or current shifts up to 10 MegaRads). Flicker noise before radiation is very high (lower MegaHertz range), but does not degrade after radiation. GaAs IC technology is fairly immature at this point of time, and therefore it is not considered here as a realistic choice to implement front-end electronics for the SSC. However, within a few years, it may become a suitable alternative, due to its superior radiation hardness. Hence, the investigation in GaAs analog low-noise circuit design will be continued (see appended letter of support), although with external funding.

b) Design of fully-integrated rad-hard BiFET charge preamplifiers

A prototype has been realized of a low-noise, radiation hardened preamplifier that was designed for a 10 pF detector cell, which is part of a warm liquid forward calorimetry experiment [12]. This charge preamplifier was integrated in a junction-isolated BiFET process with a 80 MHz f_T for the P-JFET, and 260 MHz f_T for the NPN bipolar transistors. This technology was selected because it is readily available, very mature (standard analog IC's such as the TL074 and LF356 are manufactured in quite comparable processes), and therefore it is well characterized and inexpensive. On the other hand, it is only moderately hard, due to deep junctions, and junction isolation. A circuit schematic of the integrated BiFET preamplifier is shown in Fig.1.

This preamplifier is essentially a single-input, folded-cascode amplifier, in which all bipolar current sources have resistive emitter degeneration to reduce input referred noise. The feedback capacitor is 1 pF, the detector capacitance is 10 pF. This amplifier has been manufactured and tested before and after the application of a strong radiation dose. The most important measured specifications of this preamplifier are below:

Specification	Prerad	After 1.5 MegaRad	After 2E13 n/cm^2
Rise Time	50-80 nsec	< 160 nsec	< 160 nsec
Noise	< 900 el. RMS	< 2,200 el. RMS	< 1,500 el. RMS
Power Cons.	< 80 mW	< 80 mW	< 80 mW

This circuit was the first published fully-integrated, rad-hard charge preamplifier ever integrated in a industrial IC technology, that was tested for radiation levels compatible with SSC operation [13,14]. For more information on this circuit, a copy of a paper presented recently at the Bipolar Circuits and Technology Meeting in Minneapolis [14] has been appended.

It is however clear that the lifetime of this circuit would not exceed half a year to one year for realistic radiation dose rates.

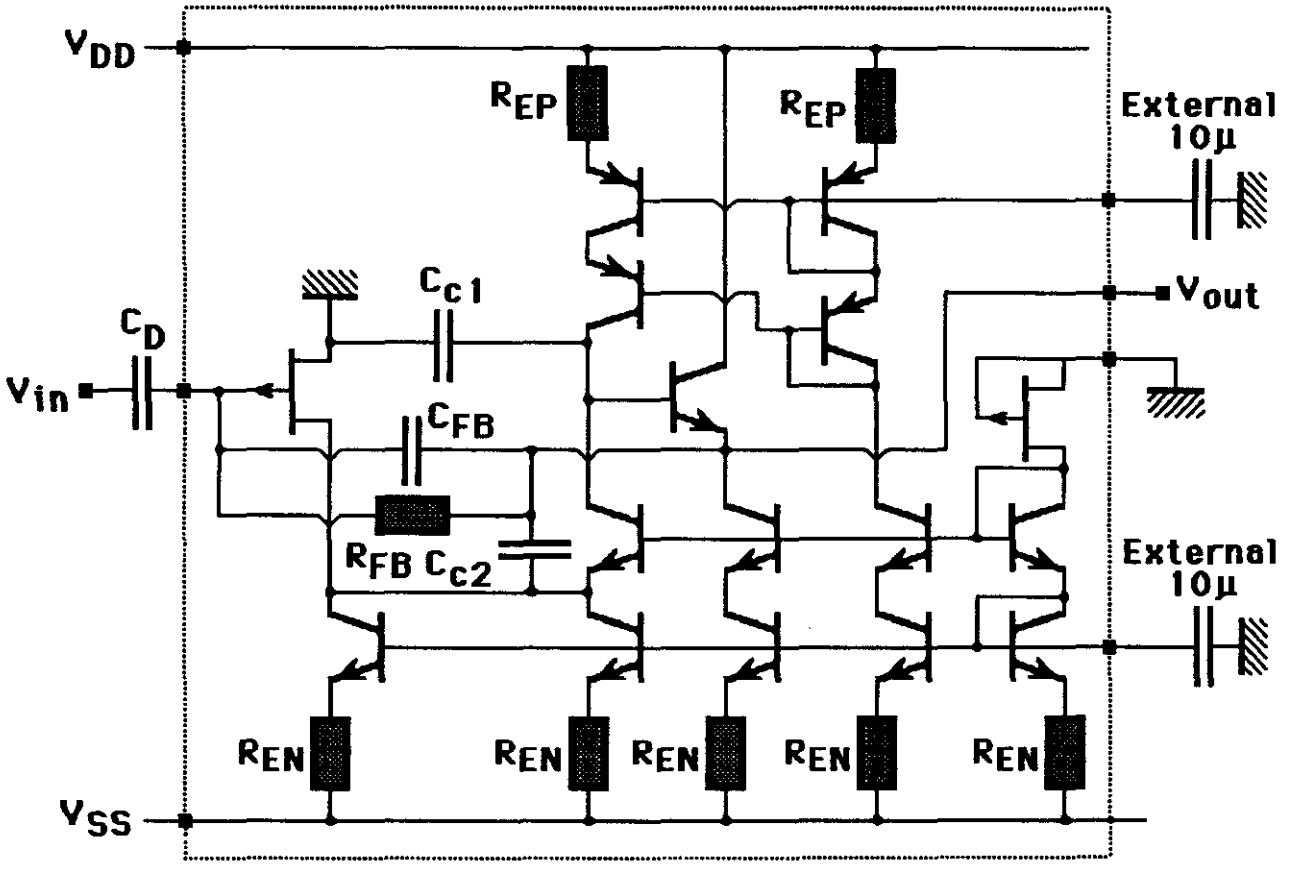


Fig.1: Internal circuit schematic of low-noise BiFET charge preamplifier.

Therefore, we have negotiated the use of the state-of-the-art dielectrically-isolated BiFET process of Harris to integrate a second preamplifier circuit prototype. This technology is hard to both neutrons and Gamma radiation, far beyond what is required for maintaining circuit performance in SSC. First samples of this new circuit are expected middle of Fall '89. Results will be presented to the engineering community shortly after that. The major unknown is (again) the effective degradation in flicker noise performance.

c) Establishment of Instrumentation Laboratory

We have built up, with support from DOE and NSF, a very versatile and efficient instrumentation laboratory to analyze the characteristics of semiconductor devices and circuits. The available equipment includes DC Parameter Analyzers (HP4145, HP4140), a S-Parameter Analyzer (HP8753), a 1 GHz Waveform Recorder (HP54111) and a high-performance Spectrum Analyzer (HP3585). The measurement equipment is controlled by HP9000 UNIX workstations. The whole network is shown in Fig.2. State-of-the-art software tools have been developed on this network to test high-performance analog circuits in a joint effort with Hewlett-Packard in Loveland, CO. These workstations also link the evaluation environment to the I.C. design environment (on SUN and Apollo workstations).

Radiation tests can be conducted on-campus through two sources:
a) A Co^{60} source for Gamma radiation damage tests.
b) A nuclear reactor in the Texas A&M University Nuclear Science Center yields controlled quantities of neutrons (with a Gamma ray background).
In this way we have the ability to test performance degradation of developed electronics in increments up to about 10 MegaRads of Gamma dose, and $5x10^{14}$ neutrons/cm^2, which exceeds by far the expected total doses in SSC.

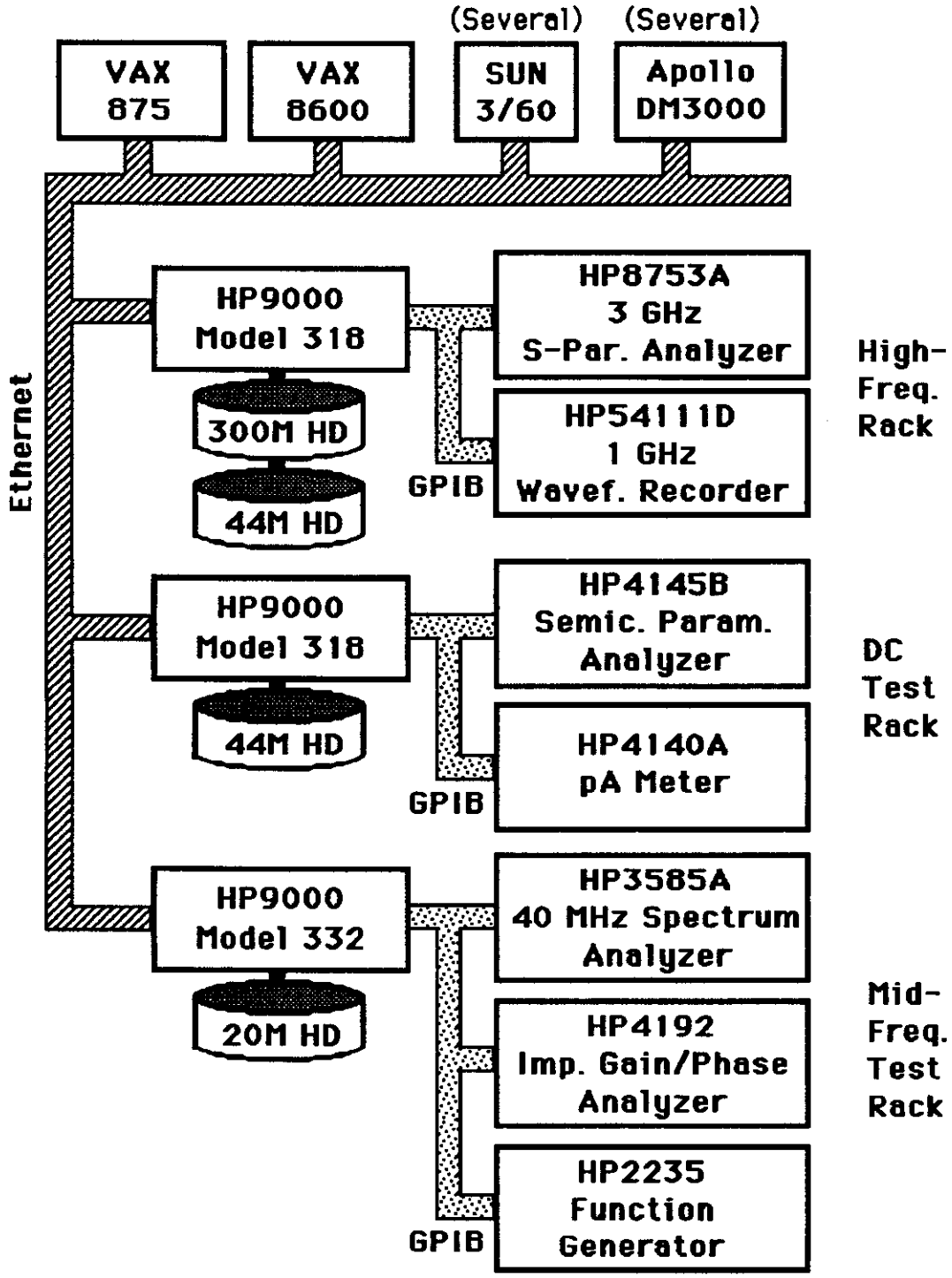


Fig.2: Current equipment and workstations in the VLSI System Evaluation Laboratory.

2. Project Description, Timing and Milestones.

We propose here to build, over the next two and a halve years, a fully-integrated version of the data acquisition electronics for particle detection. In the first pass, we will deliberately confine our developments to data acquisition for the warm liquid calorimetry. Therefore, samples of these chips will be transferred to the research group of Dr. D. DiBitonto at the University of Alabama at Tuscaloosa, who is preparing warm liquid calorimetry experiments for SSC. In a later stage, we will investigate also whether the circuits that are developed by us can be applied also in other calorimetry applications such as Liquid Argon calorimetry.

The proposed data acquisition chip set will include the following functions, as also indicated on Fig.3:

1°: A charge preamplifier which is optimized for detector capacitances between 10 and 30 pF. This preamplifier will have the following specifications:

Input referred noise:	< 1,000 electrons
Sensitivity:	< 1 mV/fC or 160 μV per 1,000 electrons
Response time:	< 100 nanoseconds
Large-signal linearity:	< 1% THD for ±1 Volt output swings

2°: A noise shaper with a signal gain of 6. This will result in a sensitivity of about 1 mV for each 1,000 electrons input charge. Noise, linearity and speed will be designed such that the charge preamplifier will dominate performance.

3°: A trigger processor will be designed which will have an input referred noise of less than 2,500 electrons RMS equivalent input noise, and a response time of less than 10 nanoseconds.

4°: A simple calibration circuit will be added; this will be a pulse generation circuit with the pulse height controlled by a simple bandgap reference generator (accuracy of step: less than 1%). The pulse will be applied to the input node of the charge preamplifier through a small 0.1 pF capacitor. To avoid any noise coupling through this capacitor during normal operation of the charge preamplifier, we will disconnect that capacitor from the sensitive preamplifier input node by a low-capacitance JFET switch.

5°: An analog memory will be designed with a length of 16 samples. The sample/hold amplifiers in it may have some additional gain to boost signal amplitude somewhat.

6°: A high-speed 10 bit ADC will be designed to transfer the data in digital format to the outside world. Eventually, an optical link can be used for the interconnection from inside the vessel to the outside electronics, to reduce the effect of electromagnetic interference. The actual architecture of the ADC will depend heavily on the minimal conversion time. This conversion time itself depends on the stochastics of how frequently "meaningful" events occur, and how clustered these are, and also on how many collision cycles one is allowed to skip if such a meaningful event occurs.

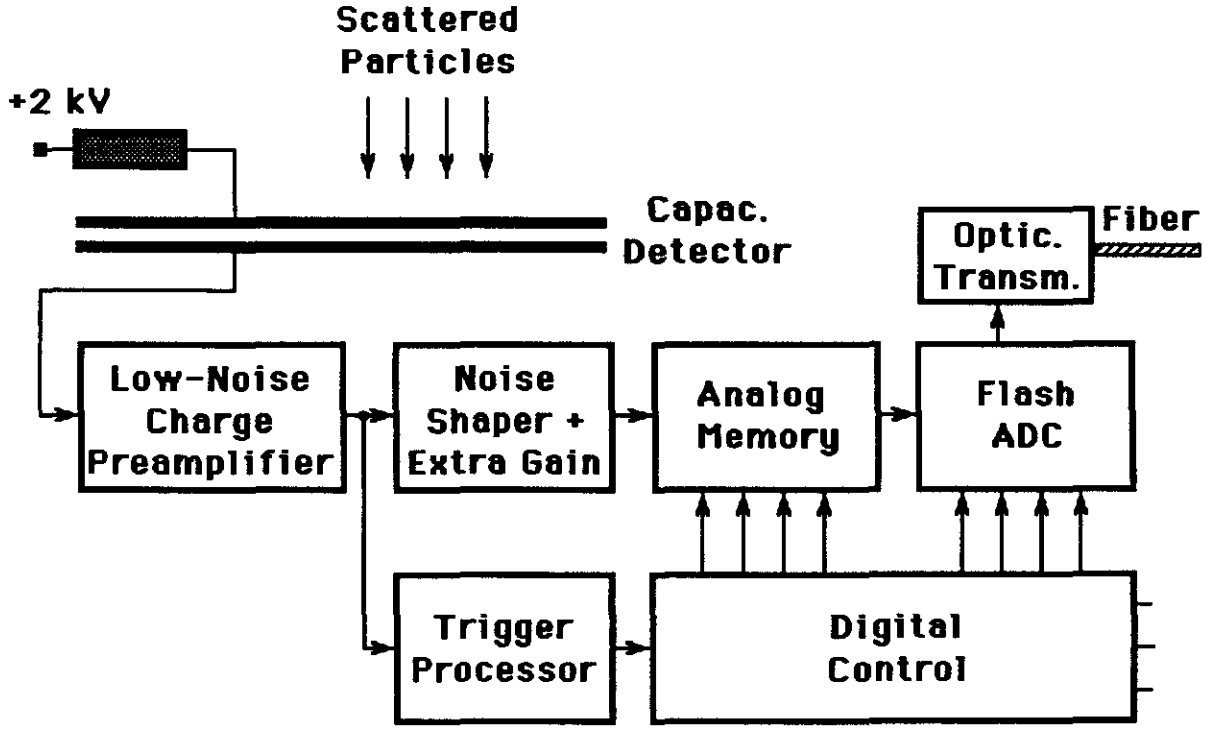


Fig.3: Block diagram of a complete rad-hard particle detection data acquisition channel, to be mounted on the detector.

The optimal partitioning of this system in individual I.C.'s is not so clear at this time. Based on power consumption and cross-talk specifications, it seems logical to put a complete single data acquisition channel, as defined higher, on one I.C. However, the front-end modules (i.e.: preamplifier, noise shaper and trigger processor) have the most stringent speed and noise specifications. Therefore, we can achieve a significant improvement in total cost, yield and reliability, if a few front-end channels are combined on one IC which is integrated in the hardest and most high-performance IC technology, and if the remaining electronics such as the analog memory and ADC's are integrated in another IC technology with more relaxed radiation, speed and noise performance, but

which is more optimized for circuit density, low price, and high yield. A rad-hard BiCMOS technology might be suitable for this, as long as the CMOS devices are not used for high-performance analog functions. Based on preliminary cost calculations, we expect to be able to develop IC's with a production cost of $30.00 per channel.

During the first year of this project (i.e.: FY '90), we propose to develop a prototype of a BiFET integrated circuit which contains two front-end channels with each a charge preamplifier, a noise shaper, a trigger processor and a calibration circuit.

We have budgeted IC processing through two semiconductor manufacturers. We will use the Dielectrically-Isolated BiFET processes of both Texas Instruments and Harris Semiconductor Corporation. This implies that we plan to conduct in parallel two IC developments of the same type of circuits. Although this is quite uncommon, it should not be seen as a waste of energy, time and money. To prove this, we would like to point to the following extremely important arguments:

1°: The developed IC's will always be rather sophisticated custom integrated circuits. This implies that these circuits later can only be purchased from that particular vendor that developed these. Experiences at other large high-energy physics programs (e.g. CERN) have clearly shown that it is not very wise to depend for essential electronic components on one single manufacturer. This is independent of how good the relationship may be with that particular vendor.

2°: Through the cooperation with Texas Instruments and Harris, we have learned that only rarely the available precharacterized devices and subcircuits were appropriate for our developments. Also, the slow build-up of radiation damage in SSC is not comparable to the impulse-type radiation exposure, typical in other, military-type applications. Therefore, success in this project can only be achieved if we cooperate in a very intimate way with the device technologists of our industrial partners, to assess how device performance can be improved to serve better our goals. The two D.I. processes that we plan to use are somewhat different in nature, and the circuit design experience and interests of both industrial groups are somewhat different. Therefore, the goals set in this project do not only cover the succesfull completion of the planned IC's, but also how to enhance the awareness in the major rad-hard semiconductor manufacturing companies for the specific needs of SSC.

To conclude, we are convinced that the very large number of detector data acquisition circuits that have to be developed can only be manufactured in a relaible way, if we can secure from the onset of this project a sound industrial base.

The initial phase of the development of such integrated system has already begun. Financial support by Texas Instruments and NSF has been applied to develop high-frequency integrated filters [15-17], and to design and model high-speed flash A-D Converters [18-19]. Hardware and software test set-ups have been developed to characterize high-performance mixed analog/digital VLSI circuits, with technical and financial support from Texas Instruments, Crystal Semiconductor and Analog Devices.

The following seven research tasks are planned over the next year (FY '90).

Task 1: Evaluation of Rad-Hard, Low-Noise Technologies (1 man-year)

Our industrial partners, Texas Instruments and Harris Semiconductor, provide us with models of the devices in their BiFET technology: JFET's, bipolar transistors, diodes, resistors, capacitors, zeners. These models can be given in the form of sets of model parameters that are compatible with the standard circuit simulator SPICE. They provide us also with samples of these devices, which are fully characterized in our laboratory, both before and after exposure to radiation in the Nuclear Science Center. A comparison in our research group between available SPICE models, and the measured behaviour of radiated devices, has revealed that current SPICE models of JFET's and bipolar transistors are not appropriate to provide a accurate prediction of actual performance degradation after exposure to radiation. In particular, we will derive SPICE enhancements for the following specifications:

- Effective h_{FE} of bipolar transistors (i.e.: an extension of the Gummel-Poon model).
- Leakage current in bipolar transistors and JFET's (primarily surface leakage)
- Low-frequency noise in JFET's.

Newly introduced technologies (such as GaAs) or new devices in existing technologies will be investigated as these become available to us.

Milestones:

a) July 1990: we will present an updated SPICE model for DC biasing of bipolar transistors and JFET's. These SPICE model extensions will be made available in a SPICE 3 version to all participants in electronics design for SSC. The actual device parameters which refer to the Texas Instruments and Harris Semiconductor technologies will remain the proprietary information of these companies.

b) December 1990: we will present an updated SPICE model which will also include a better low-frequency noise model for JFET's. We will also present a measurement and fitting procedure to obtain values for all newly defined device parameters.

Task 2: System Design of Complete Channel (1 man-year)

The fraction of all collisions that produces a meaningful event in a particular set of detector channels is very low. These statistics can be applied to reduce significantly the throughput rate, and therefore area and power consumption of the analog memory banks and ADC's. An important issue will be whether we can afford to throw away incoming data while the ADC is converting. The new high-level behavioral circuit simulator SABER [20] will be used to model the complete system, to assist in selecting the right ADC architecture, and to facilitate the partitioning of the complete system into smaller modules, to optimize performance.

Milestones:

a) March 1990: set-up of front-end part of data acquisition channel (charge preamplifier, noise shaper, trigger processor) is completed in SABER, using simplified circuit equations for least critical blocks, and actual transistor circuits for very sensitive subcircuits.

b) July 1990: a complete data acquisition channel, including analog memory and ADC is built in SABER. Models for several alternative ADC architectures have been developed.

c) December 1990: a study is completed which shows the trade-off between power consumption, resolution and bandwidth of the ADC's versus the expected stochastics of charge deposition on a related bank of detectors, and versus the percentage of relevant events that can be purged without affecting the experiments too much. During this study we will consult with other groups, which develop the hardware and software, that process the data acquired by our electronic circuits.

Task 3: Circuit Design of Charge Preamplifier, Noise Shaper, Trigger Processor and Calibrator in BiFET Technology (2 man-years)

As has been said, we will cooperate with Texas Instruments and Harris Semiconductor to develop the front-end modules of the particle detection electronics, using their D.I. BiFET technologies. In each technology, we will optimize the design of the preamplifier, noise shaper, trigger processor and calibrator. Ample experience has been gathered on the charge preamplifier in some prototype development prior to the start of this project.

Milestones:

a) February 1990: a low-noise preamplifier (two channels) which is currently being processed by Harris, will be tested completed, including radiation hardness. Results will be reported to SSC and the Microelectronics community. This prototype circuit will be used as a vehicle to compare device modeling with the prediction of performance degradation after radiation exposure in actual circuits (see: Task 1).

b) July 1990: masks will be generated for test runs which will contain independent test circuits for all the different modules, and a two-channel version of the complete system.

c) November 1990: test I.C.'s will be available for a wafer level scan test, and for device modeling. All test circuits will be tested, including evaluation of radiation damage. About 100 I.C.'s, containing the two-channel version of the data acquisition, will be packaged, tested, and shipped to Dr. D. DiBitonto at the University of Alabama at Tuscaloosa. These chips will be mounted on the detectors developed before, and a complete experimental set-up will be prepared there. We will consult with this group to interpret data, and to discuss possible circuit improvements or enhancements.

d) December 1990: We will report to SSC on the performance of the manufactured circuits, and will provide small numbers of test circuits to other participating research groups for evaluation purposes.

3. Commitments to the R&D by the proponents / contact person.

Grants from DOE, NSF and Texas Instruments, and equipment donations by Hewlett-Packard, have been applied over the last three years to develop a very impressive VLSI evaluation laboratory. The Department of Electrical Engineering, the Texas Engineering Experiment Station and the College of Engineering have contributed to this laboratory development with contributions of over $ 200,000.

The Texas A&M University Nuclear Science Center has agreed to cost share the radiation tests for an amount of $ 10,000. Current funding from DOE will be applied to support the ongoing evaluation of rad-hard IC technology for the present year.

Texas Instruments and Harris are providing invaluable technical support and have donated complimentary samples of devices. Harris is currently integrating a first charge preamplifier prototype in their dielectrically isolated BiFET process. IC processing and extended support services have been made available by these industrial partners at minimal costs (see appendices). Honeywell has donated complimentary samples of GaAs devices, and is currently integrating for us a few versions of a fully-integrated GaAs charge preamplifier with enhanced MESFET devices.

Due to its strong reputation in analog IC design and also due to the proximity to Waxahachie, TX, Texas A&M University is the premier choice for setting up a long-term support center for the design, development and testing of reliable instrumentation for the SSC. We are requesting external funding for the development of such center through the Texas Advanced Technology Program, through NSF, and through the University Cooperation Programs of various industrial partners.

Contact person:

Dr. Peter M. VanPeteghem
Texas A&M University, Department of Electrical Engineering
College Station, TX 77843-3128

Telephone:	(409) 845-8373
FAX:	(409) 845-7161
E-mail correspondence:	Bitnet: VANPETE@TAMVXEE
	Internet: VANPETE@EE.TAMU.EDU

4. Budget and Budget Justification (for FY 1990)

ITEM		COST
A. Personnel		
1. Principal Investigators		
Peter M. VanPeteghem	(@ 25% of full-time)	$16,250
for project supervision, and project management		
Randall L. Geiger	(@ 15% of full-time)	$12,000
for project supervision, student supervision		
2. Graduate Research Associates		
Ph.D. Student 1	(@ 50% of full-time)	$12,960
for the design of the total system, partitioning in smaller units, system simulation		
Ph.D. Student 2	(@ 50% of full-time)	$12,960
for the design of integrated data acquisition circuits in BiFET technology		
Ph.D. Student 3	(@ 50% of full-time)	$12,960
for the design of integrated data acquisition circuits in BiFET technology		
Ph.D. Student 4	(@ 50% of full-time)	$12,960
for the testing, evaluation and modeling of the resistance of the developed circuits to radiation damage.		
3. Technical Staff		
System Manager VLSI Laboratory	(@ 50% of full-time)	$9,840
will be responsible for software and hardware support during design and testing of the integrated circuits.		
Developer of Test Setups	(@ 50% of full-time)	$9,840
will prepare test setups and write software programs to acquire and process test data.		
Secretary	(@ 30% of full time)	$7,500
will be responsible for generating reports and documentation.		
B. Fringe Benefits	(@ 14.2% of salaries)	$15,232
Total Salaries and Wages		**$122,502**

C. Permanent Equipment

Bruel&Kjaer Low-Noise Amplifier/Meter	$14,000
for accurate measurement of noise performance of low-noise devices and circuits.	
2 SUN Sparcstation 1 Workstation + Peripherals	$43,400
inc.: LAN connection 800 MByte Hard Disk Laser-printer (software licenses already present)	
will be used for design, simulation, modeling and layout of BiFET integrated circuits	
IC Tester Configuration	$165,000
incl.: HP 16500A Analog/Digital Waveform Recording HP 9000 series 330 Workstation HP 4062C Semiconductor Parameter Test System Electroglass 1034X Prober	
will be used to perform extensive wafer probe testing of prototype integrated circuits and the devices in them	
Total Permanent Equipment	**$222,400**

D. Travel

1. Domestic	$8,000
Est.: 5 trips over to Texas Instruments, Dallas, TX 5 trips over to Harris Semiconductor, Melbourne, FL each for two persons, three days	
2. Foreign	$2,000
One visit to CERN or other European lab	
Total Travel	**$10,000**

E. Other Direct Costs

1. Materials and Supplies	$20,000
incl.: PCB boards hybrids	

data acquisition electronics	
connectors and miscellaneous	
2. Maintenance and Suppport of Equipment used	$10,000
3. Software contracts	$15,000
incl.: HP-UX, HP-Basic,	
SUN-OS	
various fitting, modeling and simulation tools	
as used in I.C. design	
4. Computer (ADPE) Services	$20,000
incl.: HP9000, SUN, APOLLO, VAX computers	
5. Subcontracts	$184,400
IC Processing: D.I. run at Texas Instruments	$99,759
incl.: mask generation	
processing of one lot of wafers	
technical support in device modeling and	
circuit design	
IC Processing: D.I. run at Harris Semiconductor	$75,000
incl.: mask generation	
processing of one lot of wafers	
technical support in device modeling and	
circuit design	
IC Packaging Costs	$7,400
Radiation Testing	$10,400
at the Nuclear Science Center, Texas A&M University	
6. Reporting, clerical services	$3,000
Total Other Direct Costs	**$260,559**
TOTAL DIRECT COSTS (A through E)	**$615,461**
F. University Overhead (@ 42% of dir. costs)	**$258,494**
standard Texas A&M University overhead for government or industrial projects.	
TOTAL COSTS (A through F)	**$873,955**

5. Estimate of Test Beam Needs

In this stage of the project, test beam needs are limited to a simulation of the performance of the designed electronics under radiation conditions:
a) We need to evaluate the performance degradation of the integrated electronics due to a slow build up of radiation damage.
b) We will have to monitor the presence and extent of unwanted glitches, false triggering and other transient effects due to incident radiation.

Such conditions can easily be mimicked by other radiation sources, such as present currently in the Texas A&M University Nuclear Science Center.

6. Bibliography

[1] Y NETZER, "The Design of Low-Noise Amplifiers.", IEEE Proceedings, Vol.69, No.5, pp.728-745, May 1981

[2] V. RADEKA, S. RESCIA, "Speed and Noise Limits in Ionization Chamber Calorimeters.", Nucl. Instr. and Meth. in Phys. Res., A265, pp.228-242, 1988

[3] H.H. WILLIAMS, "Fast Analog Integrated Circuits for Particle Physics.", IEEE Transactions on Nuclear Science, Vol.35, No.1, pp.146-150, February 1988

[4] Discussions at Technical Sessions at the Workshop on Calorimetry for the SSC, Tuscaloosa, AL, March 1989

[5] J.E. GOVER, T.A. FISCHER, "Radiation-Hardened Microelectronics for Accelerators.", IEEE Trans. on Nucl. Sci., Vol.35, No.1, pp.160-165, February 1988

[6] J.W. DAWSON, L.J. NODULMAN, "Development of Rad-hard VLSI Electronics for SSC Calorimeters.", Pres. at the Intern. Industrial Symp. on the SSC, New Orleans, LA, February 1989

[7] G.C. MESSENGER, M.S. ASH, "The Effects of Radiation on Electric Systems.", Van Nostrand Rheinhold Co., 1986

[8] T.P. MA, P.V. DRESSENDORFER, ed., "Ionizing Radiation Effects in MOS Devices and Circuits.", Wiley, 1989

[9] S.A. KERNS, B.D. SHAFER, "The Design of Radiation-Hardened ICs for Space: a Compendium of Approaches.", IEEE Proceedings, Vol.76, No.11, pp.1470-1509, November 1988

[10] J.R. SROUR, J.M. McGARRITY, "Radiation Effects on Microelectronics in Space.", IEEE Proceedings, "Vol.76, No.11, pp.1443-1469, November 1988

[11] V. RADEKA, "Low Noise Techniques in Detectors.", internal report, Brookhaven National Laboratory, Upton, NY, February 1988

[12] D. DIBITONTO, et al., "Advanced Forward Calorimetry for the SSC and TeVaTron Collider", to be published in Nucl. Instrum. and Meth. in Physics Research, 1989.

[13] P.M. VANPETEGHEM, et al., "On the Design of Fully-Integrated Charge Preamplifiers for the SSC", pres. at the Workshop on Calorimetry for the SSC, Tuscaloosa, AL, March 1989

[14] K.Y. LING, et al., "A Rad-Hard, Low-Noise, High-Speed BiFET Charge Preamplifier for the Superconducting Supercollider.", to be presented at the 1989 Bipolar Circuits and Technology Meeting, Minneapolis, MN, September 1989

[15] P.M. VANPETEGHEM, J.F. DUQUE-CARRILLO, "Compact High- Frequency Output Buffer for Testing of Analog CMOS VLSI Circuits.", IEEE Journal of Solid-State

Circuits, Vol.SC-24, No.2, pp.540-542, April 1989

[16] P.M. VANPETEGHEM, "On the Relationship between PSRR and Clock Feedthrough in SC Filters.", IEEE Journal of Solid-State Circuits, Vol. SC-23, No. 4, pp. 997-1004, August 1988.

[17] P.M. VANPETEGHEM, B.J. HABY, H.M. FOSSATI, "A Very-Linear CMOS Transconductance Stage for OTA-C Filters', Proceedings of the 1989 Custom Integrated Circuits Conference, Paper 25.3, San Diego, CA, May 1989

[18] P.B. SETTY, et al., "Modeling of Timing Uncertainty in Flash ADC's.", project report, Texas A&M University, 1988.

[19] E.G. SOENEN, "An Integrated Workstation Environment for Design and Evaluation of Analog Integrated Circuits.", MS Thesis, Texas A&M University, August 1989

[20] SABER, new behavioral simulator marketed by Analogy, Beaverton, OR

A Rad-Hard, Low-Noise, High-Speed, BiFET Charge Preamplifier for the Superconducting Supercollider

K.Y. Ling, P.M. VanPeteghem, S.Y. Lee, H.H. Liu, D. DiBitonto
Texas A&M University, Dept. of E.E., College Station, TX 77843-3128

Supported by DOE (DE-AS05-81ER40039) & NSF (MIP-8809365)

Abstract

An entirely integrated BiFET charge preamplifier meeting the specifications imposed by the Superconducting Supercollider, a rise time around 100 ns, noise level less than 1,000 electrons RMS, and a power consumption of less than 80 mW, is presented. Performance has been tested up to total radiation doses of 1.4 MegaRads Gamma rays and 2×10^{13} ***neutrons/cm***^{2} .

Introduction

In high-energy physics calorimetry experiments, elementary particles that scatter from a proton-proton collision are traced by detecting the charges that are left behind in the medium through which these particles propagate. These charges are collected on a parallel-plate detector capacitor which is under a strong DC bias. Traditionally, these collected charges are sensed and read out by a transcapacitance amplifier or a charge preamplifier as shown in Figure 1. The most critical design specifications for the charge preamplifier are the sensitivity, expressed in mV/fC, and the RMS noise, expressed in equivalent electrons RMS. Charge preamplifiers of this kind are traditionally discrete or hybrid devices [1,2,3], with FET input transistors for low-capacitance detectors [4,5], or bipolar input transistors for high capacitance ones. These preamplifiers are usually connected to the detectors through long shielded cables. For a detector of several hundred pF, a rise time of around 3μs and noise levels as low as 300 electrons RMS, have been reported. However, the cost of selecting discrete matched components and manufacturing hybrid circuits is very high and the power consumption per channel tends to be excessive.

These classical preamplifiers are not suitable for applications in the Superconducting Supercollider (SSC). For the SSC, rise time must be reduced to within 100 ns, which dictates the mounting of the preamplifier right next to the detector [2]. Detector capacitance is also reduced (10 to 300 pF) and lower total charge will be detected per collision. This means that the feedback capacitance should be as small as possible, typically 1 pF, and the preamplifier noise be minimized. In addition, radiation levels inside the SSC calorimeters will be higher. Annual Gamma doses of 100 kRad or even as high as 1 MRad, and neutron doses in the order of $2\text{x}10^{13}/cm^2$ are expected, depending upon the locations of the detectors. Thus, preamplifiers have to be designed in radiation-hardened IC technologies [5]. Furthermore, power consumption allocation for front-end electronics is limited in the SSC; utilization of power beyond 100 mW per channel must be properly justified. Finally, a large amount of preamplifiers, as many as 3 millions according to certain estimates [6], must be installed in a small space.

All the above requirements make integration of the charge preamplifier on an IC a very attractive and feasible solution, since it provides analog signal processing functions in a compact, low-power manner with simple mass production. However, low-power operation results in higher noise, therefore, the basic long-term research issue is to search for an IC technology that will optimize noise performance and reliability at an affordable price.

Design of the Charge Preamplifier

In this paper, an integrated low-noise, rad-hard, high-speed charge preamplifier prototype, designed for a 10 pF detector cell for warm liquid calorimetry experiments [7], is presented. An industrial junction-isolated BiFET process with an 80 MHz f_T for the P-JETs, and 260 MHz f_T for the NPN transistors, was selected to minimize noise level for such a low detector capacitance [2,8]. Other device parameters are given in Table 1.

A circuit schematic of the BiFET preamplifier is shown in Figure 2. It is essentially a single-input, folded-cascode amplifier [9] with a JFET input transistor. The technique of resistive emitter degeneration is applied to all the bipolar current sources and mirrors to reduce the input referred noise.

The feedback capacitor, C_{FB}, is 1 pF, and the feedback resistor, R_{FB}, realized with two back-to-back diodes, is in the gigaohms range; the value of R_{FB} is not critical as long as it is in the higher megaohms region. The capacitor C_{c1} introduces a dominant pole while C_{c2} creates a positive feedback path. C_{c2} can be used to cancel part of C_{c1} to provide a trade-off between speed and noise of the preamplifier; C_{c2} has been set to zero in this prototype, to minimize noise.

The most important design equations are those that concern noise, speed and open-loop gain of the preamplifier. One premier design parameter is the feedback factor, α, which is expressed as follow:

$$\alpha = \frac{C_{FB}}{C_{FB} + C_P + C_D} \tag{1}$$

where C_D and C_P are the detector capacitance and the input capacitance, which consists primarily of the C_{GS} of the input JFET of the preamplifier, respectively. The rise time, τ, is inversely proportional to α:

$$\tau \propto \frac{C_{c1}}{\alpha G_m} \tag{2}$$

with G_m being the transconductance of the input JFET.

The input referred noise of the preamplifier can be written as:

$$e_N = \frac{8kTG}{G_m} + \frac{K_F}{f} \tag{3}$$

where G is the noise excess factor, and K_F accounts for the flicker noise which is almost entirely due to the input JFET. The noise excess factor, G, can be expressed as:

$$G = 1 + \frac{3V_P}{4\beta_N V_T} + \frac{3V_P}{4\Delta V} +$$

$$\frac{I_2}{I_1}\left[\frac{3V_P}{4\beta_N V_T} + \frac{3V_P}{2\Delta V} + \frac{3V_P}{4\beta_P V_T}\right] \quad (4)$$

Here, β_N and β_P are the current gains of the bipolar transistors, V_P is the pinch-off voltage of the JFET, V_T is kT/q, ΔV is the DC voltage drop across the emitter degeneration resistors, and I_1 and I_2 denotes the DC bias currents in the two main branches of the amplifier. As can be seen in equation (4), a low noise design requires a high I_1 in the input branch, a large ΔV over the resistors, and high β's for the bipolar transistors. Other noise sources not accounted for in equations (3) and (4) are the noise due to the feedback resistor, R_{FB}, and the JFET gate leakage current, I_{GSS}. Both of these contributions have output power spectral densities that have a -20 dB/dec slope which can be filtered out almost completely with a simple high-pass shaper. For a high-pass filter with equivalent bandwidth f_Z, the total integrated noise is approximately equal to:

$$V_{RMS}^2 = \frac{2kTG}{3\alpha C_{e1}} + \frac{K_F}{\alpha^2} log_e\left[\frac{1}{\tau f_Z}\right] \quad (5)$$

which, for negligible flicker noise, can be further approximated as:

$$V_{RMS}^2 = \frac{kTGV_P V_{SUP}}{3\alpha^2 \tau Power} \quad (6)$$

where V_{SUP} is the supply voltage for the input branch, and Power is the total power consumed by this branch. Hence, for a given power consumption, it is advantageous to reduce the total supply voltage as much as possible. This also sets a limit on the maximum allowable voltage drop over the resistors. It is often stated [1,2] that the optimal input JFET aspect ratio is one that has a corresponding C_{GS} that is equal to the sum of C_D and C_{FB}; the noise and rise time of the preamplifier are both minimized this way. This choice is however often not feasible due to excessive power consumption.

The open-loop gain of the preamplifier should be very high in order to have a linear and reproducible charge transfer, since the feedback factor, α, is much less than one. An approximation for A_{OL} (for $\beta_P << \beta_N$) is given below:

$$A_{OL} = \frac{2\beta_P^2 V_{AP} I_1}{V_p I_2} \quad (7)$$

where V_{AP} is the early voltage for the PNP transistors. In our design, A_{OL} is higher than 80 dB. From equation (7), it is obvious that IC technologies with high β's and high early voltages are more desirable choices.

Regarding radiation damages, the basic limitation is the increase in the flicker noise of the preamplifier. It is especially critical for the input JFET to maintain low K_F under radiation. From the results of our radiation tests, transistors with small geometries tend to be more radiation-hardened. Thus, it is advisable to implement large transistors by putting identical smaller transistors in parallel. Certainly, it is most essential to choose rad-hard IC technologies that can maintain low flicker noise characteristics even under high levels of radiations.

Results

The circuit in Figure 2 has been integrated and tested. A microphotograph of the input stage is shown in Figure 3. The most important specifications of the preamplifier and some of the transistor parameters, for a typical sample, before and after Gamma and neutron irradiations, are shown in Table 2. One can see that the input JFET transconductance, G_m, stays roughly constant while the gate leakage current, I_{GSS}, increases by orders of magnitude after being exposured to radiation. For the bipolar transistors, the parameter that is affected the most is the current gain, β. For the most part, the degradation in the transistor parameters, except for K_F, can be overcome by applying better circuit design techniques [5,9,14].

Figure 4 shows the noise spectral density of one of the prototype samples before and after Gamma irradiation. It is obvious that flicker noise increases significantly after irradiation. The relationship between the total RMS noise and the Gamma doses applied is shown in Figure 5. The fact that the total RMS noise increases with the Gamma dose up to a maximum and then retreats to a lower level is not well understood. One suggestion is that radiation "breaks down" the lattice of the semiconductor material and makes it less homogenous and hence causes the flicker noise to increase. This disturbance will reach a maximum and any further increase in radiation dose will randomly improve or degrade the homogeneity of the crystal lattice and thus creates higher or lower flicker noise, statistically. This suggestion is deduced from our experiments with high Gamma doses (beyond the dose where total RMS noise reaches the maximum); fluctuations of total RMS noise about the maximum value were observed.

Figure 6 shows the plot of the total RMS noise versus the gate leakage current, I_{GSS}. It follows more or less a linear relationship. The graph for rise time versus Gamma radiation dose is shown in Figure 7. It shows an increase in rise time with Gamma dose up to a maximum and then saturates at around 160 ns. One batch of preamplifiers started out with a rise time of about 76 ns while the other started out at 160 ns; however, they both saturated at about 160 ns. The batch that started out with slower rise time probably came from a wafer that was not as "clean" as others.

After exposing the prototype preamplifiers to a neutron dose of $2x10^{13}/cm^2$, no sign of degradation of performance of the preamplifiers was observed. More neutron tests will be performed in the near future and we will report on the results later.

Conclusion

The potential of using BiFET IC technology to design charge preamplifier for a radiation environment has been illustrated. The presented prototype realizes a low noise (less than 1,000 electrons RMS before radiation), low power consumption, and high speed implementation. This type of preamplifiers are expected to perform well in the portions of the Superconducting Supercollider where the total radiation doses do not exceed 200 to 300 kRad of Gamma rays and $10^{13}/cm^2$ of neutrons per year. For the limited sections with higher total radiation doses, noise level will gradually increase to 2,400 electrons RMS. Hence, there is a strong incentive to search for IC processes in which flicker noise is less dependent on radiation damage.

References

[1] E. GATTI, A. HRISOHO, P.F. MANFREDI, "Choice between FETs or Bipolar Transistors and Optimization of their Working Points in Low Noise Preamplifiers for Fast Pulse Processing.", IEEE Trans. Nucl. Science, Vol.NS- 30, pp.319-323, 1983.

[2] V. RADEKA, S. RESCIA, "Speed and Noise Limitations in Ionization Chamber Calorimeters.", Nuclear Instruments and Methods in Physics Research, A265, pp. 228-242, 1988

[3] AMPTEK Inc., A250 Data Sheet, Oct. 1986

[4] TOSHIBA, Field Effect Transistor Datasheets (2SK147, 2SK153), INTERFET Corp., FET Data Book

[5] G.C. MESSENGER, M.S. ASH, "The Effects of Radiation On Electronic Systems.", Van Nostrand Rheinhold Corp., New York, 1986

[6] Group Discussion at the Workshop on Calorimetry for the SSC, Tuscaloosa, Alabama, Feb. 13-17, 1989

[7] D. DiBITONTO, P.M. VANPETEGHEM, et al., "Advanced Forward Calorimetry for the SSC and Tevatron Colliders.", to be published in: Nuclear Instruments and Methods in Physics Research, 1989

[8] C.D. MOTCHENBACHER, F.C. FITCHEN, "Low-noise Electronics Design.", Wiley, New York, 1973

[9] P.R. GRAY, R.G. MEYER, "Analysis and Design of Analog Integrated Circuits.", Wiley, 1984

[10] S.M. SZE, "Physics of Semiconductor Devices.", Wiley, New York, 1981

[11] IEEE Std. 301-1976, "IEEE Standard Test Procedure for Amplifiers and Preamplifiers for Semiconductor Radiation Detectors for Ionizing Radiation.", IEEE Press, Jan. 30, 1976

[12] D. DIBITONTO, S. NARAYAN, P.M. VANPETEGHEM, S.Y. LEE, K.Y. LING, H.H. LIU, "Fast, Radiation-Hard Charge Preamplifier for Warm Liquid Calorimetry." Presented at the Workshop on Calorimetry for the SSC, Tuscaloosa, AL, March '89

[13] P.M. VANPETEGHEM, K.Y. LING, S.Y. LEE, H.H. LIU, D. DIBITONTO, "On the Design of Fully-Integrated Charge Preamplifiers for the Superconducting Supercollider." Presented at the Workshop on Calorimetry for the SSC, Tuscaloosa, AL, March '89

[14] L.W. Ricketts, "Fundamentals of Nuclear Hardening of Electronic Equipment.", Wiley, 1972

Acknowledgements

Hewlett Packard Corp. donated essential software for signal processing and fitting on HP9000 computer.

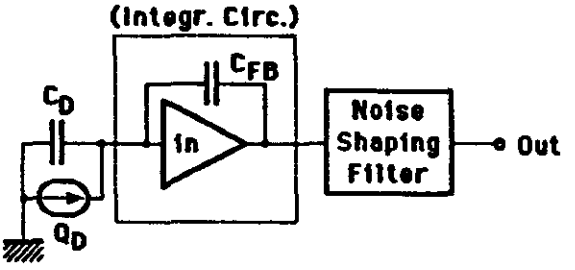


Figure 1. Circuit schematic of charge preamplifier system.

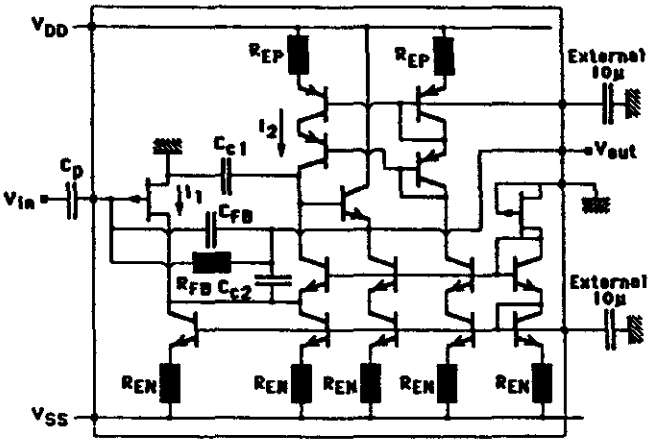


Figure 2. Internal circuit schematic of the BiFET charge preamplifier.

Parameter	NPN	PNP
β	127	250
I_{kF}	$19mA$	$0.12mA$
V_A	$200V$	$60V$
R_B	85Ω	80Ω
R_E	51Ω	5Ω
τ_F	$470ps$	$29ns$
C_{js}	$1.1pF$	$1.5pF$
C_{jC}	$0.5pF$	$1.5pF$
C_{jE}	$1.7pF$	$1.4pF$

Table 1: Typical bipolar transistors parameters (before radiation).

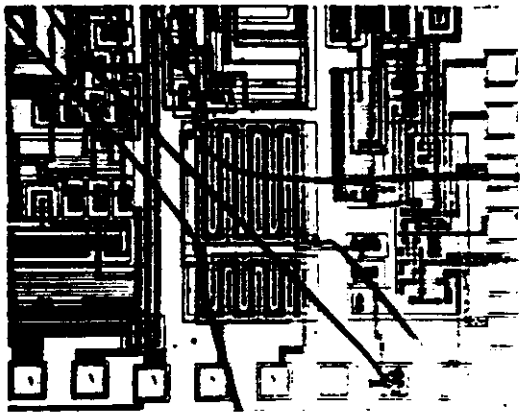


Figure 3. Microphotograph showing the input P-JFET of the charge preamplifier.

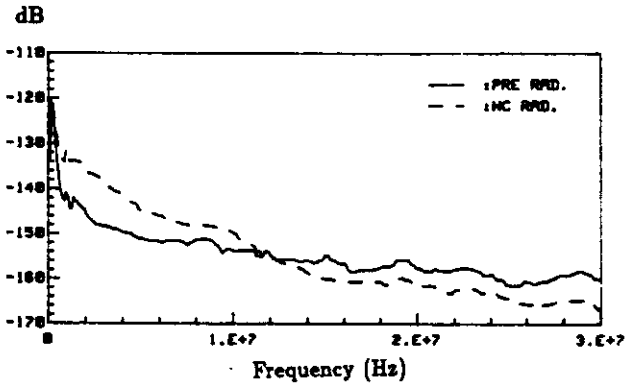


Figure 4. Measured noise spectral density of the preamplifier before and after Gamma radiation (worst case).

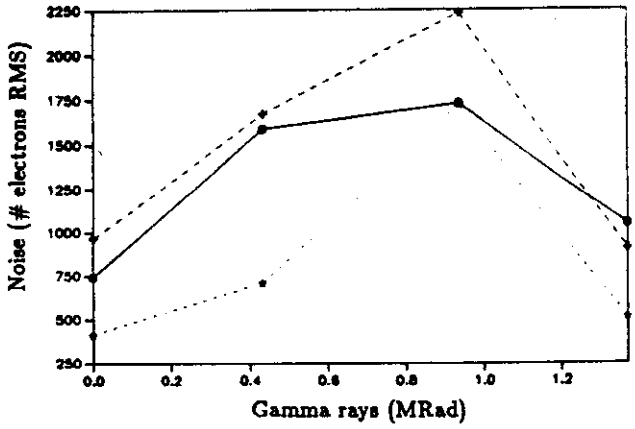


Figure 5. Measured total RMS noise vs. total Gamma radiation dose for 3 typical samples.

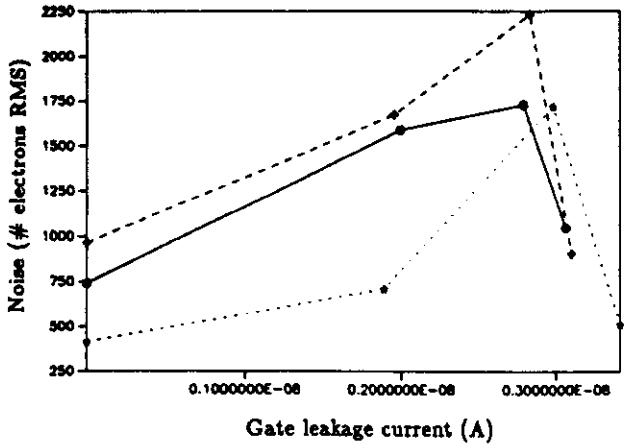


Figure 6. Scatter plot of the measured total RMS noise vs. input P-JFET gate leakage current.

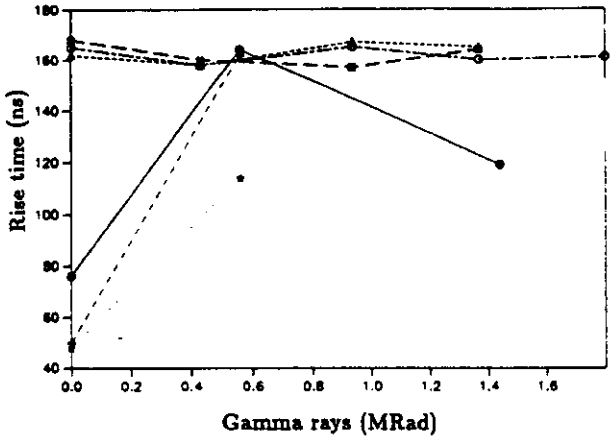


Figure 7. Measured rise time vs. Gamma radiation dose for 6 samples.

Trans./ Preamp.	Param./ Spec.	Before	Gamma (Co^{60}) 0.56M	Gamma (Co^{60}) 1.43M	Neutrons $2 \times 10^{13}/cm^2$
JFET	I_{GSS}	< 10 pA	2.0 nA	3.0 nA	0.24 nA
	G_m @$V_{GS} = 0$	8.69 mS	8.26 mS	7.1 mS	8.7 mS
	K_F	$3.7f$	$5.0f$	$6.0f$	$3f$
Bi-polar	I_S	260 fA	14 pA	15 pA	72 pA
	$\beta_{N,\,max}$	95	28	36	96
Pre-Amp.	Rise time	76 ns	164 ns	119 ns	74 ns
	Fall time	76 ns	168 ns	122 ns	74 ns
	Noise	742 e^-	1589 e^-	1730 e^-	700 e^-
	Power	< 80 mW	< 80 mW	< 80 mW	< 80 mW

Table 2. Measured typical preamplifier specifications and transistor parameters before and after radiation.

7. Subcontracts, Letters of Support, Endorsements

1) Subcontract and support from Texas A&M University Nuclear Science Center

2) Quotation for I.C. Processing and Technical Support, Texas Instruments, Dallas, TX

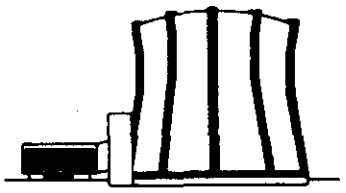
3) Quotation for I.C. Processing and Technical Support, Harris Semiconductor, Melbourne, FL

4) Letter of Support, Honeywell, Minneapolis, MN

TEXAS ENGINEERING EXPERIMENT STATION

TEXAS A&M UNIVERSITY
COLLEGE STATION, TEXAS 77843-3575

13 July 1989



NUCLEAR SCIENCE CENTER
409/845-7551

Dr. Lynne Jordan Bowers
Division of Research Programs
Texas Higher Education Coordinating Board
P.O. Box 12788
Austin, Texas 78711

Dear Dr. Bowers:

Please accept this letter in support of the proposal titled "Radiation Hardened Particle Detection for the Superconducting Supercollider" submitted by Dr. Peter VanPeteghem of Texas A&M University. The Nuclear Science Center will be used to provide neutron radiation exposures for the stated project in order to test the electronic devices constructed by Dr. VanPeteghem's team. The NSC currently provides similar services to the Electronics and Defense Sector of TRW, Inc. This program has been ongoing for over 18 months and the NSC has gained invaluable experience in this type of work. We feel that the radiation exposures and testing that Dr. VanPeteghem proposes will provide him with pertinent data in regards to his stated aim of developing radiation hardened (resistant) devices.

Dr. VanPeteghem has estimated that the project will require from 20 to 30 irradiations at the NSC using our Irradiation Cell. Each of these irradiations will typically last from 20 to 30 minutes. As stated in the NSC's Service Charge Schedule (copy enclosed) which becomes effective 1 September 1989. the charge for Irradiation Cell operations is a $500 set-up fee and a useage fee of $360 per hour with a minimum charge of 1/2 hour. Assuming the minimum charge time, then, a typical irradiation for the proposed project would have a service charge value of $680. Therefore, the proposed project would incur total projected reactor useage charges of from $13,600 to $20,400. In order to support the proposed work by Dr. VanPeteghem, the Nuclear Science Center is prepared to foregoe the set-up fees for the first 20 (twenty) cell irradiations performed under this project and charge for useage time only. In return, Dr. VanPeteghem has agreed to perform his irradiations on an as available basis with the understanding that the NSC agrees to perform at least 20 such irradiations, if requested, within 24 months from the awarding of any grant for the project. For any irradiations beyond 20, the NSC proposes to charge the project full costs with the project then gaining normal scheduling considerations. Thus, for a projected total value of $13,600 to $20,400, the NSC stands ready to contribute $10,000 dollars in services in support of this proposal. Please note that the NSC currently has scheduled use of the irradiation cell at least twice per month, and so we anticipate a minimum of delays to the proposed work due to scheduling problems.

The Nuclear Science Center is operated by the Texas Engineering Experiment Station and thus is part of the Texas A&M University System, but not part of Texas A&M University. The NSC is pleased to be able to offer this support for Dr. VanPeteghem's proposed project. If you have any questions or need any further information in regards to our participation in this proposal, please feel free to contact me either directly or through Dr. VanPeteghem.

Sincerely,

John L. Krohn
Assistant Director

JLK/ym

Enclosure

TEXAS INSTRUMENTS

27 July 1989

In reply refer to:
230-341-211
Mail Station 3137

Texas A&M University
Department of Electrical Engineering
College Station, Texas 77843-3128

ATTENTION Dr. Peter VanPeteghem
Assistant Professor

SUBJECT Request for Quotation (RFQ):
LTR-6-15-89
Fabrication of BiFET Test Circuits

ENCLOSURE (1) Technical Description

Gentlemen:

In response to the subject RFQ, Texas Instruments Incorporated is pleased to provide a cost-plus-fixed-fee (CPFF) proposal for BiFET test circuits as follows:

ITEM	DESCRIPTION	ESTIMATED COST	FIXED FEE	PRICE
001	Device Modeling	$ 7,617.00	$ 519.00	$ 8,136.00
002	Bar Layout and Masks	53,109.00	3,678.00	56,787.00
003	Wafer Processing	32,560.00	2,276.00	34,836.00
		$ 93,286.00	$ 6,473.00	
			Total CPFF:	$ 99,759.00

Enclosure (1) contains a description of our technical approach.

Terms and conditions are reserved for mutual agreement prior to acceptance of any resultant contract. This quotation shall expire on 30 November 1989.

Your consideration of Texas Instruments for the subject effort is appreciated.

If technical information is required, please contact Mr. Wayne Dietrich at (214) 480-1042. Contractual issues should be directed to Ms. Daphne L. Beer, Contract Administrator, at (214) 480-6308, telex number 6829291, Terminal ID, EGCT, or facsimile machine (214) 480-6259.

Sincerely,

J.C. Wilson
Vice President
Defense Systems & Electronics Group
Manager, Advanced Microelectronics Division

JCW/DLB/mlm 1/211

Enclosure (1) to TI
Letter 230-341-211
dated 27 July 1989

TECHNICAL DESCRIPTION

Texas Instruments Incorporated is pleased to provide the following support for your Super-Collider, Charge Amplifier Integrated Circuit development effort with prototype wafer processing, die layout clean-up and verification:

- Device modeling for a group of 10 PNP and NPN devices in any combinational group of less than 10 total PNP and NPN devices for both pre and post-radiation characterization. Each modeling run of 10 units with actual radiation exposure being performed by Texas A&M is $ 8,136.00.

- With Texas A&M providing a preliminary layout die, TI will: (1) complete the layout to our design rules for the Complementary DI /P-Ch. J-FET process on the Calma graphics system; (2) verify the layout for schematic and topological integrity; and (3) have a complete mask set fabricated for this circuit. Each pass of this design effort is $ 56,787.00, providing the circuit complexity is less than 150 transistors. Circuits of higher complexity can be designed but for an additional cost at a level of effort. TI will participate in circuit design review prior to initialization of layout by TI.

- Texas Instruments will process a single 24 wafer start lot of material with the Complementary DI with P-Ch. J-FET process in the Military Products Front End. The processing charge for this material will be $ 34,836.00 per good lot completed. It is anticipated that the wafer lot yield will be 7 finished wafers. Each wafer from this lot must meet an agreed upon static specification for the wafer's 5 static test cells. This test cell consists of a NPN, PNP, P-Ch. J-FET transistors and two resistors. For each wafer to be good and deliverable, the test cell devices must pass the probe of 4 of the 5 cells. This specification agreement must be completed prior to initialization of the die layout by TI. TI is delivering only test cell evaluated material, not circuit probed wafers to Texas A&M. Good wafer out processing time is not to exceed 9 months after receipt of the full mask set by the Military Products Frond End.

HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

August 28, 1989 In reply refer to: 90:0637\AHC

Texas A & M University
Department of Electrical Engineering
College Station, Texas 77843-3128

Attention: Dr. Peter M. VanPeteghem

Subject: Harris Semiconductor, Military and Aerospace Division (HM&AD) ASIC Proposal P-1988

Reference: Texas A & M Letter dated June 15, 1989 from Dr. VanPeteghem to Mr. T. Danhauser

Gentlemen:

Harris Semiconductor, Military and Aerospace Division (HM&AD) is pleased to provide this Rough Order of Magnitude (ROM) Proposal for the development of a mask set and wafer fabrication of Rad-Hard Particle Detection circuit.

STATEMENT OF WORK

HM&AD will take the circuit in Calma GDS II form and add drop-ins, alignment marks and perform design rule checks. A 16 level mask set will be fabricated. Following the completion of the mask set, one (1) wafer fab run of 20 wafers will be started using the VHFP process. The wafers will receive in line probing and be shipped to Texas A & M as PCM good wafers. The wafers will be circuit probed at the customers site. HM&AD would receive the probed wafers and scribe, break, and package the die in 40 pin CDIP packages.

DEVELOPMENT PRICE

This ROM price for development is currently based on using the VHFP process.

DEVICE DESCRIPTION	LIBRARY	NRE $
Pre-Amp Array	VHFP	$75,000.

DEVELOPMENT DELIVERY

Prototype delivery is 15 weeks after customer release of a approved Calma GDS II tape.

ASSUMPTIONS AND CONDITIONS OF SALE

- The prices quoted herein assume delivery of PCM good wafers only.
- NRE includes the delivery of 25 package units. No package test is included in this quotation.
- Tools, test fixtures or equipment are considered to be expendable and no inventory accountability or reporting cost is included herein.
- All pricing is based on non-classified circuits.
- No backup wafer fab runs are costed in this proposal.

MILESTONE BILLING

50%	Upon Receipt of Order
50%	Upon Shipment of First Units

TERMS AND CONDITIONS

HM&AD's Standard Terms and Conditions of Sale (Form M44B, Rev.1.8[illegible]. attached) shall apply to any resultant order.

Validity Period:	30 days from date of this proposal
F.O.B. Point:	Palm Bay, Florida, Freight Collect
Terms of Payment:	Net 30 days from date of each invoice

Should you have any questions regarding this matter, please contact the undersigned at (407) 729-5655 or the Program Manager, Mr. Joe Mayer at (407) 729-5683.

Very truly yours,

A. H. Cannone
Manager, Contract Administration

AHC/mlm

cc: J. Mayer
T. Danhauser

Honeywell

20-June-1989

To Whom It May Concern:

We are supportive of the efforts by Professors van Peteghem, Geiger, and DiBitonto of Texas A&M University in developing a radiation hardened particle detector for the superconducting supercollider. The development of radiation hard linear integrated circuit technology has application beyond energy research into key areas of defense (including SDI) as well as commercial space applications such as telecommunications, satellite exploration, and the manned space station. As an industry leader in these areas, Honeywell believes the subject proposal could serve an important ground-breaking function by performing basic research into the performance of various IC technologies under radiation as well as understanding the mechanisms involved. Providing this data for industry would accelerate the development of advanced microelectronics needed for next-generation commercial and defense systems.

Honeywell's Sensor and Signal Processing Laboratory has been collaborating with Professor van Peteghem of Texas A&M University since early 1989. Combining their expertise in circuit design with Honeywell's advanced IC processing capability enables us to progress more quickly and efficently. We plan to continue our collaboration into the forseeable future as well as involving the Texas A&M group in new programs at Honeywell. We have developed a high respect for the technical excellence of Professor van Peteghem's team and believe any effort they tackle would be well-served.

Sincerely,

David Tetzlaff
Section Head, Digital/Linear GaAs ICs
(612) 887-4052