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eLine10k: a High Dynamic Range Front-End ASIC for LCLS Detectors

A. Dragone*, P. Caragiulo, G. A. Carini, R. Herbst, J.F. Pratte, P. O'Connor, P. Rehak, D. P. Siddons and G. Haller

***Abstract*–eLine10k is a fast-frame, 64-channel readout ASIC for SLAC Linac Coherent Light Source (LCLS) detectors. The circuit has been designed to integrate the charge from high-capacitance 2D sensors with rolling shutter and 1D strip sensors. It is suitable for applications requiring large input signal range, on the order of 10^4 photons/pixel/pulse at 8keV ($22Me^-$), and a resolution of half a photon FWHM ($500e^-$ r.m.s). 2D sensors with a rolling shutter like the X-ray Active Matrix Pixel Sensor (XAMPS), for which the ASIC has been optimized, present several pixels which are bussed on the same readout line. Large input capacitance to each channel is expected leading to stringent noise optimization requirements. The large required number of pixels per channel, and the fixed LCLS beam period impose limitations on the time available for the readout of each single pixel. Giving the periodic nature of the LCLS beam, the ASIC developed for this application is a time-variant system, providing low-noise charge integration, filtering and correlated double-sampling, and a processing speed up to 500k pixel/s on each channel. To cope with the large input dynamic range, a charge pump scheme has been implemented using a synchronous zero-balance measurement method. It provides on-chip 4-bit coarse digital conversion of the integrated charge. The residual charge is sampled using correlated double sampling into an analog memory, multiplexed and measured with the required resolution using an external ADC. In this paper, the ASIC architecture and performance of the final release are presented.**

I. Introduction

The unique characteristics of X-Ray Free-Electron Laser (X-Ray FEL) sources, in terms of brilliance and narrow pulse duration, have increased the need for new large area detectors with fast readout capabilities and specifications that, depending on the experiment, can range from ultra-low noise requirements to extremely large full-scale and dynamic ranges. eLine10k (Fig. 1) has been the first of a new class "eLine" of multichannel time-variant integrating front-end Application Specific Integrated Circuits (ASIC) that SLAC has developed for the Linac Coherent Light Source (LCLS). The class is composed of two front-end ASICs, one designed for high-dynamic range applications (eLine10k) and one designed for ultra-low noise applications (eLine100 [1]). The class also include a switcher ASIC (sLine [2]) used to control the operation of column-parallel readout 2D sensors with rolling shutter, such as the X-ray Active Matrix Pixel Sensor (XAMPS), developed at Brookhaven National Laboratory.

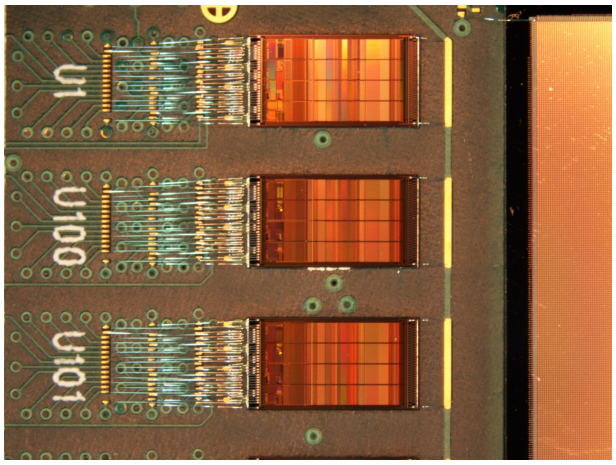

Fig. 1: eLine10k in a XAMPS detector prototype.

Since, in FEL applications, photons hit sensors simultaneously, only integrating detectors can be used. eLine10k is designed to integrate charge from high-capacitance 1D sensors or 2D column-parallel readout sensors with rolling shutter. XAMPS [3] is a pixel array detector with integrated JFET switches (Fig. 2) used to gate the transfer of charge to the front-end electronics. The ASIC was designed with a general purpose approach, optimized for XAMPS.

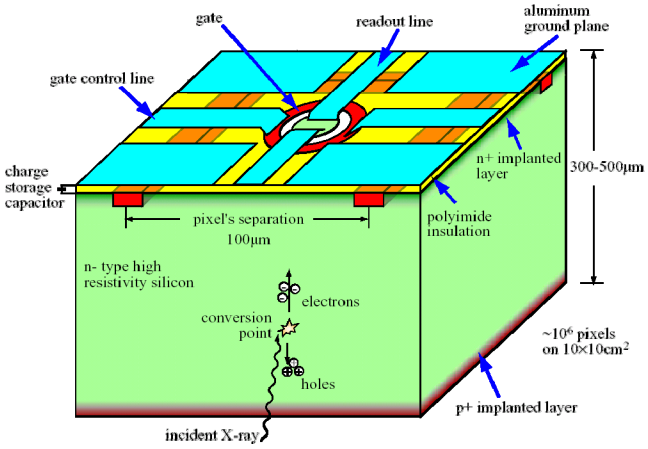

Fig. 2. XAMPS pixel structure.

In XAMPS, pixels are isolated from each other by potential barriers. The device is fully depleted by applying a high negative voltage to the junction on the entrance window of the device. When a photon is absorbed, the generated carriers drift to the exit side of the device and are collected by an implant,

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which is the floating electrode of the pixel and the source of the JFET switch. Thus, this region, which occupies most of the pixel area, together with the isolated metal layer on its top forms the capacitor in which the charge is stored. The integration and readout phases of pixels in a same row are controlled by a dedicated switcher ASIC that effectively implements the operation of a rolling shutter.

The detector is designed to satisfy stringent requirements in terms of input dynamic range, noise and timing of the X-ray Pump Probe (XPP) instrument [4] for the Linac Coherent Light Source (LCLS), where ultra-short (100fs at 120Hz) pulses are used to probe the transient state of matter excited using a fast optical laser. Depending on the experiment, X-ray absorption and emission or X-ray scattering will be recorded, requiring a 2D integrating detector [5-9; note that in these references, eLine10k is generically referred to as FEXAMPS]. Typical requirements for this instrument include input of full-scale signals for both the sensor and the electronics on the order of 10^4 photons (8keV), to be acquired with a resolution of half a photon FWHM. The large full-scale signal requires a large storage capacitance per pixel, making it difficult to satisfy the noise specifications. Furthermore, the required detector area and the pixel pitch needed for good position resolution impose limitations on the time available for readout. Tiled XAMPS detectors of up to 1024 x 1024 pixels with a pitch of 90µm are in fabrication for this instrument.

The architecture and results of the first prototype of this ASIC were presented in [5]. Herein we report on the architecture and performance of the last and final release of the ASIC. eLine10k provides low-noise charge integration, real-time adaptive time-variant filtering [10-11], and correlated double-sampling. As with all the ASICs in the eLine class, a charge pump scheme is used, implementing a zero-balance measurement method [5] to satisfy the large full-scale signals. This method provides an on-chip coarse analog to digital conversion allowing a measurement of residuals with the required resolution. The residuals conversion is performed with external 14-bit ADCs. The actual version of the ASIC has 64 channels, is 6×3.5mm^2 in size and was fabricated in TSMC CMOS 0.25µm technology. After a description of the detector systems for which the eLine class is designed, the ASIC architecture will be discussed in section III. The charge pump approach will be described in section IV. The ASIC characterization and some experimental results are reported in sections V and VI.

II. Column-Parallel Readout Detector Systems

During the first years of operation at LCLS, the need for several new large area detectors arranged in different form factors and shapes, and supporting a wide spectrum of experiments has been apparent. Modular, scalable designs are a must. To simplify integration and reduce development time, detectors have been designed around common platforms so that dedicated sensing heads could be incorporated in a common detector system. eLine is the first example of a class of ASICs for LCLS sharing a common back-end section and interface to the rest of the system. The class is designed for the readout of column-parallel readout sensors, although it can also be used for the readout of 1D strip sensors. A typical block diagram of these kinds of systems is shown in Fig. 3. Pixels in the sensor are arranged in a matrix fashion. The collecting nodes of the pixels are isolated by means of a "switch". For applications, like XAMPS, the switch could be a FET. In other cases, the collecting node could be isolated from the collection area by means of controllable potential barriers (XCPS [1, 12]). The "switches" associated with the pixels in a column are connected to the same readout line, while the gates (called transfer gates) of those associated to the pixels in a row are activated simultaneously. Columns of the sensor are read out in parallel by the front-end ASIC. This architecture allows a parallel readout of all the pixels in the same row. The full frame can be read out by cycling through the rows. Each column of the sensor is read out by a dedicated electronic channel.

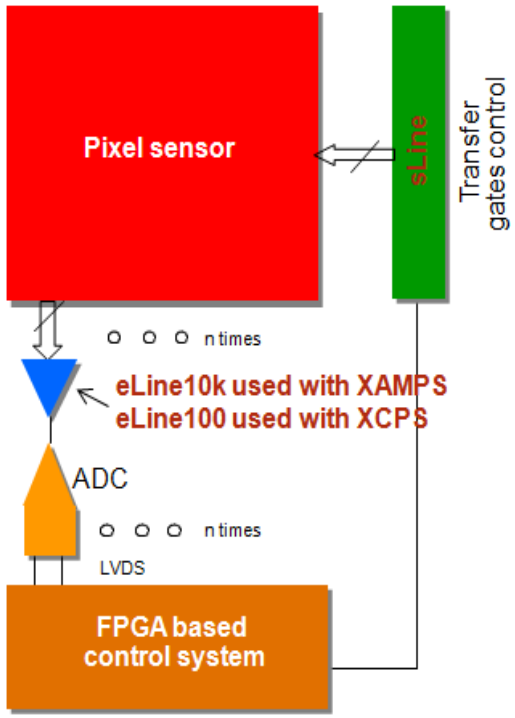

Fig. 3. Column-parallel read out system based on eLine.

External commercial ADCs are used to convert the output analog signals. The acquisition is controlled by an FPGA that maintains the synchronization between the LCLS beam and the selection of the rows to be read out. Typical array sizes (frame sizes) are in the range of 1024x1024 pixels. Given the repetition rate of the LCLS beam (120Hz) a frame has to be read out in 8ms which, because of the parallel row readout, turns into a readout time slot of not more than 8µs per row (i.e. per pixel on a specific readout channel). Multiple frame readout per pulse is desirable to perform more sophisticated corrections (acquisition of intermediate dark frames), but imposes additional timing constraints. eLine10k can process signals at a maximum rate of 500k pixel/s on each channel or 480Hz for 1024x1024 pixel frames.

III. ASIC ARCHITECTURE

A simplified block diagram of the ASIC architecture is presented in Fig. 4. The 64 channels of the ASIC are arranged in 4 groups of 16; each one connected to its own analog and digital multiplexers and dedicated outputs. The 4 blocks are read in parallel to speed up the read out phase. The acquisition is controlled by a single periodic signal (slot control, SC) whose period defines the readout time slot per row. This signal is synchronized to the LCLS beam trigger. During the active part of the SC period the charge is read out from the pixels and sampled. During the inactive period, stored data are read out and the system is reset.

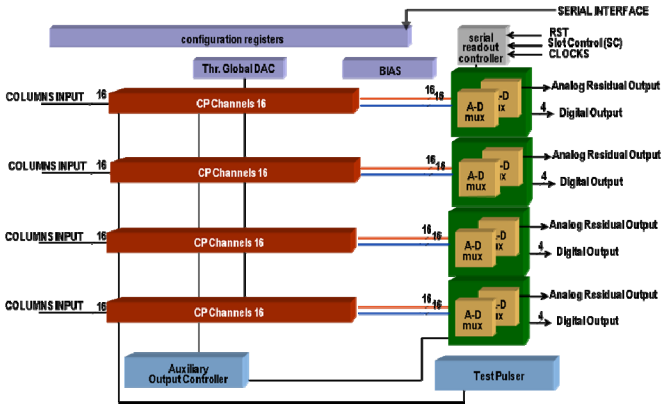

Fig. 4: Simplified block diagram of the 64-channel ASIC.

Each channel (Fig. 5) is composed of a front-end section with a double polarity low-noise charge integrator with programmable gain, a pulsed reset, a second-order non-inverting programmable LP filter, and a discriminating charge pump circuit. The back-end section of the channel is common to all readout ASICs in the eLine class and is composed of two correlated double-samplers (CDS) and the multiplexers.

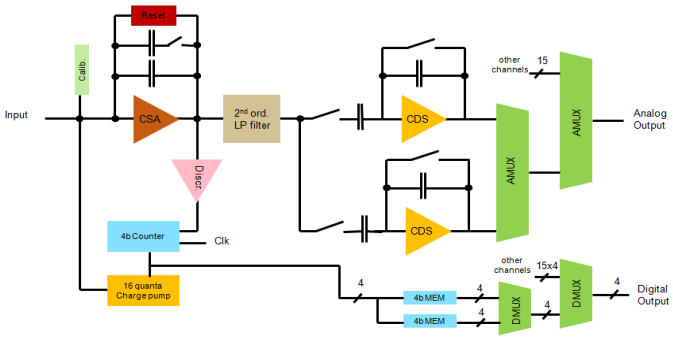

Fig. 5: Simplified schematic of a single channel.

The low noise preamplifier integrates the input charge into a feedback capacitor. Two feedback capacitors are provided allowing gain programmability (5mV/fC in standard gain mode or 2.5mV/fC in double gain mode). The preamplifier is designed in a straight cascode configuration with gain boosting. To minimize flicker noise impact, the input device is a PMOS, biased at 250µA. Its size (W= 1.5mm L=0.24µm) is optimized for a 15pF input capacitance and for noise levels within the 500e^- r.m.s. required by the application.

The pulsed reset system is able to set the DC output point of the amplifier to the same value of the input (about 2V), close to the upper rail or close to the lower rail (about 0.5V), allowing the ASIC to integrate charge of both polarities, thus accommodating different types of sensors.

To increase the output dynamic range and to minimize non-linearity effects in the preamplifier response, an output stage using zero-threshold MOSFETs has been implemented. The second-order LP filter is designed according to a Sallen-Key non-inverting topology and makes use of a rail-to-rail differential amplifier with constant trans-conductance.

The filter has two coincident real poles with programmable time constant. Since the application requires the readout of a pixel within a given time slot, the time constant value has to be set in such a way that the response of the filter reaches a flat top in half of the time slot. Eight values of the time constant are implemented resulting in readout timing slots from 1µs to 8µs in 1µs steps.

The two CDS stages are used to sample and store the filter output, purged from the fluctuations introduced by kTC noise, baseline fluctuations [11]. They also reduce low frequency noise. The two CDS stages operate in an alternating way to allow simultaneous read-write of the same channel. While one sampler holds the previous event and presents it to the active one of two analog multiplexer for readout, the other sampler is ready to process the next event. In such a way, when a row of the sensor is processed the results from the previous one are read with no dead time. This architecture allows the implementation of a "quasi-trapezoidal" noise weighting function [10-11]. Fig. 6 shows the shape of the function extracted from the full channel simulation.

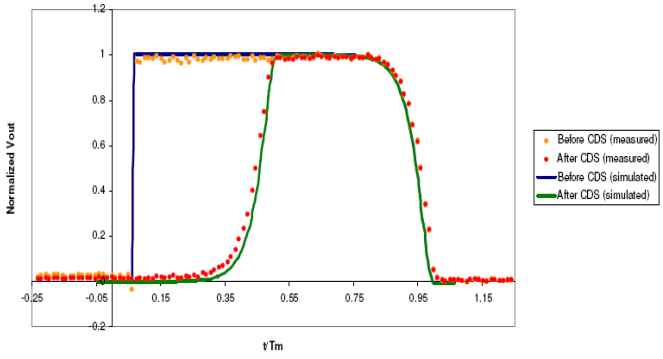

Fig. 6. Simulated and measured noise weighting function normalized to the readout time slot.

As shown in the figure, without performing the CDS a very steep leading edge in the weighting function is present. As known from noise weighting function theory [10, 11, 13], this effect leads to a large series noise (a factor 2 difference in the series noise ENC has been calculated with and without CDS). The slope of this leading edge is related to the reset system time constant. To avoid this effect, either a slow reset is required or a correlated double sampling scheme. We

preferred to implement the latter for the additional advantages of the CDS technique mentioned earlier.

To cope with the required large input dynamic range of 10^4 photons at 8keV (about 3.5pC of charge) a charge pump system, described in the next section, is included in the channel.

A number of 16:1 multiplexers are common to all channels for monitoring and read out. An automatic calibration system featuring an internal pulse generator is implemented combining a 10-bit DAC for the injection of calibration signals, and a 10-bit counter. Another 10-bit DAC is used for the global charge pump threshold setting with each channel implementing trimming for equalization. The logic for the acquisition, readout, and configuration is also common to all channels.

By making use of some innovative analog circuit solutions the ASIC presents a noise floor of 480e^- r.m.s at room temperature with a 15pF input load. It has a total dissipated power of about 3mW per channel and it is suitable for applications requiring resolutions on the order of 600e^- r.m.s and signals up to 12,000 photons at 8keV.

IV. The Charge Pump Approach

To cope with the large input dynamic range a zero-balance measurement method has been implemented. In double gain mode, the preamplifier feedback capacitance (Fig. 7) is sized to hold 1/16 of the full input signal range without saturating the preamplifier.

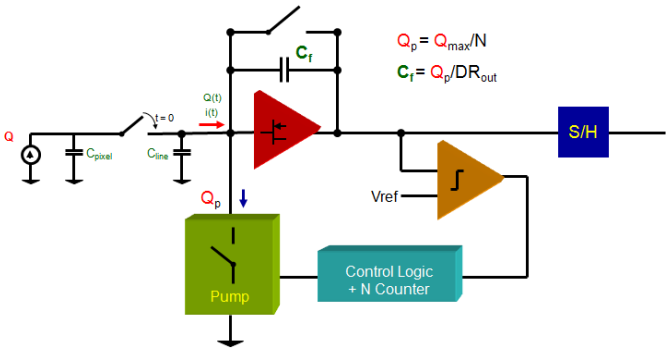

Fig. 7. Charge pump principle of operation (N=16, DRout=max preamp output voltage swing).

When larger signals arrive the preamplifier moves toward saturation and the excess charge remains stored in the input node capacitance. Our approach makes use of a charge pump connected to the input node controlled by a 4-bit counter. As soon as the saturation condition is approached, a threshold discriminator (lower limit of the range) enables the counter (driven by a periodic clock at 25 MHz). Every increment in the counter (pump step) removes 1/16 of the full range quantum of charge from the input node until the output of the preamplifier returns above threshold. At this point the residue stored in the feedback capacitor is converted through the chain described in the previous section. The value stored in the 4-bit counter is equivalent to a coarse digital conversion and represents the MSB of the digitized amplitude. The digital information is read out together with the residue, which is then digitized with an external 14-bit ADC.

The pump is designed using 15 capacitors connected together to the input node on one side and, by means of switches, to two external reference voltages (analog ground and a dedicated 2.5V supply Vdd pump) on the other side. A single capacitor is switched for each increment of the counter (Fig. 8).

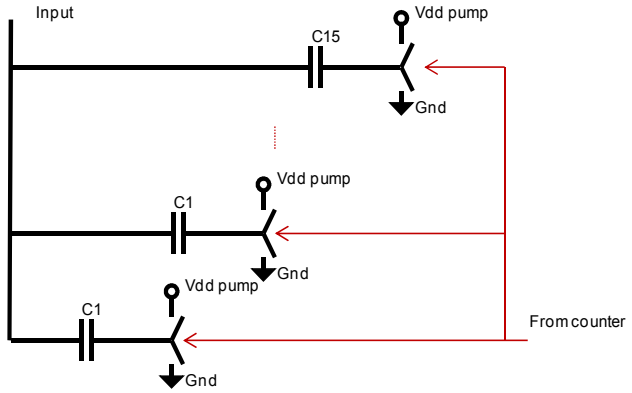

Fig. 8. Charge pump implementation.

The external reference voltage (Vdd pump) can be adjusted, allowing the size of the charge quanta to be tuned (and thus the upper limit of the range adjusted). The kTC noise contribution of such a reference is estimated to be up to 30 e^- r.m.s. using standard external voltage regulators. Thus it is negligible with respect to the required noise levels, and also affects only large signals, for which noise is dominated by the statistical fluctuations of the source.

Similar approaches with different implementations have been proposed in [14-16]. Our approach has a unique advantage. The quanta of charge pumped are not dependent on the input node voltage. In FEL applications, the charge arrives instantaneously on the detector, and if saturation occurs, the virtual ground at the preamplifier input is suddenly lost. The charge is stored in the input node and can be correctly measured if the charge pump quanta are not affected by the input node voltage. Note that in simple pad detectors losing the virtual ground would cause the charge to be collected by neighboring pixels, but this effect is prevented in sensors like XAMPS that have boundary guard implants surrounding each pixels. In normal gain mode, since the feedback capacitor is two times larger the pump switches two capacitors of the 15 in parallel (only 7 pump steps).

Because of the charge pump operation the circuit has a piecewise linear response as depicted in Fig. 9a. When the input charge increases, the output of the amplifier moves away from the baseline until it reaches the comparator threshold (pump threshold). At the first pump step, the output of the amplifier moves back toward the baseline by a voltage step (pump height) that depends on the ratio between the pump capacitors and the feedback capacitor, and on the adjustable pump voltage (Vdd pump). Each pump step has an identical slope since the circuit configuration does not change. Calibration thus only requires the measurement of the voltage

steps associated with the 15 pump steps. The programmability of the pump threshold, the pump height, the gain and the number of pump steps, provide high versatility. The characteristic can be "stretched" as depicted in Fig. 9 b-d.

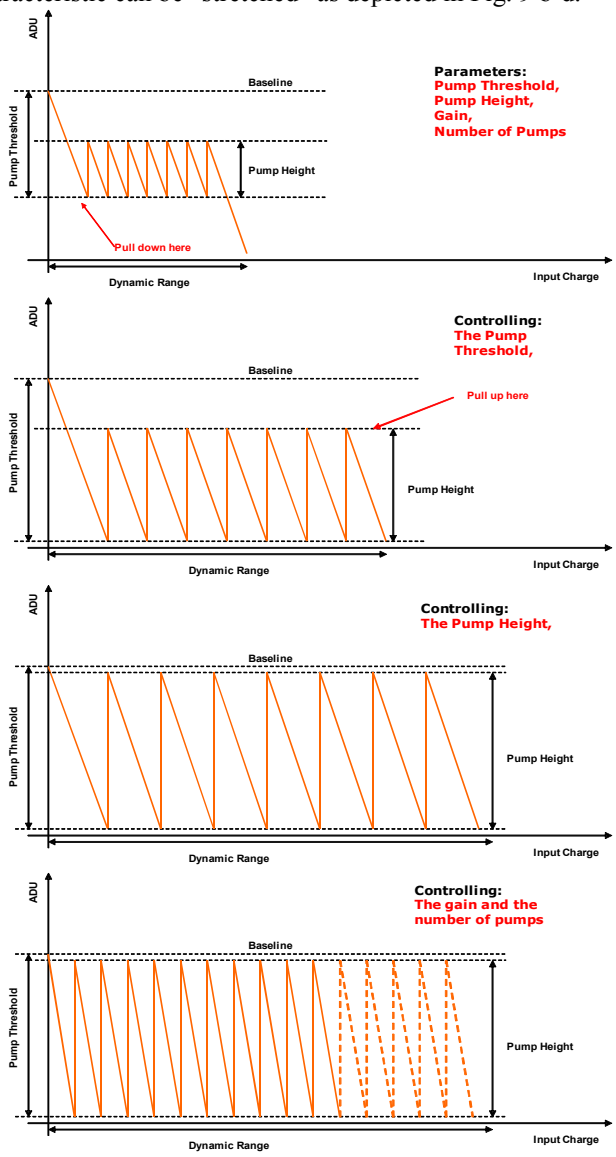

Fig. 9a-d. Sketch of typical transfer characteristics of eLine10k (a). The characteristic is "stretchable" to maximize the dynamic range. The pump threshold can be lowered until the saturation of the preamplifier appears (b). The pump height can be increased until each pump step brings the preamplifier output back to the baseline (c). The gain and the number of pumps can be programmed to increase sensitivity and dynamic range (d).

V. Measured Performance

eLine10k is fabricated in TSMC CMOS 0.25 µm technology. It has a size of 6 mm × 3.45 mm and a power dissipation of 3mW/channel. The most relevant characteristic performance results of the ASIC in a test setup are reported here. The ASIC has also been characterized in several prototype detectors including a 128x256 XAMPS detector. Performance results in these prototypes are reported in [17].

A. Gain and linearity

This first set of measurements aims at testing the linearity and the gain of the device. In Fig. 10 the analog residue response measured at the output of a channel bank is reported for different biasing conditions (current in the input device can be boosted by 50%). To maximize the exercised range of the output characteristic, the position of the baseline can be globally trimmed with 2-bits in steps of 50mV.

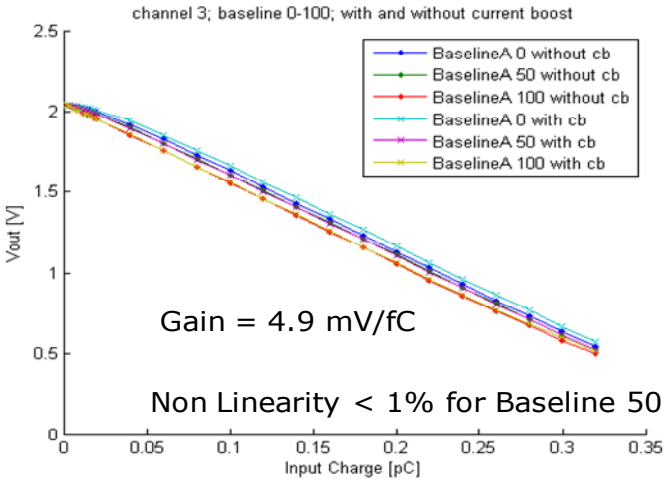

Fig. 10. Analog residue response measured at the output of a channel bank in different input transistor biasing conditions and for different baseline values.

A residual non-linearity below 1% has been measured, satisfying requirements. The overall channel gain is 4.9mV/fC, 2% smaller than the nominal value. The value is in line with the expected parasitic feedback capacitance. No significant difference has been found between the response with and without boosting the input device current, confirming the correct behavior of the preamplifier, in terms of open loop gain.

B. Transfer characteristic

This second set of measurements aims at testing the channel response as a function of the input charge, and in particular the behavior of the charge pump circuit. The analog and digital response of a channel has been scanned by injecting charge from an external pulser. The analog residues have been digitized with an external 14-bit ADC. Figs. 11 and 12 show the fitted transfer characteristics in standard gain mode and double gain mode, respectively. The curves confirm the correct behavior of the ASIC validating the charge pump concept. The charge pump circuit behaves correctly in all 16 ranges, with a negligible dispersion in the measured pump steps. Because of the limited number of sampling points, the dispersion appears large in Fig. 12, but a close up comparison of the first and last pump transitions scanned with a higher resolution is reported in Fig. 13, showing negligible variations. From the curves it is also apparent that the ASIC is able to measure signals up to 4.2pC, which is equivalent to 12,000 photons at 8keV, meeting the requirement imposed by the LCLS XPP experiment.

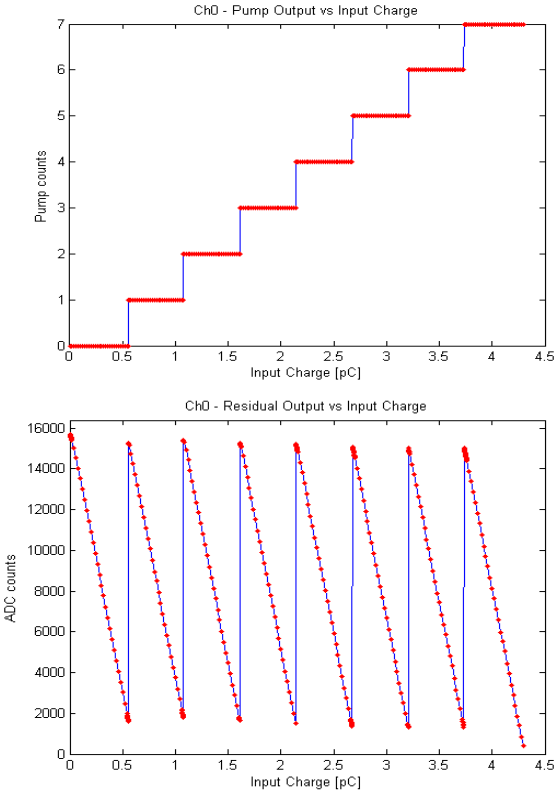

Fig. 11. Fitted transfer characteristic at the output of the chip in standard gain mode (negative polarity). Pump counts (top). Digitized analog residue (bottom)

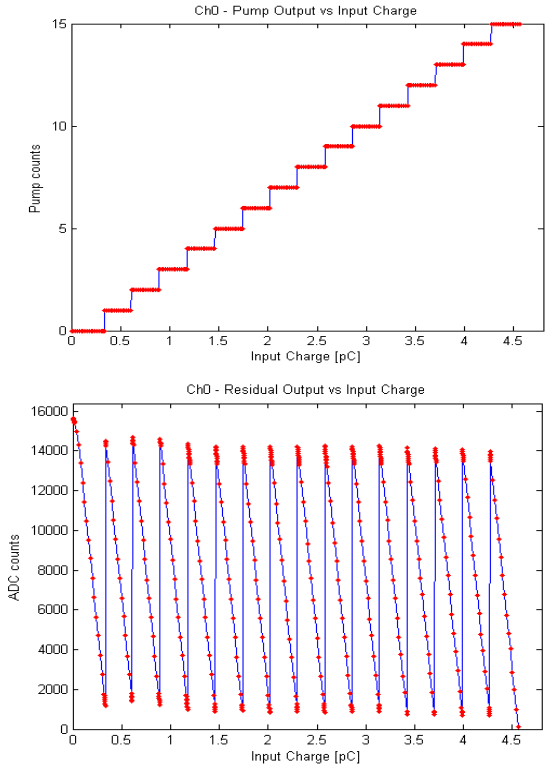

Fig. 12. Fitted transfer characteristic at the output of the chip in double gain mode (negative polarity). Pump counts (top). Digitized analog residue (bottom)

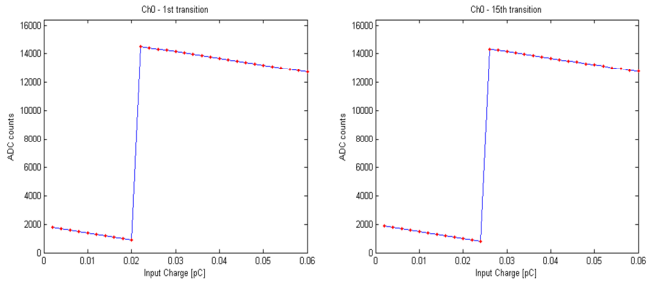

Fig. 13. Analog residue fitted transfer characteristic at the output of the chip in double gain mode (negative polarity). Close out comparison of the first (a) and last (b) pump transitions scanned with a higher resolution.

As an example of the calibration procedure the measured charge reconstructed by combining the pump counts and the analog residuals information is reported in Fig. 14 plotted against the injected charge.

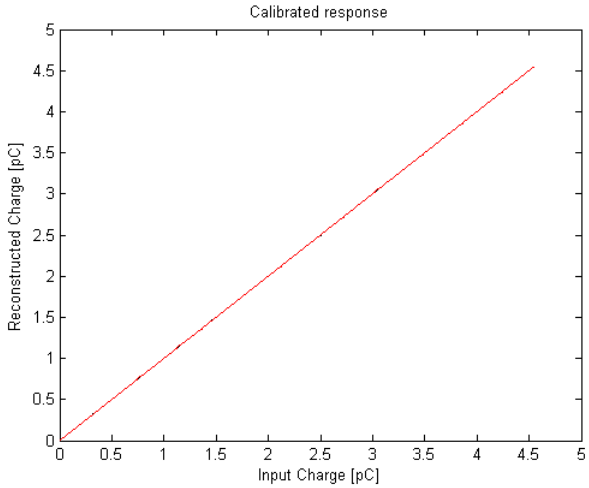

Fig. 14. Measured charge reconstructed combining the pump counts and the analog residuals information versus the injected charge.

In this measurement, the internal 10-bit pulser is used to scan the full transfer characteristic of the channels. Since the slope of the 16 pump ranges is constant, a simple script can easily align the sampled data in each range to those acquired in the first range. This is equivalent to the measurement of the pump steps. An off-set coefficient can be associated with each pump step. These off-set coefficients can then be stored and applied during normal operation to reconstruct the measured charge.

C. Noise measurements

The third set of measurements aims at evaluating the noise performance of the ASIC. The first test performed is related to the measurement of the system noise weighting function. Following the definition of such a function [10] a charge pulse is injected at the input of a channel and the analog output before and after the correlated double sampler is monitored. The sampled value at the measurement time (just before the end of the Slot Control signal period) is recorded as a function of the delay between the charge injection and the sampling time. The measured values are reported in Fig. 6 together with

the simulated weighting function. Curves are normalized to the measurement time, and also in amplitude. The close matching between simulated and measured curves shows the good performances of the filter.

The second test measures the noise level at the channel output. In the measurement, the filter was set to reach the flat top in 4µs as required by the 8µs row time typical of LCLS applications. The ASIC is operated in double gain mode and loaded with 15pF external capacitors at the channel inputs to mimic the expected load of the sensor. Fig. 15 shows the equivalent input r.m.s noise charge as a function of the channel. Good uniformity among the channels is achieved with an average noise level of 480e$^-$ r.m.s. In comparison, Fig. 16 shows the simulated noise behavior of the device as a function of the input capacitance, showing agreement between simulated and measured values.

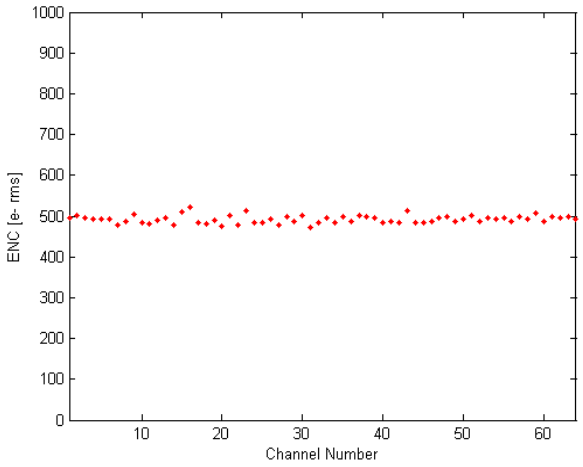

Fig. 15. Equivalent Noise input Charge (ENC r.m.s.) as a function of the channel.

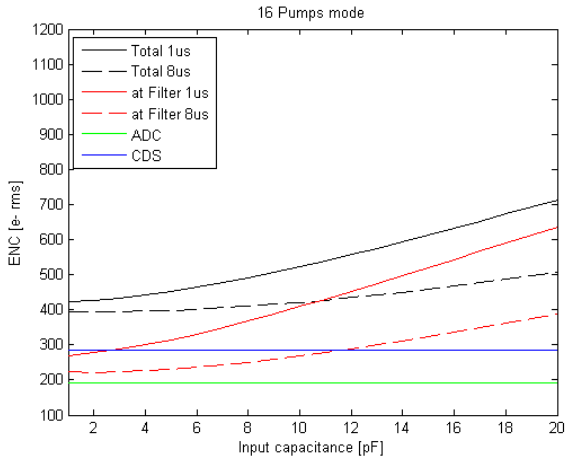

Fig. 16. Simulated Equivalent Noise input Charge as a function of the input capacitance for 1µs and 8µus time slot operation.

It is also interesting to consider the plot in Fig. 17, in which the equivalent input noise is also plotted as a function of the time slot, when the ASIC is set to read out a frame of 256x64 pixels at a 120Hz rate. The uniform response shows that in acquisition mode, the fast readout operation of the device does not affect the noise performance, assuring a uniform noise response across the full frame.

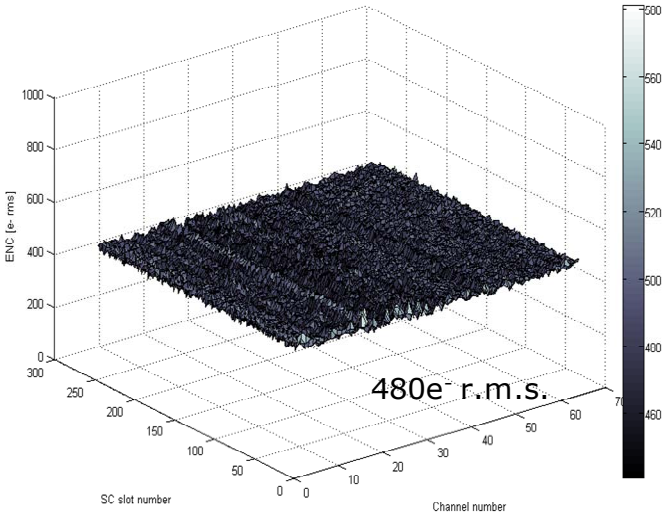

Fig. 17. Equivalent Noise input Charge (ENC r.m.s.) as a function of the channel and of the time slot (row) for the readout of a 256x64 pixel frame at 120Hz rate.

VI. Experimental Results

As an example of the performance achievable with eLine10k, we here present a copper target fluorescence image of a detail of a California native plant (Fig. 18) taken at SSRL with a 128x256 prototype of XAMPS. Cosmetic defects have been partially corrected from the image by interpolation. In the ASIC-sensor bonding scheme, five chips were used to read out the 256 channels: this was required to compensate for the space between the sensors, and results in 32 non-connected channels at the end of each sensor (black bands).

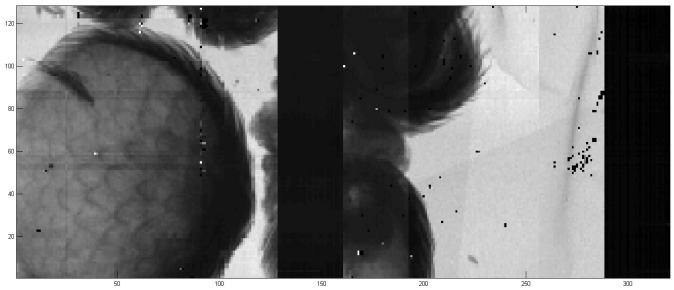

Fig. 18: California native plant: fluorescence image with XAMPS.

Additional experimental results with different detector prototypes are reported in [17].

VII. Conclusions

A new class of ASICs, eLine, for the readout of column-parallel readout sensors has been designed to satisfy the demanding experiments at LCLS. The class is composed of two front-end ASICs and a dedicated controller. eLine10k is the front-end tailored for high dynamic range applications. Optimized for XAMPS detectors and the requirements of the XPP experiment at LCLS, it is a charge-integrating time-variant architecture operating synchronously with the LCLS

beam structure. To cover the large input dynamic range of 10^4 photons at 8kV, a charge pump architecture has been successfully implemented. The ASIC presents (Tab I) a noise floor of 480e^- r.m.s at room temperature with a 15pF input load. It has a total dissipated power of about 3mW/channel and is suitable for applications requiring resolutions on the order of 600e^- r.m.s and signals up to 12,000 photons at 8keV. It is suitable for fast-frame rate detectors and can process up to 500k pixel/s on each channel.

TABLE I
ELINE10K PERFORMANCE

Technology	TSMC 0.25µm
Die Area	6 mm x 3.5 mm
Number of Channels	64
Optimum Input Load	15pF
Programmable Gain	5mV/fC or 2.5mV/fC
ENC	480e^- r.m.s. @ 15pF
Maximum Signal	26Me^- (12k photons @ 8keV)
Dynamic Range	95dB
Power Consumption	3mW/channel
Speed	500k pixel/s/channel

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