SLAC-TN-71-18
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M. Fishman

INSTRUCTION MANUAL FOR PDP-8/L to KENNEDY MODEL 1400 INCREMENTAL MAGNETIC RECORDER

INTRODUCTION

The following sections describe the basic requirements and detailed implementation for interfacing a PDP-8/L computer with an incremental magnetic recorder.[1] In addition, a brief checkout routine is presented to assist in trouble-shooting.

BASIC FUNCTIONING

Control of data recording is effected by three basic instructions as follows:

(1) SKIP ON UNIT READY (IRS)

(2) READ STATUS REGISTER (ISR)

(3) MOVE COMMAND (IMC)

IRS COMMAND

The skip-on-unit-ready command has the octal code 6701. Details of this command are presented in the DEC SMALL COMPUTER HANDBOOK. Basically, an IOT pulse is presented to the interface near the beginning of the machine cycle. Upon an IRS command, the next sequential instruction will be skipped if the unit is ready. However, if the incremental recorder is not ready, the instruction following the IRS (6701) will not be skipped. That is, the skip will not be allowed if any of the following occur:

(a) Tape is not tensioned.

(b) Transport is not ready.

(c) Write buffer is not ready (i.e., for 2.5 ms. after write step).

(d) Tape gap is in progress.

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1. Kennedy Model 1400/5, Ser. 259 (Write Only). This unit has positive input logic, and writes 7 track tapes at 556 BPI. It includes echo check feature, indicating failure of the write electronics.

(e) Tape is rewinding (REWIND command issued but REWIND flip-flop not reset)

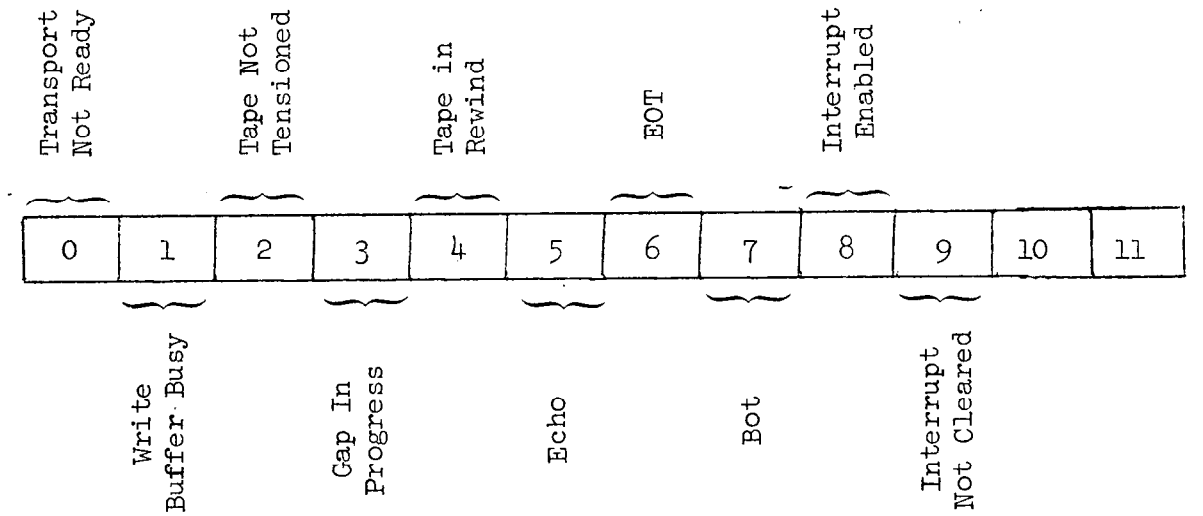
(f) Interface electronics gave an ECHO check error (ECHO)

(g) Tape is at end of tape (EOT)

(h) Tape is at beginning of tape (BOT)

ISR COMMAND

The status register is read into the accumulator upon receipt of an ISR command (octal code 6702). The contents of the status register is read into bits 0-9. The accumulator should be cleared before this instruction is executed. See Figure 1 and Table 1 for the state conditions. The ISR command is effected near the middle of a machine cycle.



TRUE = + ve = bit set

Bit	Function	
0	Transport ready	(TRUE - transport not ready)
1	Write Buffer Status	(TRUE = in write mode)
2	Tape tension	(TRUE = tape not tensioned)
3	Gap in progress	(TRUE = gap in progress)
4	Rewinding	(TRUE = tape is rewinding)
5	Elec. echo check	(TRUE = echo test failed)
6	End of Tape	(TRUE = tape at end)
7	Beginning of Tape	(TRUE - tape at beginning)
8	Interrupt enabled	(TRUE = tape interrupt enabled)
9	Interrupt not cleared	(TRUE = interrupt not cleared)

IMC COMMAND

The contents of the accumulator are read into the interface upon MOVE COMMAND (OCTAL CODE 6704) near the end of a machine cycle. The upper four bits AC 0-3 are decoded in the interface to produce the following command

FUNCTION	AC BITS	OCTAL CODE
	0 1 2 3	0000
NO OP	0 0 0 0	0000
REWIND	0 0 0 1	0400
WRITE END OF RECORD & GAP	0 0 1 0	1000
WRITE END OF FILE & GAP	0 0 1 1	1400
WRITE/STEP	0 1 0 0	2000
INITIALIZE SYSTEM	0 1 0 1	2400
RESET ECHO FLAG	0 1 1 0	3000
ENABLE INTERRUPT	0 1 1 1	3400
NOOP	1 0 0 0	4000

FUNCTION	AC BITS	OCTAL CODE
SET INTERRUPT	1 0 0 1	4400
RESET INTERRUPT	1 0 1 1	5400
RESET END OF TAPE FLAG	1 1 0 0	6000
NO OP	1 1 0 1	6400
NO OP	1 1 1 0	7000
SET STANDBY (RESET INITIALIZE)	1 1 1 1	7400

INTERFACE DESIGN

The interface electronics consists of five plug-in cards plus two cable connectors and a control/display panel. The function of each card is discussed in detail.

BUFFER-INVERTER M101

Data from the accumulator is applied to a standard DEC type M101 card which is mounted in position A08 of a DEC interface adaptor. Buffered Accumulator outputs are connected from a card at position A11 to the M101 and carry information from lines BAC00-BAC11. A clock pulse applied at A08C1 allows information to be transmitted through M101 which contains a set of NAND gates.

DEVICE SELECTOR M103

Address codes applied to lines A12, D2, E2, F2, H2, J2, and K2 from the buffered memory bus are decoded by a DEC type M103 device selector in position A12. The device selector generates the $\overline{\text{IOT1}}$, $\overline{\text{IOT2}}$, IOT4, and $\overline{\text{IOT4}}$ timing pulses corresponding the $\overline{\text{IOT6701}}$, $\overline{\text{IOT6702}}$, IOT6704 and $\overline{\text{IOT6704}}$ respectively. Details of the M103 device selector can be found on page 256 of the SMALL COMPUTER HANDBOOK.

Application of a ground level at A12J1 results in a zero-level signal at A12N1 which supplies the clock signal to M101. This inhibits the flow of information through M101.

COLLAGE BOARD #1

Collage Board #1 is mounted in position A06-B06 of the interface adaptor. Instruction words bits AC 0-3 are inverted in M101 and transmitted to the inputs of G1. Upon receipt of $\overline{\text{IOT4}}$ at A06F1, the signals applied at G1-2, G1-5, G1-8 and G1-11 are inverted gated through G1 to the outputs. The outputs of G1 in turn are applied to G7 and G8 which are Signetics Type 8251A Binary-Coded-Decimal-To-Decimal decoders. Together G7 and G8 act as Hex-to-Decimal Converters. When the output Q_o (the most significant bit) of G1 is zero, G7 rather than G8 is selected. Thus G7 decodes from Hex-0 to Hex 7. Similarly, if BAC-00 is at "1" level, a zero is applied to G8-2 thru G14 when an $\overline{\text{IOT4}}$-pulse is applied at A06F1. Consequently, G8 is selected for Hex 8 through Hex F. For example, a binary code 0011 on the BAC lines is decoded by G7 as octal 1400 and produces a command to write an end-of-file and gap. Similarly, a code 1100 on the BAC lines is decoded by G8 to produce a command to reset the End-of-Tape Flip-Flop.

BAC-6 thru BAC11 transmit the binary coded information to be applied ultimately to the magnetic recorder. After passing through the M101 buffer, the six lower-order bits are applied to latch units FF-2 and FF-3. Information on the input lines of the latch unit are stored at the trailing edge of the clock pulse obtained from IOT4.

Flip-flop FF13 is a control flip-flop comprised of two cross-coupled NAND gates from an MC-857P integrated circuit. When FF-13 is reset by a

negative pulse on FF13-6, this interface system is placed on standby. When FF13 is set by a negative pulse on FF13-1, the system is initialized. Initialization can be accomplished either by decoded command octal 2400 or by depressing switch S1. Gate G13 acts as an inverted logic "OR" gate when a negative signal is applied at either G13-12 or G13-13. The output G13-10 serves as an "initialize" pulse to reset various control flip-flops on collage card #2.

The remainder of the circuitry is used primarily to convert Kennedy Recorder Voltage levels, to drive display lamps, and to provide interrupt signals.

A signal to indicate that the transport is ready appears at high level at B06S2. After the voltage is lowered by a resistive divider network, it is applied at G14-1 and G14-2 which is an MC-857P NAND Gate. After two inversions, the Transport Ready signal appears at G18-10. A change from Xport Ready to Xport Not Ready (Xport Ready $\rightarrow \overline{\text{Xport Ready}}$) causes a negative pulse to appear at A06V2. If the voltage level at G18-10 is zero, indicating transport not ready, current flows through the light emitting diode in the display panel. Similarly, G-14 is used to indicate a broken tape and to produce a pulse when conditions change from Tape OK to Tape Broken. In a similar fashion, a Beginning of Tape (BOT) signal is transformed into a $\overline{\text{BOT}}$ output at G14-10 to drive status lights and the status register.

Collage Card #1 derives its primary +5V voltage supply (VCC) from the DEC Peripheral Expander Unit. In addition it produces a nominal +3 volt supply by dropping the VCC through a resistor and zener-diode network. In addition, it utilizes a nominal +6.2 V supply located in Collage Card #2.

COLLAGE CARD #2

Collage Card #2 serves several functions which will be described in the following paragraphs. Basically, the card consists of a number of one-shot circuits, a number of status and control flip-flops, and associated gates. It is located in position A04-B04.

A decoded write/step command input is received from Collage Board #1 via A04L1 at SS1-1, 2. If the system is initialized, a positive voltage level at SS1-3 enables the one-shot. A negative trigger pulse at SS1-1, 2 produces a positive 50- μsec. voltage pulse at SS1-8. At the trailing edge of the 50 μsec pulse, SS-3 is triggered and produces a nominal 2.5 msec pulse at SS3-8. A differentiating network applies a negative spike at G7-12 corresponding to the trailing edge of the 2.5 msec pulse. The W/S command from SS3-8 is applied to the KENNEDY CABLE via B04V2. To assure that the data on the lines to the KENNEDY RECORDER has had time to settle, it is necessary to introduce the 50 μsec delay before the actual W/S command. However, a "busy" state must be indicated promptly by the W/S status flip-flop. Therefore, an output from SS1-6 is used to set FF7 as soon as SS-1 responds to the W/S command input. FF-7 is reset by either the trailing edge of the W/S output via the input at G7-12 or by means of an "initialize" pulse applied at G7-13. The $\overline{\text{W/S STATUS}}$ is applied to DEC card, M624, in B08 via B04D1 as well as to an indicator lamp and a summary status gate G16. Assuming all other inputs to G16 are positive, when FF7 indicates a Write-Step, FF7-2, 4 is at a "zero" logic level and a positive level is therefore produced at G16-8. At the completion o the Write/Step, a negative spike is developed at G17-4. A positive pulse then appears at G17-8. If FF15 is enabled, the G18-10 inverts the positive pulse fro. G17-8 and the Interrupt

Flag is Set. FF18 can be reset by a negative pulse at FF18-6 as a result of a initialize command or a decoded "Reset Interrupt" command.

End-of-Record (EOR) and End-of-File (EOF) commands are generated by SS4 and SS6 respectively. The outputs of SS4-6 and SS6-6 are "OR"ed at G12-1, 2 and inverted. In a similar fashion, this information is "OR"-ed with the level-shifted $\overline{\text{GIP}}$ information at G12-9. Thus a summary $\overline{\text{GIP}}$ output is available at G12-11.

Flip-Flop FF10 is used to control transistor Q3 which provides a means for rewinding the recorder.

FF-9 is used to store the ECHO CHECK status from the recorder. It is not used for control.

FF-14 serves as a latch to indicate the receipt of an End-of-Tape (EOT) indication. It can be reset either by an initialize pulse or by a decoded command.

FF-15 serves as a control flip-flop for enabling or disabling the interrupt feature. It can be set and reset by decoded commands. In addition, FF15 can be reset by an initialize pulse.

Gate G16 serves as a summary status output. If the recorder is ready to accept a W/S command, then the following must be true:

(a) XPORT READY
(b) $\overline{\text{W/S STATUS}}$
(c) $\overline{\text{TAPE BKN}}$
(d) $\overline{\text{GIP}}$
(e) $\overline{\text{RWD}}$
(f) $\overline{\text{BOT}}$
(g) $\overline{\text{EOT}}$

If any of conditions (a) thru (g) are false, then G16-8 is "one" which indicates that ALLOK is false. Upon a transition from $\overline{\text{ALLOK}}$ $\rightarrow$ ALLOK, a

negative pulse is produced at G17-4 as in the case already described for the W/S status going from W/S $\rightarrow \overline{W/S}$. A $\overline{\text{SET INT}}$ command is then transmitted to FF18-1 provided that the INTERRUPT ENABLED FLIP-FLOP FF15 is set. A positive voltage level at FF15-3, 5 enables gate G18 and permits a $\overline{\text{SET INT}}$ pulse to be transmitted to FF18-1.

The transition $\overline{\text{ALLOK}} \rightarrow$ ALLOK accounts for the interrupt pulses generated at the termination of a WRITE/STEP event or at the termination of a gap-in-process event. In addition, interrupt pulses are generated when FF15 is enabled and any of the following transitions occur:

(1) XPORT READY $\rightarrow$ $\overline{\text{XPORT READY}}$
(2) $\overline{\text{TAPE BKN}}$ $\rightarrow$ TAPE BKN
(3) RWD $\rightarrow$ $\overline{\text{RWD}}$
(4) $\overline{\text{EOT}}$ $\rightarrow$ EOT

The first two cases of the above listed transitions which result in an interrupt have already been covered in the description of Collage Board #1. In the case of RWD $\rightarrow$ $\overline{\text{RWD}}$, a differentiating network between FF10-3,5 and G17-5 produces a negative spike on a transition to the REWIND OFF status. Similarly a transition from EOT $\rightarrow$ $\overline{\text{EOT}}$ is sensed by interposing a differentiating network between FF14-2,4 and G17-6. An interrupt pulse may also be generated by a decoded command (octal code 4400) provided FF15 is enabled. This is achieved by applying the decoded $\overline{\text{SET INT}}$ command via A04E2 to pins G17-2, 11, 12.

DISPLAY/CONTROL PANEL

A special panel is provided for display and control. The display lamps are Light Emitting Diodes. These are connected in series with a set of 270 Ω dropping resistors in Collage Board #2 to +VCC. The cathodes of the LED's are connected to ground through either gates or status flip-flops.

Two control switches are located on the DISPLAY/CONTROL Panel. Switch S1 is a momentary pushbutton switch which can be used to initialize the system manually. The second switch, S2, is used to disable the interrupt by grounding the reset input of FF15 by means of an input at G15-13.

The connecting cable for the DISPLAY/CONTROL Panel is plugged into position B07.

M624 BUS DRIVER

The M624 BUS DRIVER is located in position B08 of the peripheral adaptor. The function of the M624 unit is to provide a means of gating status information and interrupt signals into the computer.

CHECKOUT PROCEDURE

The decoding function of COLLAGE BOARD #1 can be checked conveniently with the aid of the computer by removing COLLAGE BOARD #2 and using the following program:

100/CLA	7200	
101/TAD	1130	C(130) = 0400
102/IMC	6704	
103/JMP	5101	

By obtaining a scope synch pulse from A06A1, one can examine the decoding functions by successively placing the scope probe on A06D1, A06J1, etc. The above program successively adds octal 400 to the accumulator and steps through each command. The same program can be single-stepped with COLLAGE BOARD #2 in the system to check overall system response to sequential command.

To check the Write/Step behavior, one can use the following program:

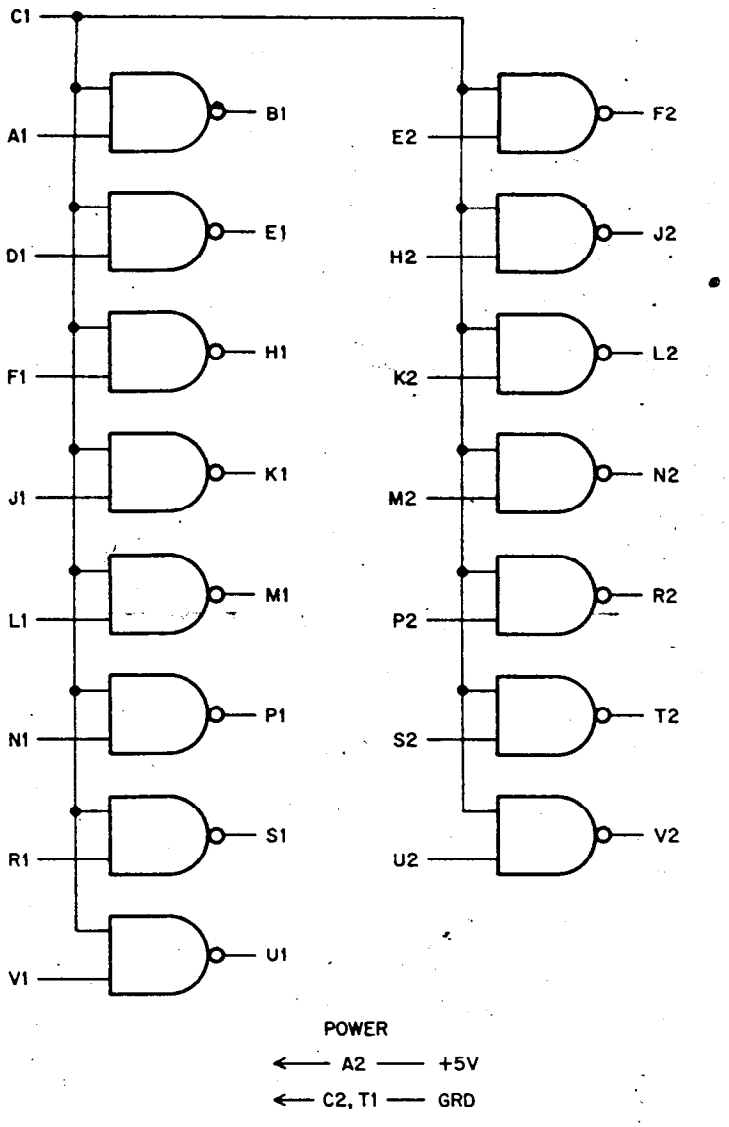
```
100/CLA         7200
101/TAD         1130            C(130) = 2400, INITIALIZE
102/IMC         6704
103/CLA         7200
104/TAD         1131            C(131) = 3400, ENABLE INT
105/IMC         6704
106/CLA         7200
107/TAD         1132            C(132) = 2000, W/S
110/IMC         6704
111/CLA         7200
112/NOP         7000
113/ISR         6702            READ STATUS REGISTER
114/IRS         6701            SKIP ON READY
115/HLT         7402
116/HLT         7402
117/JMP         5100
```

If instruction 115 is changed to a JMP to 114 and 116 is changed to a NOP then the program will loop continuously. That is, we change the above program as follows:

```
114/IRS         6701
115/JMP         5114
116/NOP         7000
115/JMP         5100
```

BUS DATA INTERFACE
M101

M SERIES



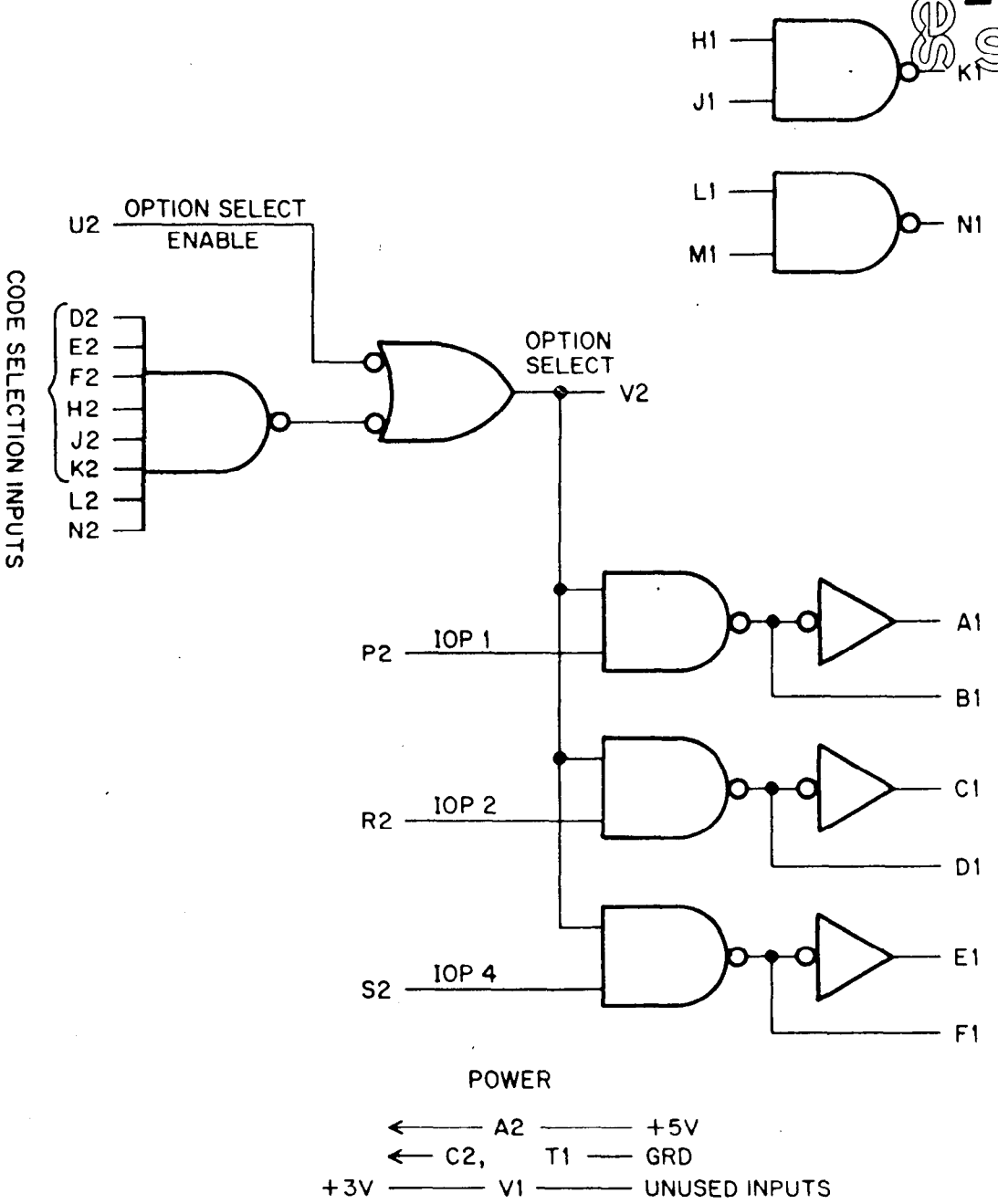
The M101 contains fifteen, two-input NAND gates arranged for convenient data strobing off of the PDP8/I or PDP8/L positive bus. One input of each gate is tied to a common line so that all data signals on the second input of each gate can be enabled simultaneously. The M101 can also be used as inverters or a data multiplexer. All data inputs are protected from a negative of more than −0.8 volts.

Inputs: Each data signal input presents one TTL unit load. The common line input presents fifteen unit loads.

Outputs: Each output can drive ten unit loads.

Power: +5V at 82 ma. (max.)

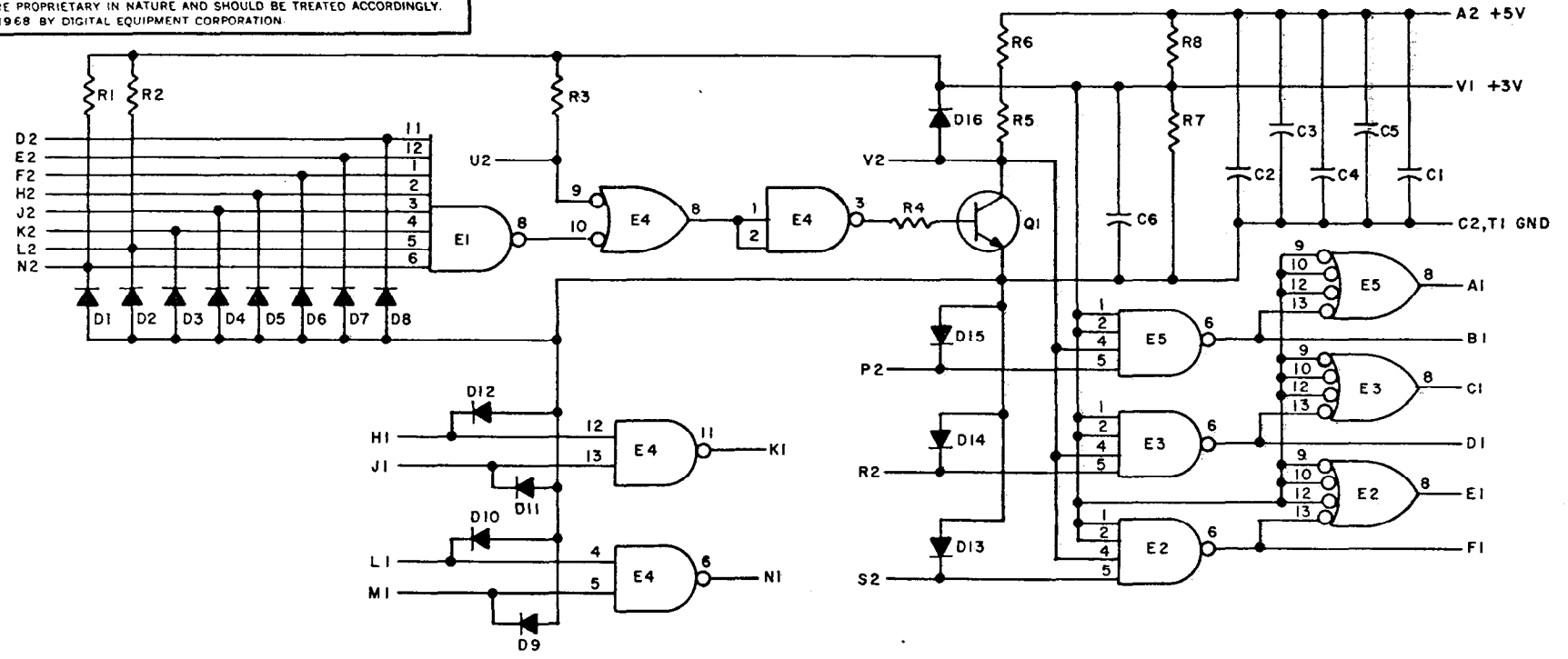
M103 device selector



M103 device selector

The M103 is used to decode the six device bits transmitted in complement pairs on the positive bus of the PDP8/I and PDP8/L. Selection codes are obtained by selective wiring of the bus signals to the code select inputs D2, E2, F2, H2, J2, and K2. This module also includes pulse buffering gates for the IOP signals found on the positive bus of the above computers. Two two-input NAND gates are also provided for any additional buffering that is required.

SIZE	CODE	NUMBER	REV.
B	CS	M103-0-1	A



Q1	TRANSISTOR DEC3009B-S	1503100
E4	INTEGRATED CKT. DEC7400N	1905575
E2, E3, E5	INTEGRATED CKT. DEC74H40N	1905586
E1	INTEGRATED CKT. DEC7430N	1905578
R8	RES. 330 1/4W 5% CC	1300295
R4-R7	RES. 750 1/4W 5% CC	1301401
R1, R2, R3	RES. 6.2K 1/4W 5% CC	1303179
D1-D16	DIODE D664	1100114
C1-C6	CAP. .01MFD 100V 20% DISC	1001610
	PARTS LIST	A-PL-M103-0-0
REFERENCE DESIGNATION	DESCRIPTION	PART NO.

PARTS LIST

REVISIONS			
REV	A		
CHG NO	00001		
CHK			

DRN	M Keller	DATE 10-4-68
CHK'D		DATE
ENG		DATE
PROD		DAT

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC3009B	2N3009		
D664	IN3606		

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MAYNARD MASSACHUSETTS

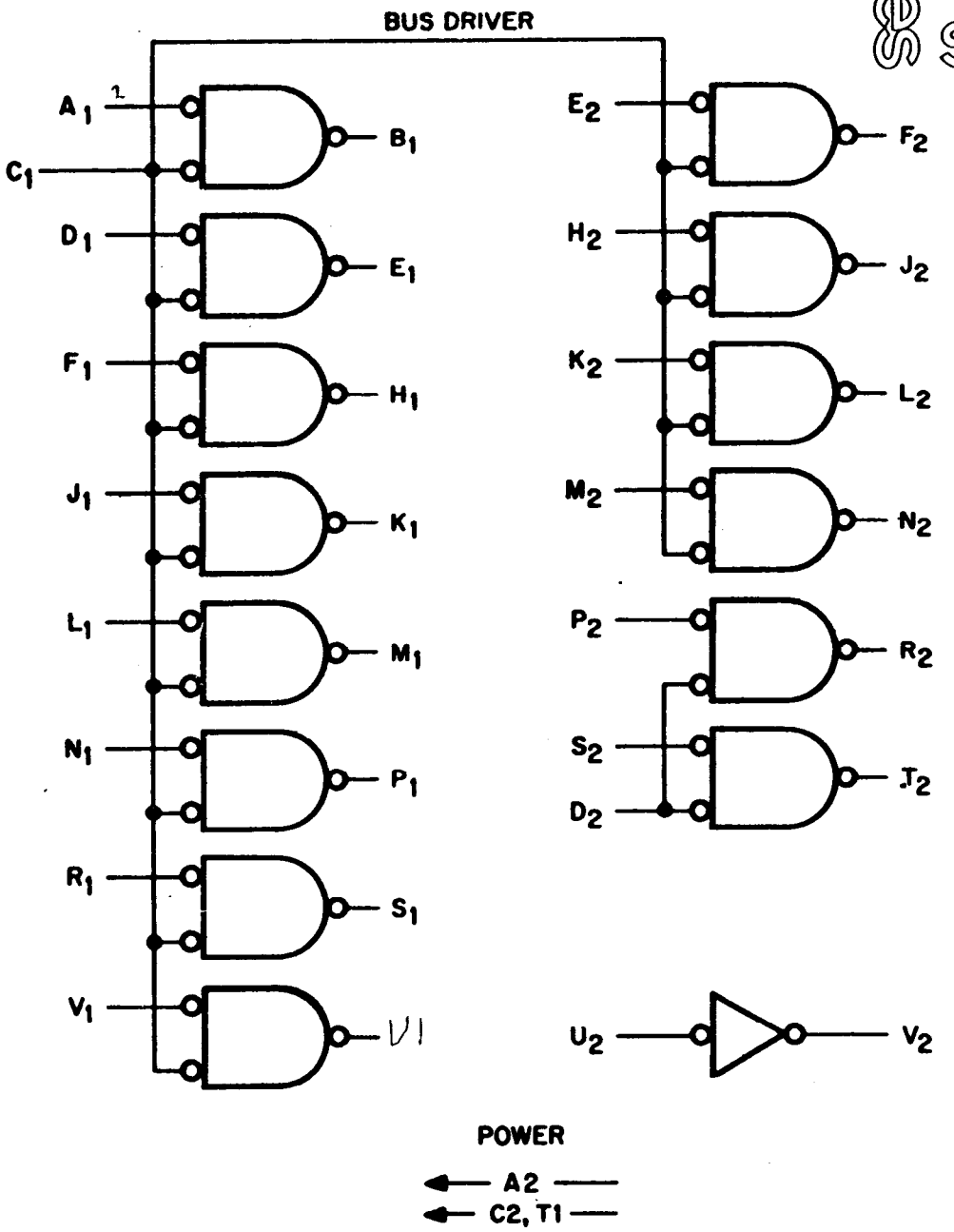
TITLE: DEVICE SELECTOR M103

SIZE	CODE	NUMBER	REV
B	CS	M103-0-1	A

PRINTED CIRCUIT REV B

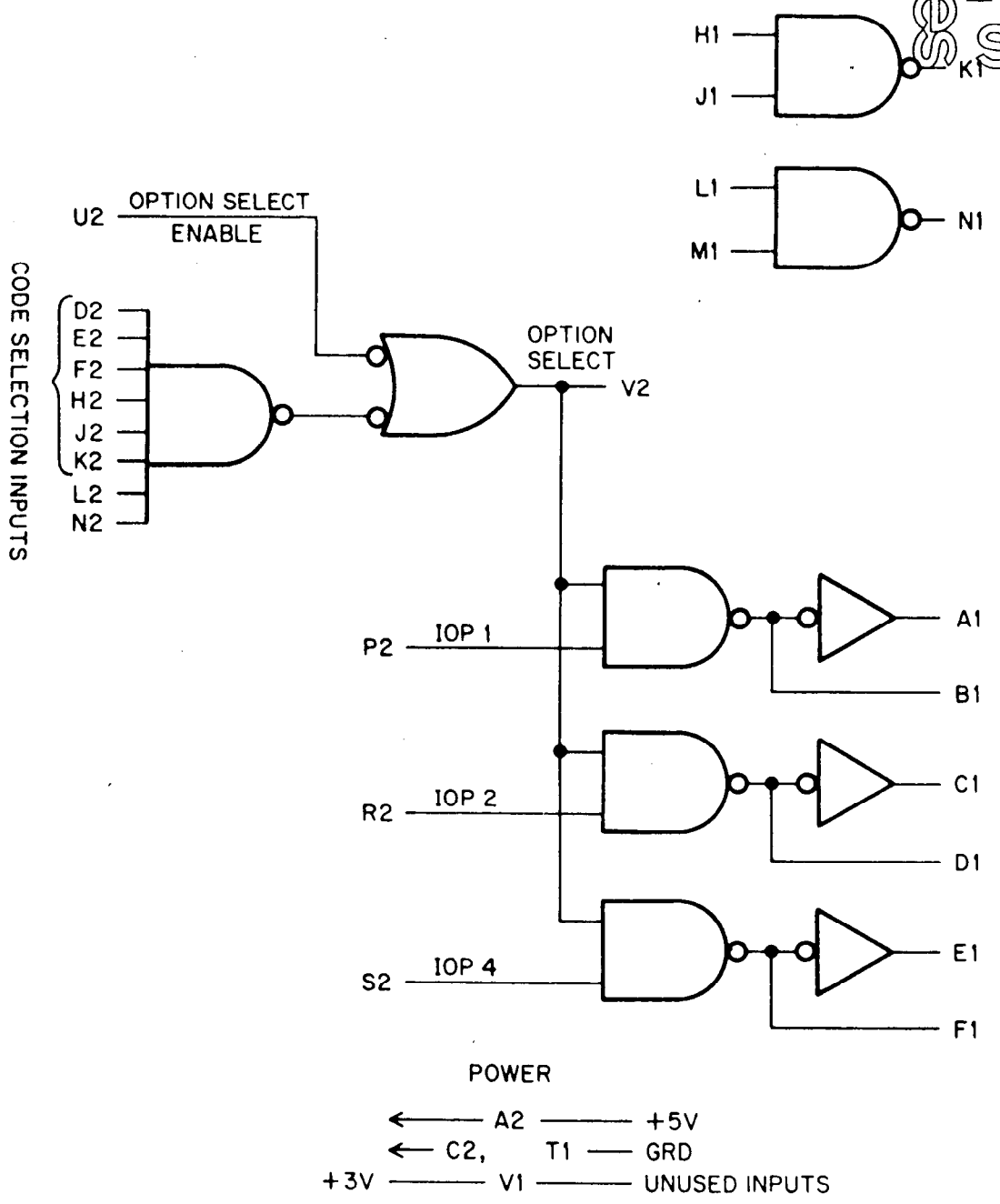
DEC FORM NO 048 REV

M624 bus driver



The M624 contains fifteen bus drivers intended for convenient driving of the positive input bus of either the PDP-8I or PDP-8L. Twelve of the drivers have a common gate line and would be used for DATA. There are three additional drivers, two of which share a common gate line and the third without a gate line. These three additional drivers were intended to accommodate the functions of "Program Interrupt", "IO Skip" and "Clear AC".

M103 device selector



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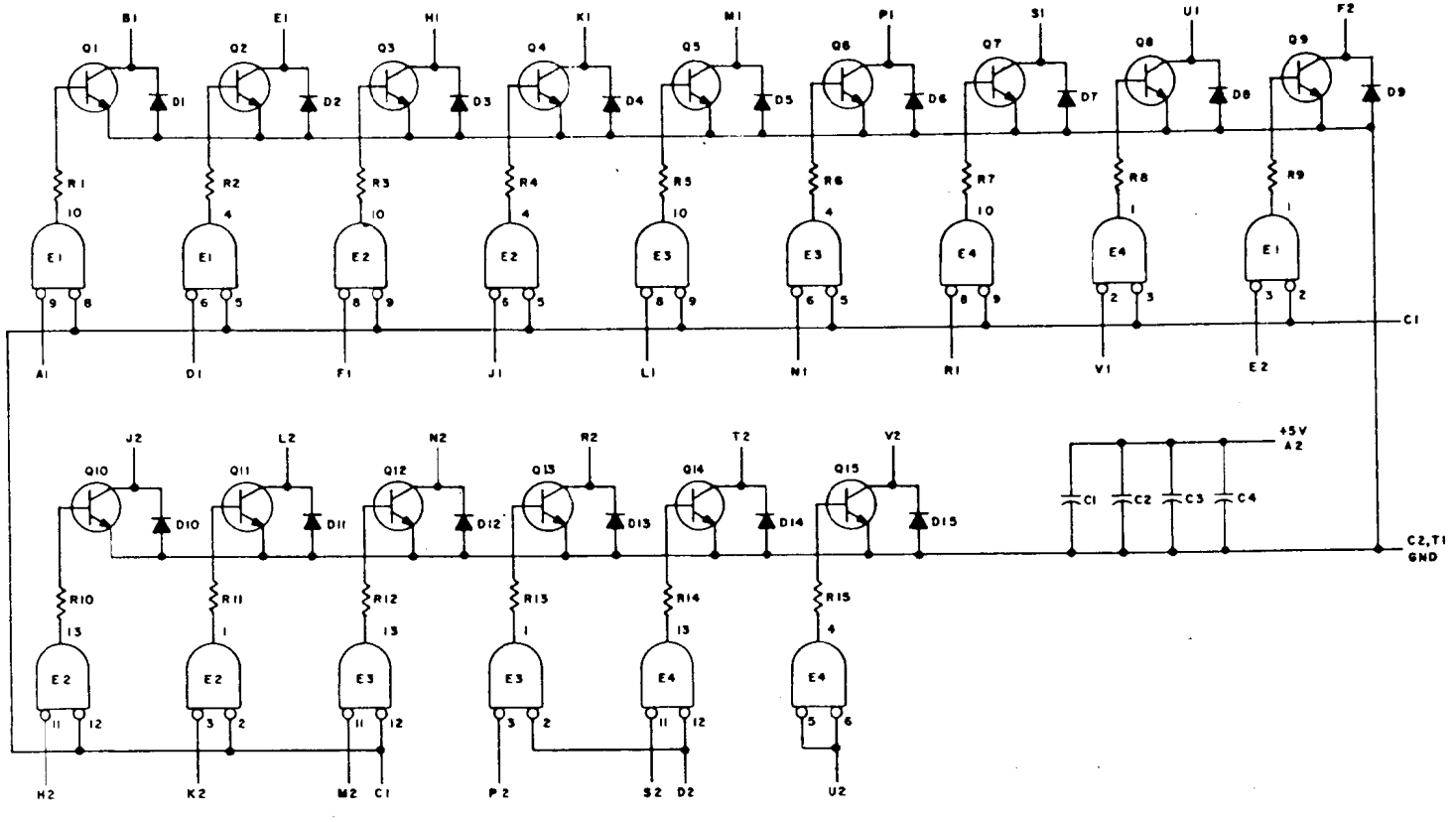


NOTES
PIN7 ON EACH IC = GND
PIN14 ON EACH IC = +5V

REFERENCE DESIGNATION	DESCRIPTION	PART NO
	PARTS LIST	
E1-E4	INTEGRATED CKT DEC7402N	1309004
Q1-Q15	TRANSISTOR DEC 3009B-S	1503100
R1-R15	RES 390 1/4W 5% CC	1300309
D1-D15	DIODE D664	1100114
C1-C4	CAP .01 MFD 100V 20% DISC	1001610
	PARTS LIST	A-PL-M624-0-0

PARTS LIST

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D664	1N5808		
DEC 3009B	2N3009		

REVISIONS

LTR	CHG NO	REV

DRN	DATE 8-7-69	
CHKD	DATE 2-20-69	
ENGR	DATE 4/8/69	
MGR	DATE	

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

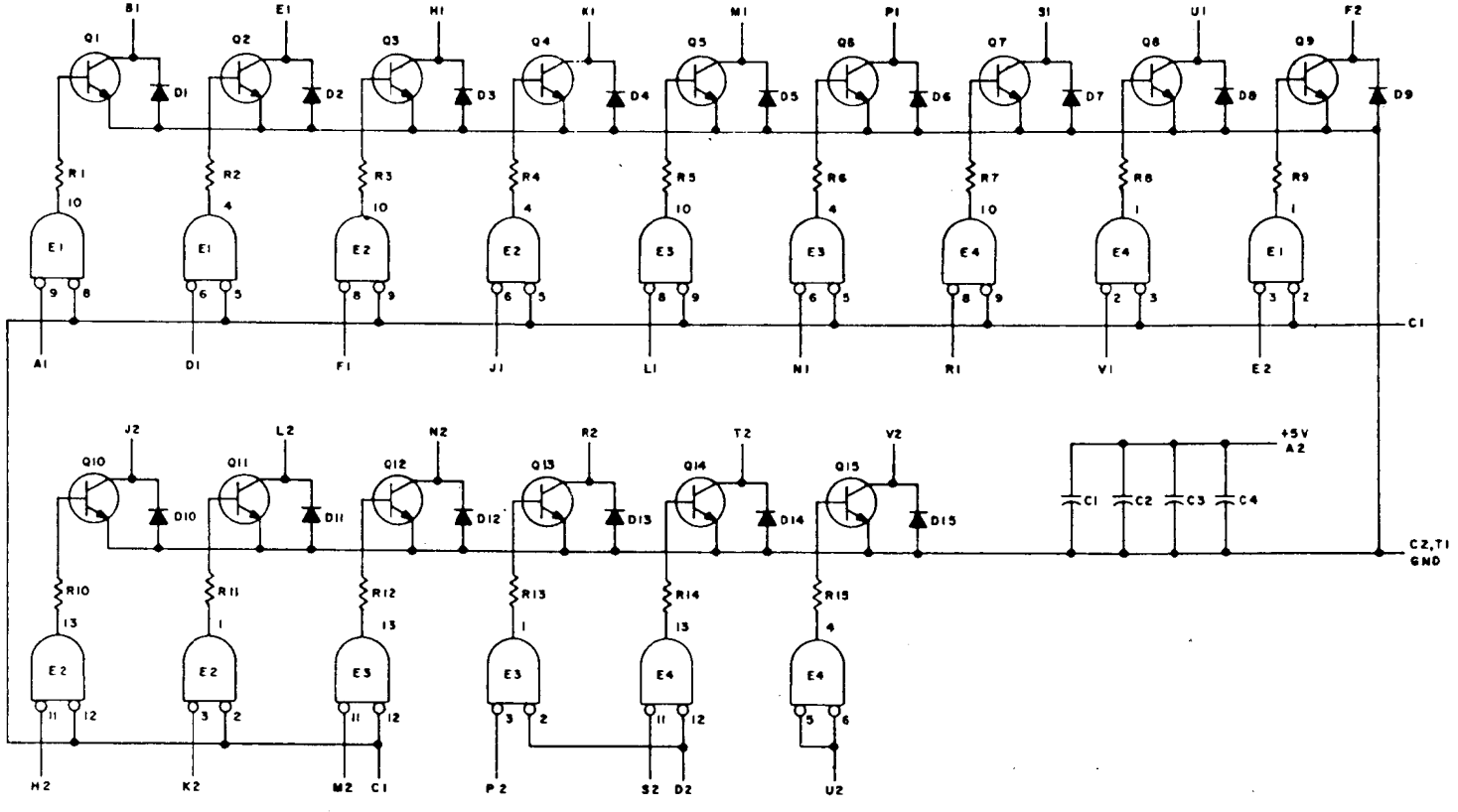
TITLE: BUS DRIVER M624

SIZE	CODE	NUMBER	REV
C	CS	M624-0-1	

PRINTED CIRCUIT REV: A

DIST. 324,434 455 PINK

SIZE C | CODE CS | NUMBER M624-0-1 | REV



NOTES
PIN7 ON EACH IC = GND
PIN14 ON EACH IC = +5V

REFERENCE DESIGNATION	DESCRIPTION	PART NO
	PARTS LIST	A-PL-M624-0-0
C1-C4	CAP .01 MFD 100V 20% DISC	1001610
D1-D15	DIODE D664	1100114
R1-R15	RES 390 1/4W 5% CC	1300309
Q1-Q15	TRANSISTOR DEC 30098-6	1503100
E1-E4	INTEGRATED CKT DEC7402N	1909004

PARTS LIST

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D664	1N3606		
DEC30098	2N3009		

ORIG [illegible] DATE 8-7-69
CHK [illegible] DATE 2-20-69
ENG [illegible] DATE 4/8/69
APPD DATE

REVISIONS
LTR | CHG NO | REV

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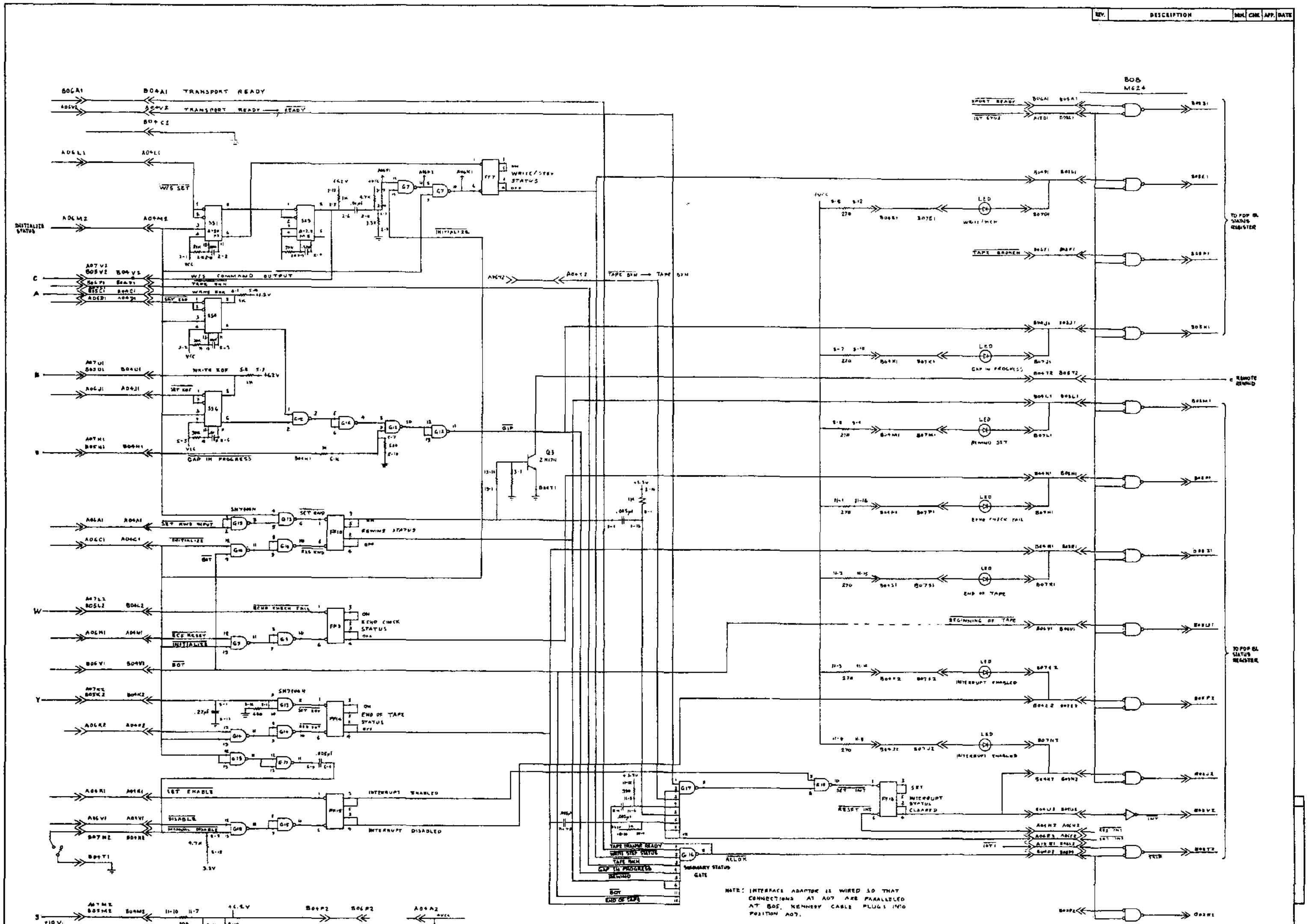
TITLE BUS DRIVER M624

SIZE C | CODE CS | NUMBER M624-0-1 | REV

PRINTED CIRCUIT REV A

DIST. 324, 434, 435 P.M.K.

SIZE C | CODE CS | NUMBER M624-0-1 | REV



NOTE: INTERFACE ADAPTOR IS WIRED SO THAT CONNECTIONS AT A07 ARE PARALLELED AT B05. KENNEDY CABLE PLUGS INTO POSITION A07.

KENNEDY INCREMENTAL RECORDER INTERFACE COLLAGE BOARD #2
M624 AND CONTROL DISPLAY PANEL

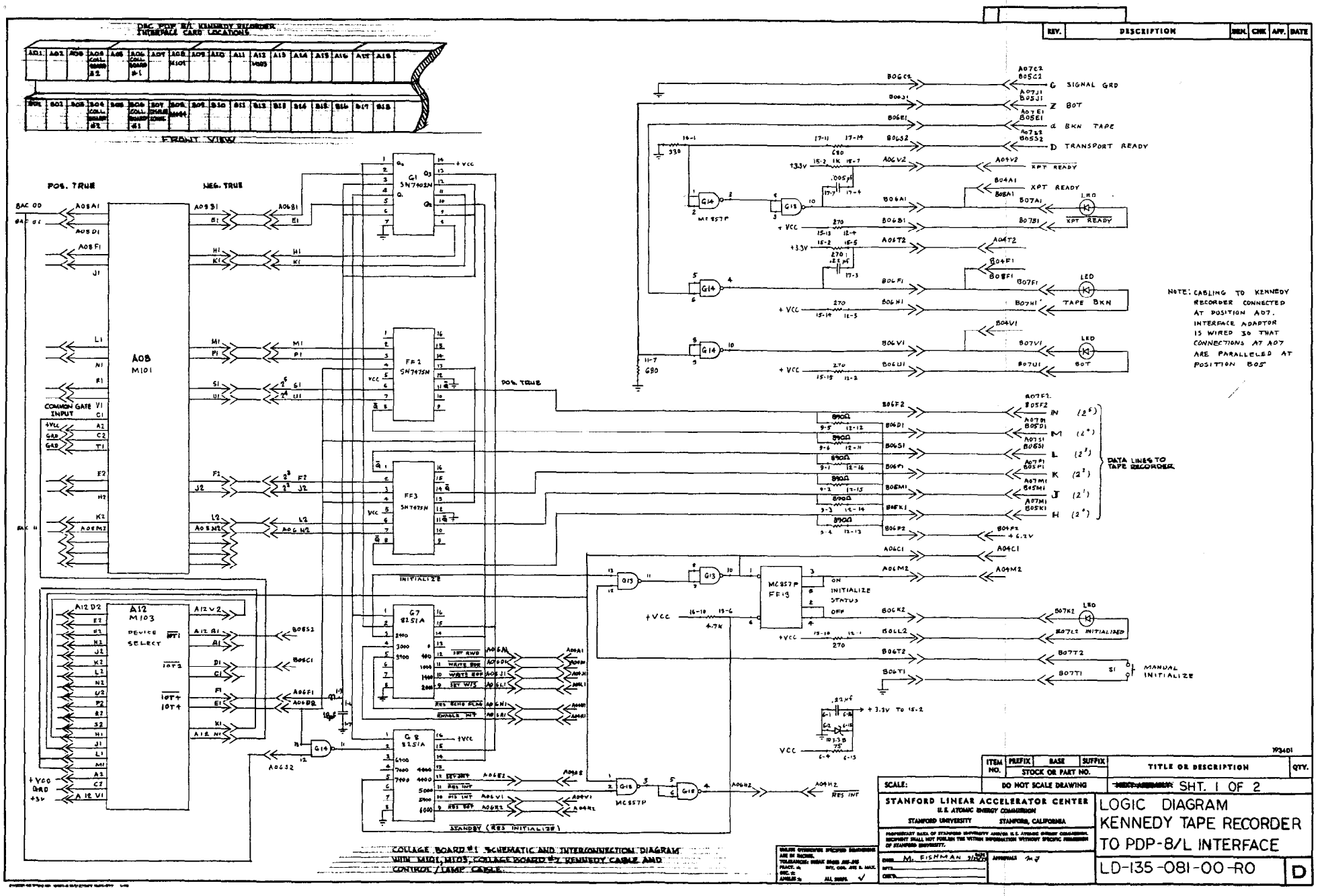
ITEM NO.	PREFIX	BASE	SUFFIX	TITLE OR DESCRIPTION	QTY.
	STOCK OR PART NO.				

SCALE: | DO NOT SCALE DRAWING | [redacted]: SHT. 2 TO 2

STANFORD LINEAR ACCELERATOR CENTER
U.S. ATOMIC ENERGY COMMISSION
STANFORD UNIVERSITY STANFORD, CALIFORNIA

LOGIC DIAGRAM
KENNEDY TAPE RECORDER TO PDP-8/L INTERFACE

LD-135-081-00-RO | E



REV.	DESCRIPTION	DRN.	CHK	APP.	DATE

ITEM NO.	PREFIX	BASE	SUFFIX	TITLE OR DESCRIPTION	QTY.
	STOCK OR PART NO.				

SCALE: DO NOT SCALE DRAWING SHT. 1 OF 2

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U.S. ATOMIC ENERGY COMMISSION
STANFORD UNIVERSITY STANFORD, CALIFORNIA

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DRAWN M. FISHMAN 3/1/71 APPROVALS
DATE
CHK'D

LOGIC DIAGRAM KENNEDY TAPE RECORDER TO PDP-8/L INTERFACE

LD-135-081-00-R0 D