It is about time

Design and test of a per-pixel high-resolution TDC

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Contents

Introduction

The beginning of modern science commonly is dated back in the 17th century with Galileo and his scientific method. Unlike the philosophers before him, Galileo trusted only things that could be proven by experiments. Later in the 20th century Karl Popper, a German philosopher, introduced the concept of falsifiability as demarcation between what is scientific and what is not. While no number of measurements can prove the absolute truth of a statement, a single measure can be enough to prove a theory false [1]. The ideal line which connects Galileo to Popper is the idea that the experiment is the crucial part of every scientific theory.

In the 20th century, physicists continued their search toward the infinitely small and, on the opposite side, to the infinitely big. Common to both directions of investigation is the need for sophisticated tools to be able to perform experiments required by the scientific method to prove theories true or false.

The last century radiation detectors have developed from the Geiger tube [2] in 1908 to the large experiments at accelerators as the Large Hadron Collider (LHC). Gas, liquids and solids all became available as detector medium in particle physics, every one of them with their own advantages and disadvantages. A common feature of all the detectors is that they have to be read out to make use of the data collected. In the first particle detectors (e.g., emulsions or bubble chambers) pictures were taken and they had to be analyzed manually to reconstruct the events which were recorded. On the other hand, detectors like the Geiger-Muller tube could automatically provide only a count of how many particles were detected in a specific time interval over a certain area.

Improvements in the readout of the detectors came with the availability of integrated circuits technology which allow an increase in the number of channels while, at the same time, decreasing the single channel area. This, in turn, permits us to reconstruct with increasing precision not only the particle's track but also its energy and momentum.

Modern detectors have to provide an ever increasing precision, that goes from the order of nanosecond in the large high energy physics experiments at

CERN to picoseconds for other precision experiments. Moreover, they have to be capable of handling increasing particle rates both on the detection side and on the data readout speed.

This thesis is focused on time measurements in gaseous pixel detectors and it is structured as follows. In chapter 1 a brief history of pixel detectors is presented, focusing mainly on the features of their readout systems. In the second part of the chapter, the focus is on the modern detectors at the Large Hadron Collider and their planned upgrades. Chapter 2 presents the operation principle of gaseous detectors with the basic mechanism behind ion-electron couples production and transport mechanism. GridPix detectors are also introduced describing some basic properties. Chapters 3 and 4 contain the main results of this thesis, illustrating the design and testing of two prototype chips featuring high-resolution Time to Digital Converter (TDC). The results on the TDC are complemented with results on other circuitry which has been designed and tested in view of a full size chip. Finally, chapter 5 presents the analysis of data from a beam test using a telescope that contains three GridPix detectors. Their limitations are studied and are used as a justification for the design of Timepix3, a full size chip which features some circuits developed in the prototypes.

Chapter 1

Pixel detectors in particle physics

1.1 Introduction

Silicon detectors are crucial tools used in modern high energy physics (HEP) experiments to detect particles, especially in the proximity of the interaction point. The information collected by these detectors is used to reconstruct the particle's track and primary and secondary vertex positions with high spatial resolution. There are two families of silicon detectors used in HEP: strips and pixels.

Strip detectors have been used for longer time in tracking experiments since they are easier to build and read out due to the lower number of channels. On the other hand, they provide position information in only one dimension, forcing the use of multiple planes of detectors rotated with respect to each other to obtain several coordinates to reconstruct the particle's track. This solution however increases the amount of material of the detector and hence the multiple scattering probability, which in turn degrades the overall resolution. Moreover, multiple particles create ambiguities which make pattern recognition less robust.

Research on detectors that could provide two dimensional information started immediately after the first reports on strip detectors [3]. The first type of pixel detector was a charged coupled device (CCD) [4]. Developments of this technology started in parallel with strip detectors for applications where the expected event rate was lower, since one of the main limitations of CCDs is the very slow readout speed. Pixels became common in high energy physics experiments after developments both in detector connectivity (bump bonding) and integrated circuits (ICs) technology. Pixel detectors are used today in many fields besides

tracking, like medical imaging, fluorescence microscopy or, to stay in high energy physics, calorimetry. These applications, however, are beyond the scope of this work and will not be discussed.

In the following sections a brief history of silicon detectors will be given, highlighting mainly the achieved resolution and the electrical characteristics of the readout electronics. After that, a more detailed description of the state of the art detectors and readout chips will be given to form a reference framework in which this work has been developed.

1.2 Tracking silicon detector: overview

Figure 1.1 shows the most important accelerators used for high energy physics discoveries during the past 50 years. In describing the developments of silicon detectors we will focus on the experiments built to collect data coming from these machines after a brief discussion of the first successful results in using silicon detectors.

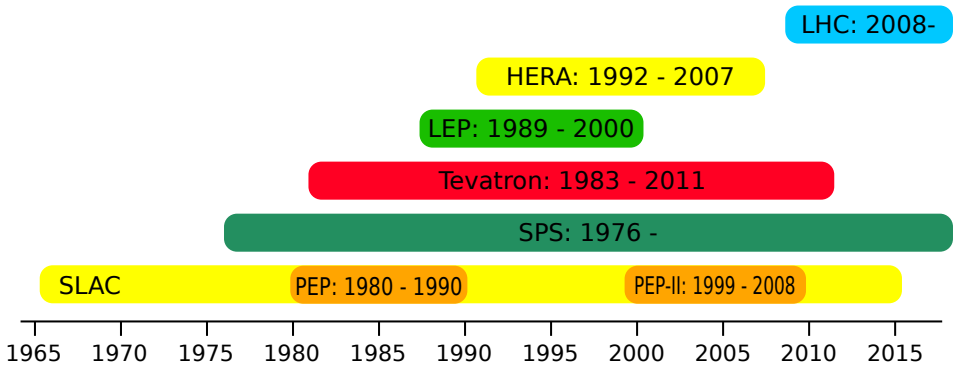


Figure 1.1. *Timeline of the most important accelerators used in high energy physics in the past decades.*

The first working silicon strip detector was used at CERN at the NA11 experiment [5] installed in the SPS accelerator in the early 80's. The NA11 experiment was aimed at studying short lived particles and in particular charmed hadrons [6]. The first prototype consisted of 100 strips 140 µm wide, 30 mm long with a pitch of 200 µm and a total sensitive area of 20 mm $\times$ 30 mm. The final detector consisted of 1200 strips with a pitch of 20 µm; it had 4.5 µm single hit resolution and an analog readout made of hybrid preamplifiers and Analog to Digital Converters (ADCs). This first detector proved its usefulness in vertex reconstruction but also gave clear indications that improvements both in the manufacturing

Experiment	Chip name	Type	Year	Technology
Mark II (SLC)	Microplex	Strip	1988	5.0 µm
DELPHI (LEP)	MX3	Strip	1991	3.0 µm
DELPHI (LEP2)	SP8	Pixel	1997	3.0 µm
ALEPH (LEP)	CAMEX64	Strip	1991	3.5 µm
OPAL (LEP2)	MX7 Microplex	Strip	1997	1.2 µm
BaBar	Atom	Strip	1995	0.8 µm
CDF (Tevatron) / L3 (LEP)	SVX	Strip	1992	3.0 µm
D0 (Tevatron)	SVX II	Strip	2001	1.2 µm
HERMES/HERA-B (HERA)	HELIX 2.2	Strip	2001	0.8 µm
H1 (HERA)	APC128	Strip	2001	0.8 µm
ZEUS (HERA)	HELIX 3.0	Strip	2001	0.8 µm

Table 1.1. *Overview of the developments in readout chips for silicon detectors for the main high energy physics experiments.*

of the detectors and in the readout electronics were required for future experiments.

As mentioned, the readout of the detectors used in the NA11 experiment was still difficult and discrete components were used: to allow the miniaturization of the detector and to increase the number of channels available Application Specific Integrated Circuits (ASICs) were necessary to provide small area, high speed readout systems. In 1985 successful tests of silicon strip detectors with ASIC readout were carried out [7].

Also charge coupled devices (CCDs) started being used soon after their invention [8] in fixed target experiments [9] and in collider experiments such as SLD at the SLAC linear collider. The VXD2 detector was assembled using commercial CCDs of area $1\,\mathrm{cm}^2$ and pixel size $22\,\mu\mathrm{m} \times 22\,\mu\mathrm{m}$. The pixel readout rate was 2 MHz with a shaping time of 300 ns and a noise level of less than 300 electrons. In this case the signals from the pixel were still processed by external electronics.

Miniaturization and high readout speed were not the only difficulties to overcome. The detectors are generally placed close to the interaction point thus collecting a lot of radiation that can damage them, degrading the performance or in extreme cases causing the complete failure of the device. Radiation hardness then became another key aspect to take into account during the development of silicon detectors. Table 1.1 gives an overview of the various readout ASICs discussed in this section and shows the continuous trend of improvements in the available technology and the performances of the ASICs produced.

Following the first successful results, silicon detectors for tracking started to become widely used. Mark II at the Stanford Linear Accelerator Center (SLAC)

used silicon microstrips [10] readout by a custom designed ASIC, Microplex [11]. The chip contained 128 charge sensitive amplifiers with multiplexed analog output. It was produced in 5 µm nMOS technology and the final ASIC had an active area of 4.4 mm $\times$ 6.4 mm and it could withstand more than 1 Mrad before failure.

Experiments at the Large Electron Positron (LEP) collider also installed silicon tracking detectors. At DELPHI, the tracking detector consisted of three layers of silicon microstrips with a pitch of 25 µm [12]; the 73728 total channels were readout serially by the MX3 chips produced in 3 µm CMOS technology. The chip consisted of 128 charge sensitive amplifiers, with every channel dissipating 0.5 mW. The serial readout guaranteed a rate of 2.5 MHz and the signal to noise ratio was 15:1. The radiation dose causing chip failure was in the range from 5 krad to 85 krad.

For the upgrade of LEP, DELPHI replaced the microstrips with two layers of pixel detectors plus two layers of microstrips [13]. The pixel detector had in total 1.2 million channels. Each pixel was 330 µm $\times$ 330 µm except for pixels at the edges which were bigger to minimize the inactive area. They were read out by the SP8 chip; in every pixel there was a preamplifier, a shaper, a discriminator and a 1 bit memory. A notable feature was the implementation of a zero suppression readout scheme, that allowed to read out only the pixels with a hit.

The ALEPH vertex detector [14] was also a microstrip detector with active area 49 mm $\times$ 49 mm and strip pitch of 25 µm or 50 µm for P or N type strips. The CAMEX64 readout chip was built in 3.5 µm technology, it had 64 channels which individually dissipate roughly 1 mW of power and had a baseline noise of 335 electrons. The chip could sustain 25 krad of radiation before it stopped functioning. Both the detectors and readout chips were updated for phase two of operations (LEP2), with improvements mainly in radiation hardness and noise performance.

L3 installed a silicon microstrip detector in 1993 as an upgrade of the existing tracker which did not use any silicon system [15]. To have the detector ready in time for the installation they decided to use the same readout chip as CDF (described later in this section).

OPAL, the fourth experiment at LEP, installed a silicon microstrip tracker during the first upgrade [16]. The 65502 channels were read out by the MX7 chip and its radiation hard (MX7-RH) version which was used in proximity of the interaction point and built in 1.2 µm technology. The noise was kept below 350 electrons and the power consumption was 2 mW per channel. The signal to noise performances could be kept within 80% up to 700 Gy of absorbed dose. Each channel contained a Charge Sensitive Amplifier (CSA) and a bandwidth filter with the output connected by switches to two storage capacitors.

At SLAC (California, USA) also the BaBar experiment used silicon strips as

vertex detectors. The 128 strips were read out by the Atom chip built in 0.8 µm technology. The peaking time of the chip was selectable among 100 ns, 200 ns and 400 ns giving a different ENC from 380 to 220 electrons respectively with an average power consumption of 4.5 mW per channel.

The next generation of collider experiments to use silicon vertex detectors were CDF and D0 at Tevatron at Fermilab (Illinois, USA). The CDF silicon strip tracker [17] was readout by the SVX IC chip which was built using 3 µm CMOS technology [18]. The 128 channels in a single chip consumed 150 mW while the signal to noise ratio was between 10 and 15. The readout speed was either 1 MHz, when reading out the analog information, or 10 MHz when only the digital part was transmitted off chip. The chip had an example of a sparse-readout system: one could choose to readout only strips where a hit was detected instead of reading out all the channels. Tests on radiation hardness proved that the noise would double after an exposure to 20 krad of radiation making the chip not usable beyond the end of the scheduled RunI.

For the upgrade of the detectors for RunII of Tevatron, also D0 installed a microstrip tracker [19]. The SVXII chip was the upgrade of the SVX made in 1.2 µm radiation hard technology and had 128 channels. It featured sparse readout, a signal-to-noise ratio of 20 and power consumption approximately of 3 mW per channel [20].

Around the same time ZEUS, HERMES and HERA-B at the Hadron-Electron Ring Accelerator (HERA) at DESY (Hamburg, Germany) installed a strip vertex detector for the first upgrade in 2000 [21], [22]. The strips had a 20 µm pitch but only one in six was AC coupled to a readout line. The signals were readout by the Helix3.0 ASIC built in 0.8 µm CMOS technology. Each chip contained 128 channels, each one equipped with a charge amplifier and shaper with a measured ENC of $340 + 40C$ electrons, where C is the input capacitance in pF. The signals were then sampled in an analog pipeline with a maximum latency of 128 samples. The readout was performed through a serial bus and multiple chips could be daisy chained together. A chip dissipated 2 mW per channel and could sustain up to 100 krad radiation dose before deteriorating operations [23].

The other general purpose detector at HERA was H1. H1 had a backward silicon tracker which was upgraded during the 2000 shutdown with a forward and a central silicon tracker. The first version of the readout chip was called APC128 [24] and it was produced in a 2 µm technology. Each one of the 128 channels consisted of a CSA followed by an analog event pipeline with a total power consumption of 300 µW. The noise measurements showed values as 675 electrons + 28 electrons pF^{-1}. For radiation doses over 100 krad a change in the behavior of the chip was detected, making it unreliable for further operation. For the central tracker a radiation hard version of the chip was produced [25]. The main difference between this new version and the previous one is the 2 µm

DMILL radiation hard technology which consequently lead to the redesign of the analog frontend, in particular the amplifier, to respect the new design rules.

1.3 Modern silicon detectors at the LHC

The Large Hadron Collider [26] (LHC, see figure 1.2) is a proton accelerator installed at CERN in the 27 km tunnel which previously hosted the LEP accelerator.

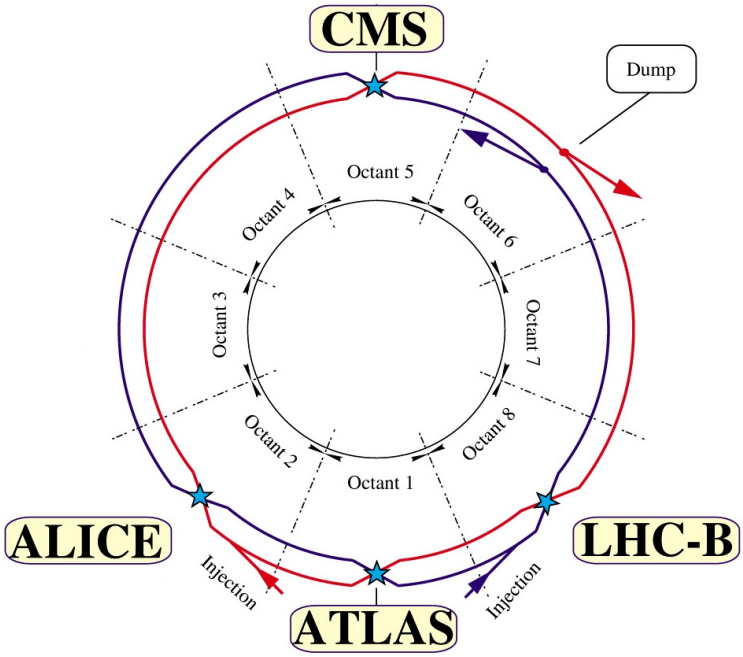


Figure 1.2. *Schematic layout of the LHC. The two beams are running in opposite directions.*

One ring of superconducting magnets and RF cavities stabilizes and accelerates two bunches of protons which travel in opposite direction. At four interaction points the two beams collide every 25 ns with a nominal center of mass energy of 14 TeV. At the four collision points experiments have been built: two high luminosity, general purpose experiments (ATLAS and CMS), a B-physics experiment (LHCb) and one dedicated heavy ions experiment (ALICE)[1]. The

[1]LHC is designed to run not only with protons but also with lead ions.

Experiment	Chip name	Tech. (µm)	Pixel size (µm)	Dimension (mm)	Power (µW/ch.)
ATLAS	FE-I3	0.25	400 × 50	7 × 11	40
ATLAS (up.)	FE-I4	0.13	250 × 50	20 × 19	6.6
CMS	PSI46V2	0.25	100 × 150	7.9 × 9.8	29
LHCb	Beetle	0.25	NA	6.1 × 5.5	5
LHCb (up.)	VeloPix	0.13	55 × 55	14 × 14	46
Medipix coll.	Medipix3	0.13	55 × 55	14 × 14	15
Medipix coll.	Timepix	0.13	55 × 55	14 × 14	14

Table 1.2. *Overview of the latest developments in pixel readout chips.*

target luminosities are $10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ for ATLAS and CMS, $2 \times 10^{32}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ for LHCb and $10^{27}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ for ALICE during the ion runs.

The overview of tracking detectors given in section 1.2 pointed out clearly the trend in miniaturization, lower power, low noise and increased radiation hardness for detectors used in high energy physics applications. A list of the most important requirements for modern tracking detectors includes:

- low noise frontend;
- low power consumption per channel;
- high granularity;
- radiation hardness of both the sensor and the readout electronics;
- high readout speed;
- low cost.

It is clear that the four detectors at the LHC, given the harsh environment where they have to operate, stretch the use of available technology to the limit in terms of required radiation hardness, readout and processing speed, detector granularity, cooling and overall performance. In the following sections an overview of ATLAS, CMS and LHCb will be given, focusing in particular on the pixel silicon detectors and their readout electronics. Common feature to all the readout chips currently used in the three experiments are the 0.25 µm technology used and special layout rules used to ensure higher radiation hardness with respect to the standard design rules [27]. Table 1.2 summarizes the characteristics of the chips that will be presented in the new sections about LHC and multi purpose readout chips that will be introduced subsequently.

1.4 The Atlas pixel detector

ATLAS (A Toroidal LHC ApparatuS) is a general purpose detector [28] installed at the LHC at CERN. Figure 1.3 shows a cut-away view of the ATLAS detector. The detector is approximately 25 m high and 44 m long with a weight of roughly 7000 t.

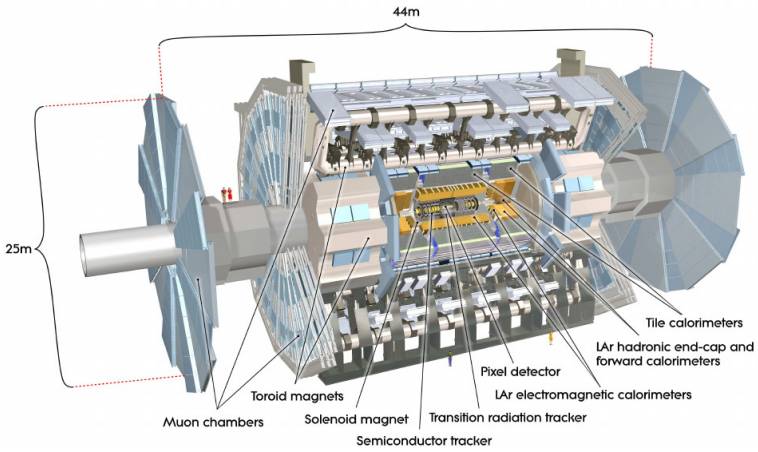


Figure 1.3. *Cut-away view of the ATLAS detector.*

In this thesis, we will focus on the characteristics of the pixel tracker which provides the required momentum and vertex resolution together with the microstrip and the straw tube detectors. The pixel detector has approximately 80.4 million readout channels and it has to withstand a 1 MeV neutron equivalent fluence (F_{neq}) between $46 \times 10^{12}\,cm^{-2}$ and $270 \times 10^{12}\,cm^{-2}$ for a maximum dose of 15.8 Mrad[2]. Over the ten-year design lifetime of the experiment, the pixel inner vertexing layer must be replaced after approximately three years of operation at design luminosity.

The FE-I3 (FrontEnd Iteration 3) pixel chip [29] is the currently used readout chip for the pixel sensors. It contains 2880 pixel cells with dimensions 400 µm × 50 µm arranged in a 18 × 160 matrix with the final size of the chip being 0.7 cm × 1.1 cm. Power consumption per channel is kept within 40 µW while the noise is lower than 200 electrons.

Each pixel cell contains a CSA where the signal from the sensor is integrated, and a digital part where the signal from the analog block is compared to a

[2]Assuming an inelastic cross section of 80 mb, a luminosity of $10^{34}\,cm^{-2}\,s^{-1}$ and a data taking period of 10^7 s. Simulation results.

programmable threshold in the discriminator. Figure 1.4 shows the digital part of the pixel. The "D" block generates two short (ns) pulses at the rising and falling edge of the signal which are used to calculate and store the Time over Threshold (ToT) information as the combination of two different time stamps. The complete hit information is then available after the falling edge. The readout part transfers the hit pixel address, the time stamp and the ToT information to the periphery of the chip; unless a trigger signal arrives from the Level-1 trigger in less than 3.2 µs the hit is deleted. Otherwise, the triggered events are serially readout from the chip in order of trigger arrival.

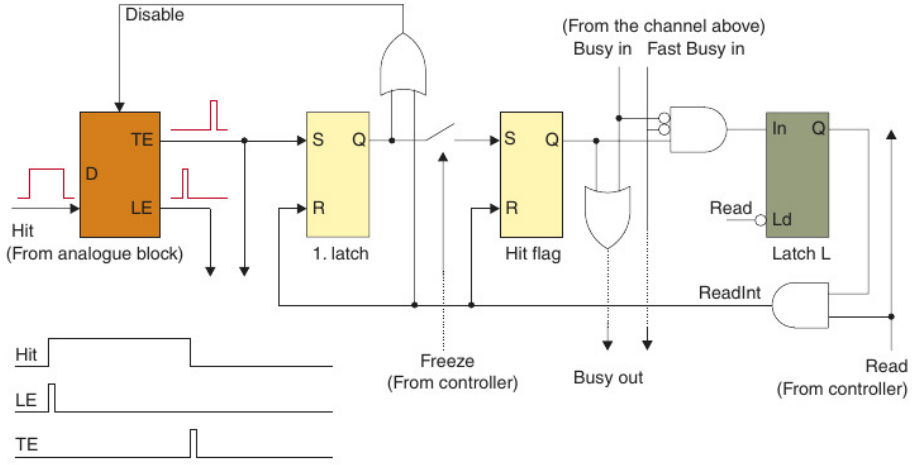


Figure 1.4. *The digital part of the FE-I3 pixel with the timing diagram. The "D" block generates the two short pulses used to determine the ToT information from the two respective time stamps. ToT, ToA and the pixel number are then transferred to the periphery of the chip. If a trigger arrives the hit is readout, otherwise it is deleted.*

1.4.1 Atlas upgrade

After the first three successful years of operations, LHC shut down to prepare the machine for the 14 TeV operation. During the shutdown the ATLAS detector has been extended with a pixel layer close to the beam pipe which uses a new readout chip.

The FE-I4 ASIC [30], successor of FE-I3, is designed in 130 nm CMOS technology. It contains 26880 hybrid pixels arranged in a matrix of 80 columns with 250 µm pitch and 336 rows with 50 µm pitch. The dimensions of the chip are

2 cm $\times$ 1.9 cm. The FE-I4 architecture is fundamentally different from FE-I3. In particular, it has been decided that the hit recorded in the pixel should not be moved to the periphery of the chip and then wait the decision to keep it or not based on the level 1 trigger decision. Instead the hit is stored locally until the same level 1 trigger decides if it is to be kept or not. The pixels are organized in double columns and divided in 2 $\times$ 2 groups, as shown in figure 1.5. Each pixel is equipped with its own analog frontend but the digital logic is shared among the four pixels in the group and it is called Pixel Digital Region (PDR). It has been shown [31] that this solution minimizes the physical resources needed to store and process the hit information. Moreover, the calculated inefficiency is below 0.1% for the innermost pixel layer at 3 times the full LHC luminosity and assuming a latency of 120 bunch crossing.

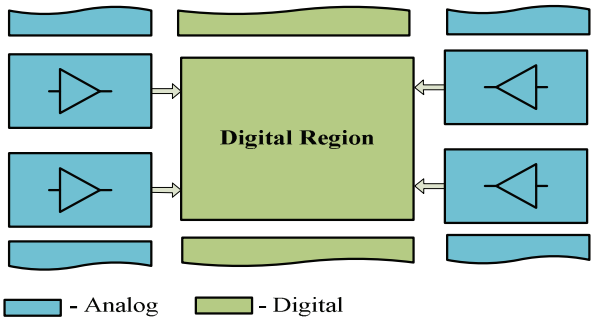


Figure 1.5. *Double column layout: a group of 2 $\times$ 2 pixels, each one with its own analog frontend, shares the digital logic to minimize the physical resources needed to store and process the hit information.*

The global time stamping is common to the PDR while the ToT is locally produced in the single pixel with a counting technique with a four bits resolution. The storage of the ToT values is done in the PDR which can contain up to five events. Since the four pixels are readout only if a trigger arrives the activity on the common double column bus is lower with respect to FE-I3.

The analog frontend [32] has been designed as a two stages architecture (see figure 1.6). The first stage is a CSA whose purpose is charge collection. The second stage is a voltage amplifying stage with no shaping of the signal. Once the charge is collected the amplification takes place in this stage which is decoupled via the input capacitor C_c isolating in practice the second stage from any DC shift that may occur due to radiation effects. The ENC is kept below 300 electrons.

An 8bit/10bit encoding has been chosen to send the data off chip. However,

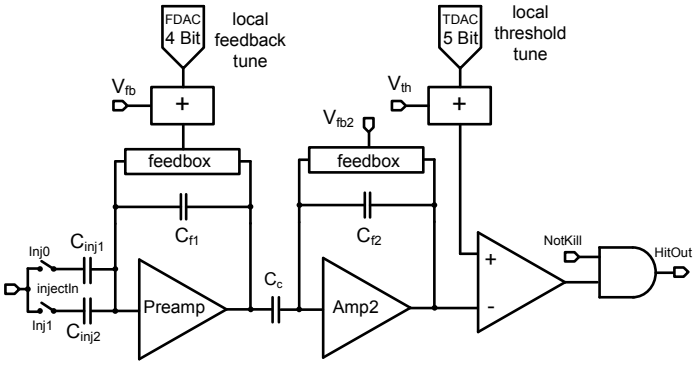


Figure 1.6. *FE-I4 frontend block diagram. The double stage architecture allows to decouple the charge collection and shaping stage from the amplification one. The capacitor C_c decouples the first part from the second, isolating the last stage from DC shifts due to radiation effects.*

in order to cope with the required data rate expected a faster clock than the 40 MHz has to be used for the readout. This clock is produced on chip using a Phase Locked Loop (PLL) and allows a readout speed of 160 Mbit s^{-1}.

1.5 The CMS pixel detector

The Compact Muon Solenoid (CMS) detector [33] is the other general purpose experiment at LHC. The detector (see figure 1.7) is 21.6 m long and has a diameter of 14.6 m. It has a total weight of 12 500 t. The main feature driving the design of the full detector is the superconducting solenoid that provides the 4 T magnetic field for the muon momentum measurements.

The tracking volume is a cylinder 5.8 m long with a diameter of 2.6 m. It is composed of ten layers of silicon microstrips to provide the required granularity and precision in tracking and of three layers of silicon pixels which are placed close to the interaction region which improve the reconstruction of secondary vertices. The total detector surface of the silicon tracker is about 200 m^2. The pixel detector covers the interaction point at radii between 4.4 cm and 10.2 cm and it consists of 1440 pixel modules. The operating conditions foresee a hit rate density of 1 MHz mm^{-2} at a radius of 4 cm. Since the size of a pixel is 100 µm × 150 µm the occupancy is around 1%.

The sensors are readout by the custom chip PSI46V2 [34] which contains a

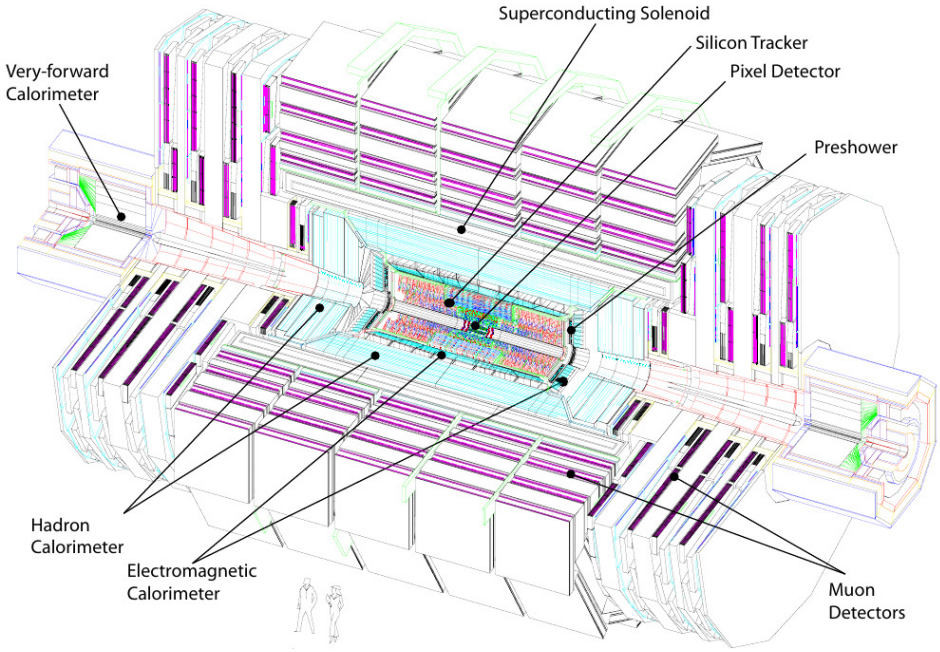


Figure 1.7. *Compact Muon Solenoid overview.*

matrix of 52 $\times$ 80 pixels with the total size of the chip being 7.9 mm $\times$ 9.8 mm. The three main blocks of the chip are the single pixel units which are organized in double columns, the end of column (EOC) periphery which controls the readout and trigger of a single double column and the periphery of the chip where the supply and controls are located. A single readout chip consumes 120 mW (29 µW per channel).

Figure 1.8 shows the single pixel block diagram; the signal from the sensor is amplified and shaped by a two-stages CSA plus a shaper. The signal from the frontend is followed by a comparator which has a 4 bits programmable threshold. This threshold is used to mitigate the transistors mismatch inherent to each production process. Once the signal goes above threshold the output of the shaper is recorded in a sample and hold circuit. The periphery of the double column is notified of the hit immediately through a double column common OR and the pixel is inactive until the signal is readout. Thus, the dead time of the single pixel is short but it depends on the occupancy. An event activating multiple pixels in the same double column will result in those same pixels being inactive for a long time.

The readout of the pixel occurs when a token from the double column pe-

riphery arrives. It is important to remark that the CMS pixel chip stores and sends the analog information (pulse height) to the chip periphery which is then digitized, unlike the ATLAS pixel chip in which the digitization is done at the pixel level. The analog information is sent out together with the pixel address and stored in buffers in the EOC where the data are then compared to the higher level trigger which is externally produced and subsequently kept to be sent out of the chip or discarded.

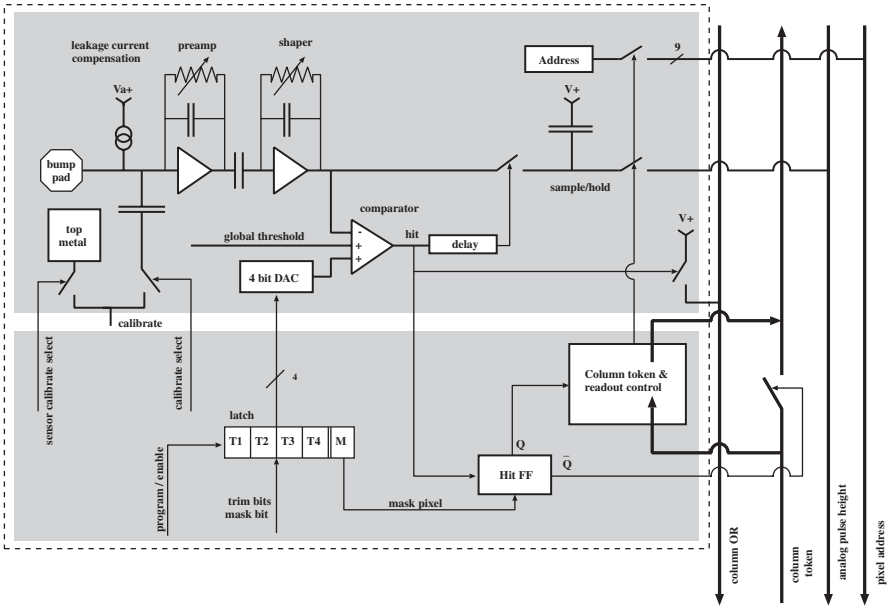


Figure 1.8. *Single pixel block diagram of the CMS pixel chip.*

1.6 The LHCb Vertex Locator

LHCb [35] is an experiment dedicated to the study of heavy flavor physics and in particular to the decay of beauty and charmed particles to detect any violation of the CP symmetry. Figure 1.9 shows an overview of the detector.

The tracking system of LHCb is divided in two parts: the Vertex Locator (VELO) and the Silicon Tracker (ST). In the following section only the VELO will be described with its upgrade, since it is connected with the chips developed in this work.

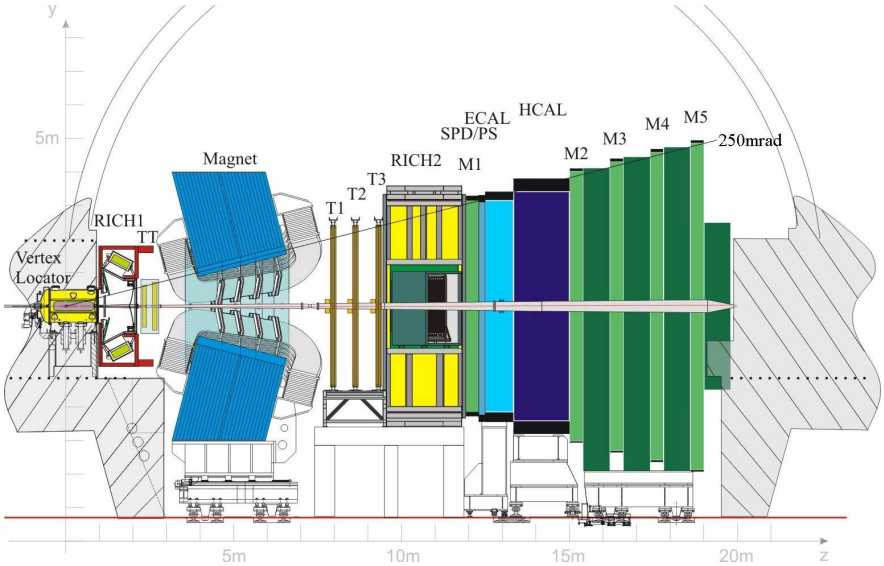


Figure 1.9. *LHCb detector overview.*

Given a certain number of constraints (geometrical, environmental, integration with the surrounding detector systems), the LHCb VELO detector is quite different in concept with respect to the ATLAS and CMS trackers. To cope with the high rate of LHC and to produce a fast high level trigger, simulations prove that the best choice for the coordinate system are the polar coordinates $R\phi$ instead of the usual xy scheme. This feature led to the design of two different sensors, one called ϕ-sensor and the other one R-sensor, the former providing information on the azimuthal angle the latter on the distance from the beam. A sketch of the two different sensors can be seen in figure 1.10 where for clarity only a portion of the strips is depicted.

The VELO is readout with a custom ASIC called Beetle. It has a die size of $6\,1 \times 5.5\,\mathrm{mm}^2$ and 128 readout channels each equipped with a CSA and CR-RC shaper as shown in picture 1.11. A comparator per channel provides a binary signal. The output of the shaper or of the comparator is then sampled into an analog pipeline at 40 MHz. The measured noise of the frontend is equal to 500 ± 48.3 electrons/pF. The minimum rise time is less than 25 ns with the remainder adjustable to be less than 30%. The chip has a typical power consumption of 5 mW per channel.

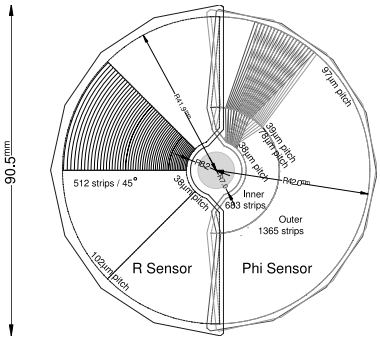


Figure 1.10. *LHCb VELO sensor sketch.*

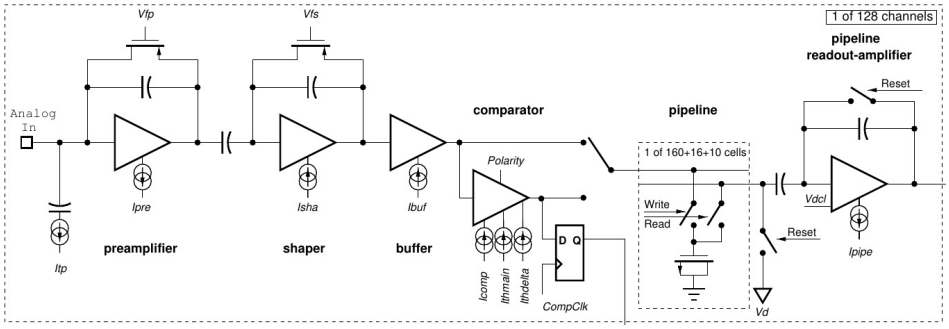


Figure 1.11. *LHCb VELO frontend.*

1.6.1 VELO upgrade: VeloPix

For the upgrade LHCb decided to replace the current strip detector with a pixel detector called VeloPix [36]. VeloPix is derived from the latest iterations of the Medipix/Timepix series of chips (see section 1.7) and it shares with them some characteristics like the 130 nm technology and the 256 $\times$ 256 pixel matrix with a pixel size of 55 µm $\times$ 55 µm. Moreover VeloPix uses many circuits already developed for Timepix3 (see section 5 for more details): a fast frontend (rising time < 25 ns), zero suppression and data driven readout. Since VeloPix will be placed in proximity of the interaction point at a distance of about 7 mm both the radiation hardness of the chip and the readout speed are of great importance. The chip has to be able to survive doses up to 400 MRad in a foreseen lifetime of 10 years and it has to be capable of handling a hit rate of 500 MHits/s which requires an output bandwidth larger than 12.2 GBit/s. The chip will consume

less than 3 W.

One notable characteristic of VeloPix derives directly from the need to process such a big amount of hits. To reduce the amount of bits to send to the periphery an approach similar to the one used for FE-I4 has been adopted. 2×4 pixels are grouped in a structure called Super Pixel. This allows to reduce by 25% the required bandwidth since duplicate information such as the timestamp will be sent only once. The consequence is that the layout of the Super Pixel requires a different positioning of the analog frontends on the sides while the central part is used for the common digital blocks. VeloPix is in the design phase and the first production run is foreseen in summer 2015.

1.7 The Medipix family

In the previous sections the focus has been on detectors and readout chips used in collider experiments. However it is clear that the applications of silicon detectors are not limited to this field. In the early nineties a collaboration was formed with the aim of developing a photon counting chip for imaging purposes which was built in 1997 called Medipix1 [37]. The chip contains a matrix of 64×64 pixels of size $170\,\mu m \times 170\,\mu m$ covering a total active area of $1.2\,cm^2$ and was developed using a 1 µm technology. Each pixel contains a CSA and a shaper. The signal collected and amplified by the analog frontend is then compared with an externally set threshold in the discriminator: if the signal exceeds the threshold one event is counted up to 32767 events (15 bits counter). The maximum count rate is 2 MHz with a maximum readout speed of 384 ms at 10 MHz.

Following the success of Medipix1 and with the purpose of taking advantage of the submicron technology that were becoming available to increase the number of pixels per chip and include more functionality, the Medipix2 chip was developed [38] in 2002 in 0.25 µm technology. The matrix was enlarged to 256×256 pixels of size $55\,\mu m \times 55\,\mu m$ with an active area of $2\,cm^2$. The chip consumes less than 1 W. While the structure of the frontend remained the same with the usual amplifier-shaper-discriminator chain, the input was upgraded to accept both positive and negative charge to allow the use of different materials as sensors. Moreover, with Medipix2 the concept of an energy window was introduced: it is possible to select two thresholds (upper and lower) to accept only photons inside that energy window. Each pixel can accept a rate of 100 kHz in an adjustable time window. Readout is performed after exposure of the chip to minimize the dead time and can be done serially or in parallel. In view of large area applications the chip was designed to be 3-side buttable.

Medipix3 [39] is the last arrival in the Medipix family. While the physical dimensions are the same as Medipix2, it uses a 130 nm technology which allows

to put more transistors and hence more logic in the single pixel cell while retaining the same low power consumption. The upgrades consist in particular in the operation modes of the chip; to mitigate the effects of charge sharing a charge summing mode has been implemented. When a cluster of neighboring pixels is hit, all the charge is allocated to the cell with the highest charge deposit. Moreover, it is possible to configure the chip in spectroscopic mode. In this case, 4 pixels are connected allowing the use of 8 different thresholds at the cost of losing some spatial resolution.

1.8 The Timepix chip

The surprising application of the Medipix2 chip as readout for Micro Pattern Gaseous Detectors (MPGD) such as Micromegas or Gas Electron Multipliers (GEM) sparked the desire to design a chip that could provide information on the ToA of the electrons from the ionization trail as well as information on the charge collected. This led to the design of the Timepix (Timepix1) chip [40].

Timepix is a general purpose chip which allows to record the ToA, the ToT or count the number of events on a per pixel basis. The chip has an active area of 1.4 cm $\times$ 1.4 cm. The pixel pitch is 55 µm and the power consumption is 14 µW per channel. The periphery is located on one side, making Timepix three side buttable.

Figure 1.12 shows the time diagram for the different modes of operation of Timepix. In any operation mode the shutter must be open to record the incoming hits; this signal is set externally by the user. In Time of Arrival (ToA) mode the first hit to arrive with the shutter open starts the recording of the system clock by counting. The counting stops when the shutter is closed. A second hit detected in this time window in the same pixel does not have any influence. In Time over Threshold (ToT) mode, instead, the time spent over threshold by all of the detected hits when the shutter is open is recorded, giving information on the total amount of charge detected. The different modes can be selected on a per pixel basis.

Figure 1.13 shows a block diagram of the Timepix pixel. The analog frontend is made of a single stage CSA and a discriminator. Given the application in MPGDs particular care has been taken in the design of the preamplifier to combine low noise and high gain. To reduce the input capacitance (and hence reduce the noise) a cascode has been added in the amplifier; the biasing is controlled with a global 8-bits DAC. The high gain limits the linear output range but makes the rise time faster which is important to reduce timewalk (see section 3.1).

The digital part of the pixel includes the Timepix Synchronization Logic (TSL), a 14-bits shift register and the 8-bits of pixel configuration. The TSL syn-

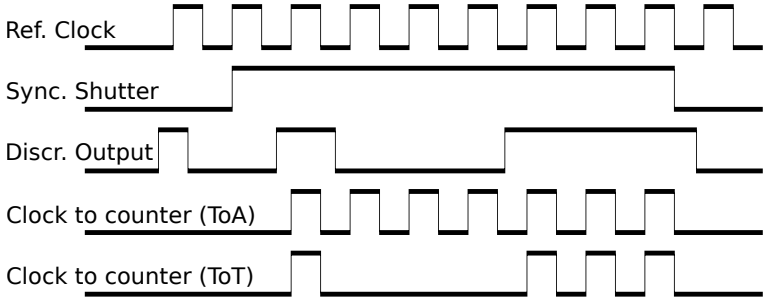


Figure 1.12. *Timepix time diagram.*

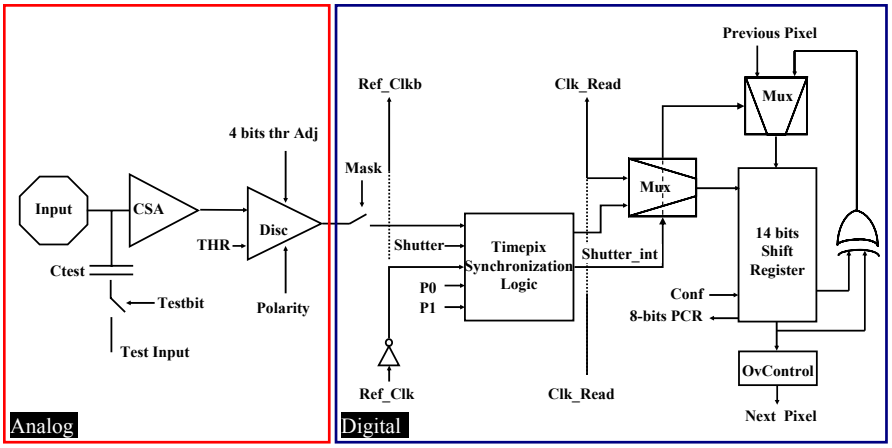


Figure 1.13. *Timepix pixel block diagram.*

chronizes the externally produced shutter with the system clock so that every pixel receive a glitch-free internal shutter. It is composed of two state machines designed with an asynchronous network which uses SR flip-flops. Besides not propagating glitches to the counter, it takes care that the digital logic works only when there is a hit, to minimize power consumption.

An important feature of the chip to highlight is that the system clock, which determines the resolution, can be set externally up to 100 MHz. This is crucial when it comes to Timepix as readout for MPGD and in particular for GridPix detectors (see section 2.1 for more details) since the resolution in the direction perpendicular to the chip plane is determined by the time resolution available: in Timepix this is then limited to 10 ns which is not enough to use GridPix as tracking detector.

Given the limitations of Timepix as readout chip for GridPix detectors the design of a new chip called Timepix3 started in 2010. The chip has been taped out in 2013 and is described in more details in section 5.2 together with the first measurement results.

1.9 Conclusion

In this chapter an overview of the most important strip and pixel detectors used in high energy physics experiments has been presented. The focus on the readout chips has highlighted how since the beginning the design and performance of the chips rapidly evolved with the newer technologies available. There is a clear trend towards readout chips that are radiation hard and consume the least possible amount of power. In addition, more functionality is being implemented in the single readout cell thanks to the available submicron technologies.

Chapter 2

Gaseous pixels and high resolution time measurements

The review presented in Chapter 1 focused mainly on readout chips developed for silicon detectors. Gaseous detectors like Time Projection Chambers existed but they were usually readout with planes of wires. However in the past decade a new trend in gas detectors emerged with concepts like Micromegas detectors or Gas Electron Multipliers requiring studies on gas properties and detector characteristics and the development of new, dedicated readout chips. The main feature of a Micro Pattern Gas Detector (MPGD) is the 3D reconstruction of a particle's track which can be obtained by measuring the trail of the electrons in the detection gas volume. To reconstruct this trail one measures the time it takes the individual electrons to travel to the anode.

In the following sections the operational principles of a particular type of MPGD called GridPix will be presented, followed by the basic concepts of ionization and electron transport in gases. Finally, a review of the most common time measurement techniques will be presented.

2.1 GridPix detectors

At Nikhef a novel concept was developed some 10 years ago, GridPix. A GridPix detector is a miniaturized Time Projection Chamber (TPC) that uses a pixel chip as readout plane. The detector is built combining a Timepix chip with an Integrated Grid (InGrid) on top of it. A schematic diagram of this kind of detector can be seen in figure 2.1. The first proof of concept of the readout of a micro-TPC using a pixel chip as readout plane was given in 2004 [41], [42] using a Medipix2

chip [38] with a Gas Electron Multiplier (GEM) foil on top [43]. Medipix2 is a photon counting chip and cannot measure the drift time of the electrons created by an incoming charged particle in the drift volume. On this premise, Timepix chip was developed at CERN [40], based on the existing Medipix2.

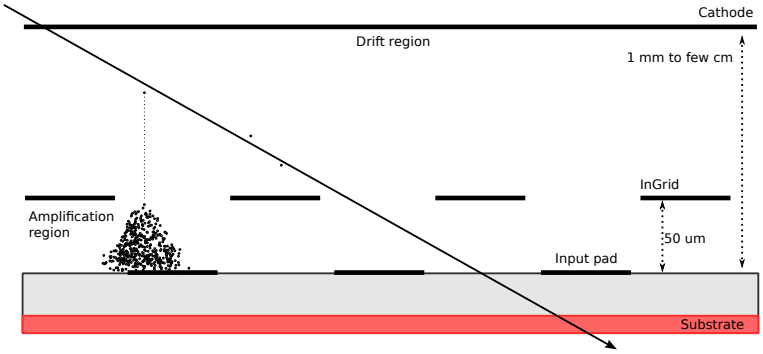


Figure 2.1. *Schematic representation of the working principle of a GridPix detector. A charged particle passes through the drift region and it ionizes the gas molecules. The generated electrons drift towards the grid. In the region between the grid and the chip an avalanche process takes place due to the strong electric field applied. The electrons of the avalanche are then collected at the input pad.*

On top of Timepix, an aluminum grid is built using MEMS[1] technology at a height of 50 µm, defining the amplification region. The grid contains holes which are aligned with the pixel pads underneath. On a larger distance from the chip a cathode is placed, which defines the drift volume and is chosen accordingly to the application. The amplification and drift volumes are filled with a gas mixture and an electric field is applied between the cathode and the chip and between the grid and the chip, which is always at ground potential. When a charged particle passes through the drift region it ionizes a few gas molecules. The liberated electrons drift by means of the applied electric field toward the grid. Once an electron traverses one of the holes in the grid an avalanche process takes place due to the strong electric field (70 to 100 kV cm^{-1}, depending on the gas mixture) in the amplification region, with typical gain values around 10^4. The electrons of the avalanche are then collected at the input pad and the resulting signal is processed by the frontend electronics.

Compared to conventional TPCs, that use a plane (or multiple planes) of wires for the readout, the main advantage of using a pixel detector is the in-

[1]Micro Electro Mechanical Systems

creased spatial resolution that can be achieved. In fact the granularity is such that most pixels record avalanches that originate from a single electron. Compared to regular silicon pixel sensors, the use of gas as detector medium on top of the chip may result in less material and hence a lower multiple scattering probability. Moreover, the input capacitance due to the detector itself is reduced, thereby reducing the input noise. It is worth noticing that a pixel chip can be used also for the readout of large TPCs if one could build such large area GridPix detectors.

Figure 2.2 shows an example of an event recorded with a prototype GridPix detector [44] having a drift distance of 3 cm. The detector was inside a magnetic field of 0.2 T with the field lines running parallel to the drift direction. The electrons from ionization of single atoms in the He/isobutane gas mixture used are traceable; different colors represent the different Time of Arrival (ToA) recorded by the Timepix and translated to height in the drift volume.

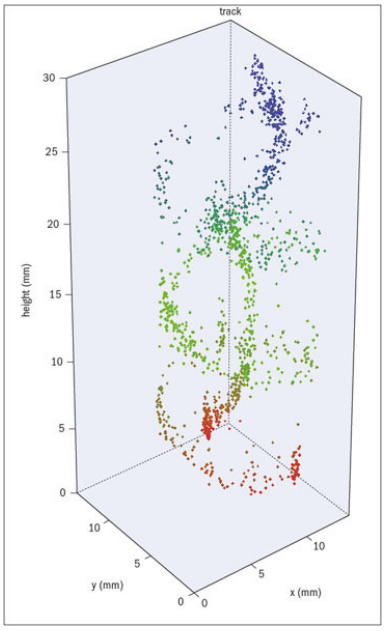


Figure 2.2. *Event recorded with a GridPix detector. The height of the drift volume is* 3 cm *and a magnetic field was applied. The different colors along the track represent measured arrival times.*

Even though a long R&D phase has shown the virtues of GridPix detectors, the viability still needs to be proven to make it reliable and suitable for operations as tracking detector in full scale experiments [45].

2.2 Gas properties

When a charged particle passes through the gas in the drift volume of a GridPix detector the relevant processes that take place from the moment the particle arrives to the detection of the signal at the input pad of the pixel chip are:

- the ionization of gas molecules;
- the drift of the generated electrons to the grid;
- the amplification of the signal in the region between the grid and the pixel pad;
- charge induction.

In the next paragraphs, some details on every step of the process will be given.

2.2.1 Ionization in the gas

A charged particle passing through the gaseous drift volume of a GridPix detector loses energy and ionizes some gas molecules [46]. Given a gas atom X and a charged particle p the interaction can be described as:

$$X + p \rightarrow X^+ + p + e^-$$

where X^+ is the positive ion and e^- is the primary electron. This process can only happen if the energy of the incoming particle is bigger than the ionization energy E_i of the gas molecules. Notice that if the primary electron energy after the first ionization is big enough, it might start a trail:

$$X + e^- \rightarrow X^+ + e^- + e^-$$

and in this case the secondary is called δ-electron.

Defining n_p as the average number of primary ion pairs per cm and n_T the average number of ion pairs including the one created by the δ-electrons one can write

$$< n_T >= \frac{L \cdot < \frac{dE}{dx} >_{\text{ioniz}}}{W_i} \tag{2.1}$$

where $< \frac{dE}{dx} >_{\text{ioniz}}$ is the mean energy loss of the incident particle, L is the path length of the gas layer the particle has to cross and W_i is the average energy of

Gas	I (eV)	W_i (eV)	$\frac{dE}{dx}$ (MeV g^{-1} cm^2)	n_p (cm^{-1})	n_T (cm^{-1})
H_2	15.4	37	4.03	5.2	9.2
Ar	15.8	26	1.47	29.4	94
Xe	12.1	22	1.23	44	307
CO_2	13.7	33	1.62	34	91

Table 2.1. *Gas properties*

the ion pair. Table 2.1 gives the values of some relevant quantities for different gases.

The energy loss process that enters in formula 2.1 to determine the number of ionizations produced is described by the Bethe-Bloch equation 2.2 which gives the mean rate of energy loss for a moderately relativistic particle of charge z passing through a material with atomic number Z and mass number A:

$$-\left\langle \frac{dE}{dx} \right\rangle = Kz^2 \frac{Z}{A} \frac{1}{\beta^2} \left[\frac{1}{2} \ln \left(\frac{2m_e c^2 \beta^2 \gamma^2 T_{\max}}{I^2} \right) - \beta^2 \right] \tag{2.2}$$

where $K = 4\pi N_A r_e^2 m_e c^2$, m_e is the electron mass, r_e is the classical electron radius, N_A is the Avogadro number, $T_{\max}$ is the maximum kinetic energy that can be transferred to a free electron in a single collision and I is the mean excitation energy[2]. The most difficult parameter to determine is I and it is usually derived from measurements. Figure 2.3 shows the results obtained for several elements [47]. For a particle with mass M and momentum $M\beta\gamma c$, the maximum kinetic energy transfer $T_{\max}$ is given by:

$$T_{\max} = \frac{2m_e c^2 \beta^2 \gamma^2}{1 + 2\gamma m_e / M + (m_e / M)^2} \tag{2.3}$$

Figure 2.4 shows the mean energy loss rate for different particles in different substances while figure 2.5 shows the simulated most probable number number of ionizations per cm for different types of particles in CO_2/DME (50/50), which is the chosen gas for the GridPix detectors.

The number of pairs produced can be estimated analytically. The production of pairs is a Poissonian process which can be described as:

$$P(n_p, < n_p >) = \frac{< n_p >_p^n \cdot e^{-<n_p>}}{n_p!} \tag{2.4}$$

[2] $m_e c^2 = 0.511$ MeV, $r_e = 2.818$ fm, $N_A = 6.022x10^{23}$ mol^{-1}

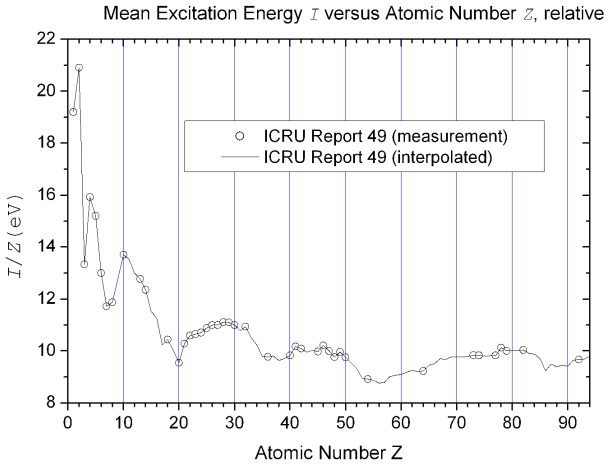


Figure 2.3. *The mean excitation potential I of atoms versus the atomic number Z.*

with $< n_p >= \frac{L}{\lambda}$ and $\lambda = \frac{1}{n_e \sigma_I}$ (n_e is the electron density, σ_I is the ionization cross section and λ is then the mean distance between ionization events). The probability of having zero interactions is $P(0) = exp{-}L/\lambda$. Knowing the intrinsic efficiency of a gas detector one can then experimentally determine the parameters λ and σ_I of a gas.

2.2.2 Electron transport in the gas

Once an electron is produced it is accelerated by the electric field applied between the cathode and the grid. In vacuum, the electron would be accelerated to high velocity and reach the grid in a short time. However the electron will scatter isotropically with the gas molecules. The net effect at the microscopic level is a random motion which is superimposed to the preferred direction of drift (toward the grid). Thus, there are two terms to take into account to describe the electron moving in the gas under the effect of an electric field: one related to the drift velocity v_D which is caused by the electric field and one related to diffusion which is the macroscopic effect of the microscopic random motion.

In the most general case, the motion of an electron in an electromagnetic field is described by equation 2.5

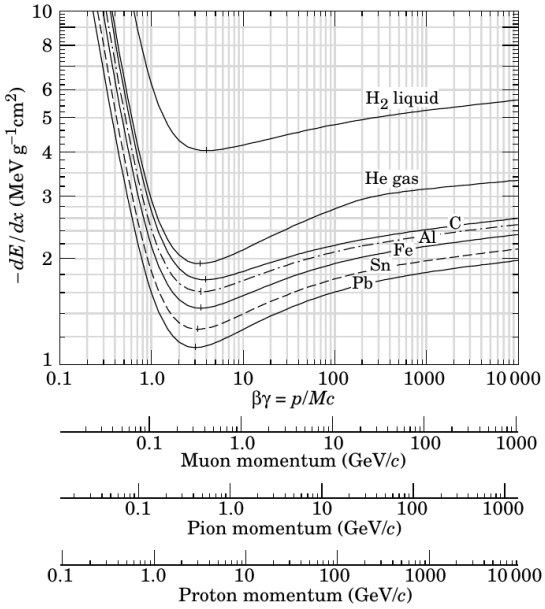


Figure 2.4. *Mean energy loss rate in liquid (bubble chamber) hydrogen, gaseous helium, carbon, aluminum, iron, tin, and lead.*

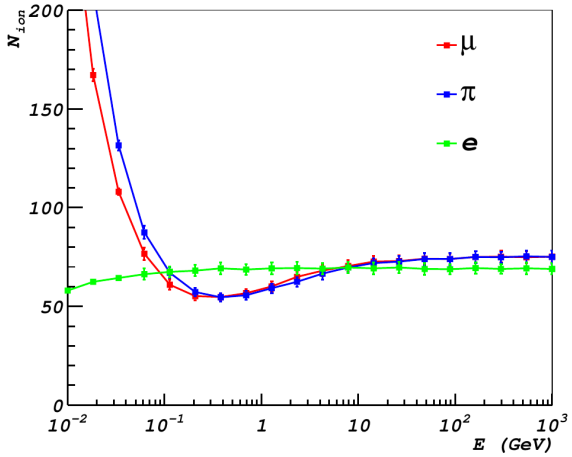


Figure 2.5. *Most probable number of ionizations per cm for different types of particles in CO_2 / DME (50/50). Calculation performed with Magboltz.*

$$m\frac{d\vec{v}}{dt} = e\vec{E} + e(\vec{v} \times \vec{B}) + Q(t) \tag{2.5}$$

where $\vec{v}$ is the instantaneous velocity, and $Q(t)$ is a time dependent term due to collisions with the gas atoms. Assuming a time between collisions τ, $\vec{E}$ and $\vec{B}$ constant between collisions (and in general across the drift volume) and averaging over a $\Delta t >> \tau$ then:

$$m < \frac{d\vec{v}}{dt} >= e(\vec{E} + < \vec{v} > \times \vec{B}) - \frac{m}{\tau}\vec{v}_D \tag{2.6}$$

which gives for the drift velocity:

$$\vec{v}_D = \mu\vec{E} \tag{2.7}$$

where

$$\mu = \frac{e\tau}{m} \tag{2.8}$$

is the electron mobility and depends on the gas. In general, one can distinguish two types of gases with respect to μ: so called hot gases for which the electron loses a small fraction of its energy during the collision, giving $\mu \propto \tau$. Typical values of v_D are, for example, 3-5 $\mathrm{cm\,\mu s^{-1}}$ in Ar/CH_4 (90/10). The other type of gas is called cold: the electrons lose a lot of energy during the collisions and thus μ is approximately constant and $v_D \propto E$. CO_2/DME (50/50) is an example of a cold gas.

The drifting electrons scatter with the gas molecules. The final random motion that is the result of this scattering process can be characterized by the mean energy ϵ and gives rise to diffusion. The total motion can be described by

$$\vec{J} = n\vec{v}_D - D\vec{\nabla}n \tag{2.9}$$

where the constant D is called diffusion coefficient. The term $n\vec{v}$ describes the motion due to the drift while the second term describes the diffusion process. The motion of the electrons follows also the continuity equation:

$$\frac{\delta n}{\delta \tau} + \vec{\nabla} \cdot \vec{J} = 0 \tag{2.10}$$

The solution of equation 2.9 in the simplest case is then given by

$$n = \left(\frac{1}{\sqrt{4\pi Dt}}\right)^3 \cdot \exp(-\frac{r^2}{4Dt}) \tag{2.11}$$

where $r = x^2 + y^2 + (z - v_D t)^2$. From equation 2.11 one can see that the diffusion width σ of an electron cloud after starting point-like and traveling for a time t is:

$$\sigma = \sqrt{2Dt} \tag{2.12}$$

so that equation 2.11 can be rewritten as

$$n = \left(\frac{1}{\sigma\sqrt{2\pi}}\right)^3 \exp(-\frac{r^2}{2\sigma^2}) \tag{2.13}$$

However, experimentally one can see that this equation is not completely valid. The electric field introduces a non-symmetric behavior in the electron motion, which is described by introducing two different diffusion values, longitudinal (D_L) and transversal (D_T). Taking into account this effect, equation 2.13 is adjusted as follows:

$$n = \left(\frac{1}{\sigma_L\sqrt{2\pi}}\right) \cdot \left(\frac{1}{\sigma_T\sqrt{2\pi}}\right)^2 \exp(-\frac{x^2 + y^2}{2\sigma_T} - \frac{(z - v_d t)^2}{2\sigma_L}) \tag{2.14}$$

2.2.3 Amplification

The electrons produced by ionization do not form a signal strong enough to be detected by current frontend electronics (for example, the input noise per pixel could be roughly 100e$^-$). For this reason, an amplification step is necessary and it is provided by the strong electric field present between the grid and the readout chip. For the purpose of this discussion such field is assumed homogeneous in the amplification region.

A primary electron can produce secondary ionization if the energy it receives from the electric field accelerates it enough to ionize another gas molecule. The secondary electrons can also receive enough energy to ionize more molecules, thus leading to the avalanche formation.

To provide a simple description of the multiplication process let's introduce a parameter α called Townsend coefficient. Given a number of electrons n that travel for a distance dx in a region with uniform electric field E the number of electrons produced will be

$$dn = \alpha n dx \tag{2.15}$$

Integrating over the total path, the total number of electrons in the avalanche will then be

$$n(x) = n_0 \exp(\alpha x) \tag{2.16}$$

with n_0 being the initial number of electrons. One can introduce the gas gain factor $G = \frac{n}{n_0} = \exp(\alpha x)$ which depends only on the gas. Experimentally, it is possible to see that for values of $\alpha x > 20$ the conditions are such that sparks start to occur in the gas, making the system unreliable.

This model, however, is too simple to explain the observations made in experiments. It is possible to obtain a more realistic result introducing an ionization parameter that depends on the avalanche size: $\alpha(n, x) = \alpha(x)(1 + \theta/n)$. One can then find out that:

$$P(n) = \frac{1}{\bar{n}} \frac{(\theta+1)^{(\theta+1)}}{\Gamma(\theta+1)} \left(\frac{n}{\bar{n}}\right)^{\theta} e^{-\frac{(\theta+1)n}{\bar{n}}} \tag{2.17}$$

The previous distribution is called a Polya distribution and it describes quite well the behavior of the multiplication process for many gases by tuning the parameter θ. However it must be said that the physical interpretation of such parameter is still unclear. Figure 2.6 shows different Polya distributions for different values of the parameter θ.

2.2.4 Signal development

The multiplication process that takes place in the high electric field region leaves behind a large number of electron-ion pairs. Due to the electric field, the two constituents move in opposite directions toward the pixel pad or the grid. By construction, most of the pairs will be produced close to the anode. Considering also that the electrons have higher mobility the final result is that the electrons will reach their electrode much faster than the ions. The outcome is that most of the signal is induced by slower departing ions.

The charge induced can be described as a current flowing between the electrode and ground. Then, applying the Shockley-Ramo theorem [48] the current can be calculated as:

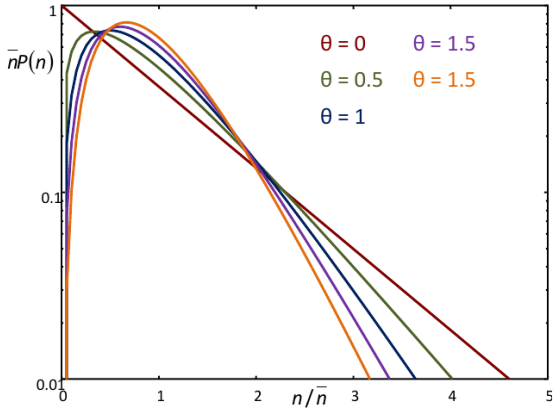


Figure 2.6. *Polya distribution for different values of θ.*

$$i(t) = q\frac{\vec{v_d} \cdot \vec{E_w}}{V_w} \tag{2.18}$$

where $\vec{v_d}$ is the drift velocity and $\vec{E_w}$ and V_w are the weighting field and potential. These last two terms are calculated by setting all the potentials and the charges to zero except for the electrode under study. The total charge collected after the moving charge has finished drifting is then

$$Q = \int_0^{\Delta t} i(t)dt = q\Delta V \tag{2.19}$$

A more precise treatment for complex geometries can be found in [49], [50] and [51] but it is beyond the scope of this thesis.

2.3 Basic frontend characteristics

In the previous section the signal coming from the primary ionization electrons was amplified through a multiplication process. Once the avalanche has been produced one needs to collect the electrons and process the resulting signal to extract the needed information. In the following paragraphs the typical frontend chain implemented in many chips (as the ones shown in section 1.3) will be discussed.

Figure 2.7 shows the basic blocks which constitute a typical electronic frontend for a chip used as readout for particle detectors.

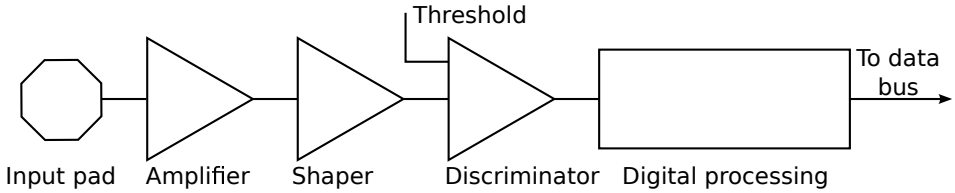


Figure 2.7. *Basic blocks which constitute the frontend electronics of a typical chip used for the readout of particle detectors.*

The avalanche signal is collected on the input pad and the resulting signal is amplified and shaped. It is worth noticing that the amplifying and shaping stages are usually performed together by the same circuit. The signal so generated is then compared to an external threshold in the discriminator. If the signal exceeds the threshold value it is then digitized and the data is transmitted on the data bus ready to be read out.

2.3.1 Charge sensitive amplifier

The signal coming from the electrons in the avalanche is collected at the input pad and amplified. While there are different types of amplifiers (voltage sensitive or current sensitive, for example) only the charge sensitive amplifier will be discussed here, since it is the one used in this thesis. Figure 2.8 shows the basic principle of a charge sensitive amplifier. The central part is an inverting amplifier to which is connected the detector, here represented with its capacitance C_d. In the ideal case the amplifier has an infinite input resistance so that no current can flow into it. Given an (inverting) gain $-A$ ($A \gg 1$), if the input signal produces a voltage v_i at the input then at the output there will be a corresponding $v_o = -Av_i$. The voltage difference between the two ends of the feedback capacitance C_f will be then $v_f = v_i(1 + A)$ which gives a stored charge of $Q_f = C_f v_f = C_f(A + 1)v_i$. Given the (mentioned) assumption that no current can flow into the amplifier one obtains that $Q_i = Q_f$: the entire input charge is collected on the feedback capacitance.

The amplifier input appears as a capacitance $C_i = \frac{Q_i}{v_i}$. Such a capacitance is called dynamic capacitance, since it varies with the input signal. It is then possible to calculate the conversion gain in terms of the input charge:

$$A_Q = \frac{v_o}{Q_i} = \frac{Av_i}{C_i v_i} = \frac{A}{C_i} = \frac{A}{(A+1)C_f} \approx \frac{1}{C_f} \tag{2.20}$$

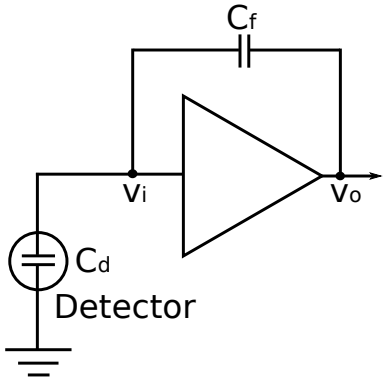


Figure 2.8. *Basic schematic of a charge sensitive amplifier. The detector is represented by an equivalent capacitance C_d.*

In conclusion, in a charge sensitive amplifier the conversion gain is controllable simply with one parameter, the feedback capacitance C_f. The treatment of the realistic circuit requires a more complex analysis of the feedback loop and of the stability of the amplifier, but the basics remain the same: the gain element must have a high input impedance and the input capacitance must be large compared to the sensor capacitance to minimize the loss of input charge.

2.3.2 Shaper

After the input signal has been amplified the shaping stage takes place. The purpose of shaping the signal is twofold: on one hand one wants to transform the very fast input signal into a more easily processable shape; on the other hand one wants to cut off the noise introduced with the input stage to improve the signal to noise ratio. In general a shaper will put a limit at high frequencies, which will set the rise time, and at low frequencies, which will set the pulse duration. However, increasing too much the pulse duration comes with an augmented dead time of the electronic chain. The amplifier stage can be also used as shaping stage: since any real amplifier as a limited bandwidth the shaping of the signal comes naturally with it.

2.3.3 Discriminator

In the simplest form a discriminator takes as input the shaped signal and compares it to an externally set threshold: if the signal is above threshold the discriminator output goes high and the presence of a pulse is recorded. This system

is called binary, because the only thing it does is detecting the presence/absence of a signal[3].

2.4 GridPix at work: an example

For tracking applications one is often interested in minimizing the thickness of the drift volume, to minimize the material. For GridPix the minimum possible height is 1 mm, since with smaller drift volumes the probability of having ionization is so small that the efficiency suffers.

Consider as an example figure 2.9: two events are shown side by side. The left event has been recorded with a detector that has a 1 mm drift height, while for the detector used to record the event on the right the drift height is 1.9 cm. It is clear that for the former event the track reconstruction is quite difficult because the number of electrons produced by ionization is small, hence the resolution will be poorly determined.

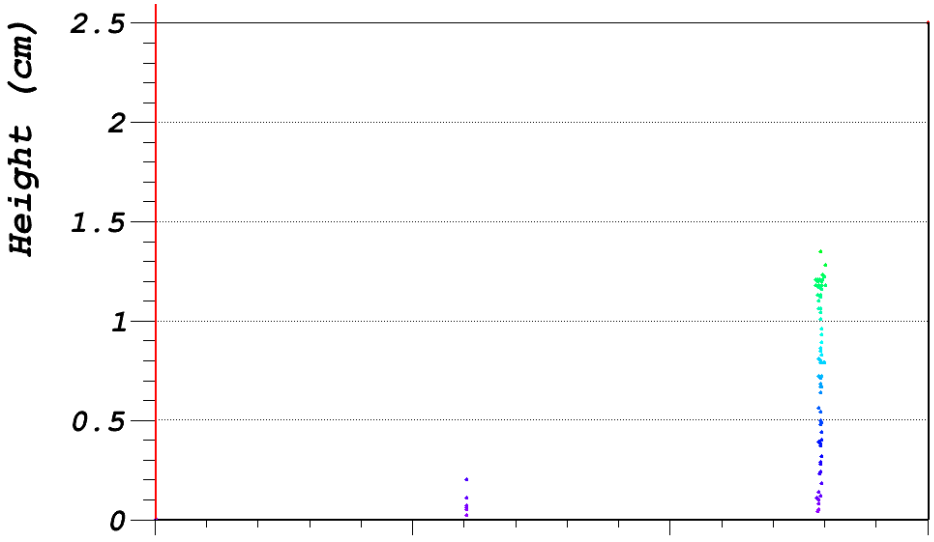


Figure 2.9. *Event recorded with two GridPix detectors, with* 1 mm *(left) and* 1.9 cm *(right) drift height respectively. With such a small number of primaries detected in the left case, it is difficult to perform a good track reconstruction.*

[3]In more complex applications one might want to record the length of the signal (Time over Threshold (ToT)) or its moment of arrival (Time of Arrival (ToA)). In those cases the output of the discriminator has to be a linear function of the input pulse.

In particular, the resolution of GridPix is degraded by several factors:

- diffusion, both in the x-y plane of the readout chip and in the perpendicular z direction;
- time resolution, since it directly affects the reconstruction of the z point of production of the electron;
- pixel size, which affects the resolution in the x-y plane;
- timewalk.

In this thesis we will focus on improving the resolution by means of improving the pixel chip used as readout for a GridPix detector. In particular, to increase the resolution in the z direction it is necessary to have available a high time resolution, down to a nanosecond to be able to reconstruct with high precision the production point of an electron in the drift volume. Having available such a readout chip will allow to reconstruct events like the one on the left in figure 2.9 with good precision.

There are different approaches available to reach such resolution, but it is important to point out the principal constraints that must be taken into account to decide which solution is best for the design of a pixel chip.

- Area: the circuit must fit in a relatively small area, since what is needed is a per pixel high resolution time measurement. Hence the pixel should be kept as small as possible to not degrade the x-y resolution but large enough to contain all the required logic;
- power consumption: due to high occupancy in some tracking applications, a big portion of the chip might be active at the same time; it is then fundamental to keep the power consumption at reasonable levels. Moreover, low power consumption means less cooling requirements which in turn means less material in the detector and thus leads to a better spatial resolution.

2.5 High precision time measurements

There are a number of techniques available to measure time intervals per pulse duration with integrated circuits with high precision ([52], [53]) and each one of them has its own advantages and disadvantages. We are specifically interested in obtaining a nanosecond resolution with a relatively long dynamic range in the order of hundreds of microseconds; the former for tracking applications, the latter for large TPC applications similar to the one proposed for the International Linear Collider (ILC). For the purpose of this work, the main features to take into

account to decide which method is better are the area occupied and the power budget.

A first distinction that can be made when talking about time measurements is the type of measure performed: absolute or relative. In an absolute time measurement the moment of detection of the signal is timestamped using a system wide clock which is sent to all the Time to Digital Converters (TDCs). In a relative time measurement the arrival time is instead measured with respect to a fixed signal (usually a common stop) that is sent at a known time.

Additionally, one can differentiate between analog and digital methods, even though a digitization of the time interval measured occurs also in some analog methods to simplify the readout. In general, analog methods are based on current integration while digital methods are based on a counting principle. A brief review of some common solutions will be presented in the following paragraphs, highlighting in particular the methods suited for a future implementation in a pixel chip.

2.5.1 Ramp interpolate

A simple analog method to measure a time interval involves the use of a capacitor. The capacitor is initially discharged at zero Volt and it is charged with a constant current I_0 when the start event occurs until the stop arrives. The applied constant current causes the voltage across the capacitor to linearly increase to the value V_f. When the charging process is completed, V_f can be measured using an Analog to Digital (ADC) converter.

Alternatively, when the capacitor has reached V_f, it can be discharged linearly to the initial state: a clock starts at the beginning of the discharge process and stops when the capacitor is back to initial conditions.

Using a capacitor one can obtain a very high precision (down picoseconds) but it is not easy to implement in a chip. The technology is very good in reproducing a ratio between components, but cannot guarantee good reproducibility in obtaining an absolute value; the spread between different channels would then be too high to obtain reliable measurements. Moreover, a capacitor of the size needed to achieve a good dynamic range would be impractical to implement in a pixel chip due to the small area available.

2.5.2 Vernier line

The Vernier method is a digital time stretching method. In its basic implementation it consists of two oscillators which oscillate at slightly different frequencies f_1 and f_2 (see figure 2.10). The first oscillator starts when the start signal arrives, while the second oscillator starts with the stop signal. A set of counters record

the number of clock cycles for each of the oscillators (n_1 and n_2) until the two oscillators are in phase and give a coincidence. The measured time interval T is then:

$$T = \frac{(n_1 - 1)}{f_1} - \frac{(n_2 - 1)}{f_2} \tag{2.21}$$

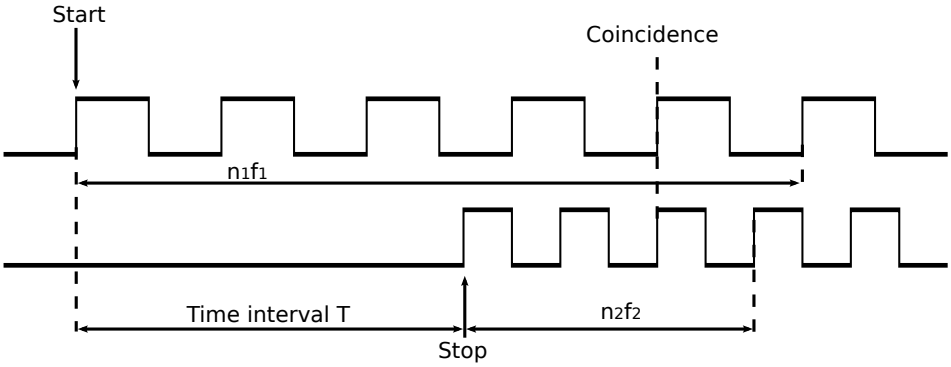


Figure 2.10. *Time diagram of the Vernier method: one oscillator is started by the start signal, while the other is started by the stop. The two oscillation frequencies are slightly different. The presence of a coincidence stop the counting of the clock cycles for both oscillators.*

The challenge when using this method is mainly to obtain good and reliable oscillators. Also of concern is the power consumption of the oscillator. Moreover, in view of an application in a pixel chip, it is straightforward to notice that this method would take a considerable amount of area (two oscillators per pixel).

2.5.3 Delay line

In general a delay line is made from a number of basic delay units which have delay τ. The start signal, propagating through the line, is delayed; when the stop signal arrives, the line is no longer active: the number of activated delay elements is recorded and it provides the desired time measurement. A simple implementation of this method is made with latches, as shown in figure 2.11. The start signal is propagated through the latches; when the stop arrives, the latches down the line "close", avoiding further delay of the start; the number of latches crossed by the initial signal is proportional to the time interval between start and stop.

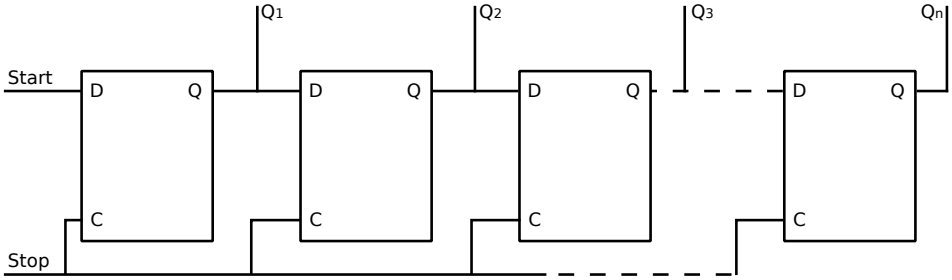


Figure 2.11. *Schematic of a delay line made of D latches. Each element has a characteristic delay τ. The start signal is propagated through the line until the stop signal arrives. The number of latches that reacted at the passage of the start is proportional to the time interval to measure between start and stop.*

The implementation of a delay line in an ASIC is possible [54], but the area requirements are too demanding for a per pixel TDC especially for the technology used in the present work in which a single latch takes roughly 1% of the pixel area. Moreover, the number of cells increases linearly with the range so this architecture is best implemented in applications that require a fast measure and have short range.

2.5.4 Counter method

Another digital method to measure time relies on an oscillator and a counter. The high frequency clock (hundreds of MHz) from the oscillator is transmitted to a counter from the start signal to the stop. The dynamic range can be very large, since it depends on the number of bits of the counter. The challenge, as in the case of the Vernier line, is the design of an accurate oscillator. It is possible to double the resolution of this method using two oscillators which start in opposition of phase (in this case, two counters are required) or it is also possible to use both the rising and falling edge of the high frequency clock if it has 50% duty cycle. This method, in both implementations, is anyway not suitable for pixel chip applications since the oscillator has to run for a very long time, increasing the power consumption. However, applying the Nutt technique to the counter method allow us to reach the required resolution while keeping the area and power consumption within the required specifications. This method is described in details below.

2.5.5 Counter method with Nutt technique

The demand for low power consumption and small pixel size are two important constraints which must be taken into account. In addition, a chip designed for tracking in a LHC-like environment should be capable of handling a high rate and should not have the functionality compromised by high occupancy events. For other applications, where the demands on pixel area or power consumption are less stringent, it is possible to reach a higher resolution [55].

In this work, the key component to achieve the objectives of low power and a small pixel area while measuring time with high precision is a fast oscillator that provides a clock with the desired frequency and a counter to record the number of oscillations. Unlike in a simple counting application, however, the oscillator runs only for a short amount of time; another counter, recording the clock cycles of a second, slower clock, is used to increase the dynamic range. This clock is not generated in the pixel; it is instead generated at the periphery of the chip or externally and it is then distributed across the entire pixel matrix.

When the input signal crosses a pre-defined threshold (figure 2.12) the oscillator is started and it will be stopped by the first rising edge of the system clock (in this work the system clock is always considered to be 40 MHz in view of LHC applications, unless otherwise noted). The number of oscillations that occur in this time is recorded by a counter (Fast counter). At this point, another counter is started, the Slow counter, which is then stopped when an external Trigger (common stop) arrives, synchronous to the reference clock: in this way, combining the information obtained from the Fast and the Slow counter together, we can compute the Time of Arrival (ToA) as shown in equation 2.22.

$$\mathrm{ToA} = \left(\frac{n_{fast}}{f_{fast}} + \frac{n_{slow}}{f_{slow}}\right) \tag{2.22}$$

The combination of the information obtained by two counters running at different frequencies is known as Nutt technique [56]. This solution is implemented in the design of the chips discussed in this thesis (GOSSIPO-3 and GOSSIPO-4). In this case an early arrival of the hit implies a high ToA value.

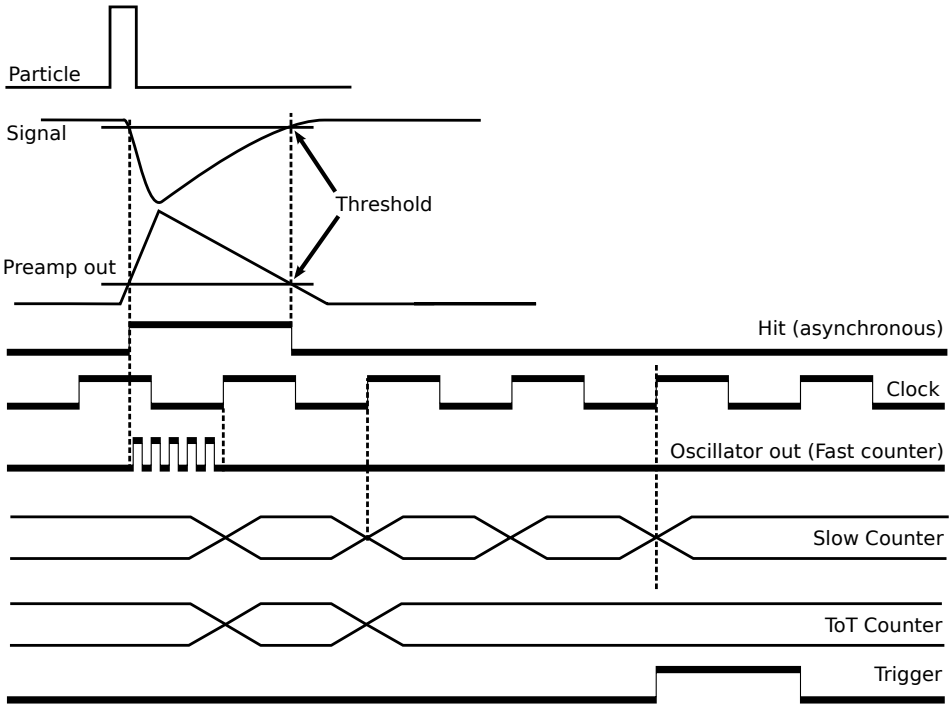


Figure 2.12. *Timing diagram that illustrates the chosen way to measure time. When the signal crosses an externally set threshold the fast oscillator starts and is stopped by the first rising edge of the system clock. The number of oscillations is recorded with a counter. Another counter records the number of system clock cycles until an external Trigger (stop) arrives. The combined information from these two counters gives the Time of Arrival with respect to the common stop signal.*

Chapter 3

Prototype TDC: Gossipo-3

3.1 Introduction

As described in section 2.1 the GridPix detectors developed so far have limited resolution in the time or z direction due to the maximum frequency available (100 MHz) in Timepix chips. To overcome this limitation the design and test of a series of prototype chips called GOSSIPO was started at Nikhef in 2004. The main goal was the design of a per pixel, low power, high resolution Time to Digital Converter (TDC) to improve the performance of GridPix detectors with a small drift gap (1 mm to 2 mm) called GOSSIPs. The prototypes were named GOSSIPO which stands for Gas On Slim Silicon Pixel where the O indicates that we are talking about a prototype chip for GOSSIP detectors.

In 2010, CERN, Nikhef and Bonn University started together the design of Timepix3, the successor of Timepix. Timepix3 includes a high resolution TDC per pixel with a nominal resolution of 1.5625 ns. The chip has been taped out in July 2013 and it is described in section 5.2.

This chapter introduces the design and the most important simulation results of GOSSIPO-3 in section 3.3. Before describing the developed Data Acquisition software in section 3.6 and the measurements results with 10 prototype chips in section 3.7 a generic description of analog to digital converters and the quantities used to characterize them will be given.

3.2 GOSSIPO chips: overview

It is well known that, in particular for small signals, the Time of Arrival (ToA) measurement is affected by timewalk [57]. A signal is detected by the pixel if it crosses the threshold set in that pixel. The crossing point of signals arriving

at the same time is influenced by the magnitude of the signal: a large signal will cross the threshold before a small one (see figure 3.1). Having information on the magnitude, for instance from a Time over Threshold (ToT) measurement would allow to correct the measured ToA [44]. Thus, the GOSSIPO prototypes where designed to measure the ToA with nanosecond resolution but at the same time record the ToT.

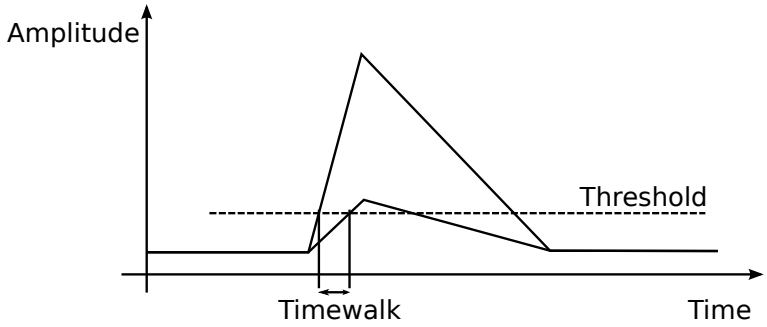


Figure 3.1. *Example of timewalk. Both the signals arrive at the same time, but the smaller one is detected later than the larger one.*

In the past years three prototype pixel chips have been designed and tested. The first prototype chip was built in 2005 to test an improved preamplifier with a discriminator. GOSSIPO-1 demonstrated that the analog input is not sensitive to input switching noise thanks to the use of the triple wells in the design, which permit isolation of the input transistor from the bulk [58].

The second prototype chip, GOSSIPO-2, developed during 2006-2007, features a 16×16 matrix of pixels [59]. Every pixel contains a 4 bit TDC with a resolution of 1.6 ns, a 4 bit system clock counter (40 MHz) and a DAC for threshold tuning. The chip has a serial readout and in addition at the input of the Charge Sensitive Amplifier (CSA) there is a protection circuit against high voltage breakdown in view of the possibility to add an InGrid to build a working detector. Even though the main functionality of the chip has proven to behave according to the design specifications, the TDC characteristic showed a discontinuity when the hit signal is detected close to the leading edge of the system clock as shown in figure 3.2. Despite this bug in the design, a GOSSIPO-2 chip has been used to build a GridPix detector with a drift gap of 1.3 mm and with a total active volume of 1 mm^3 of gas. The detector performed remarkably well and reached a resolution of 10 µm in XY direction and 28 µm in the z direction [60] for a track with 6 hits.

GOSSIPO-3 is the third prototype chip developed in collaboration between Nikhef and Bonn University for the readout of gas detectors such as a large

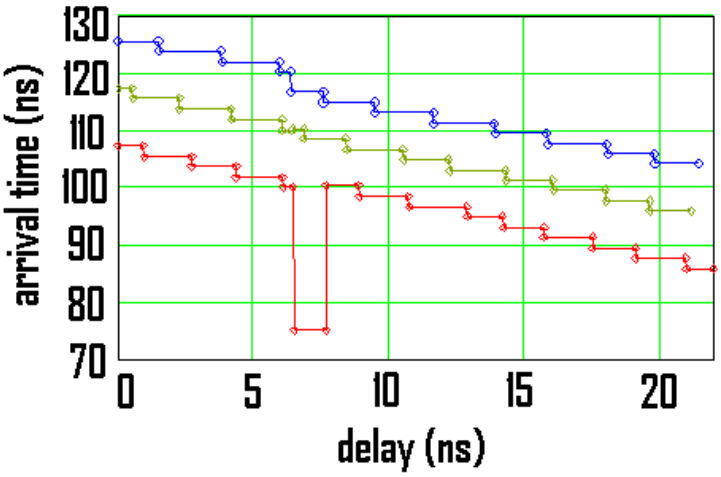


Figure 3.2. *GOSSIPO-2 TDC characteristic. The discontinuity is clearly visible. The three different curves have been taken at different power supply voltages (1.1, 1.2 and 1.3 V from top to bottom).*

Time Projection Chamber (TPC) or a Micro Pattern Gas Detector (MPGD). The main reason for the design and production of the GOSSIPO-3 test chip was the necessity to prove the functionality of several blocks: the high frequency local oscillator, the analog frontend, the new on pixel digital logic, designed in particular to address the problems shown by GOSSIPO-2, and two different types of Low Drop Out regulators. GOSSIPO-3 is designed in a commercial 130 nm technology using 8 metal layers; the bottom 5 metal layers are used for the local routing while the top layers are used for shielding and to distribute the test signals, power and ground. The two pixels present in the chip have a size of 60 µm × 60 µm. Figure 3.3 shows a picture of the chip before wire bonding.

Since the main functionality of the chip was already designed, the main focus of this work has been on the physical implementation and the testing of the pixel functionality.

3.3 Single pixel logic: design and simulations

Figure 3.4 shows the block diagram of a GOSSIPO-3 pixel. The main features are the presence of an oscillator (580 MHz) in every pixel and the Finite State Machine that controls the digital logic. In GOSSIPO-3 there are several control signals and configuration bits that must be provided by the user: Token, Trigger

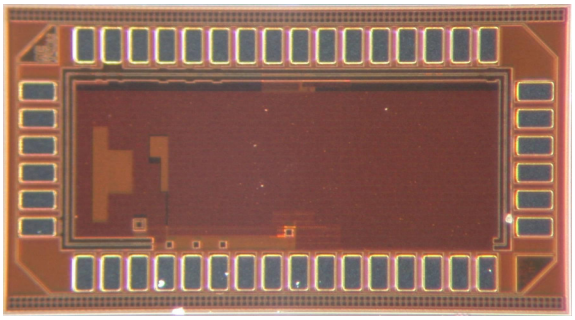


Figure 3.3. *Picture of GOSSIPO-3. The chip has an area of* 3 mm *by* 1 mm.

and Reset to control the data taking and readout phases and the 4 bits DAC used to correct for mismatch in the threshold (see section 3.3.1). In the following paragraphs a brief description of the various blocks will be given together with the main simulations results.

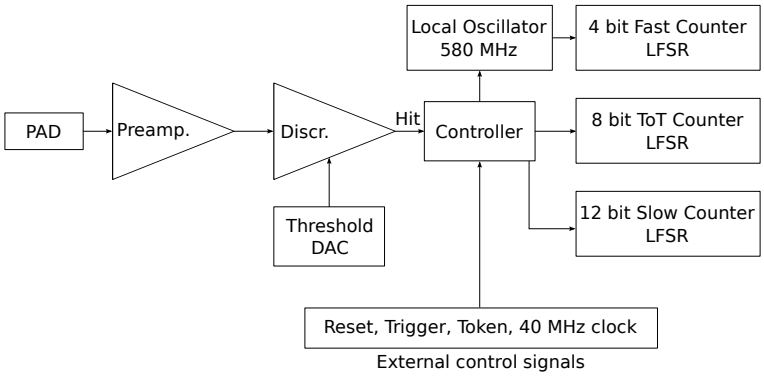


Figure 3.4. *Single pixel block diagram of GOSSIPO-3. The oscillator and the Finite State Machine that controls the pixel digital logic are present in every pixel.*

3.3.1 Analog frontend

One aspect of MPGDs is that there is no silicon sensor bonded to the readout chip, resulting in a much smaller detector capacitance. This characteristic allows the design of a high gain, low power, low noise frontend circuit.

The sources of the input capacitance are (see figure 3.5):

- pad-grid capacitance (detector capacitance);

- pad-pad capacitance;
- parasitic capacitances.

The sum of these capacitances is usually between 5 fF and 30 fF [58].

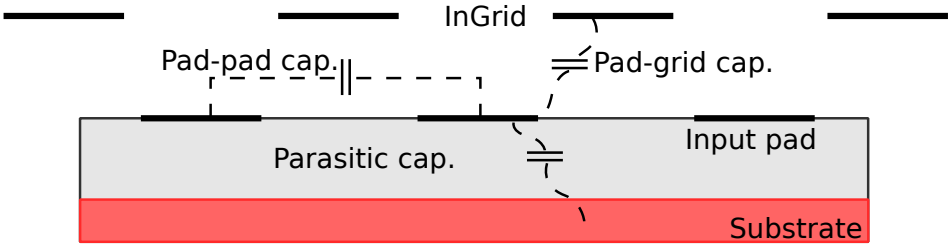


Figure 3.5. *Schematic representation of the main sources of the parasitic input capacitance for GOSSIPO-3. The pad to grid capacitance (detector capacitance) is much lower than the capacitance of a silicon sensor.*

The schematic of the frontend can be seen in figure 3.6. On the left there is the input pad that collects the charge coming from the detector and the input for the external test pulse. In the center is shown the preamplifier (OpAmp) with the feedback transistor T_{fb} and the feedback capacitance C_{fb} while on the right the discriminator with the threshold input is shown.

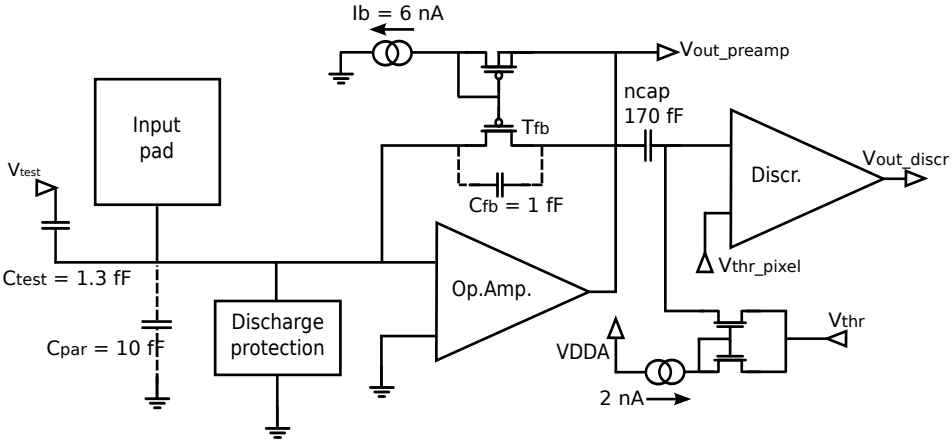


Figure 3.6. *Schematic diagram of the frontend circuit used in GOSSIPO-3. The values of the parasitic, input and feedback capacitances are extracted from simulations.*

Figure 3.7 shows the ideal response of the preamplifier. The rise time requirement of less than 25 ns is driven by the eventual application in one of the upgraded LHC detectors and it is limited by the finite bandwidth of the amplifier. Since the chip is built to measure time with high precision, the preamplifier output should cross the threshold as fast as possible to minimize the uncertainty in the arrival time. The falling edge is composed of two parts: a linear decay and an exponential one. This behavior can be understood looking at the feedback transistor T_{fb}: when the voltage across the transistor is large, T_{fb} works in its saturation region, where the current is virtually independent of the voltage and the slope of the curve in figure 3.7 is described by $-t * \frac{I_{sat}}{C_{fb}}$. When the voltage becomes smaller the transistor operates in the triode regime, where the current depends exponentially on the voltage; the resulting RC-circuit is then described by $exp(\frac{-t}{C_{fb}R_{on}})$.

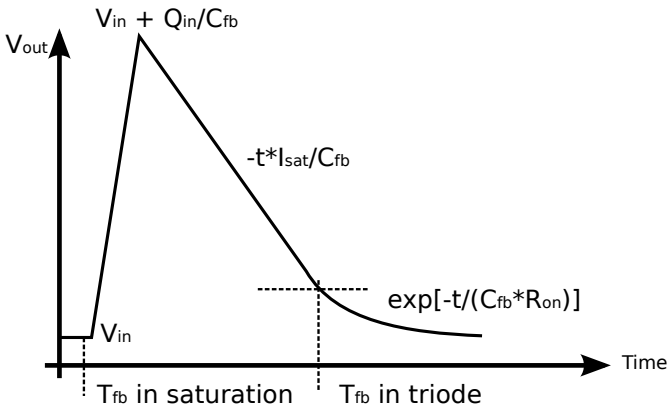


Figure 3.7. *Ideal response of the preamplifier to an input signal. The rising edge must be fast, to minimize the uncertainty in the measured arrival time. The falling edge has two components: a linear decay, when the feedback transistor is operating in the saturation region, and an exponential decay, when the transistor works in the triode regime.*

The schematic of the preamplifier is shown in figure 3.8. It is possible to estimate the noise in the preamplifier by performing a simple calculation, considering that the important transistor for this purpose is only T1.

Assuming that all the noise comes from this transistor and using the formula discussed in [61], one obtains for the equivalent noise charge (ENC):

$$\mathrm{ENC}^2 = \gamma kT(C_d + C_f)\frac{C_f}{C_l} = 9.6 \times 10^{-36}\,\mathrm{s}^2\,\mathrm{A}^2 \tag{3.1}$$

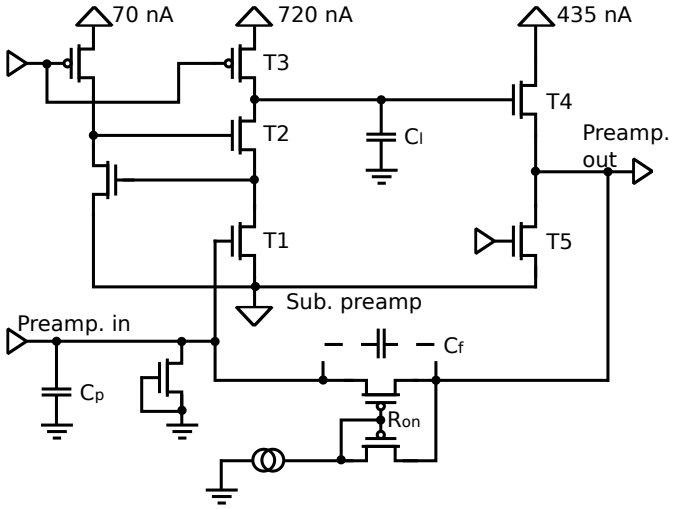


Figure 3.8. *Schematic of the preamplifier.*

where γ is the noise factor of the transconductor and it usually ranges from 1/2 to 1 (assumed 1 for this calculation), k is the Boltzmann constant, T is the absolute temperature, $C_d = 15 \times 10^{-15}$ F is the detector capacitance, $C_f = 1 \times 10^{-15}$ F is the feedback capacitance and $C_l = 6.5 \times 10^{-15}$ F is the load capacitance. From formula 3.1 one obtains a noise level of 20 e^-. The result is compatible with simulations which also show that for the frontend the channel-to-channel threshold dispersion is $\sigma = 70$ e^-, and can be reduced with a 4 bits per-pixel DAC to $\sigma = 5$ e^- after equalization. The power consumption is 3 µW per channel.

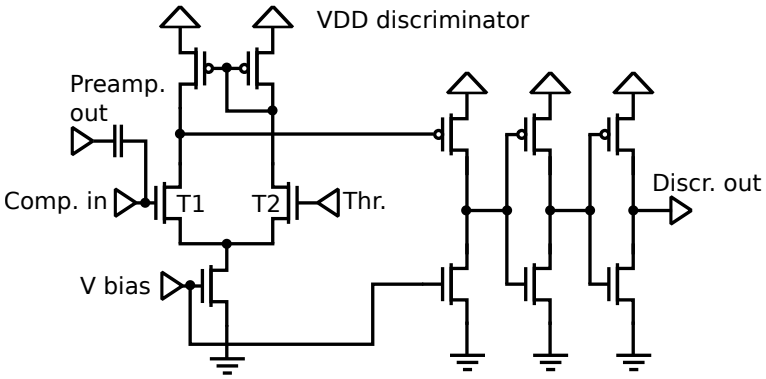


Figure 3.9. *Schematic of the discriminator.*

Figure 3.9 shows the schematic of the discriminator. The circuit has two main parts: the "real" discriminator block (on the left) and a series of inverters at the output that act both as buffers and shapers for the signal. The specification of the circuit is that the delay variation of the signal for different channels at the output due to process variations has to be less than 1 bin of the TDC for all signals (big or small). In addition, the behavior of the circuit should not be temperature or supply voltage dependent. Simulations confirm that the circuit meets the requirements.

3.3.2 Oscillator

To achieve high resolution time measurements, while keeping the power consumption low, it was decided to use an oscillator which is only running for a short time and couple it to a slow system clock to keep a large dynamic range. The solution is implemented by starting the oscillator when the hit arrives until the first rising edge of the system clock. Hence the oscillator will be active for a maximum of 25 ns, considering that we are using a 40 MHz system clock. The choices of the oscillation frequency and of the number of bits of the counter are related; on one hand a nanosecond resolution is needed, on the other hand the area occupied must be minimal. The solution is a 4 bits Linear Feedback Shift Register (LFSR) which has 15 states available (see section 3.3.4). Dividing the system clock period in 15 time bins provides the resolution of 1.724 ns (580 MHz) except for the first bin which is designed to have half the width with respect to the others ($1.724 \cdot 10 + 0.862 = 25$ ns).

The local oscillator of GOSSIPO-3 consists of a NAND gate with a chain of nine inverters in the feedback loop (see figure 3.10).

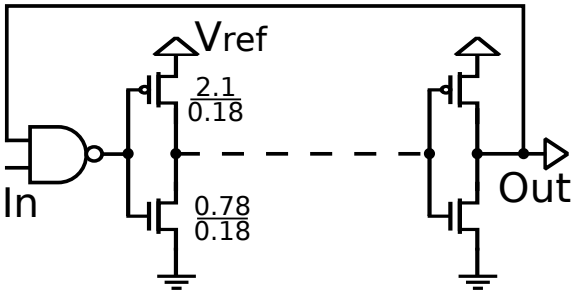
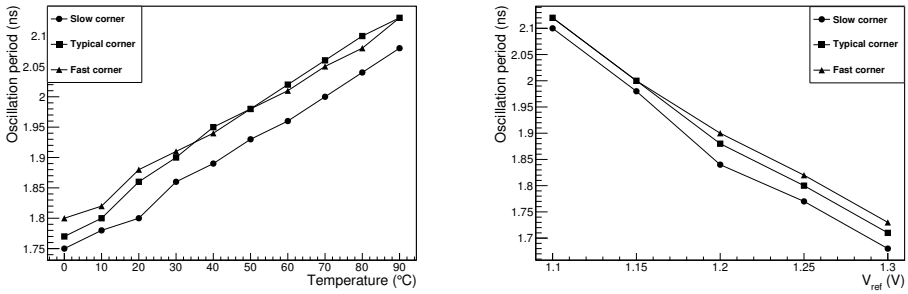


Figure 3.10. *Schematic of the oscillator used in GOSSIPO-3. It is the delay of the feedback chain made of nine inverters that determines the oscillation frequency. The transistor dimensions W/L are given in µm.*

The oscillation frequency can be controlled via V_{ref} with a sensitivity of about

0.12 %/mV as shown in figure 3.11 by the simulation results. Moreover the frequency depends on the temperature with a proportional effect on the period of about 0.2 %/ °C. The current consumption of an active oscillator is less than 100 µA. For a full size chip (256 × 256 pixels) that has to work in a LHC-like environment a maximum occupancy of 440 pixels is foreseen. Thus the maximum current consumption is 44 mA (see section 3.3.3 for more details).



(a) (b)

Figure 3.11. *Simulation results of the effect of temperature (a) and supply voltage (b) variation on the oscillation period for the oscillator used in GOSSIPO-3. The different curves are for different process corners and show a spread of about 4%.*

Variations in the behavior of the oscillator are due not only to variations in temperature or power supply but are also due to process variations during the fabrication of the ASICs. Simulations show that the frequency for ASICs produced in the fast corner of the process can be up to double the frequency for an ASIC produced in the slow corner. These variations can be compensated tuning V_{ref}. The optimal oscillation frequency can be reached for all the process corners if the supply of the oscillator can be tuned between 0.6 V to 1.1 V. To compensate for variations caused by these effects it has been decided to introduce a Low Drop Out regulator (see section 3.3.3).

3.3.3 Low Drop Out regulators

As explained in section 3.3.2 an important effect that can change the oscillation frequency from chip to chip is the variation due to the different process corners, which is unavoidable, but can be taken into account during the design phase by introducing a tunable on-chip circuit that allows to correct for those variations.

Therefore two different Low Drop Out regulators (LDO, variable voltage sources) one called Large and one Small have been designed to supply the needed voltage to the oscillators [62]. The specifications for the circuit come from the environment where a full size chip implementing a GOSSIPO-3 like TDC has to operate. The Low Drop Out (LDO) has to be capable of delivering a current $I = 100\,\mu A \cdot N_0$, where N_0 is the average number of oscillators active at the same time. When operated in a LHC-like environment this number is proportional to the number of traversing particles and varies per bunch crossing. For the implementation one has to consider the average occupancy and then use a safety margin. Considering 12 tracks/cm^2 per bunch crossing gives an average of 24 tracks per chip. Assuming every track releases 9 primaries, the number of active pixels would be roughly 220, which gives a current consumption of 22 mA. With a safety factor of two, the current consumption would be 44 mA. However, the oscillator typically is only on for half of the time on average, reducing the current consumption of another factor two.

A simplified schematic of the LDO circuit is shown in figure 3.12.

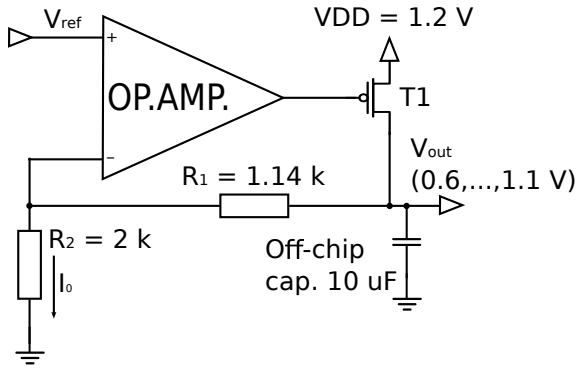


Figure 3.12. *Simplified schematic of the LDO regulators used in GOSSIPO-3. The circuit generates a reference voltage used by the oscillator, and it is used to compensate for variations introduced by process variations.*

The two components of the circuit are the operational amplifier (OpAmp) and the pass PMOS transistor (T1). The OpAmp guarantees that V_{ref} and the voltage at the inverting input are the same, so that $V_{ref} = I_0 \cdot R_2$. Moreover, in an ideal OpAmp no current is flowing from or to its inputs. Hence the feedback current defines then the output voltage: $V_{out} = I_0 \cdot (R_1 + R_2)$. Solving the two equations for I_0 gives:

$$V_{out} = V_{ref}(1 + \frac{R_1}{R_2}) \tag{3.2}$$

The generated voltage V_{out} is supplied to all oscillators in the chip (one per pixel). If the load connected to the output of the circuit changes, the OpAmp will change accordingly the voltage at the gate of the pass transistor, which in turn will adjust the current flow to compensate for the variation. The circuit generates the oscillator voltage with a dynamic range which depends on the power supply. For VDD = 1.2 V the dynamic range is 0.6 to 1.1 V; in general, the maximum power supply available at the output of the LDO is roughly VDD - 100 mV, due to the drop caused by the pass PMOS transistor.

The current drained by the load connected to the LDO is provided by the pass transistor, which always works in saturation. Using the 130 nm IBM CMOS8RF process data, it is possible to calculate the size of the transistor channel[1] as

$$I_D = \frac{1}{2}\mu_{hole} C_{ox} \frac{W}{L} V_{DSSat}^2 \tag{3.3}$$

Assuming I_D = 44 mA and V_{DS} = 100 mV and with the process parameters being $\mu_{hole} = 4.5 \times 10^{10}\,\mu m^2\,V^{-1}\,s^{-1}$ and $C_{ox} = 2\,fF\,\mu m^{-2}$ this leads to:

$$\frac{W}{L} = 10^5 \tag{3.4}$$

Choosing a transistor which has twice the minimum size L = 480 nm gives W = 48 mm. A transistor of this size introduces a very large capacitance between the gate and the source (C_{gs}) of about 300 fF which must be added to the routing net capacitance (200 fF). Due to this big load that has to be driven by the LDO an external off chip capacitor of 10 µF is needed to stabilize the circuit.

In GOSSIPO-3 there are two of these LDOs: one with the calculated transistor size (called Large) and one with W = 2 mm (called Small); this last LDO delivers less current, but occupies less area. The Small LDO should be sufficient to guarantee a stable output voltage considering that the oscillators are running for a maximum of 25 ns and after that they are off for a relatively long time (several clock cycles). On the other hand this presents limitations on using a full size chip in a high occupancy environment since hits might be lost.

3.3.4 Counters

GOSSIPO-3 pixel features three counters called Fast (4 bit), Slow (12 bit) and Time over Threshold (ToT, 8 bit). The first two counters are used in combination

[1] I_D is the drain current, μ_{hole} is the hole mobility, C_{ox} is the oxide capacitance, V_{DS} is the voltage between drain and source.

to measure the drift time or ToA of the electrons. The last one is used to record the time spent by the signal over threshold and obtain information about the size of the avalanche generated in the amplification region of the detector. The counters are Linear Feedback Shift Register (LFSR) with maximum number of states available for counting.

A LFSR is a particular type of shift register in which the current state determines the value of the bit that will be used as input in the next state. An advantage of using LFSRs is that they can be implemented with a minimum amount of logic, namely flip-flops and a few exclusive-OR gates (XOR), and hence minimize area consumption. LFSRs are used in different applications as counters, as pseudo-random number generators [63][2] or in test pattern generation.

A feature that comes with LFSRs is the number of states available: in general, a n-bits counter has 2^n states available in the counting sequence. A LFSR has a maximum of $2^n - 1$, because of the presence of a forbidden state[3] (the all-zero or the all-one state, depending on the implementation). If the counter was to enter in such a state, it would stay there indefinitely.

The bits that determine the next input bit of the LFSR are called taps: the taps are XOR-ed (or XNOR-ed, the main difference being the forbidden state) together and fed back to the LSB[4]. LFSRs can be described by a polynomial with all the coefficients that are either 0 or 1 and with a maximum grade equal to the number of bits in the LFSR. The terms with coefficient 1 are the taps of the register.

Consider for example a 4-bits LFSR: it is possible to describe it using either the primitive polynomial 3.5 or 3.6:

$$P(x) = x^4 + x^3 + 1 \tag{3.5}$$

$$P(x) = x^4 + x + 1 \tag{3.6}$$

The only difference between the two implementations is the state sequence. The terms that appear in the equations give the bit to be used as tap (4 and 3 in first case, 4 and 1 in the second). Figure 3.13 shows the schematic of the counter described by equation 3.5 which is also the LFSR used in GOSSIPO-3.

[2]The generated pattern has good pseudo-random characteristics such as long period and uniformly distributed output stream.

[3]$2^n - 1$ is the maximum count achievable by an LFSR; depending on the feedback, the number of states available might be smaller.

[4]Least Significant Bit.

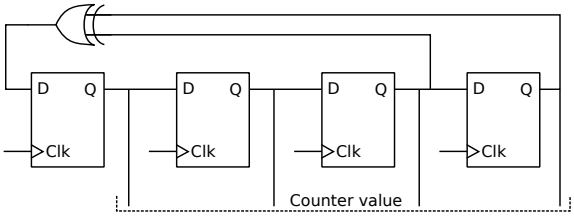


Figure 3.13. *Schematic of the 4 bits LFSR described by equation 3.5. This is the LFSR used as Fast counter in GOSSIPO-3.*

The size of the counters used in GOSSIPO-3 is defined by specifications; for large TPC applications a big dynamic range is required, hence a 12 bits Slow counter, corresponding to a range of 102.4 µs at 40 MHz. For most GridPix applications a long dynamic range in ToA measurements is not required but high resolution is the key factor. In case of the ToT counter, the frontend shows a linear response to an input charge up to 22000 electrons. This translates into a 3 µs long signal which for a 25 ns clock period implies a counter of at least 7 bits. The final choice is an 8 bits counter to accommodate extremely long signals [64].

3.3.5 Controller

GOSSIPO-3 is either running in the data taking phase or in the readout phase. This is the result of a serial readout regime in which the counters are reconfigured to act as shift registers. This design reduces the area occupied by the logic at the cost of an increased readout dead time of the pixel. Moreover, in a prototype chip like GOSSIPO-3 it is not necessary to have a sophisticated readout, since the main goal is the testing of the TDC. To control the data taking and readout phases a Finite State Machine (FSM) has been designed as shown in figure 3.14.

In the ToA mode the pixel records the ToA of the signal and makes use of the oscillator. After being reset, the FSM enters in the Standby state S1 and the pixel is ready to receive a hit. When the signal crosses the threshold the oscillator starts and it stops at the first rising edge of the 40 MHz clock. The number of oscillations is counted by the Fast counter. When the oscillator and hence the Fast counter stops, the ToT and the ToA counters are enabled (state S2.0). The ToT records the number of clock cycles until the signal falls below threshold. At this point the ToT counter stops while the Slow counter keeps counting (state S2.1) until it is stopped by the arrival of the trigger (common stop). Notice that if the trigger arrives while the signal is still over threshold the counters are both stopped and the FSM switches into the waiting state S3. In this

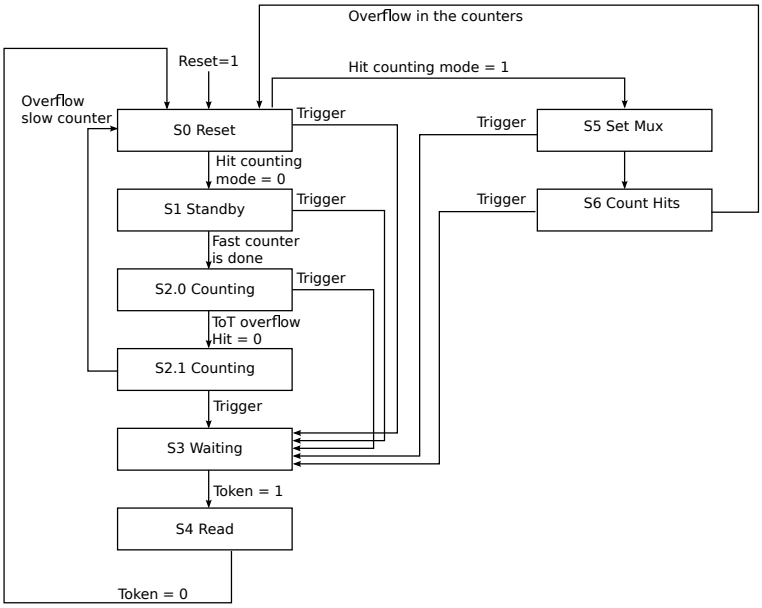


Figure 3.14. *Block diagram of the Moore FSM implemented in GOSSIPO-3.*

state, the counters are configured to act as shift registers and the 40 MHz clock is now sent to the fast counter via a multiplexer that selects between the oscillator output and the system clock. The token signal starts the shifting operations (state S4). The two pixels are chained together, and the token has to be 48 clock cycles long to allow a full readout. After readout the FSM automatically resets to state S0, clearing the content of the counters and preparing the pixel for the next acquisition. The logic designed and implemented in this way in the pixel allows to record only one event at the time. If multiple hits arrive on the same pixel while taking data in ToA mode only the first one is detected.

The second operation mode is the hit counting mode: in this case the counters are configured to count the number of hits that arrive in a certain time window. The counters are chained together (state S5) such that the Fast counter provides the LSBs of the counting sequence: when the fast counter reaches its maximum it produces an overflow signal; the ToT counter value is then increased by one. The same happens with the slow counter when the ToT reaches the overflow condition (state S6 count hits). In this way the amount of hits recorded can be computed with the following formula: Fast + (ToT $\cdot$ 15) + (Slow $\cdot$ 255 $\cdot$ 15). Mode selection is achieved by setting one external configuration bit: this will configure the FSM accordingly. The time window length is again defined by the arrival of the trigger, which moves the FSM to the S3 waiting state; from there readout

operations proceed in the same manner as in the ToA mode.

3.4 Converter characterization

This thesis is about Time to Digital Converter (TDC). However, most quantities relevant for TDCs are the same for Analog to Digital converters (ADC). In the following paragraphs, a brief overview of the most important parameters in the characterization of a generic analog to digital (A/D) converter will be presented before introducing the test setup and the measurement results.

A generic A/D converter is a device that takes as input an analog value and returns as output a digital code. The main result of this operation is that an interval of analog values will be mapped on the same digital output code; this interval of analog values is called bin. In the ideal case all bins of a converter should have the same length and there should be a sharp demarcation between two consecutive bins (i.e.: a region where the converter outputs two different but consecutive digital codes for the same input value). For a real circuit, the characterization of this demarcation describes the quality of the converter.

3.4.1 Differential Non Linearity

The Differential Non Linearity (DNL) is a measure of the deviation from the ideal characteristic curve (figure 3.15). The term Differential refers to the fact that the DNL is defined as the difference between the measured length of one bin of the converter and the theoretical value it should have in the ideal case.

Equation 3.7 shows how to calculate the single bin DNL:

$$\mathrm{DNL}_i = \frac{bin_i - IB}{IB} \tag{3.7}$$

The only quantity that is needed is the size of all the bins of the converter (bin_i), which comes from the measurements, and the size of the ideal bin (IB), which is given as design specification and is defined as the dynamic range divided by 2^N where N is the number of bits of the converter. With this definition the DNL can be positive or negative if the measured bin size is bigger or smaller than the ideal bin size respectively. Moreover, $DNL = -1$ signals that there is a missing code in the sequence. In practice, when quoting a number for the DNL of a converter the biggest DNL_i, in absolute value, is chosen.

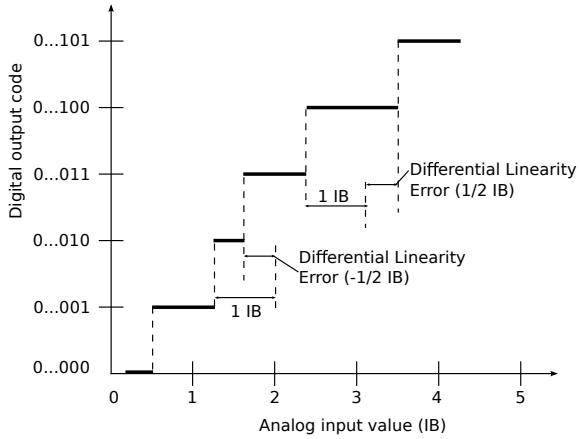


Figure 3.15. *Graphical illustration of Differential Non Linearity in a general converter. The analog input can be any quantity that needs to be discretized (voltage, time).*

3.4.2 Integral Non Linearity

The Integral Non Linearity (INL) of a converter is a quantity that describes the deviation of its characteristic curve from an ideal straight line. The name Integral comes from the fact that it is calculated taking the maximum deviation given by the sum of all the DNLs up to a certain bin (see figure 3.16).

The INL can be calculated in different ways yielding different results. The best straight line method (or independent linearity) describes the deviation of the characteristic curve of the converter with respect to the line that minimizes such deviation. This is the most flexible way to extract INL since there is no constraint on where the ideal line should be and yields the lowest INL value. Other methods, instead, put constraints on the starting point of the line (zero based linearity) or on both the starting and end point (terminal linearity). Having more constraints, these latter methods yield bigger values for the INL. Last, it is possible to further modify the terminal linearity introducing a correction for the Gain and Offset errors, which are static errors and can be corrected for (see sections 3.4.3 and 3.4.4). In practice, equation 3.8 defines the INL (best straight line method) as it is used in this thesis:

$$INL = Max[\sum_{m=0}^{j} DNL_m]_{j=1...N} \tag{3.8}$$

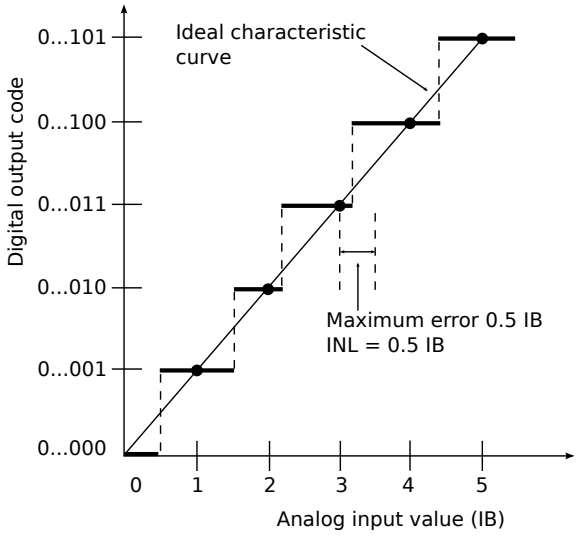


Figure 3.16. *Integral Non Linearity.*

3.4.3 Offset error

The offset error (figure 3.17) is the difference between the nominal offset point and the measured one. This error affects all the codes in the same way, and it can be subtracted from the measured transfer function of the converter.

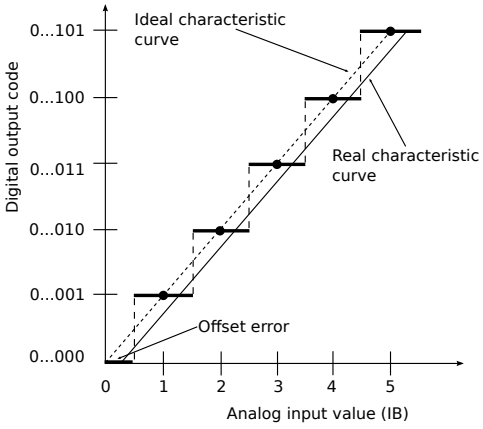


Figure 3.17. *Graphical example of the offset error: the measured characteristic (continuous line) does not start at the origin (ideal characteristic, dashed line).*

In some cases, an offset is introduced by design to adapt the characteristic curve of the converter to the requirements (see 3.4.4).

3.4.4 Quantization effects

Due to the discrete nature of an A/D converter, a small change in the input will not alter the digitized output. This introduces an error, commonly called quantization error, which increases with the increasing of the analog input, until the converter jumps to the next LSB and the error goes to zero again (the quantization error is then always included between zero and one). For converters with an offset of half LSB, the error is shifted between $-1/2$ and $+1/2$ (see figure 3.18) and the variance is $\frac{1}{\sqrt{12}}$.

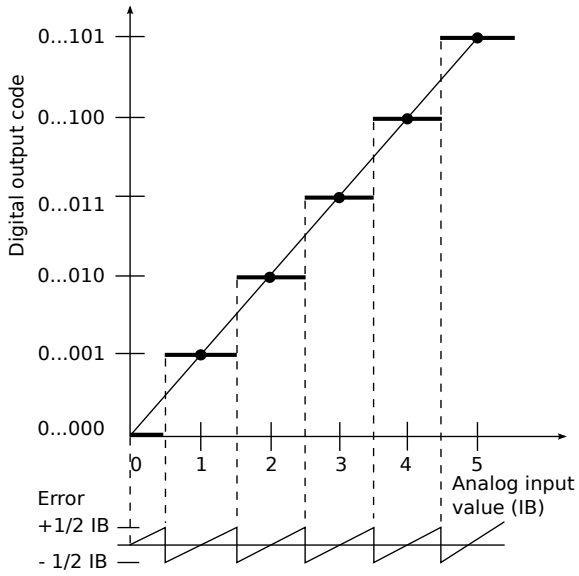


Figure 3.18. *Quantization error: for a converter with a predetermined offset, the error is between* $-1/2$ *and* $+1/2$.

3.5 Error function

In an ideal analog to digital converter the transition between two consecutive output codes is defined with infinite precision and the conversion happens then for a single analog value. In reality this is not the case; due to noise at the input, certain analog values will yield more than one output code. When measuring

time this fluctuation is called jitter. To characterize the transition regions the assumption that the jitter has a Gaussian distribution has been made. Under this assumption, the jitter can be characterized using the error function.

Consider a generic Gaussian distribution with maximum a centered around μ and with width $\sqrt{2}\sigma$:

$$G(x) = ae^{-\frac{(x-\mu)^2}{2\sigma^2}} \tag{3.9}$$

and define $f(x)$ as the integral from 0 to x (the factor $\frac{2}{\sqrt{\pi}}$ is introduced for normalization reasons):

$$f(x) = \frac{2}{\sqrt{\pi}} \int_0^x ae^{-\frac{(t-\mu)^2}{2\sigma^2}} dt \tag{3.10}$$

With the change of variable $t' = \frac{t-\mu}{\sqrt{2}\sigma}$ the formula becomes:

$$f(x) = \sqrt{2}a\sigma \frac{2}{\sqrt{\pi}} \int_{-\frac{\mu}{\sqrt{2}\sigma}}^{\frac{x-\mu}{\sqrt{2}\sigma}} e^{-t'^2} dt' = a \cdot erf[\frac{(x-\mu)}{\sqrt{2}\sigma}] \tag{3.11}$$

The last term of equation (3.11) is called error function and it describes the integral of the Gaussian. In this work, the function is used to characterize the transition regions between two consecutive bins of the TDC implemented in the chips that have been designed. A fit on that region using an error function returns four parameters of which the two important ones are:

- μ, which defines the boundary of the bin and is used to calculate the bin size;
- σ, which is the jitter.

3.6 Test environment

The block diagram of the complete test setup for GOSSIPO-3 can be seen in figure 3.19. The DAQ controls an Agilent 81110A pulse generator [65] which is used to generate the test pulse (Hit); some relevant parameters that can be set are the delay and width of the pulse, the number of pulses to send to the chip and the rise time of the hit. The jitter introduced by the generator is on the order of tens of picoseconds, so it is negligible for the scope of this work. The

DAQ also controls the communication with the S3 FPGA board and it can set the acquisition parameters like the trigger arrival or the number of acquisitions to perform. It also retrieves the data from the FPGA and writes them into a file after the readout of the chip. The DAQ software has been written in C++ using the Qt libraries [66] to create the GUI as shown in figure 3.20 .

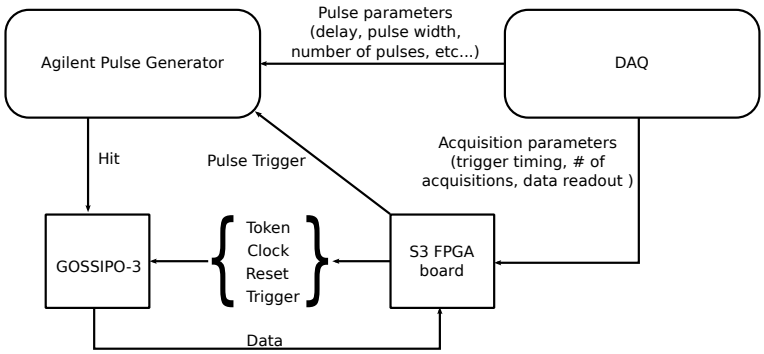


Figure 3.19. *Block diagram of the complete setup to test GOSSIPO-3. The DAQ controls the parameters of the pulse generator and the FPGA board. The FPGA, given the user defined parameters, sends the required signals to the chip and stores the data coming from it, data which are then readout by the DAQ.*

The S3 MultiIO board [67] has been provided by Bonn University and it is equipped with a Xilinx Spartan-3 FPGA [68]; other devices on the board are a Cypress USB controller and a clock generator. To interface the board to the external world, a wide range of I/O connectors is present: 6 LEMO plugs (3 inputs, 3 outputs), 4 LVDS (2 transmitters, 2 receivers), a Multi-I/O connector with 80 ports, JTAG, I^2C, SPI and a USB2.0 B-type interface. The board is powered either with an external 5 V supply or using the USB port which can be used also for the configuration of the FPGA instead of using JTAG. The firmware for the FPGA has been developed in Verilog using the Xilinx ISE 12.1 environment.

In figure 3.21 a block diagram of the firmware of the FPGA is presented: the USB_register module contains all the values that are set using the DAQ (time of arrival of the trigger, counting mode, DAC settings, number of acquisitions). These values are used by the Logic_Generator to provide the control signals to the chip (Token, Trigger, Reset) and the control signals for the external devices (Pulse Trigger). For the readout phase, the values are stored in an array created in the Readout module, and then moved to the USB_register, where they are ready to be readout by the the DAQ and saved into a file. Two additional modules are present; the first is the Digital Clock Manager (DCM), an IpCore

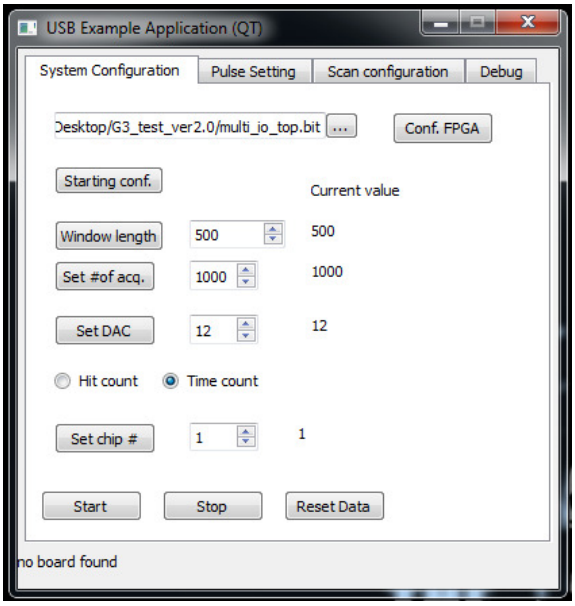


Figure 3.20. *The GUI developed to test GOSSIPO-3.*

available in ISE. This is used to generate the required 40 MHz clock from the input 24 MHz clock which is generated on the S3 board by the mentioned Cypress clock generator. The last module is used for debug/control purposes, to visualize the status of some control bits using the 5 LEDs on the board (start/stop of the acquisition, counting mode, locked clock).

3.7 Test results

All the results presented in the following sections have been obtained testing 10 chips with VDD = 1.2 V at room temperature.

3.7.1 Analog frontend

Pulse shape

Figure 3.22 shows on the left the simulated output signal of the preamplifier when an equivalent charge of 375 electrons is applied at the input. On the right, a picture taken with the oscilloscope of the preamplifier output: the same charge has been injected externally with a 46 mV test pulse. The measurement shows a

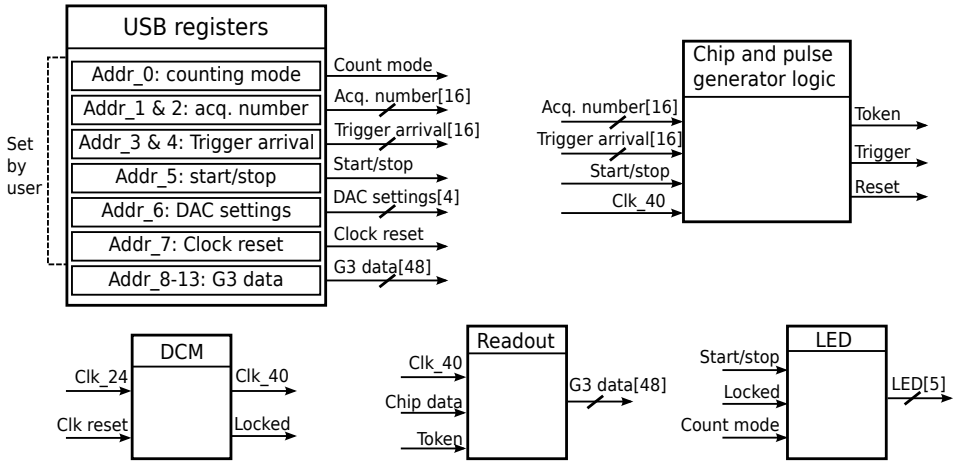
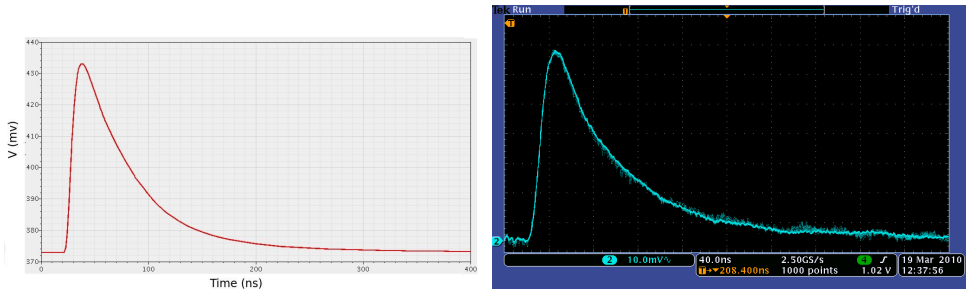


Figure 3.21. *Block diagram of the firmware used for testing GOSSIPO-3. The double arrow indicates a bus, with the bit size written in parenthesis, the single arrow is a single bit.*

good qualitative agreement with the simulations. The peaking time is less than 25 ns according to specifications.



(a) (b)

Figure 3.22. *On the left, simulation of the response of the preamplifier to an input charge of 375 electrons. On the right, measurement result of the response of the preamplifier to a pulse injecting the same charge.*

Noise

An important parameter to determine is the noise of the frontend. To do so the output signal of the preamplifier has been recorded 1000 times with an Agilent InfiniiVision DSO-X 3054A oscilloscope. The oscilloscope records a point on the waveform every 0.25 ns. For each oscilloscope time step the measurement results from the 1000 different waveforms recorded have been put in a histogram. An example of such a result for chip 2 is shown in figure 3.23. Every histogram has then been fitted with a Gaussian distribution, since the noise superimposed on the signal is Gaussian.

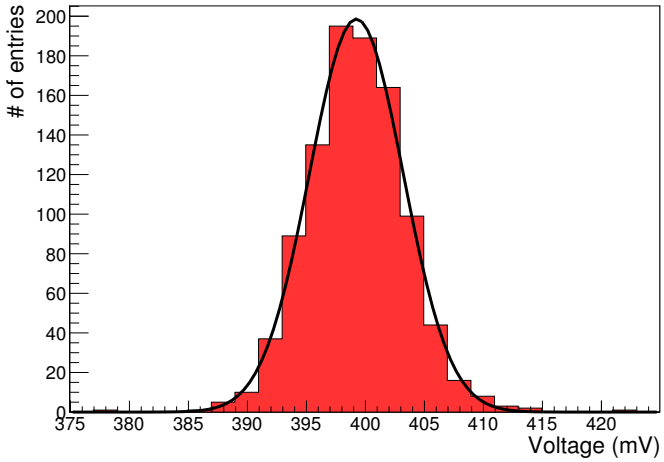


Figure 3.23. *1000 measurements with the same time step for one of the GOSSIPO-3 preamplifier.*

The widths of the distributions (σ) returned by the fits for all the time steps are then the inputs for a new histogram to be fitted again with a Gaussian distribution whose mean is the measured noise in millivolt, as shown in figure 3.25. The spurious results, i.e. the fits which give a $\sigma > 4.5\,\text{mV}$ are due to a second source of noise identified in the input transistor dynamic behavior. Looking at the evolution of the σ versus time (figure 3.24) one can see that this value increases together with the rising edge of the signal and goes back to the baseline value during the discharge. Such a behavior is not unexpected and this is why we determine the noise without the signal.

From the distribution of the widths we can extract the value of the noise in electrons knowing the value of the feedback capacitance C_f (1.3 fF). The charge injected on C_f through the test capacitance by a 100 mV pulse is $100\,\text{mV} \cdot 1.3\,\text{fF} =$

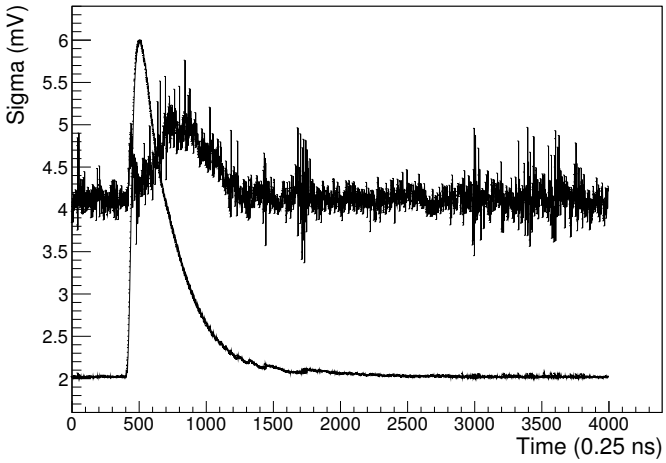


Figure 3.24. *Evolution of the value of σ for chip 2 with a* 100 mV *input pulse. The increasing values follow the signal rising and falling edges.*

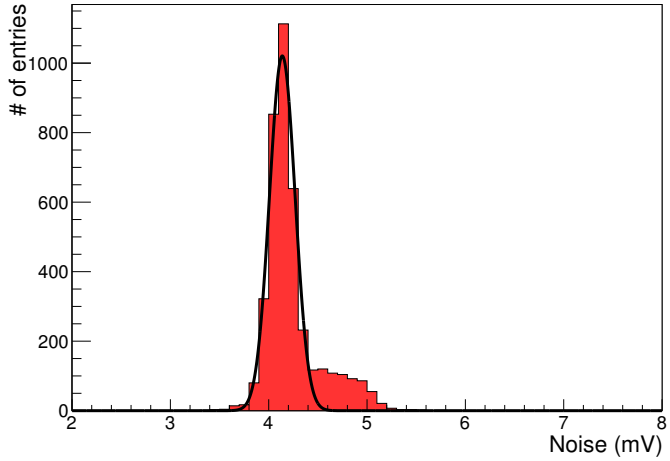


Figure 3.25. *Noise width distribution for chip 2 with a* 100 mV *input pulse.*

130 aC or equivalently 811 electrons. This charge generates a 144 mV pulse at the output of the preamplifier with a gain factor of 5.6 electrons/mV. The noise is 4.13 mV (23 electrons), which is fully compatible with simulations and calculations. Table 3.1 summarizes the results for all the tested chips. The error bars are given by the width of the distribution.

Chip	Noise (electrons)	Chip	Noise (electrons)
1	42 ± 1.4	6	23 ± 0.8
2	23 ± 0.7	7	22 ± 0.7
3	25 ± 0.7	8	24 ± 0.7
4	23 ± 0.8	9	25 ± 1.0
5	24 ± 0.9	10	25 ± 0.8

Table 3.1. *Frontend noise measurements results.*

Dynamic range

Figure 3.26 shows the response of the preamplifier for different injected charges. The plateau for large injected charges is clearly visible. The voltage across the feedback capacitance is high due to the amount of charge injected and as a consequence it is high at the output node, between transistors T4 and T5 in figure 3.8. The surplus charge is collected at the input of the amplifier and the feedback transistor proceeds to discharge C_f and C_p. When all this charge has been drained the circuit stabilizes at the normal operation point.

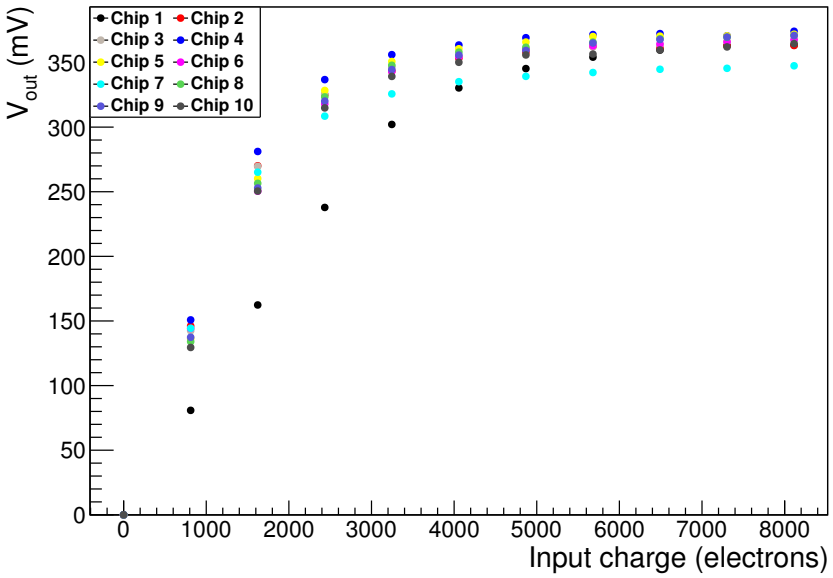


Figure 3.26. *Dynamic range of the preamplifier. For values of the injected charge larger than 3000 electrons the transistor saturates. The baseline has been subtracted from the data.*

In figure 3.26 the results of chip 1 deviate from the other chips. This is due to the amplifier giving an output which is roughly half of that of the other chips.

ToT linearity and feedback current

Figure 3.27 shows the shape of the output pulse for different injected charges.

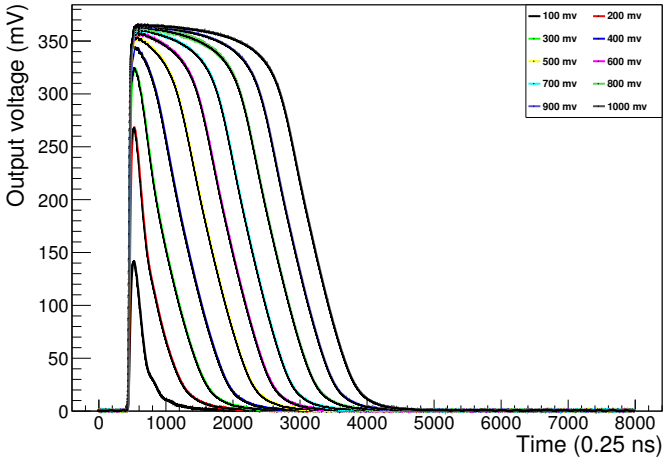


Figure 3.27. *Preamplifier responses to increasing injected charge for chip 3.*

For values of $V_{test} > 300\,\text{mV}$ the output pulse saturates. However, the ToT characteristic remains linear as shown in figure 3.28.

Even though the linearity is good the spread of ToT values from chip to chip is large as shown in figure 3.28. This is found to be due to mismatch in the feedback transistor (T_{fb} in figure 3.6). The variation of the discharge time constant due to this is up to 50%; this effect directly gives a variation in the ToT values. The fall edge jitter has been quantified in the same way as the rise edge jitter and is indicated by the error bars in figure 3.28. Another quantity which can be measured is the current drained by the feedback transistor T_{fb} that discharges the feedback capacitance when it works in saturation, as explained in section 3.3.1, by performing a linear fit on the curves of figure 3.28. The values obtained are shown in table 3.2.

Timewalk

While the preamplifier circuit introduces noise superimposed on the signal, the discriminator introduces timewalk. The net effect of timewalk is that two sig-

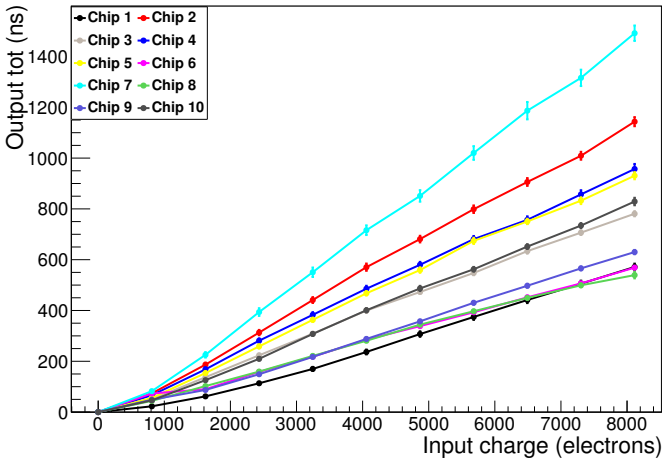


Figure 3.28. *ToT values for increasing input charge. The behavior is linear even though the spread is very large.*

Chip	Current (nA)	Chip	Current (nA)
1	2.20	6	2.28
2	1.09	7	0.83
3	1.57	8	2.25
4	1.29	9	2.02
5	1.31	10	1.50

Table 3.2. *Feedback current measurements results for all the tested chips.*

nals of different amplitudes arriving at the same time are detected at different moments. To measure this effect a relatively small charge has been injected in the frontend and the output of the discriminator has been recorded. Knowing the exact time of injection of the charge it is possible to calculate the delay introduced by the frontend and measure the timewalk. Figure 3.29 shows the results obtained for all chips.

When the relation between the signal amplitude and the delay is known a measurement of the ToT can be used to correct for the effects of timewalk.

Input jitter

Apart from timewalk, electronic noise affects the accuracy of the ToA measurement. If the rise time is large, the crossing of the threshold is defined less precisely due to fluctuations occurring at the input, giving inaccuracy in the deter-

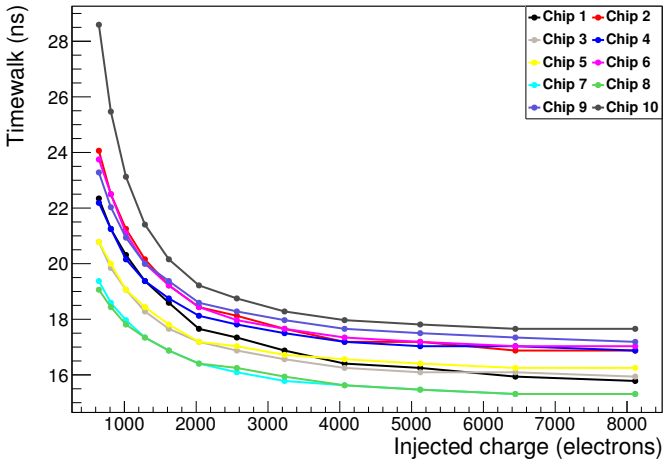


Figure 3.29. *Measured timewalk for the different chips.*

mination of the ToA. This effect is clearly visible looking at the discriminator output in figure 3.30. Here a test pulse of 370 electrons, but with rise times of 2 ns and 70 ns, respectively, is injected in the frontend; in the bottom picture, the slow rise time combined with the noise results in a not clear crossing of the threshold, which in turns gives inaccuracy in the ToA.

With the same data set used to determine the noise we can also extract the rise time jitter. In order to do so we set a "virtual" threshold, as shown in figure 3.31.

Measuring the detection moment for all the recorded waveforms one obtains a Gaussian distribution whose sigma is the jitter. This can be done for different pulse amplitudes in order to understand the impact of the increasing injected charge on the pulse detection time, as shown in figure 3.32. It is clear that injecting more charge reduces the jitter because the signal slew rate is higher and the crossing point is less affected by noise; in other words, the arrival time is better determined. The result is in line with expectations. The situation depicted here, however, is not very realistic since the expected signals have a very fast development. The limitations are mainly due to jitter.

It is possible to cross check the result obtained using the previously determined noise values since the jitter at the rising edge of the pulse is a direct consequence of the noise introduced by the preamplifier. The two are related by equation 3.12:

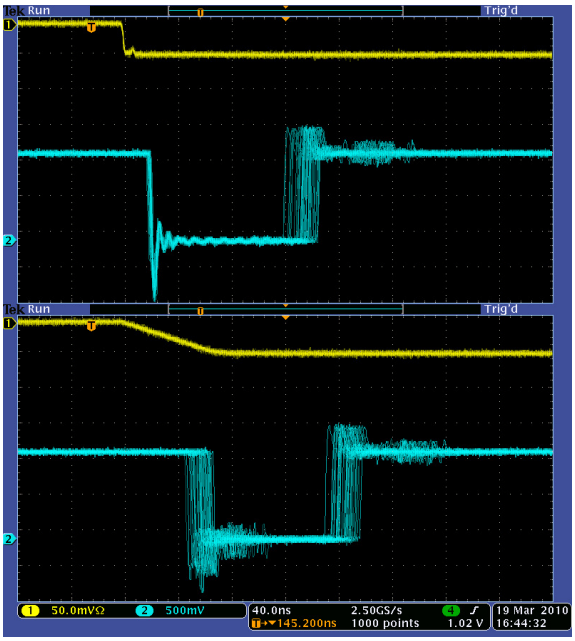


Figure 3.30. *Response of the frontend to a signal of 370 electrons with different rise times (top: 2 ns, bottom: 70 ns). Jitter due to noise at the beginning of the signal with slow rise time is clearly visible.*

$$\sigma^2_{\text{jitter}} = \left(\frac{\sigma_{\text{noise}}}{dV/dt}\right)^2 + (\sigma_{\text{jitterIntrinsic}})^2 \tag{3.12}$$

where the contribution of the intrinsic jitter is negligible. Let us consider, for example, chip 2 with a 811 electrons input pulse. Considering that $\sigma_{\text{noise}} = 4.13\,\text{mV}$ and a $dV/dt = 7.3\,\text{mV}\,\text{ns}^{-1}$ gives $\sigma_{\text{jitter}} = 0.548\,\text{ns}$ which is compatible with the results shown in figure 3.32.

3.7.2 Time to Digital Converter (TDC) characterization

The main test performed to characterize the TDC consists of injecting a pulse with different delay with respect to the system clock and for each of these pulses record the ToA, while keeping the arrival of the Trigger fixed. Figure 3.33 shows the results of such a test for the digital pixel of chip 1. The test pulse is 1 V, 1 µs long, with 2 ns rise time unless otherwise noted. The trigger arrives after 12.5 µs from the beginning of the acquisition while the pulse comes after 175 ns if the

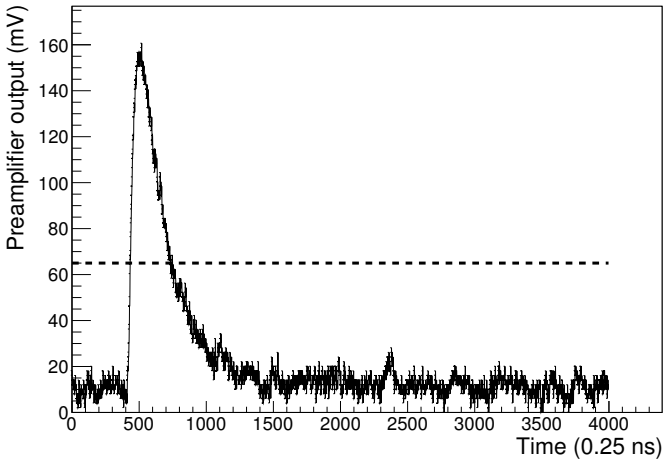


Figure 3.31. *Output of one of the preamplifiers. The "virtual" threshold (dashed line) is set externally.*

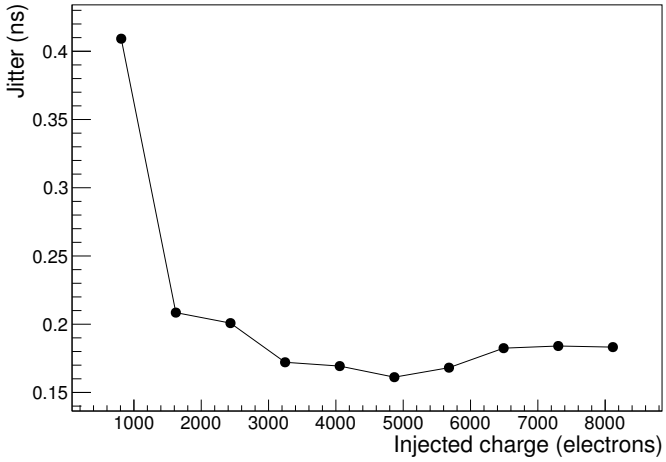


Figure 3.32. *Input jitter as function of the injected charge for chip 2. There is a clear trend of decreasing jitter.*

delay is set to 0.

The first step to extract the needed parameters from the data is to analyze the transition region between two consecutive bins of the TDC. The transition region has been fitted with an error function which returns two important parameters

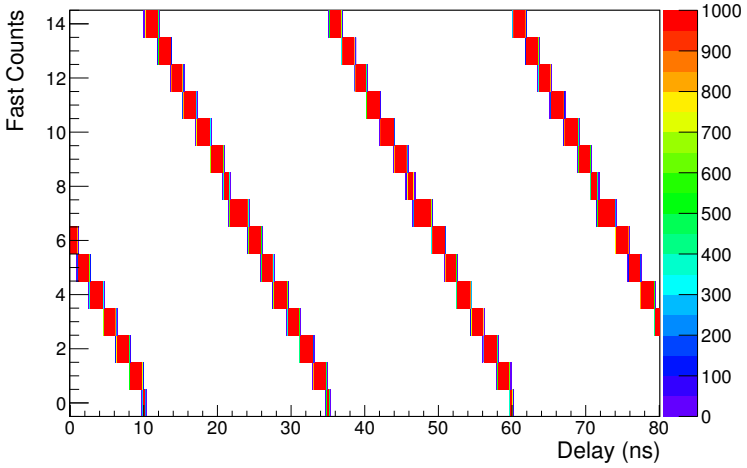


Figure 3.33. *Delay scan example for the digital pixel of chip 1. Only the values for the fast counter are shown.*

as explained in section 3.5: the value on the x axis where the function is at 50 % (the dot in figure 3.34), which is assumed to be the start/end point of the bin, and the σ of the Gaussian, which is proportional to the jitter.

The estimate of the 50 % point allows the calculation of the size of each bin; subsequently, using equation 3.7 the DNL for each bin has been calculated. Table 3.3 shows the results obtained for chip 1.

Once all the bins of every converter have been characterized, the DNL and INL values for every TDC have been extracted. The results are shown in table 3.4. Notice that the analog pixels of chip 3 and 8 are not present: this is due to chip 3 not working properly, while chip 8 has too much noise.

The values of INL for the analog pixels are bigger than for the digital one. This is due to the fact that the DNLs of consecutive bins are all smaller than the ideal bin. This means that once the INL fluctuates in one direction, away from the ideal straight line, it converges back to the ideal line only at the end.

A graphical way to display the same results of table 3.3 is shown in figure 3.35: the size of every bin is plotted against the ideal bin size (dashed line) with error bars showing the jitter for each individual bin calculated propagating to the total size the error on the beginning and the end of the bin. Bin zero is clearly off: by design, this bin is expected to be half of the ideal bin size. Measurements show that this is even smaller; bin 0 is roughly half of the expected 0.8 ns.

In figure 3.35 bin 8 is also clearly far from the ideal bin; this effect is systematic in all chips tested, but only for the digital pixel. The explanation for this

Bin	Bin size (ns)	Jitter (ns)
0	0.431	0.054
1	1.67	0.045
2	1.78	0.061
3	1.78	0.059
4	1.87	0.053
5	1.5	0.059
6	1.75	0.055
7	2.57	0.013
8	0.924	0.055
9	1.67	0.053
10	1.84	0.053
11	1.91	0.054
12	1.71	0.066
13	1.66	0.056
14	1.66	0.052

Table 3.3. *TDC of chip 1, digital pixel.*

Chip	Digital pixel		Analog pixel	
	DNL	INL	DNL	INL
1	0.65	0.79	0.38	1.8
2	0.40	0.83	0.41	1.9
3	0.40	0.72		
4	0.45	0.89	0.45	2.1
6	0.50	0.70	0.41	1.7
7	0.60	0.78	0.40	2
8	0.52	0.63		
9	0.67	0.73	0.37	2.1
10	0.62	0.88	0.46	2.1

Table 3.4. *Measured values of DNL and INL for all the chips. The missing values in the analog pixels are due to the fact that the pixels had too much noise to produce good results.*

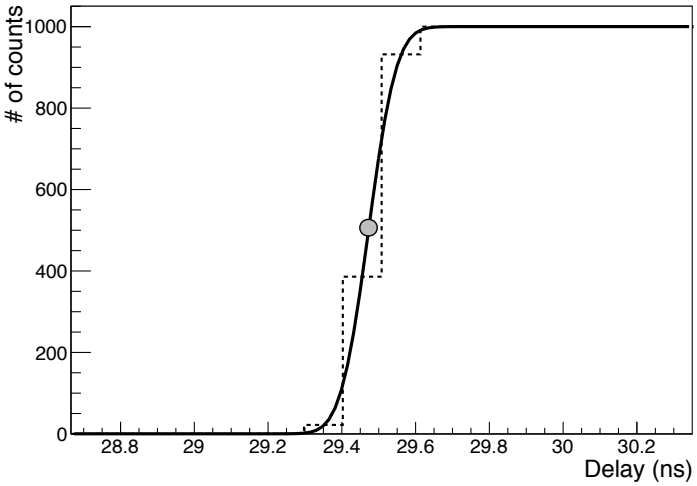


Figure 3.34. *Example of the fit performed on one bin of the TDC. The dot represents the value on the x axis where the function is at* 50 %. *This point is, by definition, the start/end point of the bin.*

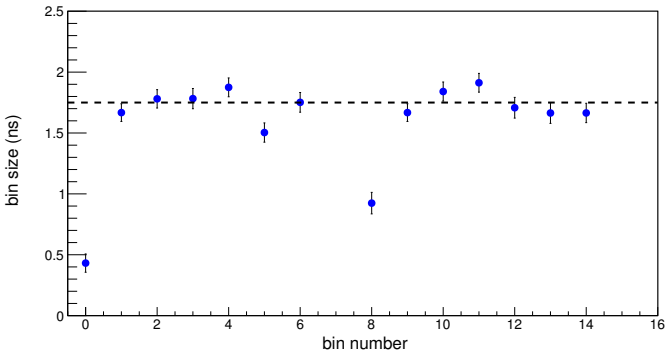


Figure 3.35. *Dispersion of the TDC-bin sizes of the digital pixel of chip 1. The ideal bin size is drawn as dashed line. The error-bars show the jitter of the individual bins.*

effect is that the falling edge of the system clock has an influence on the oscillator output and it is present only in the digital pixel due to the layout of the chip: the main line which distributes the clock has been routed on top of the digital pixel. The presence of this coupling has been verified by using a 20 MHz clock as reference clock. In this way all the fast oscillations happen in half a clock cycle

and the fast counter reaches the maximum count, producing then an extremely long last bin because the counting stops when overflowing. An example of this test is shown in figure 3.36.

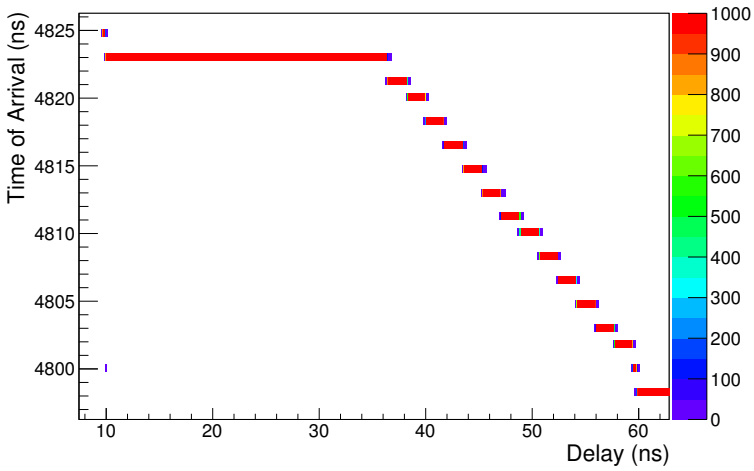


Figure 3.36. *Results of measurement using* 20 MHz *clock as system clock. The long bin is bin 14: the fast counter, when reaching the maximum count value, stops.*

Performing the same analysis on this data gives the results of figure 3.37. It is clear that bin 8 size is now compatible with the ideal bin size. Notice that bin 14 is not in the picture since it is out of scale.

3.7.3 Low Drop Out regulators

The operation point for all the measurements presented for the LDOs is always set at 1.1 V, since this is where the drop-out voltage is minimum and it is the most demanding working point for the LDOs. Figure 3.38 shows the output voltage provided by both the Small and Large LDO for different values of the reference voltage. As it can be seen in the figure, the measurements points match the simulations results.

Figure 3.39 shows the response of the LDOs to a change in load of 40 mA, similar to the calculated maximum load in a full size chip (see paragraph 3.3.3). The measurements (right) show a worse behavior than the simulations (left). This disagreement could be due to many factors; the most likely are an underestimation of the parasitics in simulations, which would reduce the bandwidth of the device, and the fact that the values for inductances and resistors for the

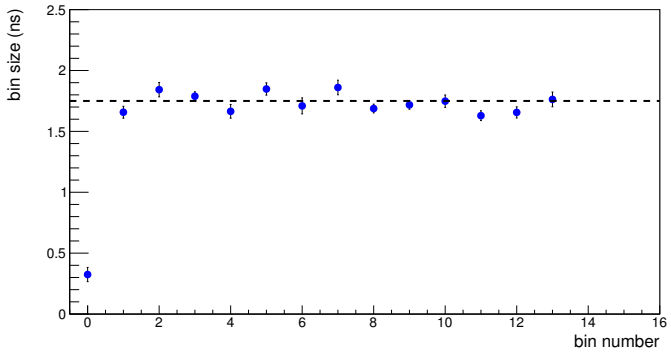


Figure 3.37. *Results of measurement using* 20 MHz *clock as system clock. Size of bin 8 is now compatible with the ideal bin size. Bin 14 is not in the picture being out of scale.*

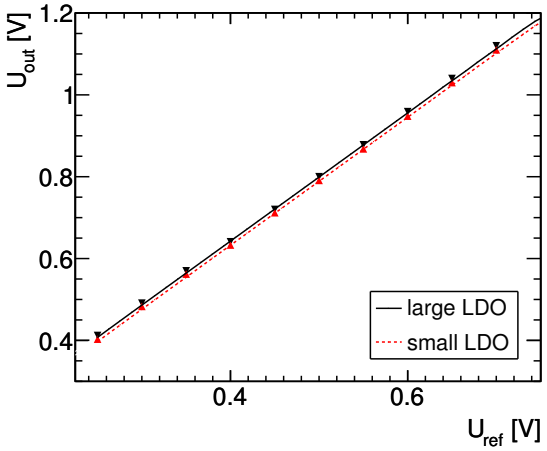
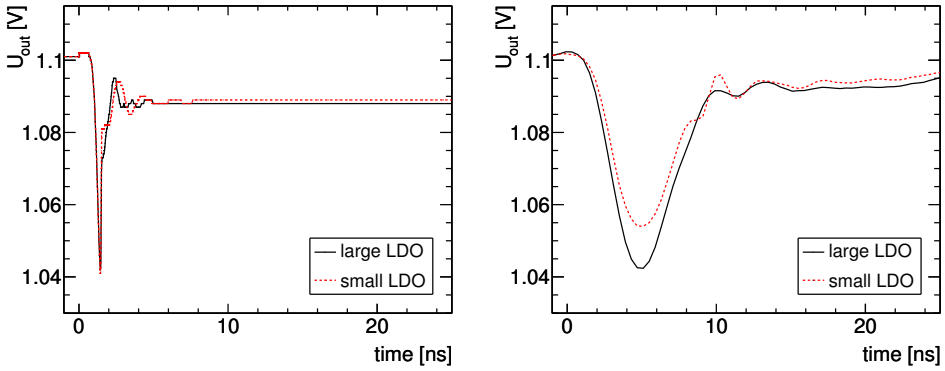


Figure 3.38. *Output voltage of LDOs with respect to the reference voltage. The measurements points (triangles) match the simulations.*

buffers capacitance are assumed to be constant, while in reality they are frequency dependent. Additionally, the load switch on the test board might introduce distortions; this effect has also not been simulated. The time needed for the circuit to recover is in the order of several nanoseconds, while simulations predicts less than one nanosecond.

The performances of the LDOs, although not matching the expectations from the simulations, are however good enough for applications in a full size chip. This can be seen in figure 3.40: the settling time of the LDOs and the correspond-



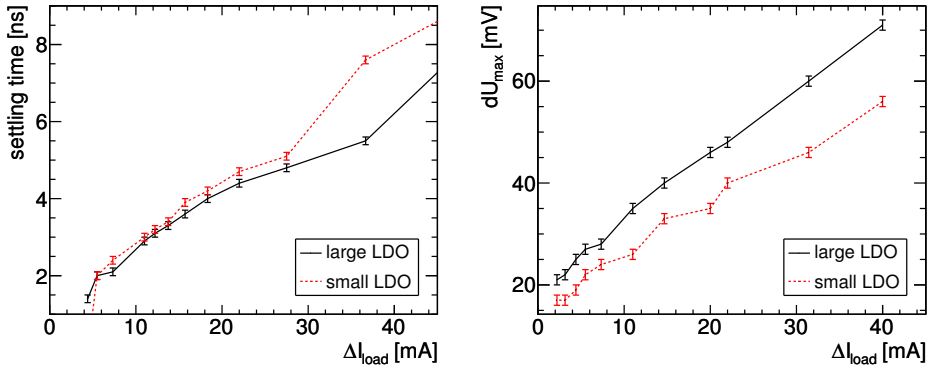
(a) (b)

Figure 3.39. *Transient response of the LDOs to a change in load of* 40 mA *simulations (left) and measurements (right).*

ing voltage drop for different load currents show, together with the transient response, that the specifications for the control characteristic of the oscillators are met: in the worst case scenario of a load step of 44 mA the settling time is less than 8 ns and the voltage drop is limited to 70 mV and 55 mV for the large and small LDO, respectively. Both are well within specifications. The small LDO could be used for a full size chip without compromising operations.

3.8 Conclusion

The tests conducted on GOSSIPO-3 have shown that the design of a per pixel high resolution TDC has been successful. The electronic frontend shows very low noise (23 electrons) and fast rise time (less than 25 ns). The design needs some improvements. A redesign of the feedback transistor is required to improve the mismatch in the ToT measurements. The TDC shows a good differential and integral non linearity. The coupling with the 40 MHz clock of the oscillator output has been understood and measurements performed with a 20 MHz clock prove that. The layout should be more carefully analyzed in a full size chip (256×256 pixels) to avoid this effect. Both the Large and Small LDOs work properly even if slightly worse than simulations. Moreover, the Small LDO is capable of delivering the required power to the oscillator given the fact that the maximum running time is 25 ns followed by a relatively long period of inactivity.



(a) (b)

Figure 3.40. *Settling time (left) and dynamic voltage drop (right) for the LDOs, when exposed to different load current.*

Chapter 4

Prototype TDC: Gossipo-4

4.1 Introduction

Timepix3 is a multipurpose pixel chip developed by the CERN Medipix3 group in collaboration with Nikhef and Bonn University. The outstanding features are the simultaneous recording of Time of Arrival (ToA) and Time over Threshold (ToT), a data driven readout and zero suppression. Moreover, every pixel features a high resolution Time to Digital Converter (TDC), similar to the GOSSIPO family of chips. GOSSIPO-4 is a prototype chip developed in the framework of the design of the Timepix3 chip. Its main features are an 8 pixel structure sharing one oscillator with a new topology, a Phase Locked Loop (PLL) to provide the control voltage to the local oscillators and a new small-area, high-density cell library. The chip was submitted in summer of 2012 and delivered at the end of the same year. In this chapter the design specifications together with the simulations and measurements will be presented.

4.2 Super Pixel: specifications and design

In the previous prototype chip, GOSSIPO-3, the idea was to have one oscillator in each pixel. This approach requires a considerable amount of area, given that a single oscillator takes approximately 6% of the 55 µm $\times$ 55 µm pixel area. In addition, power consumption is an issue; a particle going through the detector will typically cause several pixels to respond (a cluster) with an equal number of oscillators running all at the same time. Events where many particles traverse the detector at the same time would cause a large local power consumption and, in extreme cases, might cause severe damage to the chip.

For the above reasons, it has been decided to introduce the Super Pixel concept; in this configuration, 8 pixels share one oscillator. In this way it is possible to reduce the area occupied and, most importantly, the power consumption is greatly reduced. The block diagram of the Super Pixel can be see in figure 4.1. The basic operation principle is the following:

- if a pixel is hit, it locally produces the Gate signal. The Gate stays active until the first rising edge of the system clock (40 MHz);
- every pixel in the super pixel can produce this signal, thus the 8 gate signals are OR-ed: the output of the OR starts the 640 MHz oscillator (if not already running due to another pixel that was previously hit);
- the high frequency clock (output of the oscillator) is distributed to the 8 pixels;
- a pixel whose Gate is active records the number of oscillations with a counter.

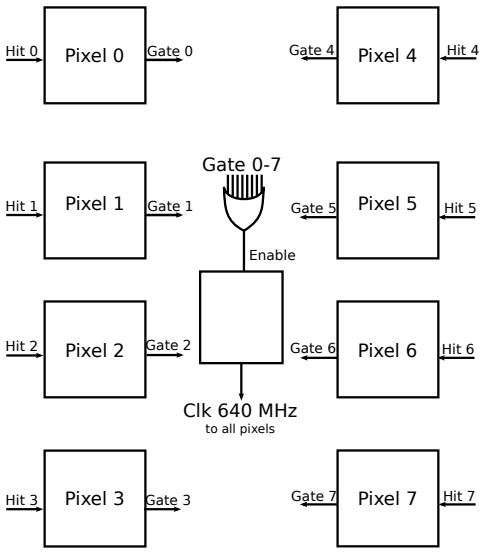


Figure 4.1. *Block diagram of the Super Pixel implemented in GOSSIPO-4. The oscillator is placed in the middle of the Super Pixel in the physical layout too, to minimize the routing length and the load.*

However, this solution brings new challenges. First, the oscillator has to be capable of restarting immediately after being stopped because the next hit could

be in the next bunch crossing. Second, the distributed high frequency clock must be synchronized to the system clock and not have glitches propagated to the counters because glitches might corrupt the counting sequence.

4.3 Pixel

The block diagram of a single pixel of GOSSIPO-4 can be seen in figure 4.2. The pixel contains no analog frontend, since the sole purpose is to test the digital logic. The Controller is a synchronous Moore Finite State Machine (FSM) and controls all the operations in the pixel (reset, data taking, readout)[1]. The Synchronization Logic is designed using asynchronous logic and provides the start and stop for the oscillator and a glitch free clock to the fast counter. The counters are maximum length Linear Feedback Shift Registers (LFSRs) with overflow detection and can record ToA and ToT at the same time. The input test pulse can be selected from 4 different configurations. A complete description of the various blocks is given in the next paragraphs.

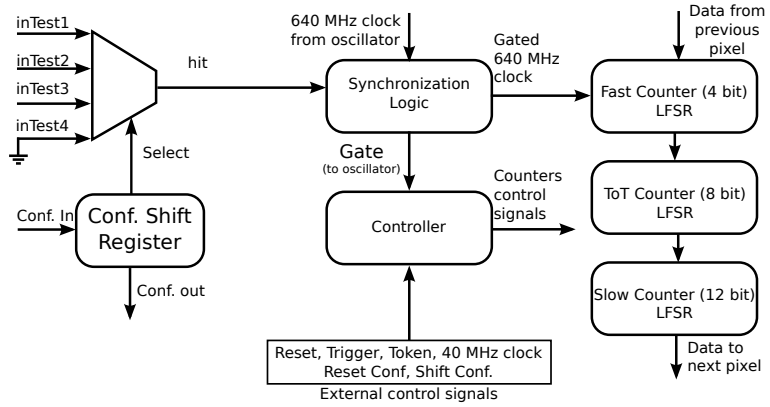


Figure 4.2. *Block diagram of a pixel of GOSSIPO-4. The Controller is a synchronous FSM, while the Synchronization Logic is an asynchronous one.*

[1]A Moore Finite State Machine is a state machine whose outputs are determined only by the current state. Other types of FSMs determine the output based on the current states and the inputs (Mealy state machine).

4.3.1 Input selection

The input selection block has been introduced to allow a complete test of the Super Pixel and in particular of the synchronization logic (see 4.3.2), since it allows to send independent test pulses to different pixels. At the input of every pixel there is a 4-to-1 multiplexer for the selection of one among 4 different inputs, as shown in figure 4.3. Selection of the input is achieved via two configuration bits which are part of the configuration shift register chain. The reset-low resets the configuration and automatically selects input 4, which is tied to ground by design.

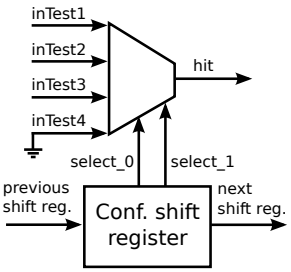


Figure 4.3. *Input selection circuit: inTest 4 is tied to ground by design and it is the on-reset selected input. The shift register is 2 bits long.*

4.3.2 Synchronization Logic

The need for a synchronization circuit follows the decision of using one oscillator which provides the fast clock to eight different pixels. In case two pixels are hit during the same system clock period the second pixel to be hit has to use the already running fast clock coming from the oscillator. If this situation is not properly handled, the risk is that a glitch propagates into the fast counter which might result in a wrong counting sequence. Consider, as an example, figure 4.4: when hit A arrives, the oscillator starts. Then, hit B is detected by another pixel in the same Super Pixel while the oscillator is already running. In the first case (red line) the first fast clock cycle is "cut" because hit B arrives when the clock is already running. In the second case (green line) for both hit A and B the last fast clock cycle is cut because of the phase between it and the rising edge of the system clock. This last situation may even occur with one hit per super pixel since it is only due to the phase difference between the two clocks. This nay result in very narrow clock pulses (the mentioned glitches). If no precautions are taken, the propagation of a glitch can cause the fast counter to enter in a wrong state due to the fact that some flip-flops in the fast counter will react to

the glitch, while others will not.

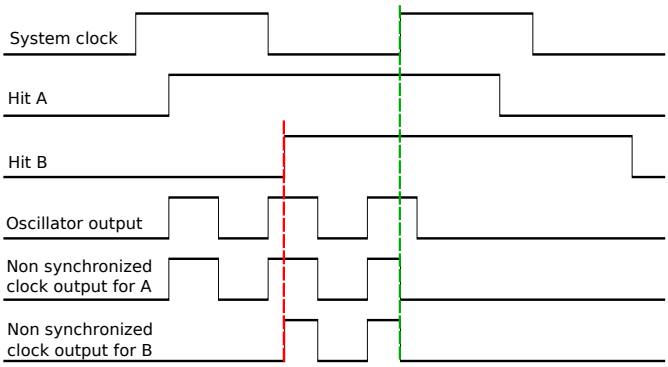


Figure 4.4. *Example of glitch propagation: hit A comes in and starts the oscillator. During the same system clock cycle hit B arrives and the relative pixel has to use the already running fast clock. System clock and oscillator output frequency not on scale.*

The specifications for the design of the synchronization circuit are the following:

- input signals: the 40 MHz clock, the hit and the 640 MHz clock from the oscillator;
- output signals: the Gate used to determine the active window of each individual pixel, to enable the oscillator and to gate the 640 MHz clock;
- the Gate starts when the hit arrives and is stopped by the first rising edge of the 40 MHz clock;
- the gated 640 MHz clock must be free of glitches.

The use of a proper synchronization logic applied to the example of figure 4.4 would then change the situation to the one in figure 4.5: only complete clock cycles will be propagated.

To minimize the area and power consumption it has been decided to use an approach that doesn't use flip-flops. Hence, an asynchronous state machine has been designed, following the method illustrated in [69]. For the complete derivation of the circuit see Appendix A.

Mixed signal simulations performed with the post layout netlist on the resulting circuit show expected behavior: in figure 4.6 a glitch at the output of the oscillator is clearly visible. Simulations have been done for different hit arrival time with respect to the system clock. In this way, glitches of varying length are

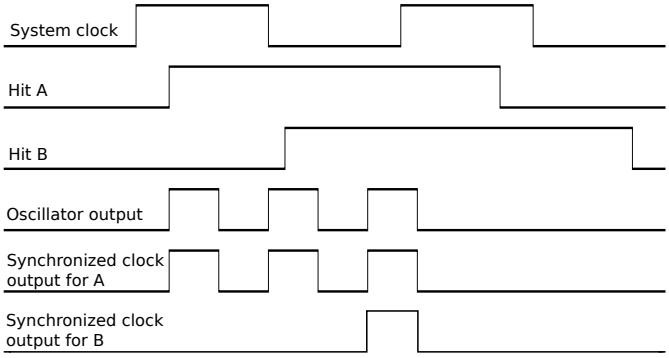


Figure 4.5. *Example of a glitch propagation problem solved by the use of a synchronization logic: no glitches are propagated, leaving only full clock cycles.*

generated. In all cases, the synchronization logic makes sure that these glitches are not propagated to the fast counter.

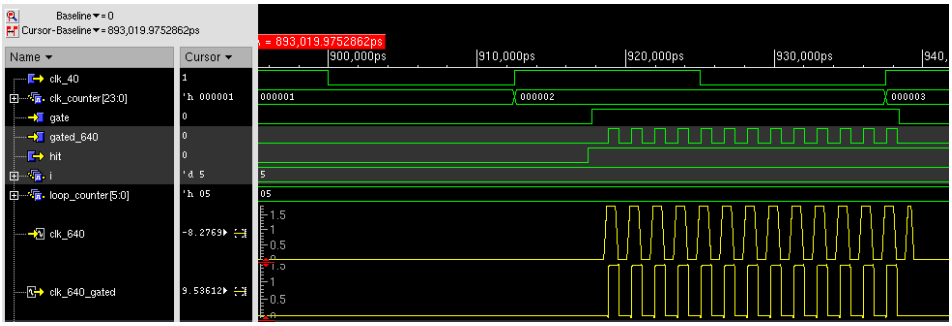


Figure 4.6. *Simulation example: the output of the oscillator contains a glitch. The synchronization logic make sure that this glitch is not propagated to the fast counter in the pixel.*

4.3.3 Counters

Similar to GOSSIPO-3, the counters in GOSSIPO-4 are LFSRs. The main difference is that in GOSSIPO-4 a technique has been applied which gives a n-bit LFSR with 2^n states instead of $2^n - 1$. This technique is known as De Bruijn method [70]. The method detects the forbidden state and supplies the condition which makes it possible to leave the forbidden state at the next count. The NOR

output is then inserted in the feedback with a XOR to the typical LFSR feedback, providing the wanted behavior, as shown in figure 4.7. The counting sequence for such a counter compared to the normal LFSR one can be seen in table 4.1. As in GOSSIPO-3 there are 3 counters for Fast ToA, ToT and Slow ToA, with a size of 4, 8 and 12 bits respectively. The characteristic polynomials for the three counters are given in equations 4.1.

$$\begin{aligned} \text{Fast counter:} \quad & P(x) = x^4 + x^3 + 1 \\ \text{ToT counter:} \quad & P(x) = x^8 + x^6 + x^5 + x^3 + 1 \\ \text{Slow counter:} \quad & P(x) = x^{12} + x^{11} + x^{10} + x^4 + 1 \end{aligned} \tag{4.1}$$

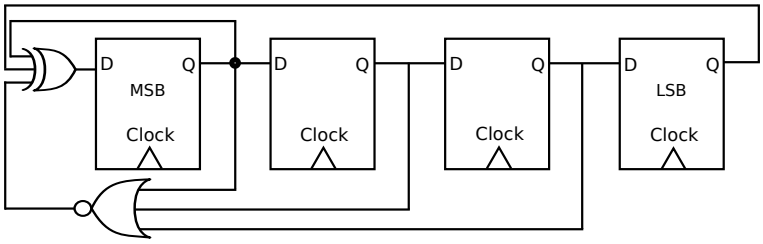


Figure 4.7. *Example of a 4 bit De Bruijn LFSR: the NOR gate takes all the FF outputs except for the LSB and is XOR-ed together with the usual LFSR feedback.*

4.3.4 Controller

The Controller is a Moore Finite State Machine that controls the operations of the other blocks in the pixel (counters, shift registers, etc...). It is a synchronous state machine in which the inputs are evaluated at each rising edge of the system clock and where the outputs change at the same rising edge. Operations (see figure 4.8) start with an external Reset assertion: the FSM enters in the Reset state, where all the counters are reset to their initial value. Subsequently, when the reset goes back to one, the FSM enters in the Wait state: the pixel is now ready to receive a hit. When a hit arrives, the Fast Counter records the number of oscillations of the Gated Fast Clock produced by the Synchronization Logic (see paragraph 4.3.2). At the first rising edge of the system clock the stop_gate_sync signal is produced: the FSM enters the Count-1 state, disabling the fast counter and enabling the slow and ToT counter. The system waits until the signal goes to zero or the overflow in the ToT counter the FSM enters in the Count-2 state,

Count value	Regular LFSR sequence	De Bruijn sequence
0	1111	1111
1	0111	0111
2	1011	1011
3	0101	0101
4	1010	1010
5	1101	1101
6	0110	0110
7	0011	0011
8	1001	1001
9	0100	0100
10	0010	0010
11	0001	0001
12	1000	0000
13	1100	1000
14	1110	1100
15		1110

Table 4.1. *Counting sequence for a regular LFSR counter (second column) and a De Bruijn counter (third column). Notice the forbidden state (count value = 12) and the subsequent insertion of a 1 in the De Bruijn sequence which appears in the next state.*

disabling the ToT counter while the Slow counter stays active until the arrival of the Trigger.

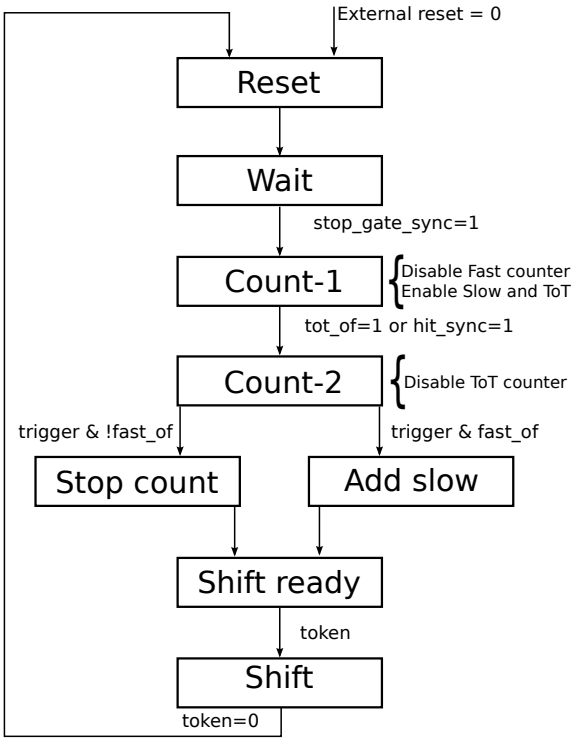


Figure 4.8. *Block diagram of the State Machine implemented in GOSSIPO- 4.*

When the Trigger is sent the Slow counter stops and then two things can happen:

- If the fast counter reached the maximum count (overflow), one count is added in the slow counter (Add Slow state) and then the FSM goes to the Shift Ready state; notice that the counters don't stop when they reach the overflow, but continue the counting sequence. The overflow is signaled with a separate overflow bit.

- If the fast counter didn't overflow, the FSM goes to the Stop Count state, and after 1 clock cycle it goes to the Shift Ready state; the Stop Count state is a dummy state, inserted just to use all the 8 possible states available to avoid the possibility that the state machine, entering in an undefined state, stays there indefinitely.

When the FSM goes into the Shift Ready state the counters are reconfigured as one 24 bit long shift registers and are ready to shift out the data. This happens when the Token is sent (Shift state): the shifting then proceeds as long as Token is asserted. When Token is deasserted, the FSM enters in the Reset state, and it is ready to receive the next hit.

For long signals, the Trigger is sent when the ToT counter is still active: in this case, the FSM goes directly into the Shift Ready state and then proceeds with normal readout operations.

4.4 Oscillator

Given the results obtained with the tests on GOSSIPO-3 (see section 3.7.2) the oscillator has been redesigned to minimize the dependence of the oscillation frequency on power supply voltage. The desired frequency is now obtained as the delay introduced by a series of RC components (see figure 4.9) compatible with the desired frequency while the inverters act only as buffers. The special feature of this circuit is formed by the capacitors called varactors. Their main property is that the value of the capacitance is a function of the voltage across them as shown in equation 4.2

$$C_{\mathrm{nom}}(V) = C_A \cdot L \cdot W \cdot F + C_L \cdot 2 \cdot L \cdot F + C_W \cdot 2 \cdot W \cdot F + C_F \cdot F \tag{4.2}$$

where C_A is the capacitance per area, C_L, C_W, C_F are fringe capacitances, L and W are the active layer length and width and F is the number of capacitances in parallel.

In GOSSIPO-4 this voltage is produced at the periphery of the chip by a PLL which contains a replica of the oscillator present in each the Super Pixel. The PLL locks at the desired oscillation frequency (640 MHz) and generates the required control voltage (V_{cntr}) for the local oscillators. It is important to notice from figure 4.10 that for a given value of V_{cntr}, for VDD $>$ 1.2 V the oscillation period stays constant; this is relevant for a full chip application as Timepix3 because due to the large area of the chip (the active area is 1.4 cm $\times$ 1.4 cm) a certain decrease of supply voltage across the chip is unavoidable. With a power supply voltage of 1.5 V, even a voltage drop of 200 mV will guarantee stable operation of the oscillators across the entire chip.

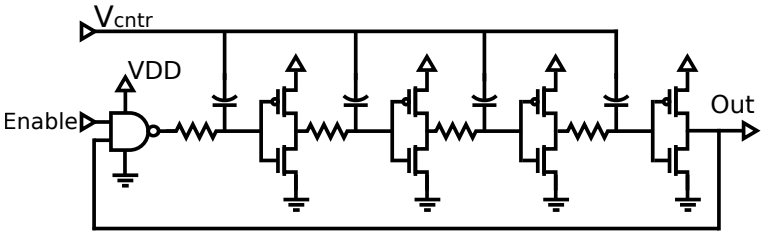


Figure 4.9. *Schematic of the oscillator used in GOSSIPO-4. The oscillation frequency is determined by the RC components, while the inverters only act as buffers.*

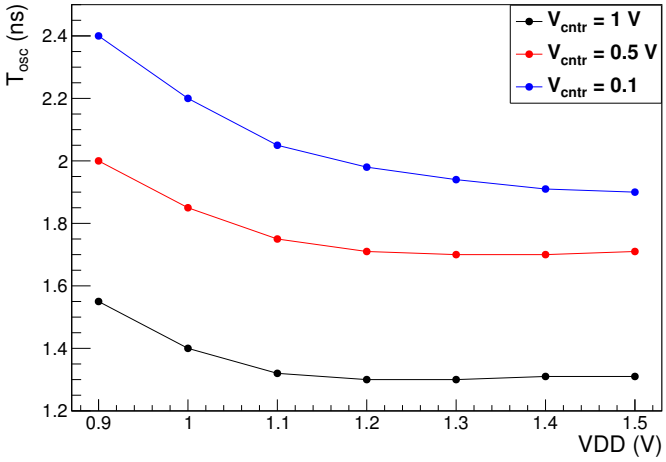


Figure 4.10. *Simulation results of the oscillator; for power supply bigger than* 1.2 V *the oscillation frequency is independent from the supply voltage.*

4.5 Phase Locked Loop

As has also been shown in chapter 3 for GOSSIPO-3, a solution to tune out variations in the oscillation frequency uses a Low Drop Out regulator to provide the voltage to the oscillators. Using an LDO requires an external capacitor to stabilize the circuit and is not considered practical. Such a control voltage (V_{cntr}) in GOSSIPO-4 is produced at the periphery of the chip by a PLL, designed at Bonn University. The PLL occupies an area of 208 µm $\times$ 106 µm and contains a replica of the oscillator used in the Super Pixel (see figure 4.11). This replica produces locally in the PLL the fast clock; after being divided by 16 it is then compared to an externally provided clock. Using a phase frequency detection mechanism

the PLL adjusts the control voltage until the oscillator frequency and phase are equal to the ones of the external clock. The control voltage is sent to all oscillators in the chip, which are then guaranteed to produce the same frequency. This solution is robust against temperature and supply voltage variations, provided that the PLL can reach the locked state. This implementation requires, for a full chip, a strong buffer to distribute the control voltage.

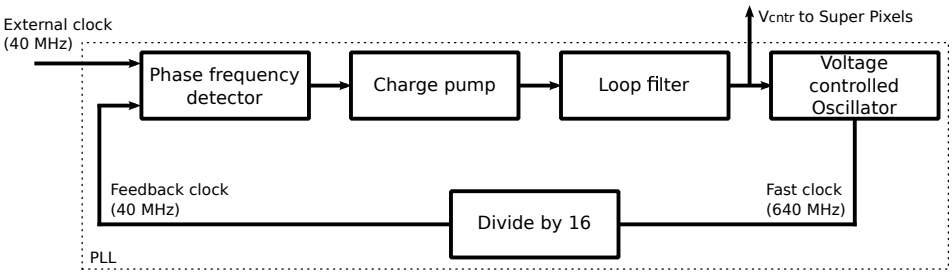


Figure 4.11. *Block diagram of the PLL used in GOSSIPO-4.*

Figure 4.12 shows the phase frequency detector circuit on the left and the operation mode on the right. The circuit has two inputs, an external reference clock and the (divided) fast clock coming from the oscillator replica. There are two types of phase difference that can occur: if the reference clock is leading the feedback, as shown on the right in figure 4.12, then UP is 1 for a long time and DN is 0 for a short time. Vice-versa if the feedback clock is leading. In case the two signals are in phase, a regular train of pulses is produced at the two outputs.

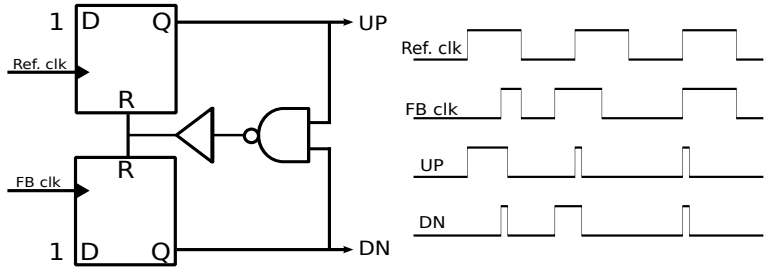


Figure 4.12. *Schematic of the phase detection circuit. A situation where UP = 1 and DN = 0 signals that the reference clock is leading the feedback; vice-versa, UP = 0 and DN = 1 means that the feedback clock is leading. A stream of regular pulses at the UP and DN outputs is produced when there is no phase difference.*

The buffer in the circuit has been introduced because simulations show that

the circuit would not respond to small phase differences (order of 10 ps), creating a dead zone in the control. With the additional delay (T_g) introduced by the buffer a minimum pulse width of the UP/DN pulses is ensured which solves the problem.

UP and DN are then used as input for the charge pump. The two signals are used to control two switches (which are minimum size transistors) that inject or sink current to/from the loop filter (see figure 4.13). For each cycle the time during which the switches are closed is proportional to the phase difference. In this way, it is possible to regulate the control voltage, which is then sent to the local copy of the voltage controlled oscillator closing the loop. In summary: if, for any reason, the output of the oscillator is changing, the phase detection circuit would notice this change. By opening the appropriate switch it would then change the voltage across the capacitors of the loop filter resulting in a change of the control voltage. This voltage proportional to the phase difference would, in the end, cancel the phase difference with the reference clock.

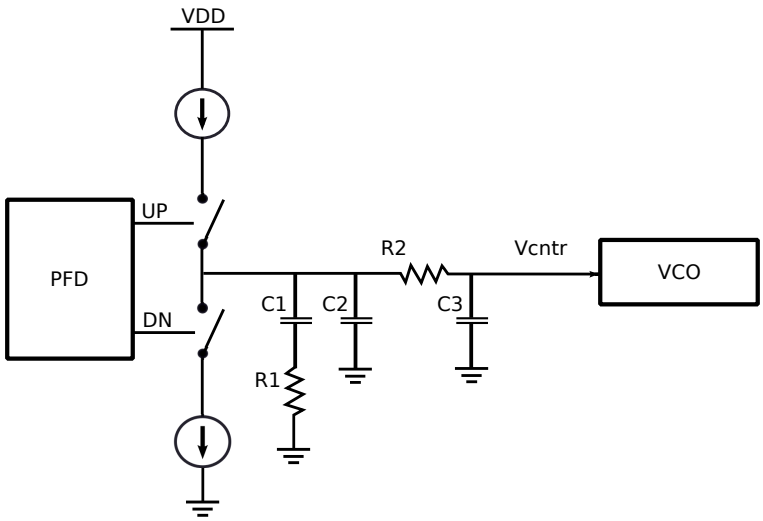


Figure 4.13. *Schematic of the charge pump and loop filter.*

The loop filter has been designed to have four poles in order to have a strong spurious signals suppression effect. Considering that the fourth pole has to be away from zero and that a phase margin bigger than 50° is required, the values of the capacitors and resistors of the filter are the ones shown in table 4.2.

Resistor	Value	Capacitance	Value
R_1	22 kΩ	C_1	7.43 pF
R_2	11 kΩ	C_2	710 fF
		C_3	320 fF

Table 4.2. *Values of the resistors and capacitances of the PLL.*

4.6 GOSSIPO-4 characterization

The characterization of GOSSIPO-4 has been performed using the same FPGA and chip board used for GOSSIPO-3: special care has been taken during the design phase to make sure that GOSSIPO-4 pin layout was fully compatible with GOSSIPO-3 to fit in the same test board. The core of the FPGA firmware is the same used for GOSSIPO-3 with the addition of a shift register to store and shift the configuration pattern for the test input selection. The equipment is the same that has been used for GOSSIPO-3. In total, 10 chips have been fully tested and characterized and the results are shown in the next sections. Unless otherwise noted, the power supply voltage is 1.5 V.

4.6.1 Single pixel characterization

Before characterizing the interplay of different pixels in the same Super Pixel, the complete characterization of all the single pixels has been performed. To do so, every pixel has been tested separately: a test pulse (1 µs width, 2 ns rise time) has been delayed in small steps (0.1 ns) and for every value of the delay the TDC value was recorded 1000 times. An example of the results of such a delay scan is shown in figure 4.14. The picture shows only the values of the fast counter.

The two important parameters to extract from the data are the bin size and the jitter as was done for GOSSIPO-3 in section 3.7.2. The results are summarized in figure 4.15. The low value of the jitter is expected since the circuit is purely digital, so no noise is introduced by the analog frontend. Table 4.3 shows the values of the DNL and INL for all the pixels in chip 1.

It is worth noticing that both DNL and INL are dominated by the value of bin 1: this bin is the one that has the biggest difference from the ideal bin size. However, this behavior is constant in all the pixels and chips, showing that the reproducibility of the circuit is good (see table 4.3).

Bin 1 of the TDC is clearly off with respect to the ideal bin size (designed to be 1.56 ns). The oscillator probably requires time to startup and to deliver a good quality clock to the fast counter in the pixel. When the first count of the fast clock happens this could explain why bin 1 is shorter than the others. It is possible to verify this hypothesis by looking at two pixels reacting to two

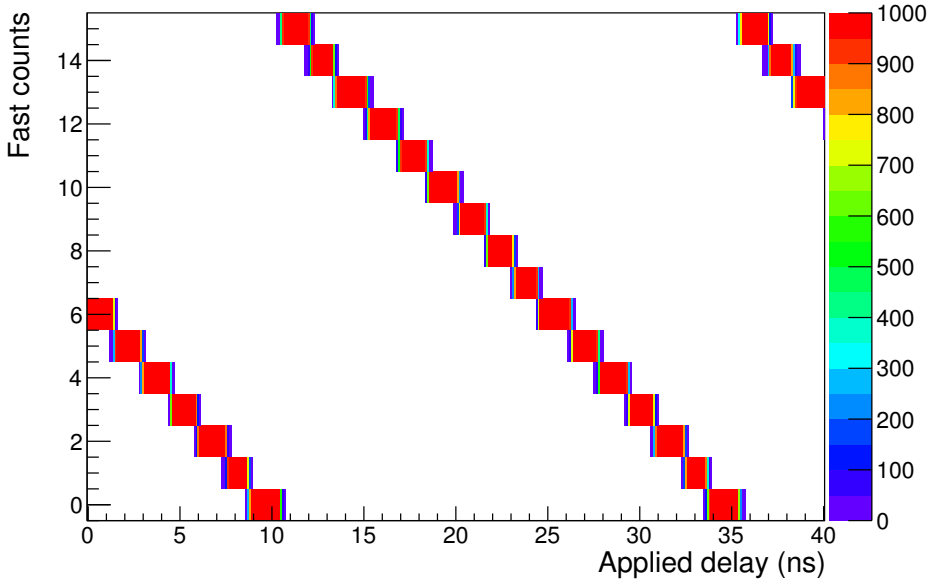


Figure 4.14. *Result of a delay scan test with 1000 pulses per step for chip 1, pixel 0. Only the fast counter values are shown.*

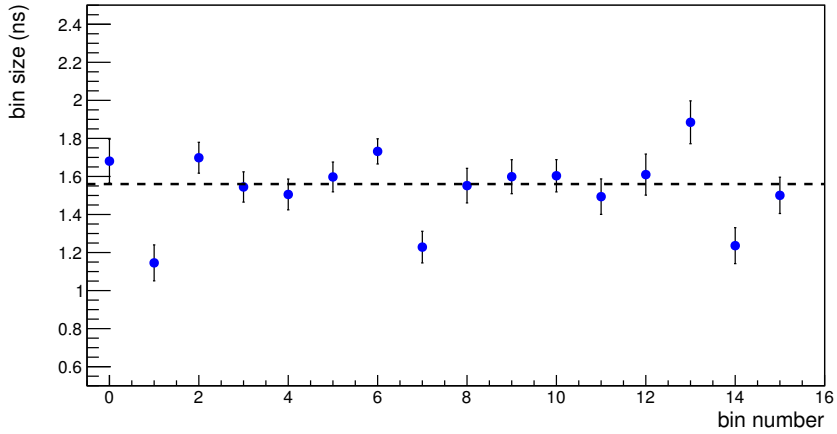


Figure 4.15. *Measurement results for chip 1, pixel 0.*

different input pulses provided during the same system clock cycle: in this case, the pixel reacting to the late pulse uses the already running clock, so it shouldn't

Pixel	DNL	INL
0	0.27	0.23
1	0.19	0.19
2	0.18	0.18
3	0.21	0.15
4	0.24	0.33
5	0.21	0.18
6	0.18	0.22
7	0.25	0.30

Table 4.3. *DNL and INL values for all the pixels of Chip 1. Both values are dominated by bin 1, which is the bin that differs the most from the ideal bin. The pixel to pixel variation is small.*

show a small bin 1. This assumption is confirmed by the results of section 4.6.2.

Figure 4.16 shows the distribution of DNL and INL for all the 10 chips (8 pixels each). The results are good. There are no TDCs with missing codes, the values for DNL and INL are low and the chip to chip variation is also low, showing that the mechanism of locking the oscillators to an on-chip PLL works as expected and satisfactory. This mechanism is used also in Timepix3 (see chapter 5).

4.6.2 Full Super Pixel response

To comprehend the behavior of the Super Pixel it is important to test the response of such a circuit to an event that activates all pixels at the same time. Such an event, even though rare, might cause a wrong response of a pixel if the fast clock is not properly distributed or if too many active elements are connected to the output of the oscillator. To simulate the occurrence of such an event, the same test pulse has been sent to all the pixels: in this case, besides a difference due to the different delays introduced by the routing of the test pulse from the input to each individual pixel, all pixels are expected to give the same response. Figure 4.17 shows the response of all pixels in the chip. The picture clearly shows some "wrong" count values. This is not an issue since it happens only for Chip 1, pixel 5 and also the amount of the wrong counts is negligible (less than 10%).

Figure 4.18 shows the measured bin size for the TDC of pixel 0 disregarding the spurious hits of figure 4.17. Compared to figure 4.15 the spread around the ideal bin size is reduced. This confirms the hypothesis made in section 4.6.1 that at the startup the oscillator takes some time to deliver stable oscillations. Pixel 0 reacts later with respect to other pixels like for example pixel 7, since at delay =

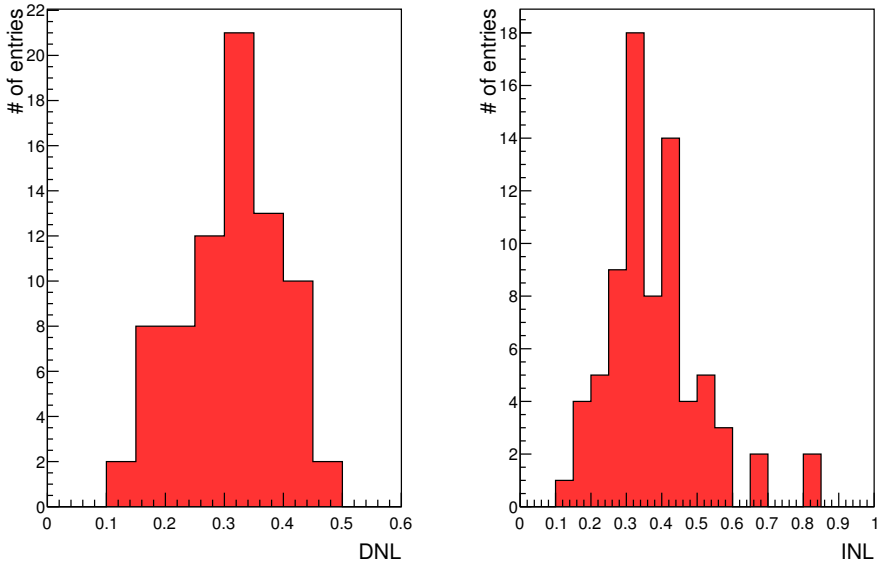


Figure 4.16. *Distribution of the DNL and INL values for all the chips.*

0 the latter is counting 7 while the former is counting 6.

Table 4.4 reports the values of the DNL and INL for Chip 1. The results are compatible with what has been obtained for the single pixel characterization. This is confirmed by figure 4.19 which shows that the distribution of the DNL and INL for all the chips doesn't change significantly proving that the operations of the pixels are not influenced by an event activating the entire super pixel.

4.6.3 Multiple hits test

The results presented in section 4.6.2 already showed that the synchronization logic is working properly and that the hit distribution and synchronization mechanism is reliable. However, to test a more realistic situation a specific test using two different pulses with a slightly different delay has been performed. The first pulse, hit-1, is delayed between 0 ns and 40 ns. The second pulse, hit-2, is fixed at 16 different delays of the scan, with a 1.6 ns difference for each one. Four different situations can then occur:

- hit-1 arrives before hit-2 and in the previous system clock cycle;
- hit-1 arrives before hit-2, in the same system clock cycle;

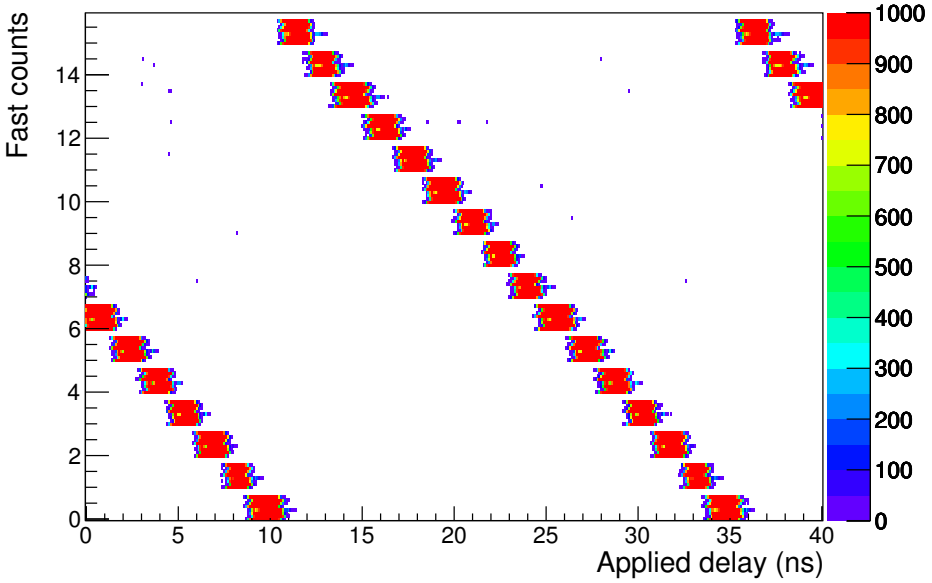


Figure 4.17. *Result of a delay scan test for chip 1. All pixels are displayed in the picture. Only the fast counter values are shown.*

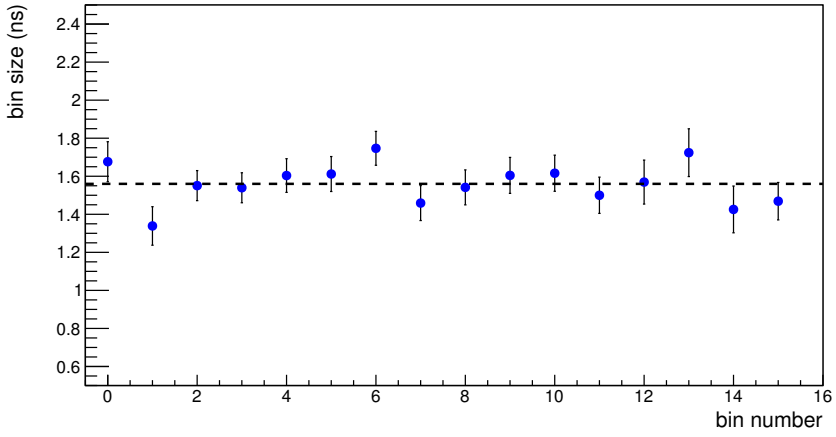


Figure 4.18. *Measurement results for Chip 1, pixel 0. The results have been obtained with all the pixels active at the same time.*

Pixel	DNL	INL
0	0.14	0.15
1	0.24	0.26
2	0.13	0.35
3	0.18	0.18
4	0.24	0.18
5	0.16	0.53
6	0.18	0.20
7	0.21	0.17

Table 4.4. *DNL and INL values for all the pixels of Chip 1; all the pixels were active at the same time.*

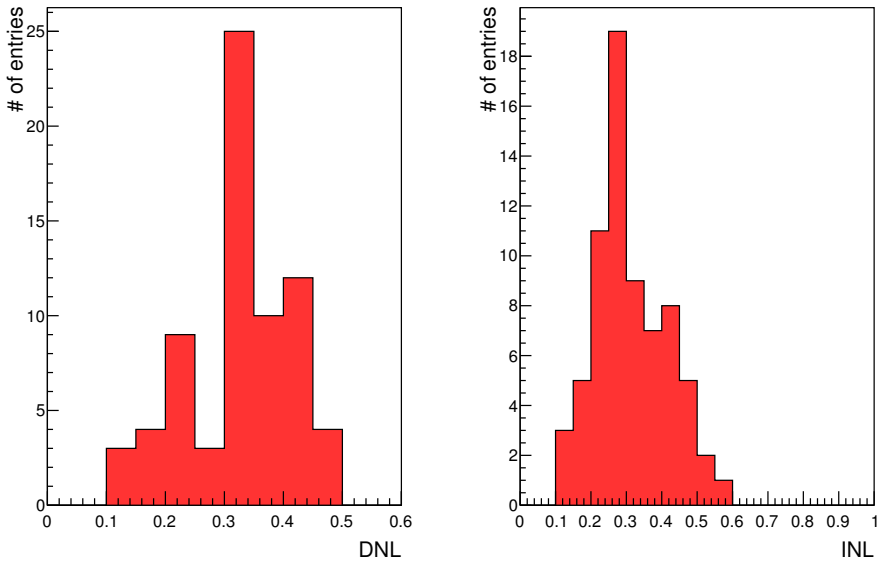


Figure 4.19. *Distribution of the DNL and INL values for all the TDCs. All 8 pixels in the super pixel are hit at the same time.*

- hit-1 arrives after hit-2, in the same system clock cycle;
- hit-1 arrives after hit-2 and in the following system clock cycle.

An example of the result of such a test is shown in figure 4.20. The picture shows the results coming from both the hit pixels. Hit-1, which is being delayed, reproduces the usual TDC characteristic. Hit-2, which is fixed, produces the

horizontal (almost) continuous line. The four situations described above are recognizable: when hit-1 is in the previous system clock cycle with respect to hit-2, the measurement result for hit-2 is always the same. When hit-1 enters in the same clock cycle, hit-2 is flipping between two values: this happens because at this point the phase of the fast clock with respect to the system clock plays a role; when hit-1 and hit-2 are in the same clock cycle but hit-1 arrives before the oscillator is started by the former with the latter using the running clock to count. In this case this implies, given the delay of hit-2, that for half of the fast clock cycle one count more is detected. Then, when hit-1 arrives later, the behavior goes back to the usual one.

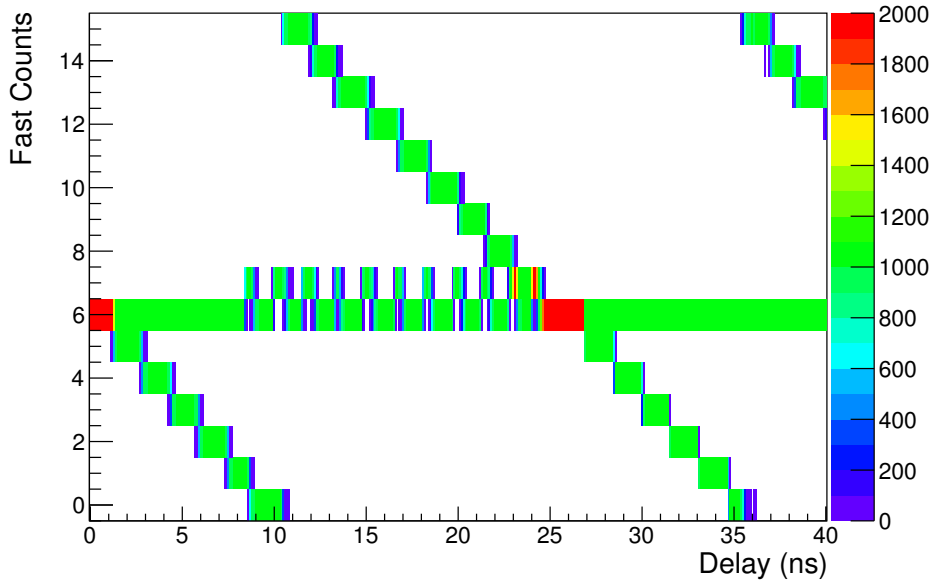


Figure 4.20. *Delay scan of chip 1, pixel 0. Pixel 1 receives a hit always at the same time.*

It is worth noticing also the size of bin-1. The data show that bin-1 recorded in the first case (hit-1 before hit-2) is shorter than the one recorded in the second case (hit-1 after hit-2).

4.6.4 Phase Locked Loop measurements

The PLL provides the control voltage to the oscillator. To measure its performance, however, one can look at the fast clock produced by the oscillator which

is present in the loop. On the test board the output of the VCO is not directly available; what can be measured is the 320 MHz clock coming after the first division of the fast clock through a differential couple of LVDS outputs. Figure 4.21 shows the eye diagram of the clock. The distortions which are visible in the picture are caused by crosstalk from the positive and negative edge of the fast clock, but they are not an issue of the PLL but of the test board, since the two LVDS outputs are located next to each other. The total eye opening is 1.37 ns and 340 mV.

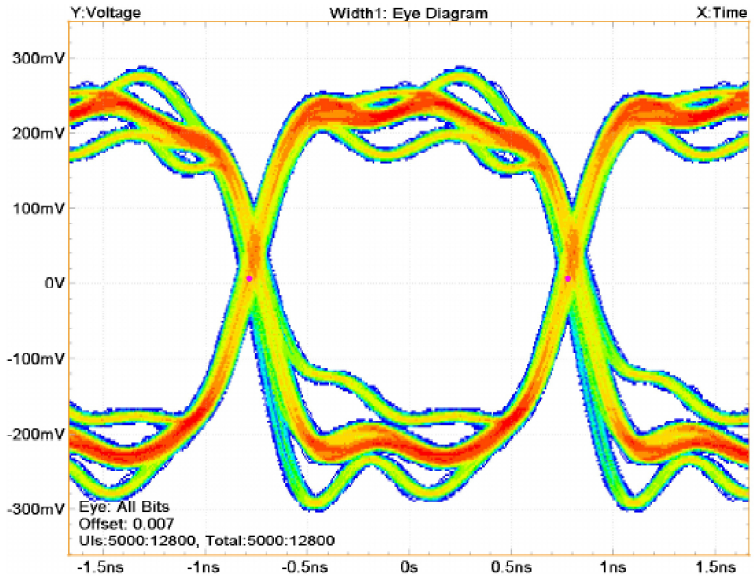


Figure 4.21. *Eye diagram at* 320 MHz.

The Time Interval Error (TIE) is defined as the measured distance of the active edge of the clock from its ideal position. Figure 4.22 shows the results of such measurement. Fitting with a Gaussian gives a σ = 23.4 ps. A summary of the most important measured properties of the PLL is shown in table 4.5.

4.6.5 Supply voltage dependence

In order to understand the operational limits of GOSSIPO-4, a power supply voltage scan has been performed. In this type of test, all pixels have been individually characterized at different supply voltages. This test is important because it shows the maximum voltage drop due to power distribution that can be allowed in a full chip. All the chips have been tested with VDD of 1.3 V and

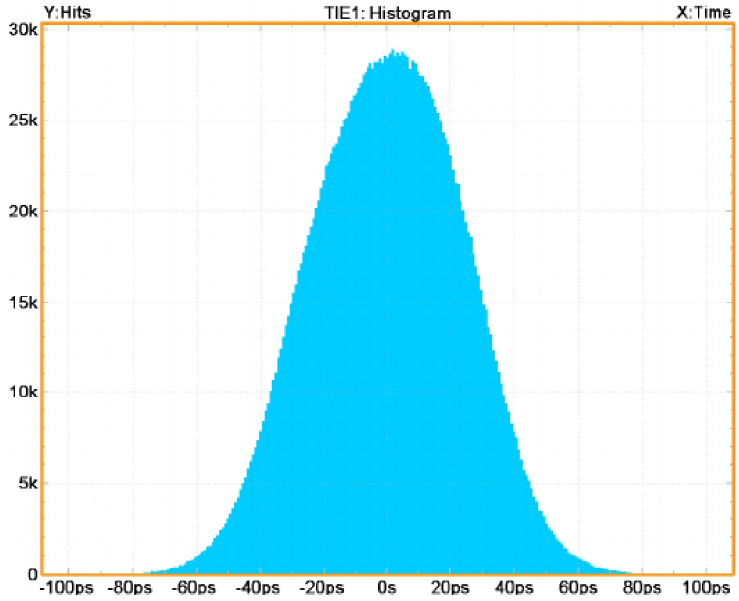


Figure 4.22. *Time Interval Error (TIE) at* 320 MHz*. Courtesy of Y. Fu.*

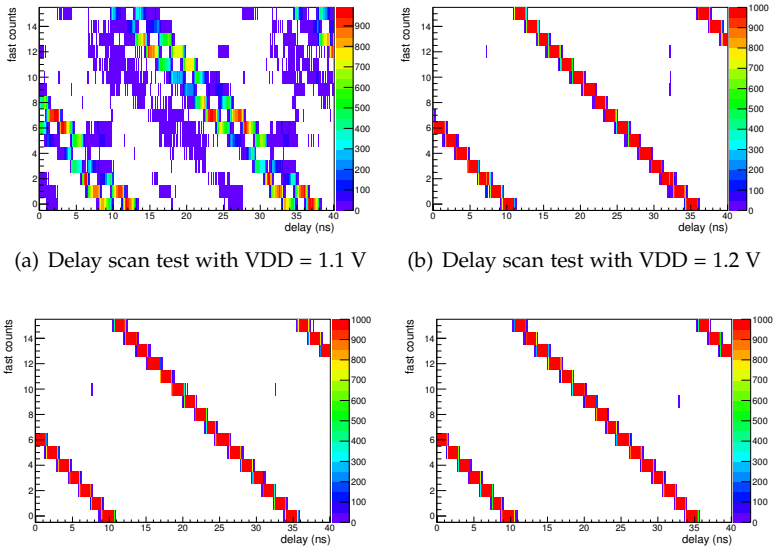
1.4 V. For some chips tests were performed at 1.1 V and 1.2 V but the results showed that not all of them were working properly, so it was decided to limit the tests to the mentioned power supply voltages.

Figure 4.23 shows the results for Chip 1, pixel 0 (the same test performed at VDD = 1.5 V is shown in figure 4.14).

Figure 4.23(a) shows an example of a delay scan done at 1.1 V as a test. It is recognizable a pattern that resembles the TDC characteristic but the behavior of the pixel is clearly wrong. The other scans of figure 4.23 show a good TDC characteristic; there are some wrong counts, but they are very few (less than 10%) and they have been taken out of the analysis. Again, the characterization

TIE	23.4 ps RMS
duty cycle	50.75%
power consumption	4 mW
time to lock	2 µs
VCO output frequency range	490 MHz - 740 MHz

Table 4.5. *Summary of the measured properties for the PLL. All quantities have been measured for the* 320 MHz *clock.*



(a) Delay scan test with VDD = 1.1 V

(b) Delay scan test with VDD = 1.2 V

(c) Delay scan test with VDD = 1.3 V

(d) Delay scan test with VDD = 1.4 V

Figure 4.23. *Results of a delay scan test performed at different supply voltages for chip 1, pixel 0. The top left picture shows clearly that the chip is not working properly. In the other cases, despite some wrong counts, the chip is still responding well.*

(bin size, jitter, DNL and INL) for the single pixel TDC has been performed. Figure 4.24 shows the measurement results for chip 1, pixel 0 while figures 4.25 and 4.26 show the DNL and INL distributions. The results are compatible with the chips operating at 1.5 V, showing that a drop up to 200 mV in power supply voltage does not compromise chip operations.

4.6.6 Oscillator control voltage dependence

Figure 4.27 shows the change of the control voltage as a function of the supply voltage. For VDD $>$ 1.3 V it is clearly visible that V_{cntr} has small variations, on the order of 20 mV for a 100 mV change in VDD. This means that considering a full size chip like Timepix3 a drop of 200 mV on the VDD due to the power distribution does not create noticeable effects on the oscillation period (less than 10%). A small change in VDD does not directly influence the oscillation frequency if the change is in the plateau region of the oscillator (see paragraph

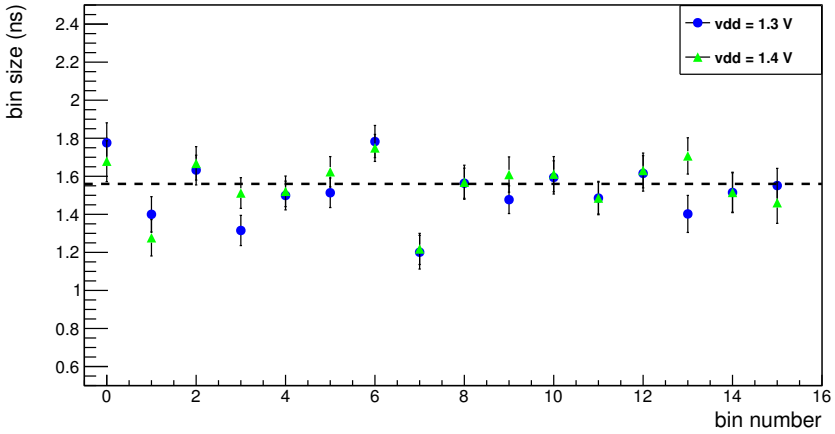


Figure 4.24. *Bin size of chip 1, pixel 0 for different power supply voltage values.*

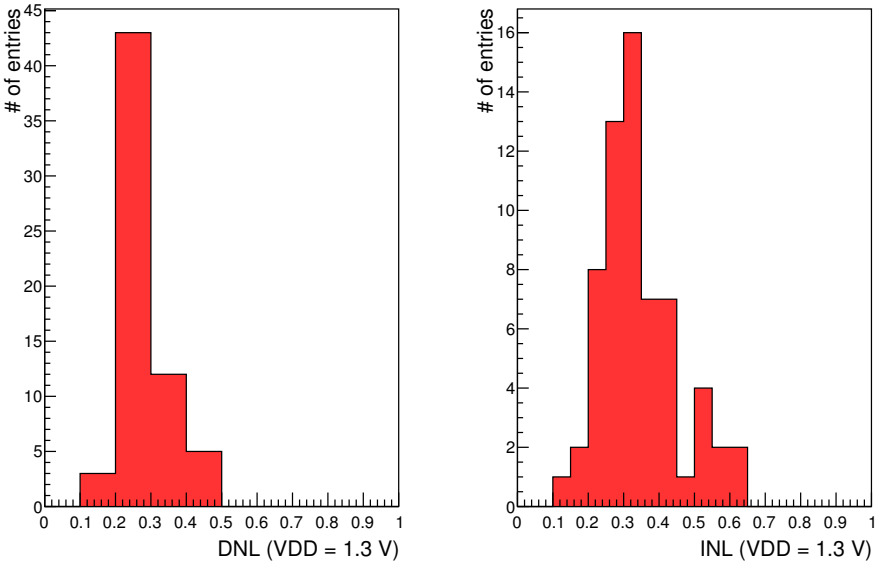


Figure 4.25. *DNl and INL distributions at* 1.3 V

4.4). In a full chip there is only one PLL: once this PLL is locked, it is producing a certain V_{cntr} which is distributed to all the oscillators in the chip.

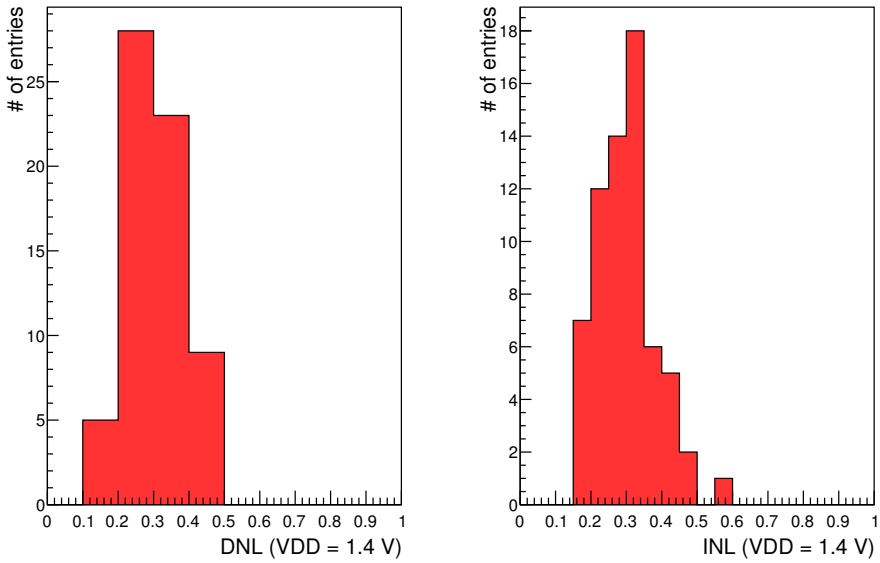


Figure 4.26. *DNl and INL distributions at* 1.4 V

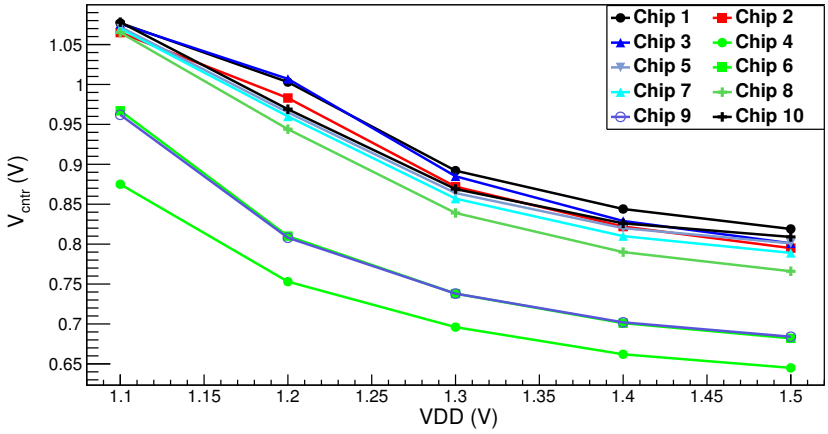


Figure 4.27. *Change of the control voltage as a function of the supply voltage for the 10 tested chips.*

4.6.7 Control voltage scan

To conclude measurements on the performance of the PLL another behavior to study is the dependence of the frequency, hence the bin size, of the fast clock

on the control voltage generated by the PLL. In order to do so we first turn off the voltage coming from the PLL and we provide it externally. The test has been performed on several chips for pixel 0 with V_{cntr} going from 400 mV to 1.2 V in steps of 50 mV. The results are shown in figure 4.28 together with the extracted view simulations for different corners. Simulations and data are in good agreement regarding the trend. The system can lock on the target 640 MHz frequency for the full range of possible control voltages except that in the slow corner.

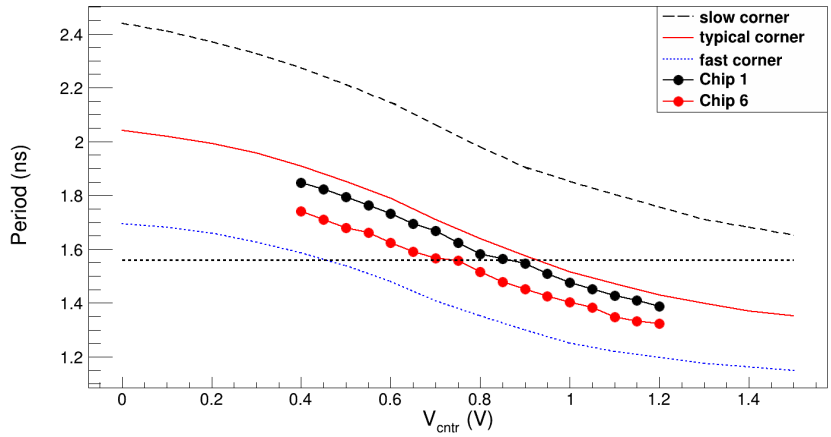


Figure 4.28. *Extracted view simulations and measurements results showing the variation of the period of the fast clock with varying control voltage. For different simulation corners the system can lock on the target period indicated by the horizontal line.*

As expected, when lowering the control voltage of the oscillator the size of the bin is increasing, signaling that the oscillation frequency is lower. This means not all the bins will we present in the 25 ns of run time. An example of such a result is shown in figure 4.29. The variation is approximately 0.5 ns per 100 mV and is in good agreement with simulations.

In order to calculate the average bin size the first and the last bin have been taken out from the analysis. For the first bin we want to avoid being sensitive to the startup of the oscillator. The last bin has been taken out because we don't know the oscillation frequency and we don't know the arrival time with respect to the system clock, which are the two effects which influence the length of this bin.

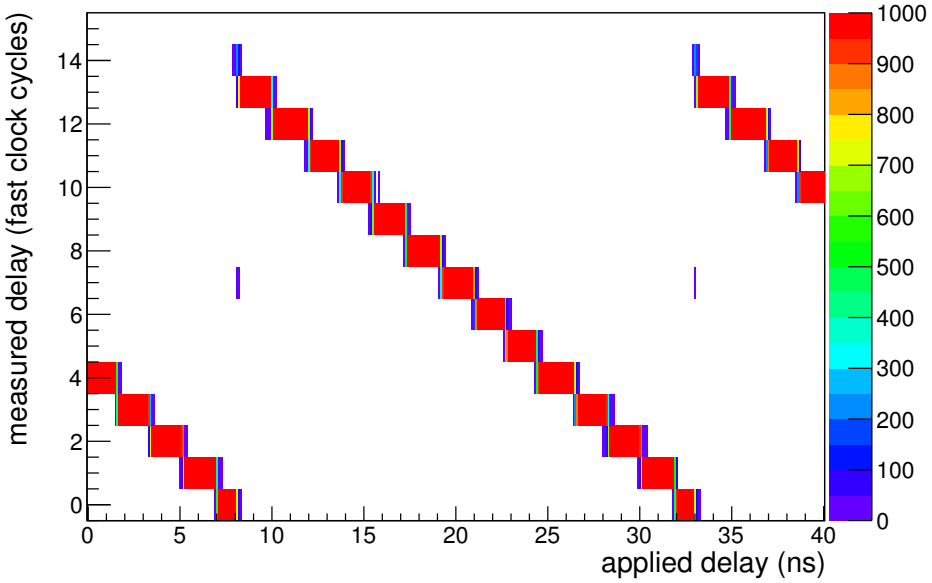


Figure 4.29. *Example of the test result obtained for chip 1 with V_{cntr}=450 mV. Notice the missing bin and one which is barely present.*

4.7 Conclusion

In this chapter the design, simulations and measurement results of GOSSIPO-4 have been presented. The prototype chip contains one super pixel, which is a group of 8 pixels sharing a common oscillator, a solution which has been adopted to minimize area and power consumption. To remove the dependence of the oscillation frequency on the power supply voltage it has been decided to use an on-chip PLL to generate a control voltage which is distributed to all the oscillators, together with a new oscillator topology made of RC elements where the capacitance value can be controlled by the voltage across it.

The measurements are in good agreement with the simulations and prove that the high-density, low-power standard-cell library developed at CERN is suitable to work at high frequency. The DNL and INL values show that the characteristic of the TDC is good and it is not influenced by a 100-200 mV drop of the power supply voltage and there are no missing codes. The synchronization mechanism works as expected and distributes the fast clock to the counters without glitches. A small but visible oscillator startup effect influences the width of bin 1 of the TDC; this effect has not been reproduced by the simulations. The

PLL measurements confirm the simulations and are within the specifications for the circuit.

Chapter 5

Timepix3 for a GridPix detector

The combination of gaseous drift layers and pixel chips may offer distinct advantages in some applications. However, as discussed briefly in section 2.4, GridPix detectors suffer from some limitations. While some of the limits come with the use of a gas as detector medium (the resolution is affected by diffusion, for example) others are limitations that come with the use of Timepix as readout chip, in particular the resolution achievable in the time (z) direction due to the maximum available clock frequency of 100 MHz. To give an indication of these effects, results from a beam test done at the CERN SPS beam with a GridPix telescope will be presented. These results will serve as a justification for the design of Timepix3, which will be introduced together with first results on the Time to Digital Converter (TDC) characterization.

5.1 Beam test setup

The telescope used during the beam test experiment consisted of three GridPix detectors with a drift height of 1.2 mm and two scintillators that provided the trigger as shown in figure 5.1. The detectors are placed at a distance of 165 mm from each other. To avoid perpendicular tracks, which would cause different ionization electrons to end up in the same pixel, the detectors are tilted by 45°around the vertical axis and by 10°around the horizontal axis defined by the first rotation. The data presented in the next sections have been recorded with an amplification electric field of $100\,\mathrm{kV\,cm^{-1}}$ and a drift electric field of $800\,\mathrm{V\,cm^{-1}}$. The gas used was a CO_2/DME (50/50) mixture. The beam consists of muons

with a momentum of 180 GeV c^{-1}.

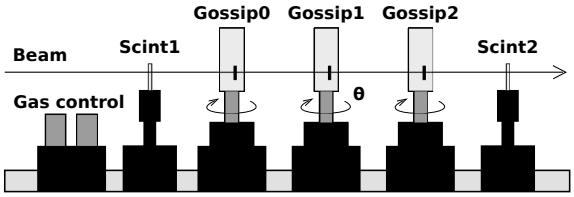


Figure 5.1. *Diagram of the beam test setup. The two scintillators provide the trigger. There are three Gossip detectors which have a drift height of* 1.2 mm.

The GridPix detectors are built on top of a Timepix chip. Timepix operations are shutter-based, which means that the chip records events when the shutter is open. The trigger setup depicted in figure 5.2 is designed to control the data taking/readout of the detectors and allows only one trigger to occur by closing the shutter after a trigger is detected as a coincidence of the two scintillators.

At the startup the circuit can be in any state. To proceed to normal operations Timer-2 has to be manually started. After 10 s it gives a signal at the set/reset unit, regardless of the status of the busy signals of the chips in the telescope. Timer-1 resets Timer-3 which generates the shutter. The shutter is sent to the telescope to signal that a data taking phase is started.

A coincidence (trigger) from the scintillators will start Timer-1 which will close the shutter after a fixed time of 5 µs. This time has been verified to be constant within 10 ns precision. The length of the shutter after the detection of a coincidence has been chosen to allow an electron generated close to the cathode to drift to the anode. If no coincidence is generated by the two scintillators then the shutter closes automatically after 10 s and the cycle restarts with timer-2.

After the shutter is closed, the readout phase takes place: the busy signal is asserted and its presence does not allow a new shutter and at the same time disables the coincidence unit. After all the detectors have been read out the busy signal goes to zero and consequently the shutter is opened again starting a new data taking phase.

5.1.1 Run characteristics

Figure 5.3 shows the time spectrum registered with detector Gossip0. The time spectrum has a limit at $n_c = 520$ counts due to the 5 µs delay of the shutter from the moment the trigger is produced. The ideal flat box distribution that one should measure is smeared due to timewalk and diffusion. This is visible at low Time of Arrival (ToA) values. The net effect is that some electrons appear to be

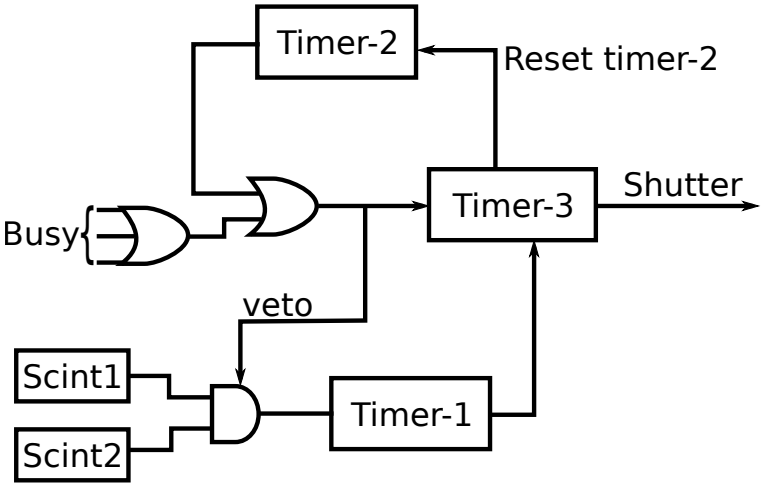


Figure 5.2. *Schematic of the trigger setup.*

produced outside the drift volume, which is clearly a non-physical effect. Since the purpose of the analysis is to evaluate the influence of the TDC resolution, timewalk and diffusion on the limitations they put in the precision of the track reconstruction, all hits with $n_c \geq 450$ will be included in the analysis.

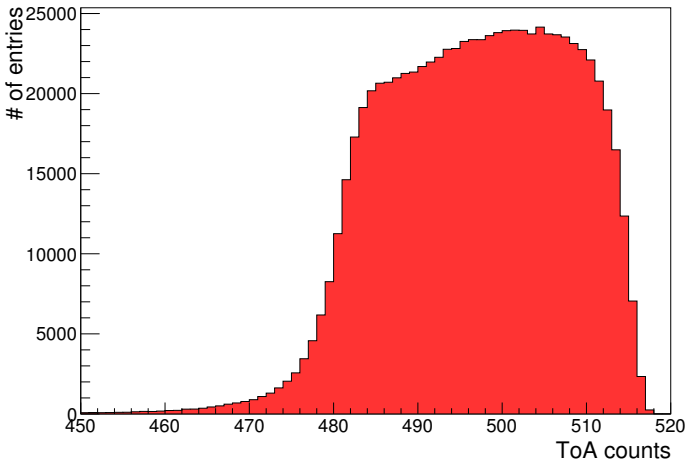


Figure 5.3. *Time spectrum of detector Gossip0. The limit at 520 counts is due to the* 5 µs *delay of the shutter.*

Given the electric field of $800\,\mathrm{V\,cm^{-1}}$ with a corresponding drift velocity of $3.78\,\mu\mathrm{m\,ns^{-1}}$ [45] and a drift gap of 1.2 mm the expected width of the time spectrum is $n_c \approx 32$, roughly in agreement with figure 5.3[1].

Figure 5.4 shows an example of the occupancy for Gossip0 where the shape of the triggering scintillators is clearly recognizable.

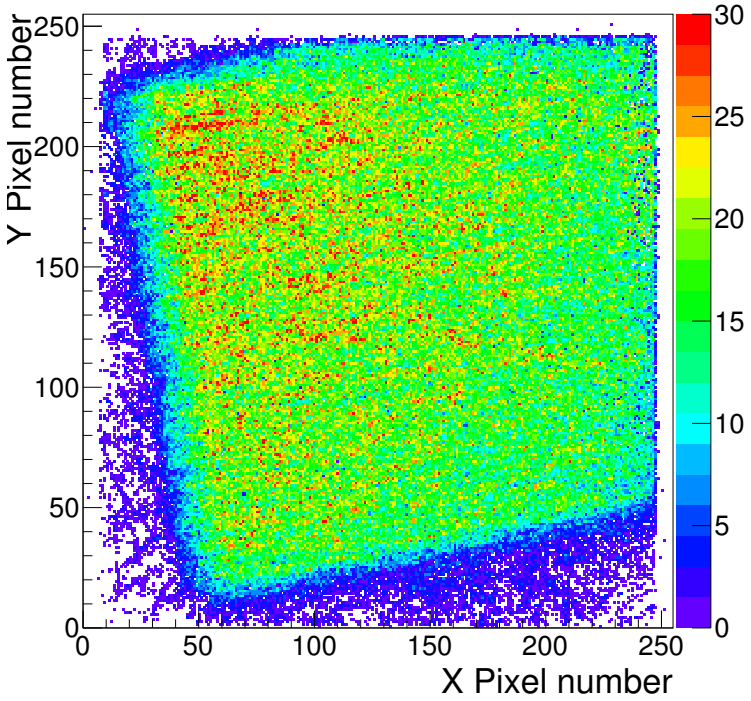


Figure 5.4. *Occupancy plot for detector Gossip0.*

Figure 5.5 shows the number of pixels hit per event recorded with Gossip0. From this plot it has been decided to cut from the following analysis events with less than 3 and more than 15 hits. The lower limit has been chosen because a straight line fit with less than 3 hits cannot be performed. The higher limit has been chosen because events with a high number of hits are usually recorded when δ electron emission occurs: due to the purpose of this study it has been decided to discard those events. As shown in section 2.2.1 the average number

[1] Extensive details about the procedure utilized to choose the values for the drift and amplification electric fields, simulation results for drift velocity and much more on the beam test results are given in reference [45]

of ionization expected in CO_2/DME (50/50) is 7 which is compatible with what the plot shows, which has a mean of 8.

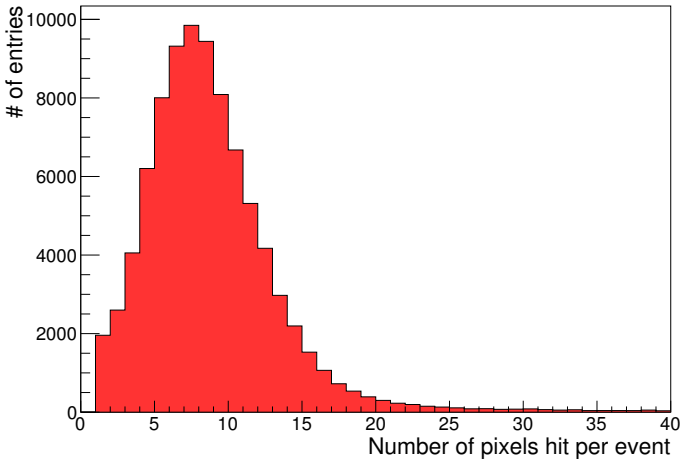


Figure 5.5. *Number of pixels hit per event for detector Gossip0.*

5.1.2 Angle distribution

After the cuts described in the previous section a straight line fit through the remaining hits in the XZ plane has been performed. In the chosen plane the nominal angle of the detectors is 45°. Figure 5.6 shows the distribution of the angle of the tracks. The peak is around the expected value of -45°. However, there are tracks with an angle which is clearly off. These are events with double tracks or events with spurious hits which affect the fit. For the purpose of this work these tracks are not important, so after the first fit all the tracks which have an angle smaller than -50° or bigger than -40° are discarded.

5.1.3 Diffusion and timewalk

To estimate the effect of timewalk and diffusion on the residuals of the track fit, the residual distribution has been studied. Given a track in a detector, one measures the distance from the reconstructed trajectory to one of the hits, if that hit has been excluded from the reconstruction. This distance is called unbiased residual. In the ideal case where the ionization electrons are produced at rest and there are no additional mechanisms, such as timewalk and diffusion, the

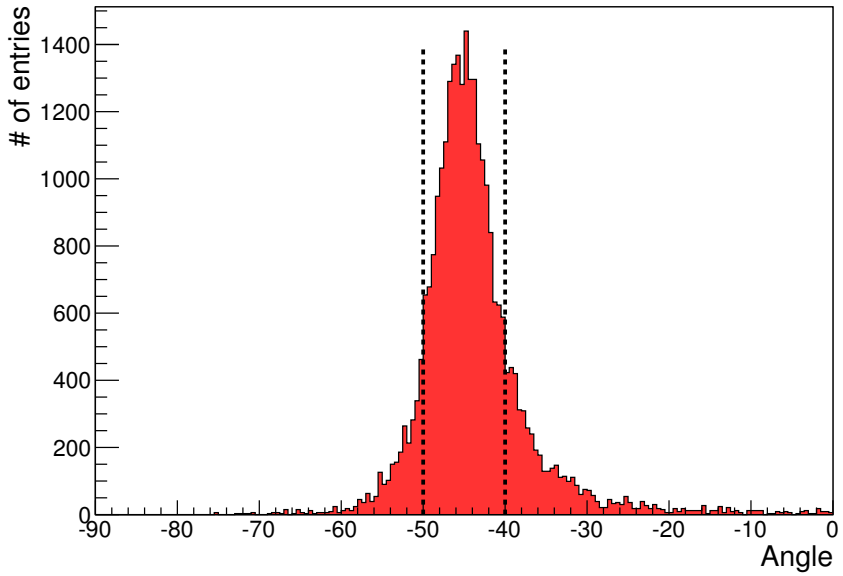


Figure 5.6. *Angle distribution for the tracks in Gossip0. The dashed lines define the cuts on the track angle.*

residuals should be zero. In reality this is not the case and studying the resulting distribution gives information on the magnitude of the two processes.

After the cuts previously described the following procedure was followed on all the remaining tracks with 4 or more hits:

- first, one hit is taken out from the track;
- a linear track fit is performed using the remaining hits;
- given the x position of the selected hit and the fitted track, the z position can be determined ($z_{\text{predicted}}$);
- the residual ($z_{\text{predicted}} - z_{\text{measured}}$) is calculated.

At the end of this procedure, one obtains a distribution as the one shown in figure 5.7 for detector Gossip0, for events with 5 hits with the hit under study close to the cathode.

Similar distributions have been produced for hits under study close to the grid. To determine in which part of the drift volume the hit was produced it is sufficient to notice that tracks with low x values are high in the drift volume

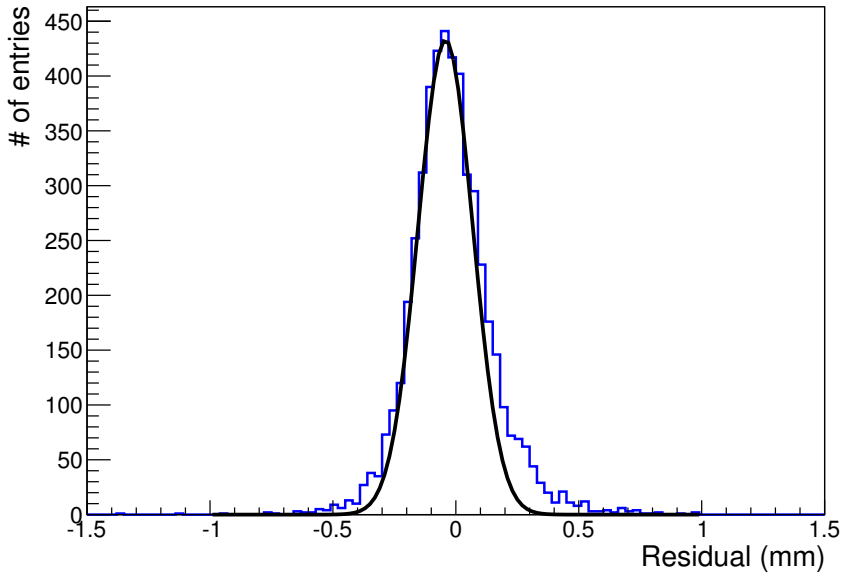


Figure 5.7. *Residual distribution for detector Gossip0 for tracks with 5 hits and hit under study close to the cathode. Superimposed is a Gaussian with parameters given by the fit done with an exponentially modified Gaussian. The tail is not well described without the exponential part given by timewalk.*

due to the angle between the beam and the detectors. Notice that for this part of the analysis only tracks with more than 5 and less than 11 hits have been used. With less than 5 hits this definition of a hit close to the cathode or close to the grid is not reliable enough and the resulting distribution leads to fit results with exceedingly high uncertainties. With more than 11 hits, instead, there is simply not enough statistics.

To extract information about diffusion and timewalk a fit with an exponentially modified Gaussian as shown in equation 5.1 has been done:

$$f(x;\mu,\sigma,\lambda) = \frac{\lambda}{2} e^{\frac{\lambda}{2}(2\mu+\lambda\sigma^2-2x)} \operatorname{erfc}\left(\frac{\mu+\lambda\sigma^2-x}{\sqrt{2}\sigma}\right) \tag{5.1}$$

The important parameters are σ and λ. The first parameter is related to diffusion via $\sigma = \sqrt{2D_l t}$ where D_l is the longitudinal diffusion coefficient of the gas. The inverse of the second parameter gives the time constant related to

timewalk.

The discrimination between electrons produced close to the grid or close the cathode has been made to extract the diffusion coefficient. Electrons which are produced close to the grid have negligible diffusion, so the only process that can influence the residuals is timewalk. In reality, a Gaussian component is present also for those hits due to a collection of other effects. For example, the hits under study might be not so close to the cathode due to the selection criteria, or the electrons produced by ionization might have an initial energy and might then travel for a short distance in any direction before starting the drift toward the grid. Also the resolution of the time measurements introduces an additional effect. The $\sigma_{\text{diffusion}}$ is then obtained as $\sigma^2_{\text{diffusion}} = \sigma^2_{\text{cathode}} - \sigma^2_{\text{grid}}$.

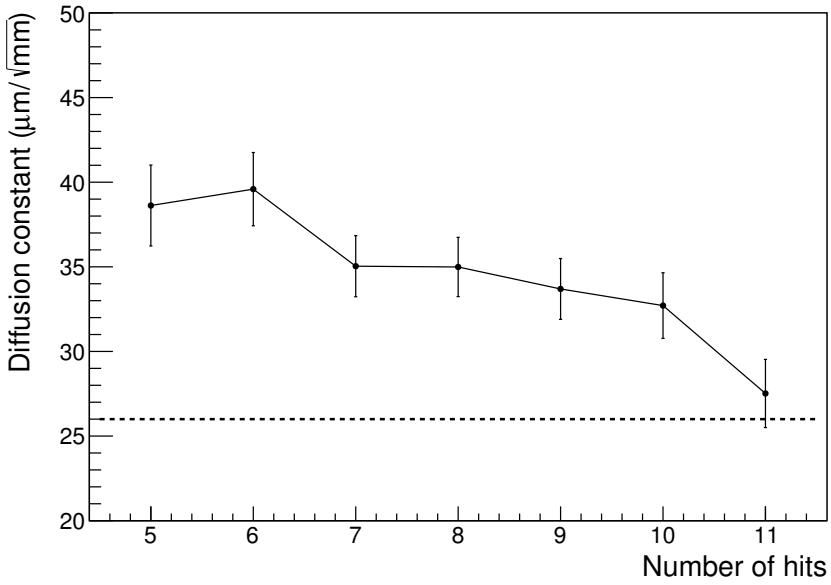


Figure 5.8. *Longitudinal diffusion coefficient versus the number of hits in the track. The dashed line is the value extracted with MagBoltz and confirmed with a different method in [45].*

Inverting the relation that connects $\sigma_{\text{diffusion}}$ and D_l one obtains $D_l = \frac{\sigma^2_{\text{diffusion}}}{2t}$. The time value t has been estimated taking the mean of the time distribution of the hits under study. Given that D_l is expressed in $\mu\text{m}\,\text{mm}^{-1/2}$ the time is multiplied by the drift velocity, giving

$$D_l = \frac{\sigma^2_{\text{diffusion}}}{2tv_d} \tag{5.2}$$

This quantity is shown in figure 5.8 versus the number of hits in the track. The errors are calculated by propagating the error on σ, t and v_d where the first is coming from the fit, the second is the RMS of the distribution and the third is taken from reference [45] and is constant ($0.13\,\mu\text{m}\,\text{ns}^{-1}$). The major contribution to the error on a single measurement comes from this last term.

The other parameter which is obtained from the fit is λ and this parameter is related to timewalk through $\tau = 1/\lambda v_d$. The errors are obtained by propagating the error on λ coming from the fit and the error on v_d, with the latter being dominant. Figure 5.9 shows the results obtained, which are compatible with what has been found in [45] and with what has been shown in [40] using an external test pulse.

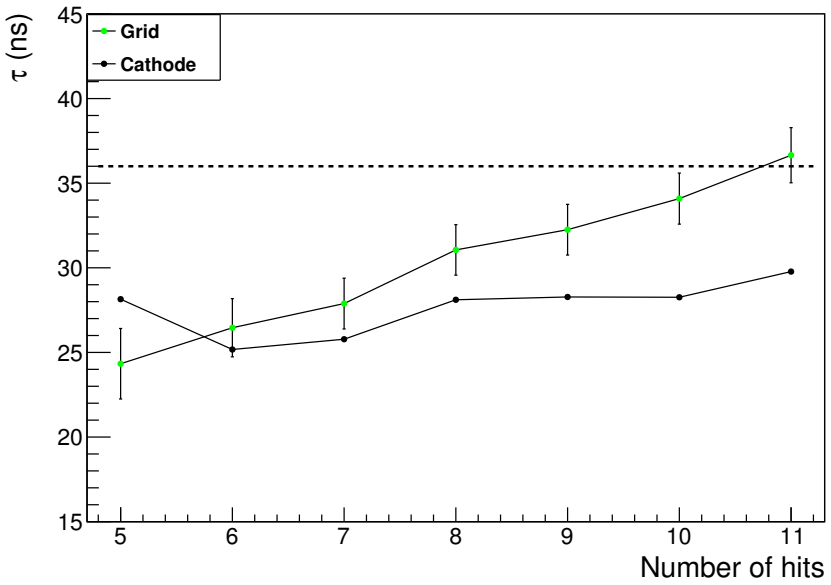


Figure 5.9. *Timewalk characteristic parameter. The dashed line is the value found with a toy Monte Carlo which can be found in [45].*

The results described in this section show that the contributions of diffusion and timewalk are similar. The contribution from diffusion cannot be corrected for, but could be reduced with a choice of a different gas. Instead, the con-

tribution from timewalk can be mitigated with a faster analogue frontend, a better time resolution and, at the same time, the recording of the Time over Threshold (ToT) information together with ToA. A better time resolution would improve the reconstruction of hits in the z direction, thus reducing the residuals. The ToT information, on the other hand, is used to correct for timewalk: through characterization of the single pixels a calibration curve of charge versus ToT can be produced, allowing an offline timewalk correction. It is on this argument that the GOSSIPO prototypes and ultimately Timepix3 have been designed.

5.1.4 Simulations

The results of the previous sections show the limitations of GridPix detectors and in particular the limits posed by the use of Timepix as the readout chip. To justify the design of a new readout chip a toy Monte Carlo (MC) simulation has been developed. The first objective is to check if the main mechanisms at play in the detector were understood. The second objective is to show that with the simultaneous recording of ToA and ToT one can use the second to improve the accuracy of the former. In this MC 100k tracks have been generated with a 45 degrees angle. Along the track a certain number of single electrons have been generated with a flat box distribution from 0 to 1.2 mm. The number of electrons is taken from a Poisson distribution with mean 8; additionally a minimum number of 5 electrons was required. To each electron, longitudinal diffusion and timewalk are applied. The former is taken from a Gaussian with mean 0 and diffusion coefficient $27\,\mu m\,mm^{-1/2}$ while the latter comes from an exponential distribution with $\tau = 36\,ns$, to match the results obtained in the data analysis. Every electron drift time, then, has been quantized with 10 ns resolution and the hit position has been quantized with a pixel pitch of 55 µm along x. The resulting time spectrum can be seen in figure 5.10.

The shape is clearly similar to the time spectrum of the data of figure 5.3. The same analysis done on the beam test data has then been performed on the MC data. The results for the diffusion coefficient and timewalk are shown in picture 5.11. The error sources are the same as explained previously in the beam test data analysis. The plots show that the simulation can reproduce the characteristics of the real data quite well.

As a check for the reliability of the analysis several values of diffusion and timewalk have been plugged into the simulation and the analysis performed on the newly generated data. Results showed that the analysis could take into account changes in the values of the two parameters unless for extreme and unrealistic cases such as zero timewalk or diffusion or very high values (more than 2 times the original values).

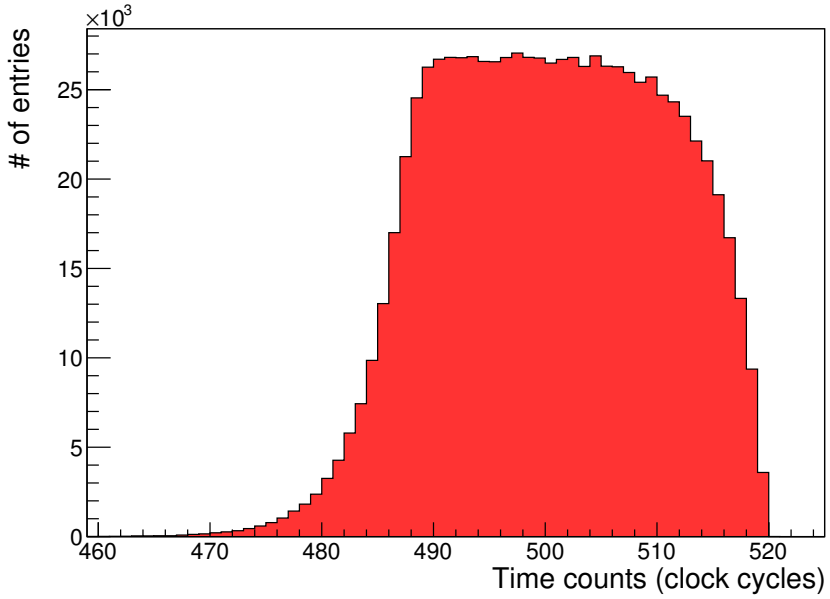
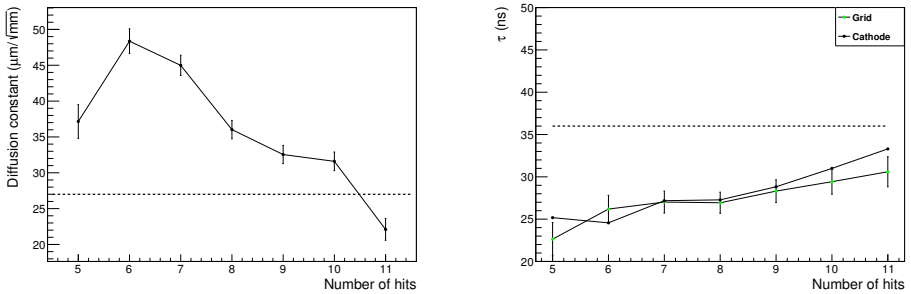


Figure 5.10. *Simulated time spectrum.*



(a) (b)

Figure 5.11. *On the left, the diffusion coefficient as extrapolated from the simulated tracks. On the right the timewalk parameter. The dashed lines represent the original values used to generate the data.*

5.1.5 Simulations with ToT

The MC described in section 5.1.4 has then been improved to include the ToT information for every generated electron. This has been done using the data

coming from several ToT runs taken during the beam test. Figure 5.12 shows the ToT spectrum for detector Gossip0. The excess of data at the end of the distribution is due to hits with very large ToT. The signal is so big that the shutter is closed before it has the time to go below threshold.

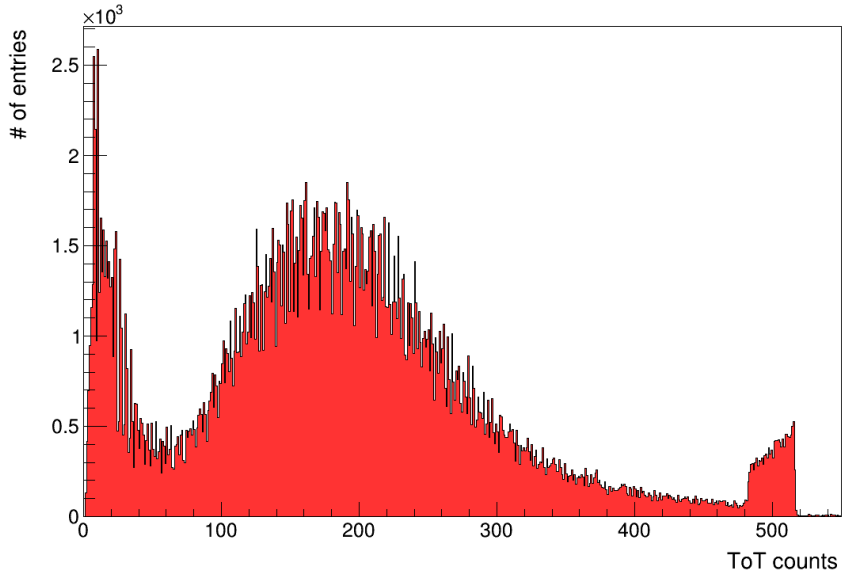


Figure 5.12. *ToT time spectrum for detector Gossip0, run 106.*

The normalized cumulative spectrum shown in figure 5.13 is then used to choose the ToT values for the electrons by generating a random number between 0 and 1 using a flat box distribution.

Given a ToT value it is then possible to generate a corresponding value of the timewalk. Considering the normalized exponential timewalk distribution, its integral corresponds to the integral of the normalized ToT distribution. If $f(t')$ is the timewalk distribution then the integral I is

$$I = \int_t^\infty f(t')\,\mathrm{d}t' = \frac{1}{\tau}\int_t^\infty e^{t'/\tau}\,\mathrm{d}t' = e^{-t/\tau} \tag{5.3}$$

which after inversion gives $t = -\tau \log I$, where t is the wanted timewalk value. In this way, for each generated ToT value we obtain a correlated timewalk value as shown in figure 5.14.

Once this relation between ToT and timewalk is known, we can generate for

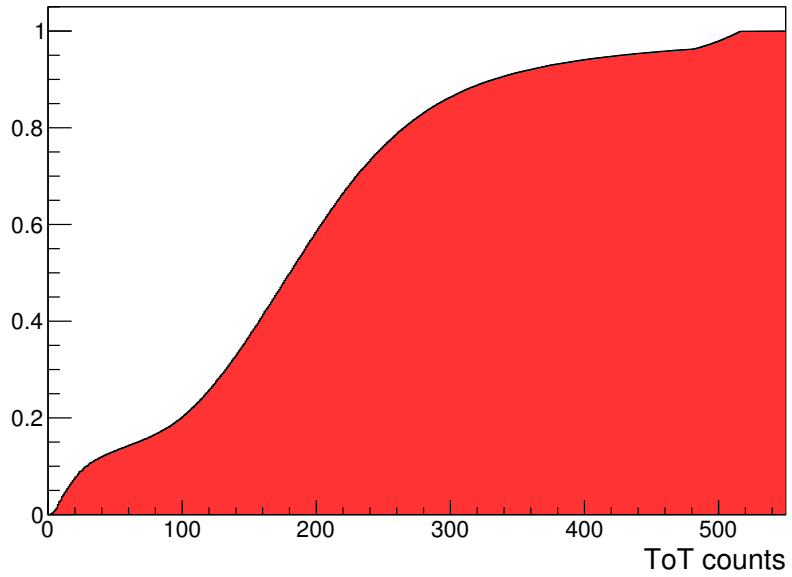


Figure 5.13. *Cumulative ToT spectrum of run 106.*

each electron its own ToT or, in other words, the final electron avalanche created in the amplification region of the detector and with it the corresponding time-walk value. Once the data are generated, one can perform the same analysis described in section 5.1.3. However, now it is possible to subtract from every measured ToA value the corresponding amount of timewalk via the corresponding ToT. This has a visible effect both in the angle distribution of the tracks (figure 5.15) and on the residual distribution (figure 5.16).

5.2 Timepix3

Timepix3 is a general purpose chip developed at CERN in collaboration with Nikhef and Bonn University and funded by the Medipix collaboration. It has been taped out in summer 2013. The chip is designed in the 8 metal, 130 nm CMOS technology and contains a matrix of 256 $\times$ 256 pixels of 55 x 55 μm^2. The periphery of the chip is located on one side of the pixel matrix making the chip 3 side buttable. The relevant features include simultaneous recording of ToA and ToT, data driven readout and a per-pixel high resolution TDC based on the circuitry developed for GOSSIPO-4. Timepix3 provides a combined absolute/relative measurement of the ToA of a hit. The absolute time measurement

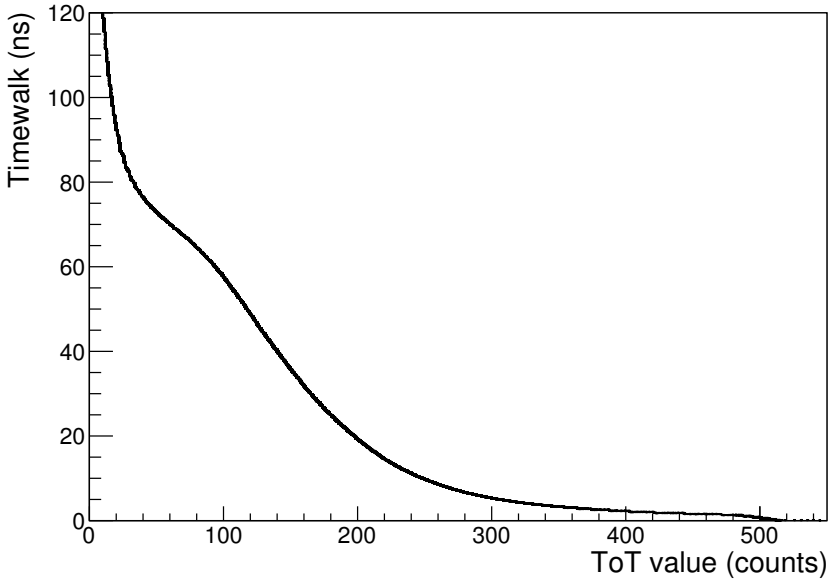


Figure 5.14. *Correlation plot between ToT and timewalk values.*

gives the coarse resolution and is achieved using a counter in the periphery which counts the slow clock cycles and distributes its value across the entire chip. The high resolution measurement is given instead with respect to the closest rising edge of the system clock as in the GOSSIPO prototypes: the local oscillator is started when the hit arrives and it is stopped by the slow clock. When the hit arrives, the value of the periphery counter is stored locally on pixel and together with the fast counter value it provides the desired high resolution time information. The ToA value is then given by:

$$\mathrm{ToA} = \mathrm{ToA}_{\mathrm{abs}} + (25 - 1.6 \cdot \mathrm{ToA}_{\mathrm{fast}}) \tag{5.4}$$

The chip has different operation modes available: simultaneous recording of ToA & ToT, only ToA, event counting and integral charge (iToT). The readout has zero suppression and can be both data driven or frame based with a maximum speed of 5.2 Gbps. In the following sections a brief description of the chip will be given focusing mainly on the high resolution TDC together with the characterization of the converter.

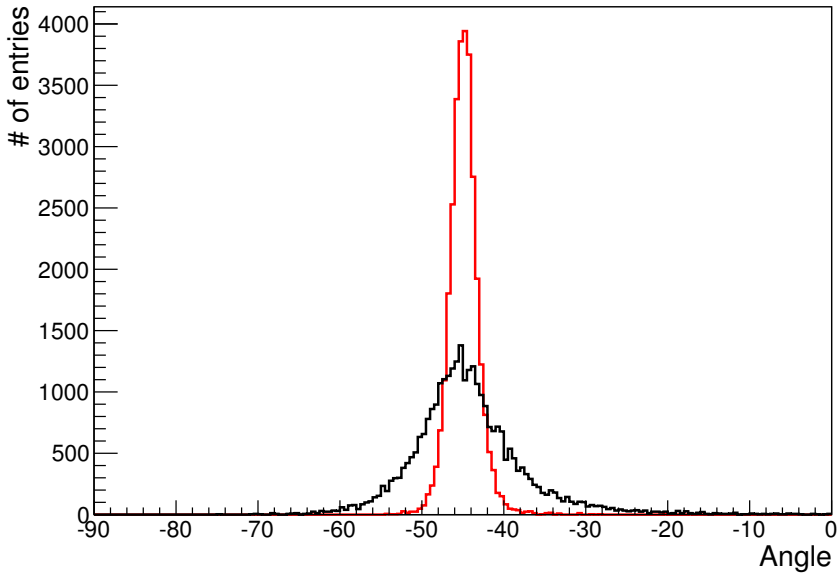


Figure 5.15. *Angle distribution for tracks whose hits have been corrected for time-walk (red) or not (black).*

5.2.1 Super pixel and pixel cell

In Timepix3 it has been decided to group 8 pixels together to form a super pixel. As in GOSSIPO-4 the 8 pixels share a common voltage controlled oscillator but additionally they also share a FIFO memory to locally store the hits waiting to be transferred to the periphery of the chip. The oscillator in the super pixel is the same oscillator tested in GOSSIPO-4 with some minor layout changes to fit the Timepix3 requirements.

Figure 5.17 shows Timepix3 single pixel block diagram. The analog frontend contains a Charge Sensitive Amplifier (CSA) with gain 50 mV per ke^- and a discriminator with 4 bits local threshold tuning. A 3 fF capacitance allows the injection of an external test pulse. The frontend can detect signals of both polarities. The digital part, alongside the counters, contains the synchronization logic which synchronizes the discriminator output to the high frequency clock from the oscillator (as in GOSSIPO-4, see section 4.3.2) and also provides clock gating to reduce the power consumption. The pixel dead time is given by the sum of the ToT time and the data transfer from the local pixel to the super pixel FIFO. The latter is 475 ns.

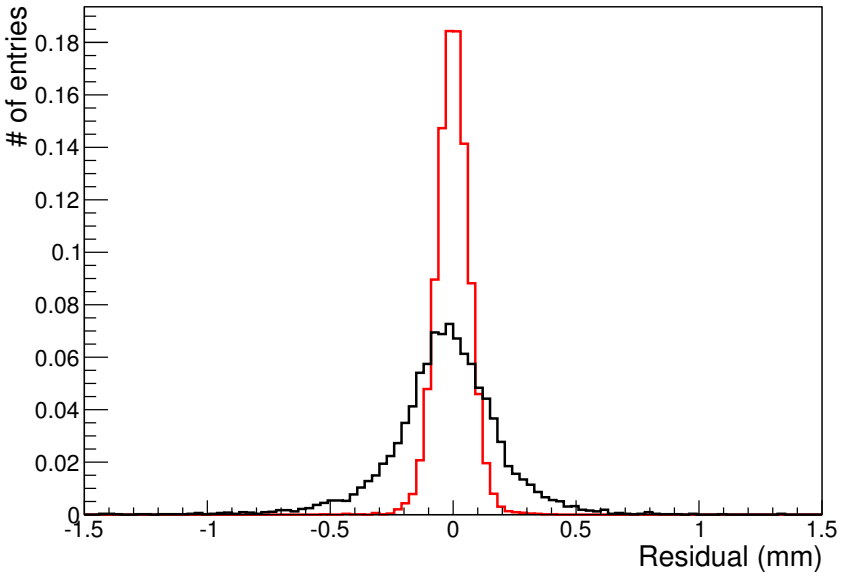


Figure 5.16. *Residual distribution for tracks with 5 hits and hit under study close to the cathode corrected for timewalk (red) or not (black). The two distributions have been normalized for comparison.*

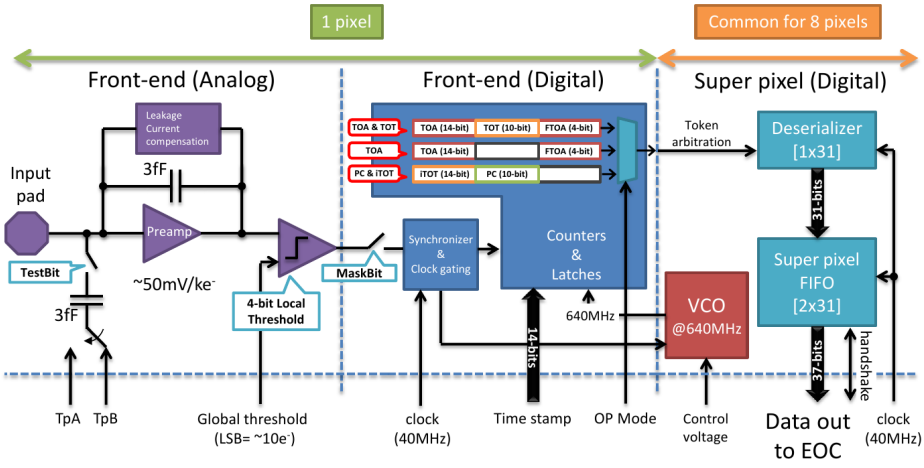


Figure 5.17. *Pixel block diagram of Timepix3.*

5.2.2 Synchronization logic

The approach used in Timepix3 for the synchronization logic is different than the one used in GOSSIPO-4. While in the prototype chip it was decided to use an asynchronous state machine without using any flip flop, the Timepix3 synchronization logic is based on a 4 flip-flop structure which is shown in figure 5.18.

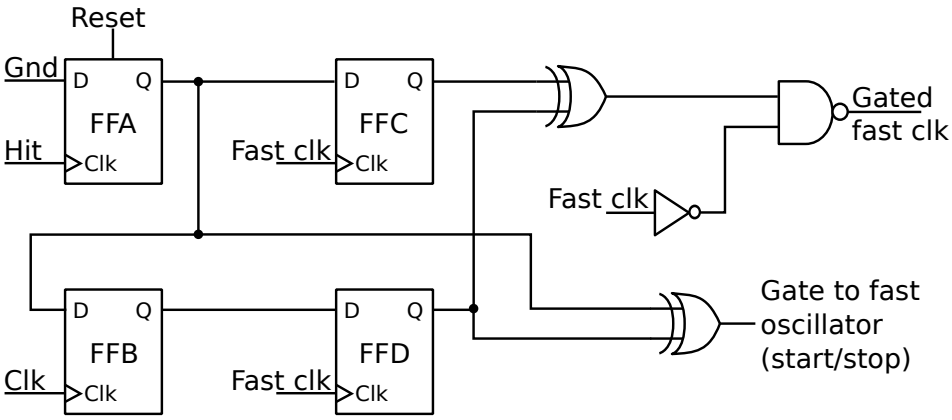


Figure 5.18. *Schematic of the synchronization logic used in Timepix3.*

FFA and FFB are responsible to create the Gate, which is then sent to the oscillator to start it, while FFC and FFD are responsible for the synchronization of the fast clock which is then sent to the fast counter.

In the initial situation the output of FFA is at 1 and both the gate and the gated clock are at 0. When the hit arrives at the clock pin of FFA the output changes to 0 which turns the Gate to 1. At this point the oscillator starts: the clock is active for FFC and FFD. After the first pulse the output of FFC changes to 0, which activates the output NAND and transmits the fast clock to the counter.

When the rising edge of the system clock arrives to FFB the 0 is transferred to the input of FFD and then to the output at the next rising edge of the fast clock. This deactivates the NAND and sets the gate to 0, so that the oscillator stops. FFA is then reset by the pixel logic.

The synchronization logic implemented in Timepix3 has some additional gates to provide clock gating to reduce the power consumption.

5.3 Characterization of Timepix3

Timepix3 is read out using the SPIDR readout system (Speedy PIxel Detector Readout) which consists of a VC707 evaluation board equipped with a Xilinx Virtex-7 FPGA that communicates with Timepix3 and to a PC via a 10 Gbit Ethernet connection. The FPGA firmware and the software API have been developed at Nikhef.

The characterization performed for Timepix3 follows the same procedure used for the GOSSIPO prototypes. A digital test pulse is sent to the pixel while moving the arrival time with respect to the system clock in steps of 20 ps. In order not to compromise chip operations only 1000 pixels are activated at the same time and in any case only one pixel is active in a given super pixel. An example of the results obtained is shown in figure 5.19.

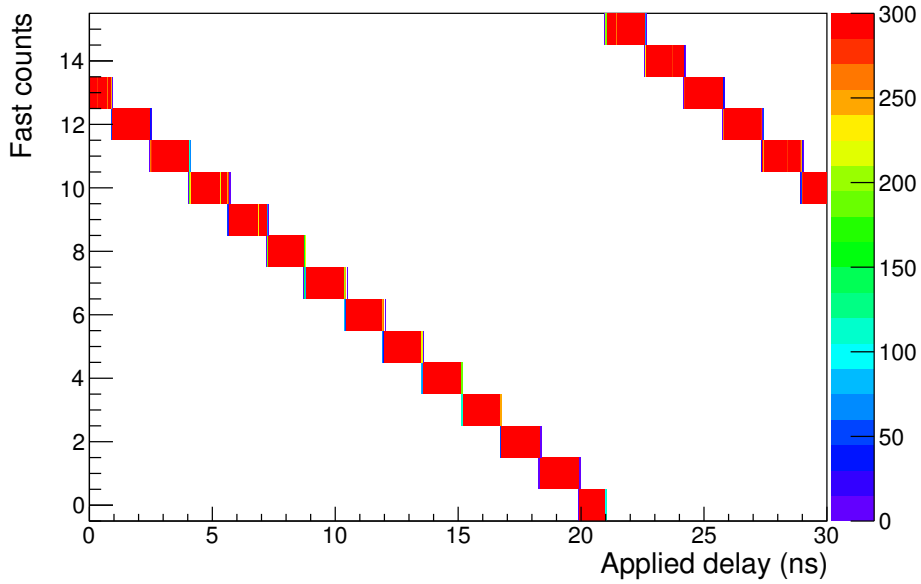


Figure 5.19. *Delay scan for a single pixel (0,0) of Timepix3.*

After collecting the data for all the pixels, one can fit the single bins using the error function (see section 3.5) and measure the size of every bin of the TDC, which is then used to calculate the DNL and INL for all the converters.

Looking at the single bins of every TDC one can look at the chip variations caused by the test pulse and system clock distribution. It is of particular interest to look at the variation of bin 0 and bin 15, the former because it might point

to oscillator start up effects, the latter because it is the bin which is most influenced in variations on the oscillation frequency. For example, if the frequency is too high, the last bin would be significantly longer than the others; similarly, for a slow oscillator, it might become very short up to the point that it could be completely absent from the converter characteristic. Figure 5.20 shows the distribution of the size of bin 0 (left) and 15 (right). For comparison, the distribution of bin 6 is also shown. The presence of effects which influence the oscillation frequency is clear. Notice how the distribution of bin 6 is clearly peaked around the design value.

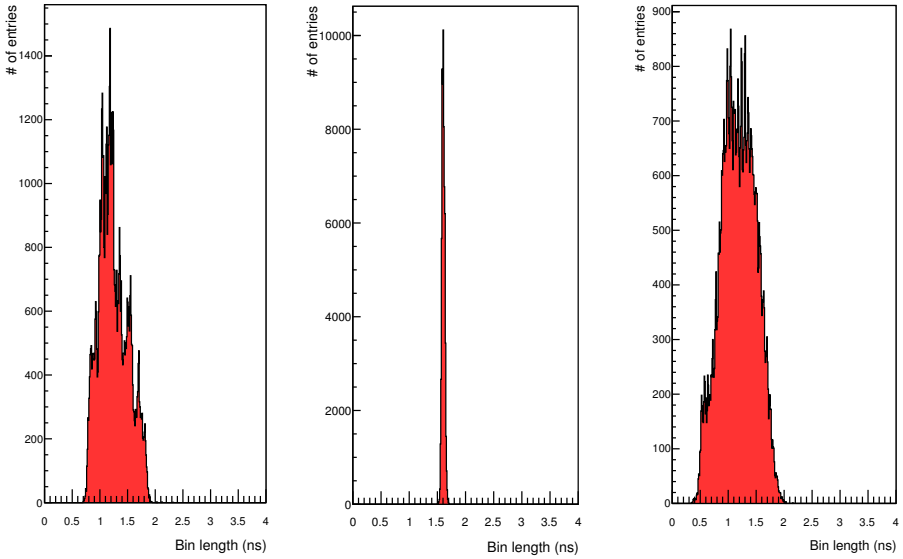


Figure 5.20. *Bin length distributions for bin 0 (left), 6 (center) and 15 (right).*

Figure 5.21 shows the DNL and INL distributions for all pixels. It is important to underline that for the DNL distribution only bin with size bigger than 1.4 ns have been considered, excluding de facto the cases where bin 1 was clearly influenced by the oscillator startup.

Also pixels with a missing bin have been excluded completely from the analysis. Figure 5.22 shows the pixels that are missing a bin in the TDC. Notice that for the purpose of the analysis, every bin shorter than 600 ps is considered as missing. A pattern in the spread of these bad pixels across the chip is clearly visible and it hints to effects connected to the distribution of the reference voltage from the Phase Locked Loop (PLL) to the oscillators.

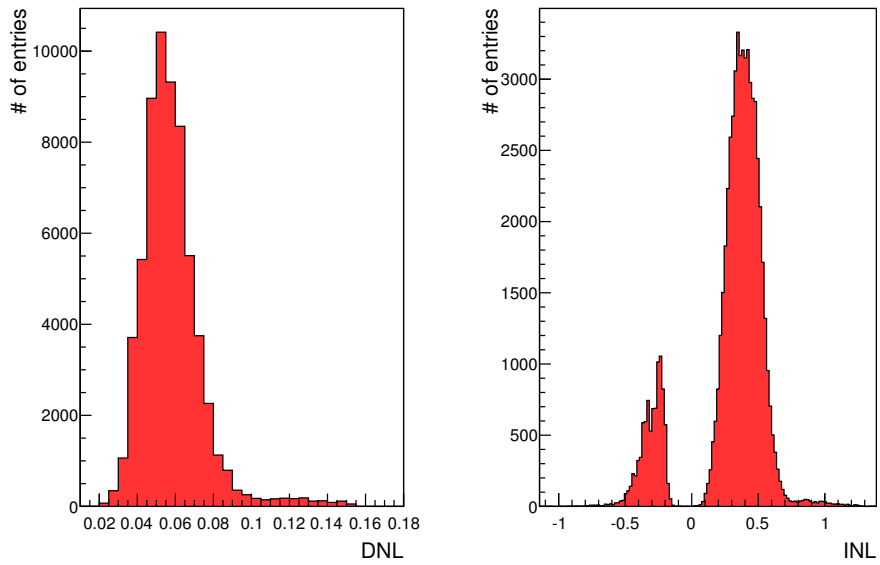


Figure 5.21. *DNL and INL distributions for all the Timepix3 pixels.*

Looking instead at the length of a single bin across the chip one can see the effect of the system clock distribution (figure 5.23). Although the spread is very low, a gaussian fit on the bin length distribution gives a $\sigma < 30\,\text{ps}$, the system clock distribution scheme on the chip has a visible, and unavoidable, effect.

5.4 Conclusion

The analysis of the data from a testbeam conducted with 3 GridPix detectors which were read out by the Timepix chip shows that a better resolution in the ToA measurements is needed. Moreover, the simultaneous recording of the ToT also has a beneficial impact since it allows to correct for timewalk. Based on these premises, a new full size chip called Timepix3 has been developed. This chip features a per-pixel high-resolution TDC based on the work done in GOSSIPO-3 and GOSSIPO-4. The first measurement results show that in general the chip is working properly and shows good TDC characteristics across the chip. However, secondary effects are present and influence the oscillation frequency, like oscillator start-up, the control voltage distribution and the clock distribution even though they don't compromise significantly chip operations.

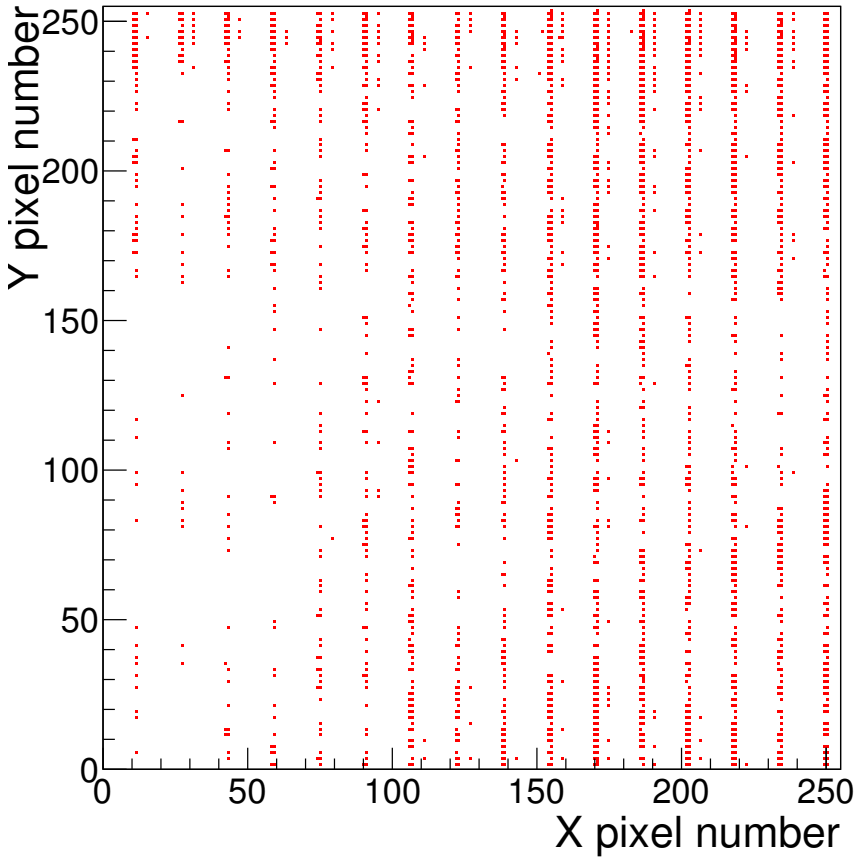


Figure 5.22. *Pixels with a missing bin in the TDC.*

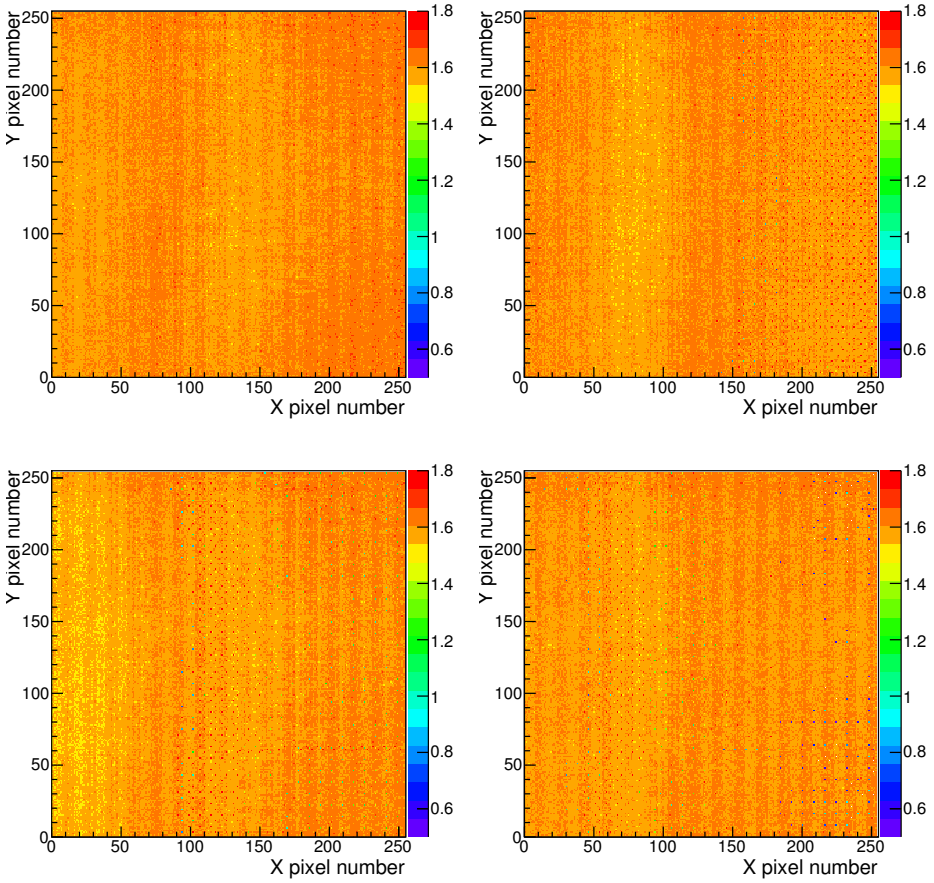


Figure 5.23. *Variation on the length of a single bin across the chip. Top left: bin 6; top right: bin 7; bottom left: bin 8, bottom right: bin 9.*

Appendices

Appendix A

Synchronization logic design

Since it was decided to not use flip-flops in an attempt of saving area and reduce power consumption, an asynchronous state machine has been designed. The design of asynchronous circuits is not compatible with the EDA tools available, so it had to be carried out manually. The functionality of the synchronization the can be split into two main blocks: one receives as input the 40 MHz clock and the hit and then generates the gate (40 MHz synchronizer). The second, receives the gate and the oscillator output and produces the 640 MHz gated clock (640 MHz synchronizer).

A.1 40 MHz synchronizer

Figure A.1 shows the input and output waveforms for the first part of the circuit. The working principle is that the output of the circuit (Gate) goes to 1 when the asynchronous hit arrives, and it goes back to 0 at the first rising edge of the system clock.

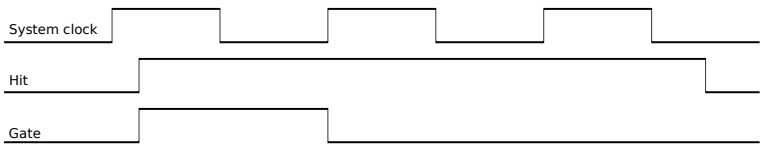


Figure A.1. *Waveform diagram with the 2 inputs and the output for the 40 MHz synchronizer.*

To design the circuit the procedure outlined in [69] has been followed; the first step is to build a Primitive Flow Table (see table A.1). To build a Primitive

	Inputs					Inputs			
State	00	01	11	10	Output	00	01	11	10
1	①	2	-	3	0	0	-	-	-
2	1	②	6	-	0	-	0	-	-
3	8	-	4	③	1	-	-	-	1
4	-	2	④	5	0	-	-	0	-
5	1	-	4	⑤	0	-	-	-	0
6	-	7	⑥	3	1	-	-	1	-
7	8	⑦	6	-	1	-	1	-	-
8	⑧	2	-	3	1	1	-	-	-

Table A.1. *Primitive Flow Table for the 40 MHz synchronizer. The right part, after the output column, is the corresponding Mealy table.*

Flow Table there is one basic assumption to make: for each state transition, only one input signal changes at a time. In our case, it is then impossible to go from a state where both the Hit and the Clock are zero to a state where both signals are 1. This is not true, since this system is intrinsically asynchronous, given the fact that the arrival time of the hit is random. But we can make this assumption here and take care of any race condition later in the design.

For a better understanding of table A.1 let's consider the situation of figure A.1. Both the clock and hit signals are low (stable state ① in the first row). When the clock goes high, the state machine moves to the stable state ② in the second row via the unstable state 2 in the first row. At this point the Hit goes high: the state machine goes into stable state ⑥ in the sixth row; notice how at this moment the output is 1. The clock then goes to 0, so the next state in ③, and the output has to stay at 1. Now the clock goes high again: the state machine enters in the stable state ④ and the output is then 0. At this point, there is a loop between stable state ④ and ⑤: the clock is changing, the hit stays high, but the output stays at zero. After a clock cycle, when the clock is low (stable state ⑤), the hit goes down as well: the state machine goes back to stable state ①.

Considering all the different combinations for the Hit and the Clock, it is then possible to build the Primitive Flow Table. After building the Flow Table we can proceed with finding equivalent stable states, that is states that for the same input produce the same output (none in this case). At this point, we build the Mealy table which is formed from the Moore table (i.e.: the table built so far, in which the output is a function of the present state only) by associating the output for each row with the corresponding stable total state in that row (the right part of table A.1). The remaining output in the Mealy table are filled

State	00	01	11	10	00	01	11	10
a (1,2)	①	②	6	3	0	0	-	-
b (3,8)	⑧	2	4	③	1	-	-	1
c (4,5)	1	2	④	⑤	-	-	0	0
d (6,7)	8	⑦	⑥	3	-	1	1	-

Table A.2. *Reduced Mealy table for the 40 MHz synchronizer.*

State	00	01	11	10	00	01	11	10
a	ⓐ	ⓐ	d	b	0	0	1	1
b	ⓑ	a	c	ⓑ	1	1	1	1
c	a	a	ⓒ	ⓒ	0	0	0	0
d	b	ⓓ	ⓓ	b	1	1	1	1

Table A.3. *Reduced Mealy table with state definition.*

with dashes. After building the Mealy table, we can reduce it (see table A.2) by grouping the rows of the Primitive Flow Table; the reduction can be done only if two rows have no state conflicts in any column. For example, row 1 and 2 can be merged because in the first two columns they have the same states, while in the third and fourth column one has a state while the other is empty (and vice versa).

After reduction, we substitute the state definition (first column of table A.2) and complete the output table to obtain table A.3. To complete the output table the transition of the state machine from one stable state to the next must occur without changing the output twice. Consider for example the first row of table A.3, column 00. If the first input goes high, the state machine goes from ⓐ (output = 0) to ⓑ (output = 1). In this case, the output table can be completed both with 1 or 0. If, instead, the state machine would go from a state with output 1 (0), to another state with the same output, the table must be completed with 1 (0), to avoid a possible race condition in the output.

The transition diagram makes clear that for every state assignment there is a race condition, which means that is not possible to move through the states without a situation where both bits have to change at the same time. To avoid the race conditions, it is necessary to add states in the table, which allow the state machine to move from one state to another while changing only one state bit. We will add these states by duplicating the existing one, as shown in table A.4: every state is split in two and the output stays the same.

Using the state assignment in the first column of table A.5 we then obtain the final table that describes the circuit.

From this, it is possible to construct the equivalent Karnaugh maps (figure

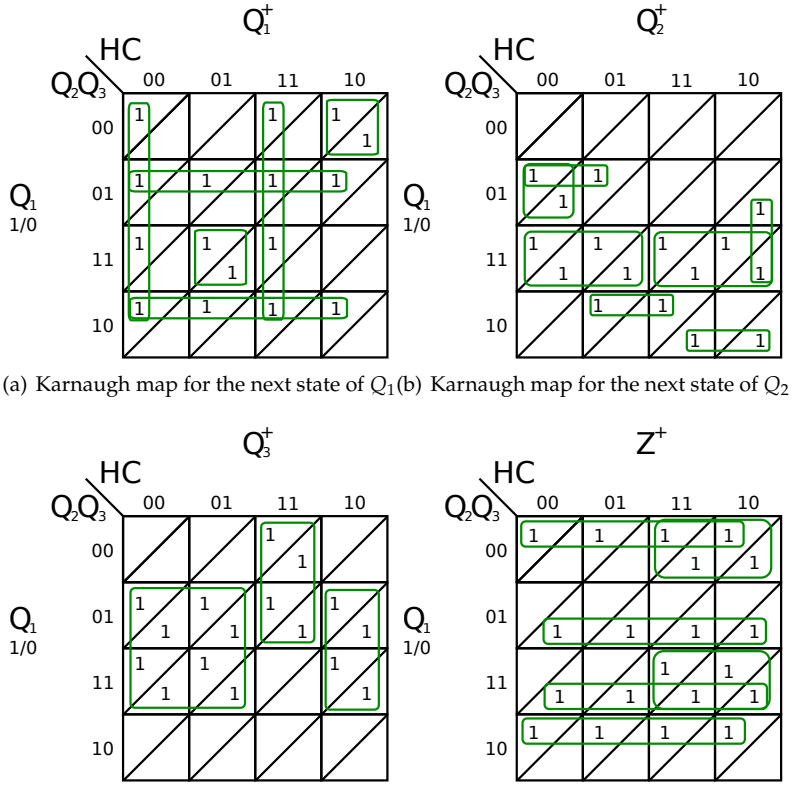
State	00	01	11	10	00	01	11	10
a_1	(a_1)	(a_1)	d_1	b_2	0	0	1	1
a_2	(a_2)	(a_1)	d_2	b_1	0	0	1	1
b_1	(b_1)	a_2	c_1	(b_1)	1	1	1	1
b_2	(b_2)	a_1	c_2	(b_2)	1	1	1	1
c_1	a_1	a_1	(c_1)	(c_1)	0	0	0	0
c_2	a_2	a_2	(c_2)	(c_2)	0	0	0	0
d_1	b_1	(d_1)	(d_1)	b_1	1	1	1	1
d_2	b_2	(d_2)	(d_2)	b_2	1	1	1	1

Table A.4. *Mealy table with race free state assignment.*

Q_1,Q_2,Q_3	Hit (H), Clock (C)				Output (Z)			
State	00	01	11	10	00	01	11	10
a_1 000	(000)	(000)	001	100	0	0	1	1
a_2 111	(111)	(111)	110	011	0	0	1	1
b_1 011	(011)	111	010	(011)	1	1	1	1
b_2 100	(100)	000	101	(100)	1	1	1	1
c_1 010	000	000	(010)	(010)	0	0	0	0
c_2 101	111	111	(101)	(101)	0	0	0	0
d_1 001	011	001	(001)	011	1	1	1	1
d_2 110	100	110	(110)	100	1	1	1	1

Table A.5. *Final Mealy table with race free state assignment.*

A.2) for the next state of each of the input variables and the output.



(a) Karnaugh map for the next state of Q_1 (b) Karnaugh map for the next state of Q_2

(c) Karnaugh map for the next state of Q_3 (d) Karnaugh map for the next state of Z

Figure A.2. *Karnaugh maps that describe the 40 MHz synchronizer. The maps descend directly from the state assignment of table A.5.*

From the Karnauhg maps we derive the equations for the description of the circuit (equations

$$Q_1^+ = Q_1(H'C' + HC + Q_2'Q_3 + Q_2Q_3') + Q_2'Q_3'HC' + Q_2Q_3H'C \tag{A.1}$$

$$Q_2^+ = Q_2Q_3 + H'Q_2'(Q_3C' + Q_1Q_3) + HQ_1'(Q_2Q_3' + Q_3C') + Q_1Q_2Q_3'C \tag{A.2}$$

State	00	01	11	10	Output	00	01	11	10
1	(1)	2	-	3	0	0	-	-	-
2	1	(2)	6	-	0	-	0	-	-
3	1	-	4	(3)	0	-	-	-	0
4	-	5	(4)	3	1	-	-	1	-
5	1	(5)	4	-	1	-	1	-	-
6	-	2	(6)	3	0	-	-	0	-

Table A.6. *Primitive Flow Table for the 640 MHz synchronizer. The right part is the corresponding Mealy table.*

$$Q_3^+ = H'Q_3 + H(Q_2'C + Q_3C') \tag{A.3}$$

$$\begin{aligned} Z^+ = H(Q_2'Q_3' + Q_2Q_3) + Q_3(Q_1'Q_2 + Q_1'Q_2') + Q_3'(Q_1Q_2' + Q_1Q_2) = \\ = H(Q_2'Q_3' + Q_2Q_3) + Q_3Q_2' + Q_3'Q_1 \end{aligned} \tag{A.4}$$

A.2 640 MHz synchronizer

The same method can be used for the 640 MHz synchronizer. Figure A.3 shows an example of the operations of this circuit.

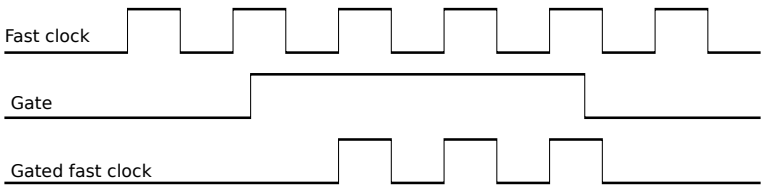


Figure A.3. *Waveform diagram with the 2 inputs and the output for the second circuit that compose the synchronization logic.*

The first step is writing the Primitive Flow Table (table A.6) and then the reduced one (table A.7)

State	00	01	11	10	00	01	11	10
a (1,2,6)	(a)	(a)	(a)	b	0	0	0	-
b (3)	a	-	c	(b)	-	-	-	0
c (4,5)	a	(c)	(c)	b	-	1	1	-

Table A.7. *Reduced Mealy table for the 640 MHz synchronizer with state definition.*

	Gate (G), Clock (C)				Output			
State	00	01	11	10	00	01	11	10
a	(a)	(a)	(a)	b	0	0	0	0
b	a	-	d	(b)	0	-	-	0
c	a	(c)	(c)	d	0	1	1	0
d	-	-	c	b	-	-	1	0

Table A.8. *Mealy table with race free state assignment for the 640 MHz synchronizer.*

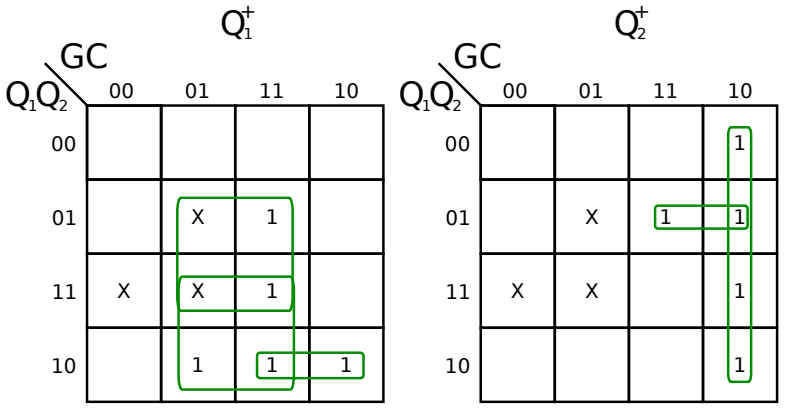
As in the previous case, any state assignment would cause a race condition, so the table as to be adjusted as shown in A.8 adding a state; using the state assignment in the first column of table A.9 the final table is obtained. From table A.9, the Karnaugh maps for the input and the output can be obtained, as shown in figure A.4.

From the Karnaugh maps, one obtains the equations that describe the circuit.

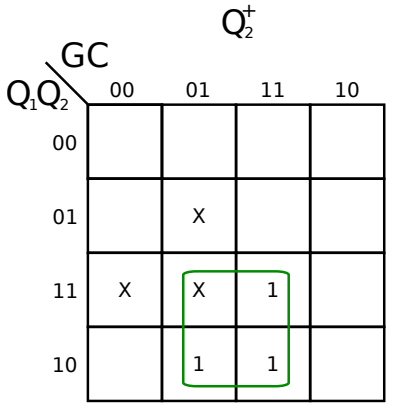
$$Q_1^+ = C(Q_1 + Q_2) + GQ_1Q_2' \tag{A.5}$$

Q_1Q_2	Gate (G), Clock (C)				Output			
State	00	01	11	10	00	01	11	10
a 00	(00)	(00)	(00)	01	0	0	0	0
b 01	00	-	11	(01)	0	-	-	0
c 10	00	(10)	(10)	11	0	1	1	0
d 11	-	-	10	01	-	-	1	0

Table A.9. *Final Mealy table with race free state assignment for the 640 MHz synchronizer.*



(a) Karnaugh map for the next state of Q_1 (b) Karnaugh map for the next state of Q_2



(c) Karnaugh map for the next state of Z

Figure A.4. *Karnaugh maps that describe the 640 MHz synchronizer. The maps descend directly from the state assignment of table A.9.*

$$Q_2^+ = G(C' + Q_1'Q_2) \tag{A.6}$$

$$Z^+ = Q_1C \tag{A.7}$$

Revision of the first circuit: hazard free design

The design of the Synchronization Logic presented in the previous sections was based on a stringent assumption: that the inputs are not changing at the same time. It is clear that this assumption does not hold for the circuit under discussion because of the intrinsic randomness of the hit. The first thing to do in order to take this effect into account is to identify two types of hazards that are present in an asynchronous circuit:

- 1 (or 0)-static hazard: if in response to an input change and for some combination of propagation delays a network output may momentarily go to 0 (or 1) when it should remain a constant 1 (or 0) then the network has a static 1 (or 0) hazard;

- dynamic hazard: in case the output is supposed to change from 0 to 1 (or 1 to 0), the output itself might change 3 or more times, then the network has a dynamic hazard.

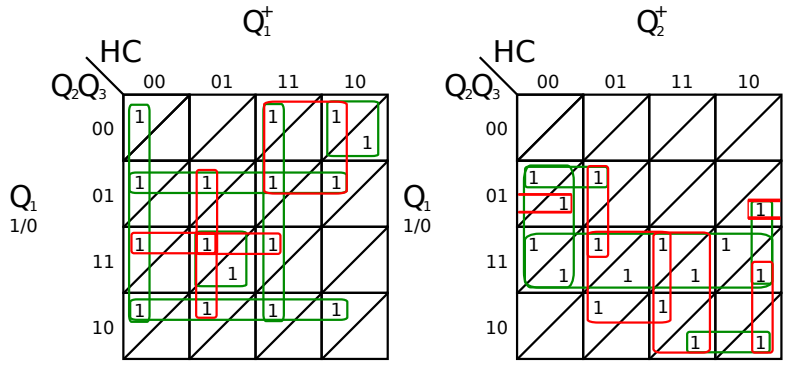
This means that any term that contains the product of a variable and its complement might cause a race condition. To generate a race free circuit we just need to change the way the grouping of terms has been done in the Karnaugh maps. Instead of trying to minimize the groups of 1-terms and so generate as little logic as possible, we have to group the 1-terms so that each pair of adjacent 1 is covered. This introduce redundant terms in the equations leading in fact to a bigger circuit but eliminating the race conditions. In figure A.5 it is possible to see thee new grouping, drawn in red (notice that, at the same time, the old grouping has been slightly optimized).

This new grouping leads to new equations for the circuit:

$$\begin{aligned} Q_1^+ = {} & Q_1Q_2'(H + Q_3 + Q_3'C') + Q_1(HC + H'C') + Q_1Q_2Q_3(H' + C) + \\ & + H'C(Q_1Q_2 + Q_2Q_3) + Q_3'H(Q_2'C' + Q_1) + Q_1(Q_3H'C + Q_2Q_3') \end{aligned} \quad \text{(A.8)}$$

$$\begin{aligned} Q_2^+ = {} & Q_2'Q_3(Q_1H' + Q_1'C') + Q_3H'(C' + Q_1C) + Q_2(Q_3 + Q_1Q_3'H) + \\ & + Q_2C(Q_1 + H) + HC'Q_1'(Q_2 + Q_3) \end{aligned} \quad \text{(A.9)}$$

$$Q_3^+ = Q_3(C' + H' + Q_2') + Q_2'HC \quad \text{(A.10)}$$



(a) Karnaugh map for the next state of Q_1.

(b) Karnaugh map for the next state of Q_2.

(c) Karnaugh map for the next state of Q_3.

(d) Karnaugh map for the next state of Z.

Figure A.5. *New grouping of the Karnaugh maps for the 40 MHz synchronizer. In red is highlighted the new grouping.*

$$Z^+ = Q_1Q_3' + Q_2'H(Q_3' + Q_1') + Q_1'Q_3 + Q_2H(Q_3 + Q_1) \tag{A.11}$$

Appendix B

Digital design work flow

In chapter 3 and 4 the design, simulations and testing of two prototype chips have been presented. In this appendix, the complete digital work flow will be shown to highlight the process which brings a chip from the specifications to the construction. The steps for such a process are shown in figure B.1.

After all the simulations are passed, the constraints are met and all the rules have been checked the design is ready to be submitted to the factory to be taped out. This requires the generation of a file which contains all the physical information about the chip; after the file is generated and checked it is sent to the manufacturer for production.

Starting with the requirements for the circuit, the first thing to do is to describe the behavior of the circuit using an Hardware Description Language (HDL) the two most used languages being Verilog and VHDL. In the present work the language of choice has always been Verilog. At this level the circuit is described at the Register Transfer Level, a level of abstraction used to model in general synchronous circuits describing the propagation of the digital signals between logic registers and the operations to perform on them. After the design is done, RTL simulations take place to verify the functionality of the circuit; this type of simulations treats the circuit as an ideal network with no internal delays or parasitics taken into account. Simulations, then, merely verify the correct behavior of the circuit under the applied stimuli.

When simulations prove to be successful the next step is the synthesis of the RTL netlist. In this step the behavioral design is translated to basic building blocks like logic gates and flip-flops. To do so one needs a library of standard cells alongside the netlist and the constraints file. The constraints can be of various types. Timing constraints represent maximum or minimum time allowed in certain signal paths like the maximum allowed delay for a signal with respect to

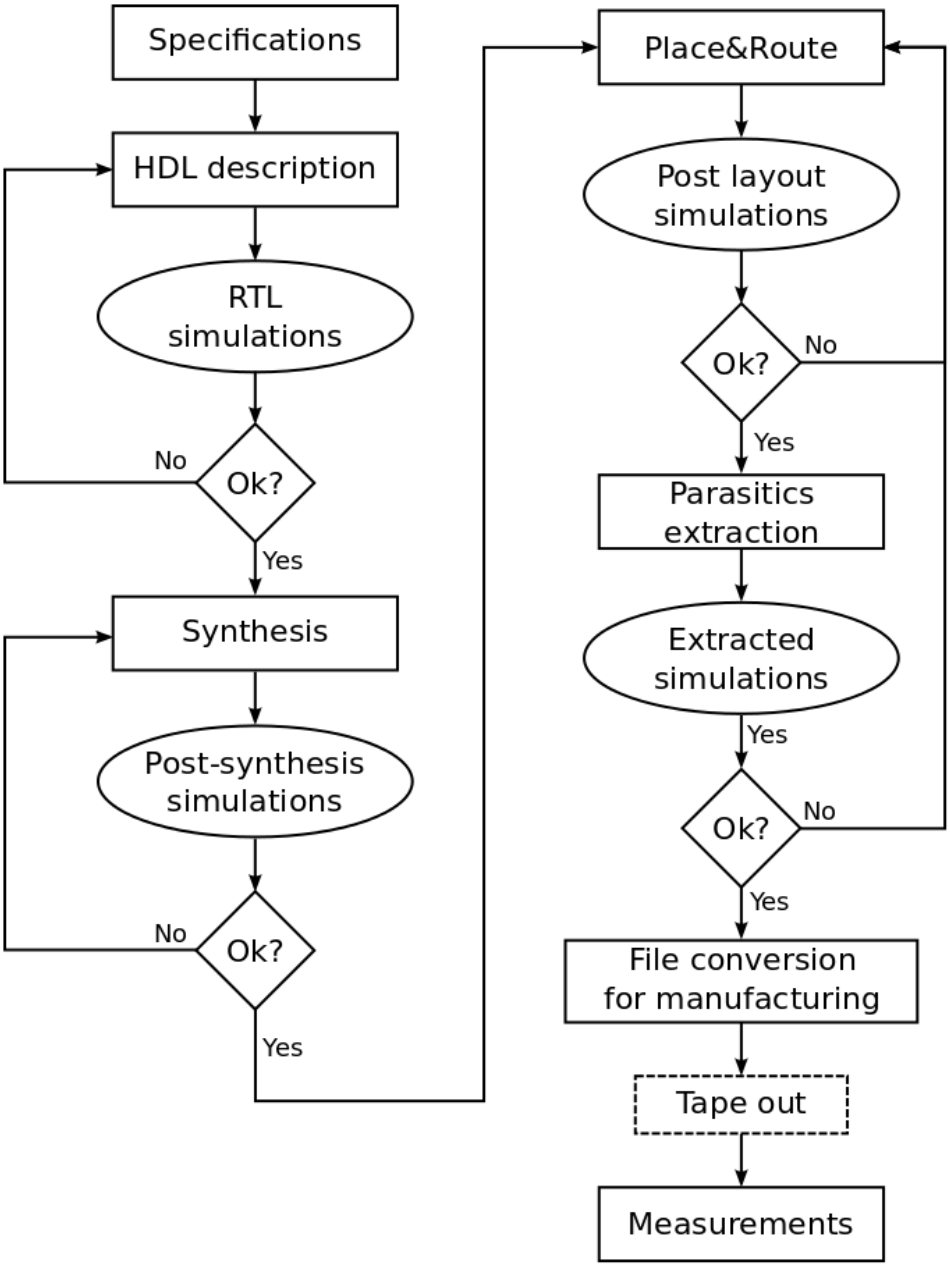


Figure B.1. *Schematic of the digital design work flow.*

the clock, for example. Physical constraints describe physical properties of the resulting circuit like the load which is foreseen on a particular pin while library constraints tell the synthesizer which cell to use in particular cases (i.e.: a particular gate to be used as a buffer). The synthesizer then processes the RTL netlist and the constraints file and gives as output a verilog netlist, which contains a circuit made of gates (AND, OR, flip-flops, etc...) and their interconnections, and a constraint file that contains the original ones plus these which are generated by the synthesis tool. The post synthesis netlist can then be simulated to check that the timing is correct and to check that the functionality has not been changed with the introduction of additional cells.

After this step has been completed successfully the placing and routing (P&R) of the design takes place. This process uses the following input files:

- the post synthesis netlist, which contains all the physical cells which are going to be placed and their connections;
- the post synthesis constraint file containing timing and physical constraints;
- the floorplan, which describes the area where the circuit must be placed;
- the library containing the physical implementation of the cells used in the circuit.

The tool must be instructed with a set of commands about the targets that must be accomplished during the creation of the physical circuit. The P&R procedure is a compromise between different constraints (minimum time delay, buffering of the signals, power consumption, available area) and the tool must be instructed on which objective is more important to accomplish. For some applications, for example, it might be crucial to minimize the area occupied by the final circuit while for others one might want to gain more robustness against timing issues at the price of consuming more power. It is the task of the designer to find a good equilibrium between all the different demands. It is during this phase that buffers are inserted and the clock distribution tree is created. The results of this step are the physical implementation of the circuit and the post layout netlist.

It is relevant to notice that both during synthesis and P&R the tools are free to insert buffers to meet the constraints. The insertion of new cells can change the behavior of the circuit. This is why it is very important to simulate after every step in the flow the resulting netlist, since there might be critical paths which have been created at any of the previous stages.

Usually P&R is an iterative process in which after each iteration one looks into the resulting netlist to check if the circuit meets the specifications. If it is

not the case, to change the resulting netlist it is usually common to modify the constraints and re-run the tool.

After P&R of the circuit one has the complete layout of the initial design. At this point there are two checks that must be performed and are called manufacturability checks. The Design Rule Check (DRC) analyzes the final layout to search for any design rule violation that might be present (a typical example of a rule violation is a wrong net or pin spacing). The design rules are set by the manufacturer. The Layout versus Schematic (LVS) tool checks that the physical implementation of the circuit corresponds to the post synthesis netlist. It might be that there are missing connections, shorts or components mismatches that must be solved before proceeding.

After the DRC and LVS both are passed one can extract the parasitic values from the layout to obtain the so called extracted view. The extracted circuit has additional information about the routing capacitance and resistance for every net and the extra devices which are introduced by the physical placing of the cells, like for example diodes or even transistors. To evaluate the influence of the parasitics, Statistical Time Analysis tools are used. Finally, simulations are performed on the extracted circuit to detect any timing problem or wrong behavior that might have been introduced.

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Summary

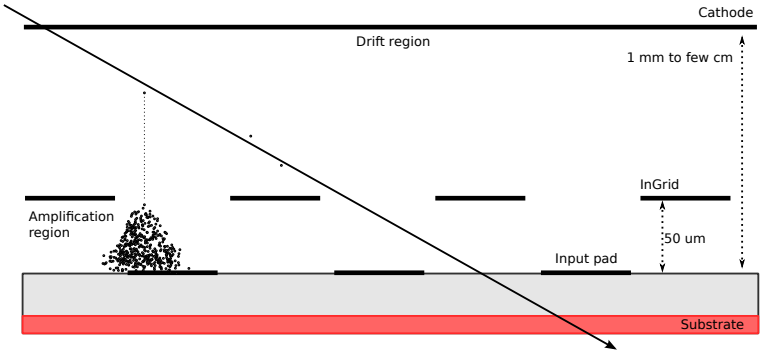
Particle detectors are among the tools used in high energy physics to study the fundamental properties of nature. The construction of the modern particle detectors with millions of detection channels in a few square meters, as in the case of a silicon vertex tracker, and with the possibility of recording and reading out hundreds of thousands of events per second, is possible thanks to the availability of electronic integration technologies. Circuits with millions of transistors can be implemented in an area as small as a thumb nail.

A detector, in general, has two components: a detection medium, which can be a solid, a liquid or a gas, and a readout circuitry. The choice of both the detection medium and the readout system are application dependent. Among different detection systems are Micro Pattern Gas Detectors (MPGD) and this is the focus of this thesis. This means that we considered detectors that use gas as the detection medium and have a pixelated readout system. In particular, a class of MPGDs is studied: GridPix detectors.

A GridPix detector is made of a metallic grid built on top of a pixel chip at a distance of roughly 50 µm using post processing techniques. At some distance (from 1 mm to few centimeters), depending on the application, a metallic foil is then mounted, which serves as cathode and defines the active detection volume. The volume between the chip and the cathode is filled with a gas mixture.

A charged particle crossing the gas volume will ionize some molecules and free a certain number of electrons depending on its energy and on the gas, as shown in figure 1. If an electric field is applied across the gas volume the released electrons will drift toward the grid. In the region between the grid and the chip a high electric field is applied (70 to 100 $\mathrm{kV\,cm^{-1}}$). The single electrons released by ionization entering this region will ionize other gas molecules thereby creating an electron avalanche. The electrons in the avalanche are collected at the input pads of the readout chip, where the resulting signal is processed by the pixel electronics.

If the chip records the Time of Arrival (ToA) of the electrons to the grid, one can perform a 3D reconstruction of a particle's track: the XY information is



Summary, Figure 1. *Schematic representation of the working principle of a GridPix detector.*

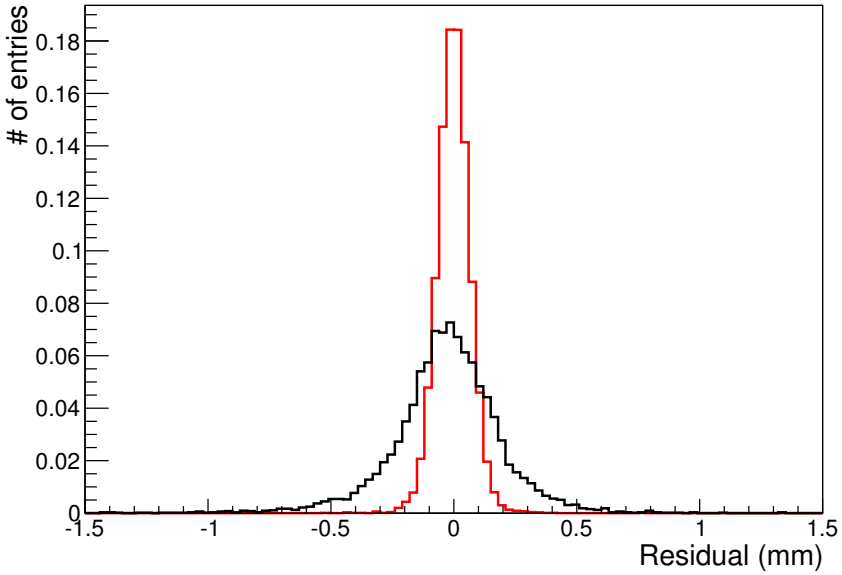
provided by the pixel plane, while the Z information can be reconstructed using the ToA and the drift velocity of the electrons in the gas.

In years of testing, GridPix detectors have shown good results in terms of track reconstruction. Nevertheless some limitations have been observed, some due to the choice of gas as the detector medium (diffusion limits the resolution, for example) and others due to the use of Timepix as readout chip. In particular, the available maximum time resolution of 10 ns and the timewalk introduced by the frontend electronics are two factors that limit the application of GridPix as tracking detector in high energy physics experiments such as Atlas. What is needed to overcome these limits is a chip that first of all has higher time resolution, in the order of a nanosecond, to better determine the z position of the ionization electrons. Second, the pixels must be capable of recording at the same time the ToA and the Time over Threshold (ToT) of the input signal which provides a measure of the charge in the avalanche. With this ToT information it is possible to correct for timewalk. With the chosen frontend configuration (single threshold discriminator) signals with low ToT have big timewalk and vice versa; calibrating the detector allows for offline timewalk correction.

The positive effect on track reconstruction provided by timewalk correction has been proven implementing a toy Monte Carlo based on data recorded with a GridPix detector during a beam test experiment at Cern in 2012. Although the ToT data is not available, since Timepix cannot provide both ToA and ToT simultaneously, it is possible to statistically correlate the two spectra and assign to each simulated ToA hit a ToT value. Figure 2 shows the residual[1] distribution

[1]The residual is defined as the distance between the recorded hit and the position of the hit calculated with the track obtained fitting all the other hits in the same event.

for tracks with 5 hits, with and without timewalk correction. It is clear that the timewalk correction greatly improves the residuals.



Summary, Figure 2. *Z-residual distribution for tracks with 5 hits and hit under study close to the cathode corrected for timewalk (red) or not (black). The two distributions have been normalized for comparison.*

It is to overcome these limitations that the design of a series of prototypes started at Nikhef in 2005. The goal was to test separate circuits that would eventually end up into a full size chip better suited for GridPix applications. In particular there was the necessity to understand the feasibility of a low noise frontend and of a per pixel high resolution Time to Digital Converter (TDC). The prototype circuits are called GOSSIPO (Gas On Slim Silicon Pixels, where the final O indicates that they are prototypes) and their design started in 2005 with GOSSIPO-1.

This first chip was built to test a new low noise preamplifier with a discriminator, which demonstrated the low noise features of the triple well design which permits isolation of the input transistor from the bulk. The second prototype chip was developed during 2006 and 2007 and it contains a 16×16 frontend matrix of pixels. Every pixel is equipped with a TDC with a resolution of 1.8 ns and a dynamic range of 350 ns. Tests show that the TDC provides the needed

resolution. However, the TDC characteristics shows a discontinuity when the hit signal is detected close to the rising edge of the system clock. The chip, despite the presence of this bug, has been used to build a GridPix detector with a drift gap of 1.3 mm. The detector performed remarkably well in a beam test experiment and reached a resolution of 10 µm in the XY direction and 28 µm in the z direction [60] for a track with 6 hits.

GOSSIPO-3 is the third prototype chip developed in collaboration with between Nikhef and Bonn University for the readout of gas detectors such as large Time Projection Chambers (TPC) or Micro Pattern Gas Detectors. This chip was built with the purpose of demonstrating the functionality of several blocks like the local high frequency oscillator, the analog frontend, a new pixel logic and two Low Drop Out regulators. The results show that the design has been successful. The electronic frontend has very low noise (23 electrons RMS) and fast rise time (less than 25 ns) and the TDC shows a good differential and integral non linearity. The discontinuity present in GOSSIPO-2 has been eliminated and the Low Drop Out (LDO) characteristics are according specifications. The chip shows the presence of a coupling between the fast oscillator output and the system clock (40 MHz) which can be eliminated with a more careful design layout.

In 2012 the last chip to be designed in view of the design of a full size chip was GOSSIPO-4. Its purpose is the testing of a new 8 pixel structure called super pixel in which 8 adjacent pixels use the same oscillator, thus reducing the amount of area and power needed for the single high resolution TDC. This solution introduces the need of a synchronization circuit which has the purpose of distributing to the single pixels the common fast clock without introducing glitches due to the asynchronous nature of the input signals. The oscillator has also been designed using a different approach: the high frequency signal is provided by a series of RC components, connected by inverters that act as buffers. The frequency can be tuned thanks to a special type of capacitors called Varactors, which have the characteristic of changing their capacitance value with the supply voltage applied. This also changes the control scheme of the oscillator. A Phase Locked Loop (PLL) located at the periphery of the chip contains a replica of the oscillator which is locked to an external reference frequency. The PLL detects any change in the oscillation frequency and provides the control voltage for all the oscillators in the chip. The chip has been designed with a new high density standard library which is also tested. The measurement results are in god agreement with the simulations. The new standard library performs well at high frequency. The differential and integral non linearity values show that the TDC characteristic is good and it is not influenced by a drop of the supply voltage up to 200 mV. The synchronization circuit works as expected and distributes the high frequency clock without glitches and also the PLL performances are according specifications.

After the design and testing of the prototype chips, Timepix3 was taped out in summer 2013. Timepix3 is a complete chip, with a matrix of 256 x 256 pixels of 55 x 55 μm^2. The relevant features of Timepix3 include simultaneous recording of ToA and ToT, data driven readout and a per-pixel high resolution TDC based on the circuitry developed for GOSSIPO-4. Timepix3 provides a combined absolute/relative measurement of the ToA of a hit. A basic characterization of the single pixel TDC of Timepix3 has been performed. The chip works very well with it TDCs showing good linearity characteristics. The chip works so well that is actually possible to highlight secondary effects, like oscillator startup and variations in the bin size due to the clock distribution scheme. These secondary effects, however, do not compromise chip operations and can be either neglected or corrected for.

Timepix3 performed remarkably well in the first beam test experiments in which it has been used in fall 2014.

Samenvatting

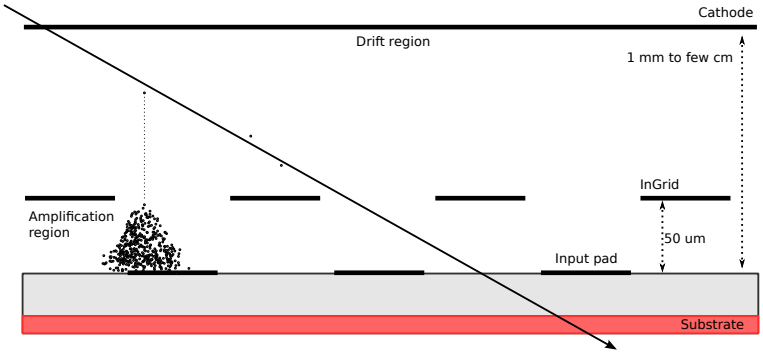
Door de beschikbaarheid van moderne elektronische integratietechnologieën kunnen elektronische circuits met miljoenen transistors geïmplementeerd worden in een oppervlakte zo klein als een duimnagel. Deze techniek vindt een toepassing in moderne deeltjesdetectoren, zoals silicium vertex trackers. Met de miljoenen detectiekanalen in slechts een paar vierkante meter is het mogelijk om zo honderdduizenden botsingen op te nemen en uit te lezen.

Een dergelijke detector bestaat over het algemeen uit twee delen: een detectie medium, dat een vaste stof, een vloeistof of een gas kan zijn en een uitlees circuit. De keuze van zowel het detectiemedium als het uitleescircuit is afhankelijk van de toepassing. De focus van dit proefschrift ligt op Micro Pattern Gas Detectors (MPGD) detectiesystemen. Dat zijn systemen die gas gebruiken als detectiemedium en pixelchips als uitleeselektronica. Meer specifiek wordt er in proefschrift een bepaalde klasse van MPDG bestudeerd: GridPix detectoren.

Een GridPix detector bestaat uit een metalen folie met kleine gaten (het 'grid') dat met behulp van fotolithografische processen parallel aan de pixelchip is gepositioneerd op een afstand van ongeveer 50 µm. Parallel aan het grid op een afstand van 1 mm tot een paar centimeters is een metalen folie geplaatst dat dienst doet als kathode en de rand van het actieve detectie volume definieert. Dit volume kan gevuld worden met een mix van verschillende gassen.

Een geladen deeltje dat het gasvolume doorkruist ioniseert de gasmoleculen. Het aantal elektronen dat daarbij geëmitteerd wordt is afhankelijk van de energie van het deeltje en het type gas, zoals is weergegeven in figuur 1. Een potentiaal verschil tussen de kathode en de grid zorgt ervoor dat de elektronen naar het grid bewogen worden. Het elektrische veld tussen het grid en de pixelchip is echter vele malen groter (70 to 100 $\mathrm{kV\,cm^{-1}}$). De elektronen die dit volume bereiken zullen op hun beurt andere gasmoleculen ioniseren zodat er een elektronenlawine ontstaat. Vervolgens worden de elektronen in de lawine gemeten door de pixels van de chip, waarna het resulterende signaal bewerkt wordt door de pixelelektronica.

Met behulp van de aankomsttijd van de elektronen die gemeten wordt door

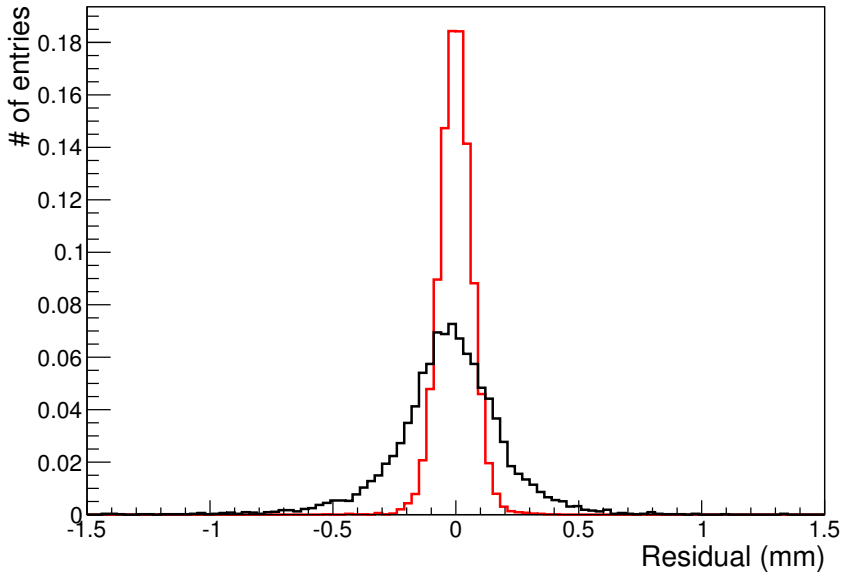


Samenvatting, Figure 1. *Schematische voorstelling van het werkingsprincipe van een GridPix detector.*

de pixels kan een 3D reconstructie gemaakt worden van het spoor van elektronen dat door het deeltje is achtergelaten in het gas. Helaas wordt de kwaliteit van de reconstructie beïnvloed door de keuze van het gas (elektronendiffusie limiteert de resolutie) en door het gebruik van Timepix als pixelchip. De maximale tijdsresolutie van 10 ns in Timepix is beperkt, verder wordt er een ongewilde vertraging in tijd geïntroduceerd door de Timepix pixelelektronica. Hierdoor wordt de toepassing van GridPix detectoren in hoge-energiefysica experimenten zoals Atlas gelimiteerd. Deze limieten kunnen beperkt worden door een chip met een betere tijdsresolutie, van orde grootte nanoseconde te gebruiken, om de positie van de oorspronkelijke ionisatie beter te kunnen bepalen. Ook zouden de pixels zowel de aankomsttijd Time of Arrival (ToA) als de lengte van het signaal Time over Threshold (ToT) moeten kunnen meten, de laatste is een maat voor de hoeveelheid lading in de lawine. Door gebruik te maken van ToT informatie kan er gecorrigeerd worden voor het effect van de vertraging in aankomsttijd.

Met de gekozen pixelelektronicaconfiguratie hebben signalen met lage ToT waarden een grote tijdsvertraging en vice versa. Kalibratie van de detector maakt correctie voor tijdsvertraging achteraf mogelijk.

De verbetering in de reconstructie van het afgelegde pad van het deeltje door toepassing van tijdsvertragingcorrectie is bewezen met een Monte Carlo simulatie gebaseerd op een experiment met geladen deeltjes in een versneller op CERN in 2012. Ondanks dat de lengte van het signaal niet gemeten werd omdat de Timepix niet geschikt is om zowel ToA en ToT simultaan te meten, is het mogelijk om beide spectra te correleren en een ToA waarde aan elke gemeten ToT toe te wijzen. Figuur 2 laat de distributie van de residuen zien voor metingen met 5 geraakte pixels, voor zowel met als zonder tijdsvertragingscorrectie. Het is duidelijk dat de tijdsvertragingscorrectie de verschillen aanzienlijk verkleint.



Samenvatting, Figure 2. *De genormaliseerde verschildistributie van paden gereconstrueerd uit vijf geraakte pixels waarbij alleen de geraakte pixels die het dichtst bij de kathode liggen zijn gebruikt. De rode curve illustreert de residuen met correctie, de zwarte curve zonder.*

In 2005 is Nikhef begonnen met het ontwerpen van verschillende series prototypechips om het effect van tijdsvertraging op de positiemetingen te beperken. Het doel was om verschillende schakelingen te testen om die vervolgens te gebruiken in volledige chips die beter geschikt zijn voor GridPix detectoren. Er was behoefte aan een hoge resolutie per pixel, een betere tijd naar digitaal convertor (Time to Digital Converter (TDC)) en lagere ruis van de elektronica. De prototypes worden GOSSIPO (Gas On Slim Silicon Pixels, waarbij de laatste O aangeeft dat het om een prototype gaat) genoemd. Het eerste ontwerp stamt uit 2005 en wordt GOSSIPO-1 genoemd.

GOSSIPO-1 is ontwikkeld om een nieuwe lage-ruis voorversterker met discriminator te testen. Hiermee zijn de lage ruiseigenschappen van een zogenoemd "triple well" ontwerp gedemonstreerd, dat isolatie van de ingangstransistor van het bulkmateriaal mogelijk maakt. Het tweede prototype is ontwikkeld in 2006 en 2007 en het bevat een pixelmatrix van 16×16 pixels. Elke pixel is uitgerust met een TDC met een resolutie van 1.8 ns en een dynamisch bereik

van 350 ns. Tests hebben aangetoond dat de TDC de benodigde resolutie biedt. Echter, de TDC karakteristieken laten discontinuïteiten zien wanneer het signaal samenvalt met de opgaande flank van de systeemklok. Ondanks deze tekortkoming is de chip gebruikt om een GridPix detector te bouwen met een gaslaag van 1.3 mm. Tijdens versnellerexperimenten bleken de metingen van deze detector van opvallend goede kwaliteit te zijn. De resoluties in het XY vlak van de detector hadden een waarde van 10 µm, in de Z richting was dat 28 µm voor metingen met zes geraakte pixels [60].

GOSSIPO-3 is de derde prototypechip ontwikkeld door een collaboratie tussen Nikhef en de Universiteit Bonn voor het uitlezen van gasdetectoren zoals grote tijdprojectiekamers (TPCs) en MPGDs. Deze chip is gebouwd om de functionaliteit te demonsteren van verschillen blokken zoals het lokale hoogfrequente klokcircuit, de analoge frontend, een nieuwe pixellogica en twee spanningsregulatoren met lage spanningsval (Low Drop Out (LDO)).

De resultaten laten zien dat het ontwerp succesvol is. De elektronische frontend heeft een zeer lage ruis (23 elektronen RMS) en een snelle stijgtijd (minder dan 25 ns) en de TDC laat een goede differentiële en integrale niet-lineariteit zien. De discontinuïteiten die aanwezig waren in GOSSIPO-2 zijn geëlimineerd en prestaties van de LDOs zijn volgens specificaties. De chip laat een koppeling zien tussen de oscillator en de systeemklok (40 MHz), die geëlimineerd kan worden met een betere layout van het circuit.

De meest recente chip, GOSSIPO-4 (2012), is ontworpen met het oog op de ontwikkeling van een volledige chip. Het doel was het testen van een nieuwe ach- pixel structuur, ook wel superpixel genoemd. Hierin gebruiken acht naburige pixels dezelfde oscillator, waardoor zowel de gebruikte ruimte en het benodigde vermogen voor de hoge resolutie TDCs worden geminimaliseerd. Deze oplossing behoeft een synchronisatiecircuit voor de distributie van de gezamenlijke snelle klok naar de individuele pixels zonder daarbij verstoringen op de ingangssignalen te introduceren. Bij het ontwerp van de oscillator is een andere aanpak gebruikt waarbij er gebruikt gemaakt wordt van een serieschakeling van weerstanden en condensatoren. De frequentie kan aangepast worden door gebruik te maken van een speciaal type condensator, genaamd Varactor, waarbij de capaciteit een functie is van het aangeboden voltage. Die vereist ook een andere manier van aansturen van de oscillator.

Een Phase Locked Loop (PLL) in de periferie van de chip bevat een replica van de oscillator die gesynchroniseerd is aan de externe referentie frequentie. De PLL detecteert eventuele veranderingen in de oscillatiefrequentie en levert de overeenkomstige stuurspanning aan alle oscillatoren in de chip. De chip is ontworpen met een nieuwe hoge-dichtheid standaardbibliotheek die daarmee eveneens getest is. De metingen zijn in overeenstemming met de simulaties. De nieuwe standaardbibliotheek presteert goed bij hoge frequenties. De differ-

entiële en integrale niet-lineariteitswaarden laten zien dat de karakteristiek van de TDC goed is en immuun is voor voedingsspanningvariaties tot 200 mV. De synchronisatie-schakeling presteert zoals verwacht en distribueert de hoge frequenties zonder verstoringen, daarbij zijn de prestaties van PLL volgens specificaties.

Na het ontwerp en testen van de prototype chips kwam Timepix3 uit in de zomer van 2013. Timepix3 is een volledige chip met een pixelmatrix van 256×256 pixels met een afmeting van $55 \times 55\,\mu m^2$. De relevante kenmerken zijn simultane metingen van ToA en ToT, datagedreven uitvoer en een per-pixel TDC met hoge tijdsresolutie, gebaseerd op het circuit dat ontwikkeld is voor GOSSIPO-4. Timepix3 levert een gecombineerde absolute/relatieve meting van de ToA van een geraakte pixel. Een eerste karakterisatie van de pixel TDCs laat goede lineaire karakteristieken zien. De chip presteert zo goed dat het zelfs mogelijk is om tweede-orde effecten te belichten, zoals het opstarten van de oscillator en variaties in de stapgrootte door het klokdistributieschema. Deze secondaire effecten hebben echter minimaal gevolg voor toepassing van de chip en ze kunnen verwaarloosd of achteraf gecorrigeerd worden.

Timepix3 heeft uitzonderlijk goed gepresteerd in de eerste versnellerexperimenten op DESY en CERN.

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Looking back at the past 6 years I can say that in my opinion a PhD is only marginally about what you learn and what you do for the advancement of science. Of course, it is the foundation stone over which one builds the future in terms of skills and competences, this cannot be overlooked. But what I find most important is the continuous state of struggling that traveled with me and that now make me say "ok, I have done this, the rest cannot be more difficult". (last famous words...).

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That's all folks. It was about time.