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Development of a charge pump for sensor biasing in a Serial Powering scheme for the ATLAS pixel detector upgrade

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Abstract: CMOS monolithic pixel detector technology is one of the options considered for the outer layer of an upgraded ATLAS pixel detector in 2026. In this upgrade pixel detector modules will be powered in series by a constant current source to reduce power losses and material budget. On-chip shunt regulators generate the local 1.8 V supply voltage from the input current to provide power to the integrated circuits. The sensor bias for monolithic sensors is often limited and not sufficiently large to allow a common bias for all sensors in the serial powering chain. In this paper, we give an introduction to the serial powering strategy for CMOS detectors with emphasis on the design and simulation results of a regulated charge pump circuit for sensor biasing. Two prototypes operating with a pumping frequency of 640 MHz, one with 6-stages and one with 19-stages, were designed and fabricated in a modified TowerJazz 0.18 µm CMOS imaging technology to provide negative bias down to –6 V and –20 V, respectively. Simulation results demonstrate good performance of the charge pump circuit which could be used to bias the CMOS sensor.

Keywords: Analogue electronic circuits; Particle tracking detectors; Radiation-hard electronics; VLSI circuits

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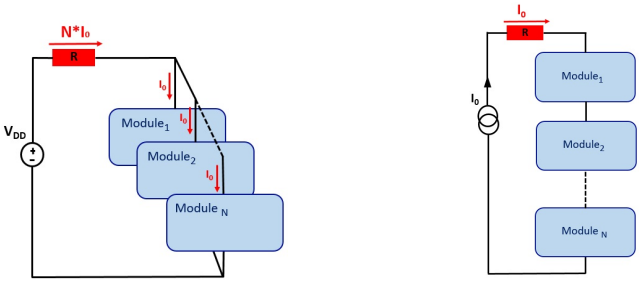
Contents

1 Introduction

The upgraded ATLAS experiment will start operating at the High Luminosity LHC accelerator (HL-LHC) in 2026 [1]. In the present ATLAS pixel detector, an independent parallel powering scheme is used to power the modules as shown in figure 1(a). The major drawback of this scheme is its very low efficiency, with 80% [2] of the power consumed as ohmic potential drop in the cables. If the modules are connected in series (see figure 1(b)), the current flowing through the individual modules is identical to the total current I_0 generated by a constant current source. On-chip shunt regulators use the input current to generate the supply voltage for the electronics. This serial powering scheme with only a single power cable drastically reduces material budget and power losses, and is now foreseen for the ATLAS pixel detector upgrade. For the CMOS chips designed for the outer pixel layers, one of the most important requirements is to design a stable shunt regulator that generates a supply voltage of 1.8 V. Studies on Shunt-LDO regulators (combining shunt and low drop-out circuits) were performed in the framework of regulator developments for ATLAS hybrid pixel detectors [3, 4].

Since the modules in a serial powering chain have different ground potentials, a specific biasing scheme for the CMOS sensors needs to be considered. One of the possibility to bias the sensing part is to derive a high voltage locally at module level to deplete the sensor. In the TowerJazz[1] (TJ) process, two different voltage levels are used for the purpose of sensor depletion. The bias voltages will be generated on-chip in a final design by using a negative charge pump circuit. The charge pump is a kind of DC-DC converter which is used to generate a DC voltage higher than the supply or DC voltage with reverse polarity. The conventional charge pump which was proposed by Dickson [5] in mid 1970's has a disadvantage of a limited voltage pumping gain due to the threshold voltage drop across the diode connected transistors. However, the topology described in section 3 uses transistors as charge-transfer switches (CTS) which eliminates the threshold voltage drop problem. The charge pump circuit has been designed and prototyped in the modified TJ 0.18 µm CMOS imaging technology, together with a shunt-LDO regulator and memory test structures, with a die area of 5 mm × 2.5 mm, as shown in figure 2.

[1] Tower Semiconductor Ltd., Israel.



(a) (b)

Figure 1. (a) Block diagram of parallel powering scheme. (b) Block diagram of serial powering scheme.

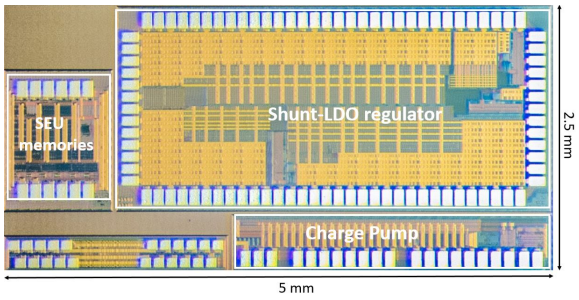
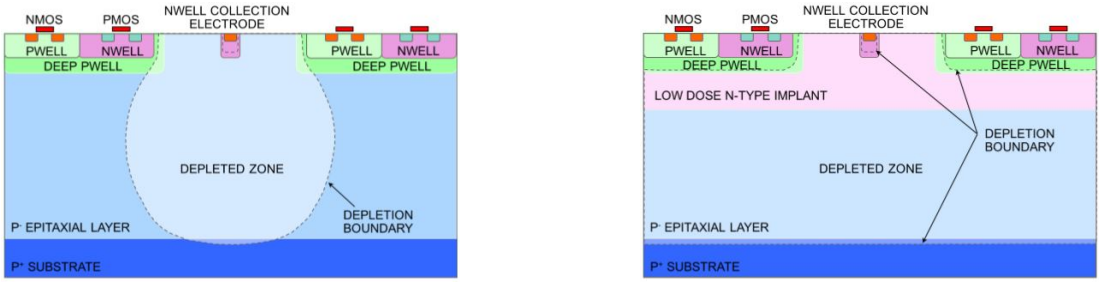


Figure 2. Die photograph of the three blocks: Shunt-LDO regulator, charge pump and single event upset (SEU) tolerant memories. All three test circuits are for the same detector in TJ CMOS technology.

2 Sensor technology

The standard TJ process, shown in figure 3(a), comes with a high resistivity (> 1 kΩ·cm) p-epitaxial layer grown on top of a p-type substrate. An nwell collection electrode of several μm^2 acts as a charge collecting diode for the charges generated by the ionizing particles. CMOS electronics is placed a minimum 2-4 µm away from the collection electrode and is shielded by a deep pwell. Negative substrate bias is used to increase the depletion region, but in the standard process it is difficult to reach full depletion of the epitaxial layer, resulting in only a moderate radiation tolerance. A process modification with an additional low dose n-implant, shown in figure 3(b), allows for full depletion and increases radiation tolerance [6] by an order of magnitude yielding promising results for pixel pitches up to 30 µm, but further process changes are being implemented to improve efficiency for larger pixel pitches [7, 8]. Design activity was therefore started also on serial power, further described in the next section, for the TJ sensor. The pwell and substrate are separated by the depleted sensitive layer and can be biased at different potentials, up to –6 V for the pwell, and more negative for the substrate (we target –20 V). Biasing the substrate less than –6 V results in further increased electrical field, better signal charge collection speed and improved radiation tolerance [6].



(a) (b)

Figure 3. (a) The standard TJ 180 nm CMOS process. (b) The modified TJ 180 nm CMOS process. Reproduced from [9]. CC BY 4.0.

3 Design of the charge pump

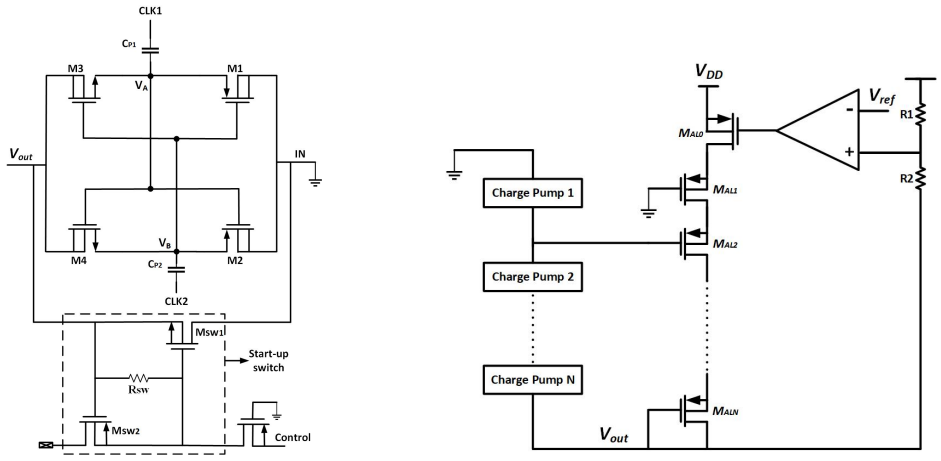
Two charge pumps variants have been designed to produce the required –6 V and –20 V supplies, delivering a load current up to 500 µA, operating at a pumping frequency of 640 MHz. A single stage of the charge pumps uses 4 CTS with 2 pumping capacitors on each side as sketched in figure 4(a). By operating at higher frequency, the equivalent series resistance (ESR) losses caused by the pumping capacitors C_P are reduced which leads to higher voltage gain. The CTS are designed with two parallel, complementary cross-coupled parts operating in opposite phases, each part providing control signal to the other one [10]. The size of a single stage is mostly dominated by the pumping capacitors C_P. To reduce parasitics and power consumption, metal-oxide-metal (MOM) capacitors are used with values of 2.35 pF in each stage. The width of the CTS in both variants is directly proportional to the load current. They are powered by the shunt-LDO regulator which generates the regulated supply voltage of 1.8 V.

The charge pump works in two phases. In the first phase when CLK 1 is high (CLK 2 is low), both M1 and M4 transistors will be turned ON which leads to transfer of charge from the input to the V_A node. In the second phase when CLK 1 goes low (CLK 2 is high), both transistors M2 and M3 will be turned ON and thereby "pumping" V_A node to $-V_{DD}$. Higher negative voltages can be generated by cascading a certain number of stages (N). Ideally, the output voltage from an N-stage negative charge pump is $-N \times V_{DD}$. However when the load current I_L is drawn from the charge pump the resulting output voltage is expressed as (3.1).

$$V_{out} = -N \times V_{DD} + \frac{N \times I_L}{C_P \times f} \tag{3.1}$$

The second term corresponds to the losses while charging and discharging the capacitor C_P, with f = 1/T the pumping frequency [11]. The output voltage is regulated in a closed-loop system which consists of an open-loop charge pump, amplifier, resistive divider and an adjustable load consisting of a string of PMOS transistors M_{AL0}-M_{ALN} as represented in figure 4(b). The amplifier is designed for a bias of 2 µA which controls the gate of transistor M_{AL0}. Furthermore, a start-up circuit is also designed to avoid latch-up issues. To properly define the sensor bias during start-up when the charge pumps are not yet operational, special start-up switches are implemented in each stage of

the charge pumps as sketched in figure 4(a). These switches tie the pwell and the substrate voltages to ground before activation of the charge pumps.

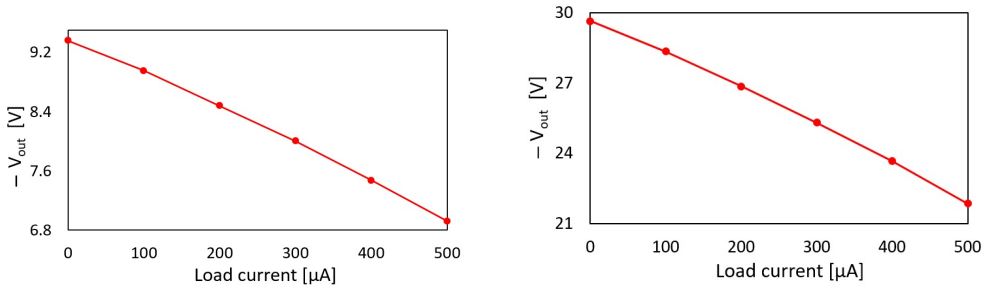


(a) (b)

Figure 4. (a) Schematic of 1-stage charge pump. (b) Block diagram of closed-loop charge pump. V_{ref} is the reference voltage which is set to 1 V.

4 Simulation results

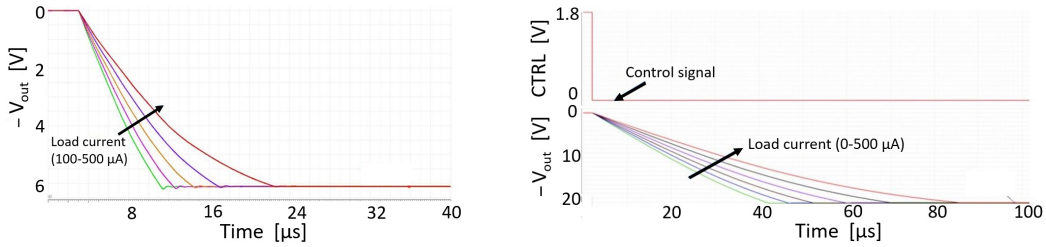
This section presents the most important simulation results for the charge pumps. The output voltages of the open-loop charge pumps with varying the load current are illustrated in figures 5(a) and 5(b). Figures 6(a) and 6(b) show the regulated output voltages of –6 V and –20 V having 6-stages and 19-stages respectively. Simulations are done with a load capacitance (C_{Load}) of 2 nF. The value of the load capacitance is calculated by the equation $C_{Load} = (\mathcal{E}_{Si} \times A)/d$, where $\mathcal{E}_{Si}$ is the dielectric constant of silicon which is equal to $11.7 \times \mathcal{E}_0$, A is the area of the final TJ CMOS chip with the dimensions of 2 cm × 2 cm, d is the depth of the p-epitaxial layer (18-25 µm) [6].



(a) (b)

Figure 5. (a) (b) Output voltage characteristics of the open-loop 6-stages and 19-stages charge pump as a function of the load current with the pumping frequency of 640 MHz.

The simulated ON resistance of the special start-up switch is 2 Ω (respectively 8 Ω) for the 6-stages (respectively 19-stages) charge pump variant. When the charge pumps are active, these switches are off and can cope with the –6 V and –20 V.



(a) (b)

Figure 6. (a) (b) Closed-loop output voltages of 6-stages and 19-stages charge pump for various load currents with the pumping frequency of 640 MHz.

5 Conclusion

Serial Powering is a feasible option for efficient power distribution and to reduce the amount of material in the services for the upgraded ATLAS pixel detector. This work presents a simple and robust solution for biasing the monolithic CMOS sensor by using a charge pump to generate the sensor bias voltages on-chip. Simulation results have shown that the charge pump circuit produces stable output voltages of –6 V and –20 V up to a load current of 500 µA. The next steps include characterizing the charge pump prototype and building test systems with several ICs in series to demonstrate the functionality of the charge pump in conditions similar to the experiment.

Acknowledgments

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