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Inner Tracking Devices at the *Belle II* Experiment

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In the future *Belle II* experiment at the SuperKEKB collider in Tsukuba, Japan, charged particle tracking in the vicinity of the e^+e^- interaction point is provided by a two-layer silicon pixel detector based on the novel DEPFET technology (PXD) and by a four-layer silicon strip detector (SVD). In this presentation, I review the technology and the design of these two devices, and describe the current state of their construction.

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1. Introduction

The *Belle II* detector is a general purpose detector [1] and will operate at the high luminosity asymmetric B-Factory SuperKEKB, collecting data from the e^+e^- collisions near and at the energy of the $\Upsilon(4S)$. The inner tracking system will play a fundamental role in the broad *Belle II* physics program, that ranges from precise measurements of CP Violation to searches for dark matter. The main task of the tracking system is to provide a very precise measurement of the track parameters, especially the impact parameters, that allow the precise determination of the position of the primary and secondary vertexes of the short-lived particles. As an example, the distance between the decay vertices of the two B-meson along the longitudinal direction is of the order of a few hundreds of micrometers, and it is fundamental in CP Violation measurements.

The challenges of the tracking system of *Belle II*, son of the experiences with the Belle and *BABAR* trackers, are represented by the considerably higher background levels and the reduced boost of the machine. The design luminosity of SuperKEKB ($8\times10^{35}\text{cm}^{-2}\text{s}^{-1}$) is a factor 40 higher than its predecessor KEKB in order to open windows on physics beyond the Standard Model with a data sample of $50\,\text{ab}^{-1}$. On the other hand, the increase of luminosity also means higher machine background levels and consequently considerable increase of the occupancy of the innermost layers, of the number of fake hits and the absorbed radiation. The design center of mass boost of the $\Upsilon(4S)$ is $\beta\gamma = 0.28$, almost a factor 2 lower than KEKB. In order to match the expected resolution in time difference an improved precision on the vertex resolution of the same factor is required.

A typical $\Upsilon(4S)$ event has an average of five neutral pions, one neutral kaon and eleven charged tracks with a soft spectrum, shown in Figure 1. With these types of events the most important factors affecting the precision of the vertex position are the distance of the first measured hit and the effect of multiple scattering, i.e. the material budget of the silicon layers. Other important factors taken into account in the design are the single hit resolution and the impact of the machine background in terms of occupancy and radiation damage.

2. Inner Tracking System

Physics and background conditions set stringent requirements on the tracking devices, which should provide an improved performance with respect to their predecessor. The inner tracking system of the *Belle II* detector is composed of a 6-layer silicon Vertex Detector (VXD). The VXD is composed of two quite different and complementary detectors: the PiXel Detector (PXD) consists of the two pixelated innermost layers, and the Silicon Vertex Detector (SVD) consists of the four outer layers equipped with double sided silicon microstrip sensors.

The two innermost pixelated layers of the vertex detector will have an excellent spatial granularity ($\sim 15\,\mu\text{m}$) and will provide the unambiguous 2-dimensional position of the hit. The PXD material budget is extremely low, just $0.2\%\,X_0$, minimising the effect of the multiple scattering which is of fundamental importance. Finally, the innermost layer will be at a distance of only 1.4 cm from the interaction point (IP), which is roughly a factor 2 closer than the previous B-Factory's innermost vertex detectors layers, considerably reducing the consequences of multiple scattering. The four outer layers of double sided silicon strip sensors are also quite light in terms of material budget, with $0.8\%\,X_0$. The SVD is designed to provide an excellent time resolution, of the order of

a few ns. The two sub-detectors are complementary to each other and only the combination of the two provides the improved track resolution requested, as shown in Figure 1.

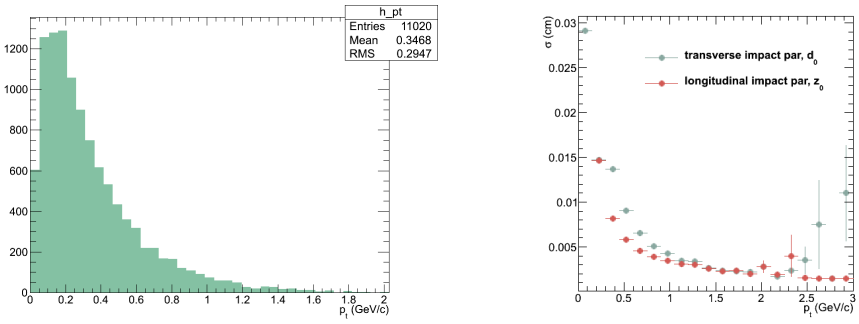

Figure 1: (left) Typical $\Upsilon(4S)$ spectrum of the charged tracks. (right) Estimated errors on the impact parameters as a function of the transverse momentum. Both plots are preliminary and are produced with the official *Belle II* full simulation.

3. The Pixel Detector

The PXD will be the first HEP detector built with the DEPFET technology (DEPleted p-channel Field Effect Transistor) [2]. In this technology the single pixel is basically a FET with an internal gate, see Figure 2: when the particle ionizes the depleted sensor, the charges are collected by the internal gate and modulate the drain current. The collected charge is digitized only when the FET is on, minimising the power consumption. This is a very low noise detector since the amplification stage is internal and the capacitance seen by the readout circuit is low. Since the sensor is fully depleted the collection of the charge is very fast and the signal is relatively large.

The matrix readout is based on the so-called *rolling shutter mode*: all pixels of four rows are read at the same time turning on their gate and digitizing the drain current, shown in Figure 2. During the first tens of nanoseconds after the gate is turned on the current grows and then it stabilises. Since the readout is not destructive a *clear* signal is turned on to remove the ionizing charges trapped in the internal gate, and then the gate is turned off. In the *rolling shutter mode* all rows are sensitive but only four rows are active at a time. The read-clear cycle is 100 ns long, resulting in a total time of 20 µs to read out the entire matrix (250 columns and 768 rows).

The SWITCHER chips are placed along the long side of the sensor, see Figure 4, and are the only part of the readout chain that is inside the tracking region. They provide fast voltage pulses of 20 V to activate the gate rows and clear the internal gate. The drain current is digitized by the 8-bit Drain Current Digitizer (DCD) with programmable gain and compensation for the pedestal current variation. The signal is then processed in the Data Handling Processor (DHP) which applies the pedestal and the common mode correction and also controls the SWITCHER sequence. The module is connected to the rest of the world through a Kapton Flex Cable (also visible in Figure 4) which transmits the data to the outside and supplies the ASICs and the matrix with the required voltages from the power supply.

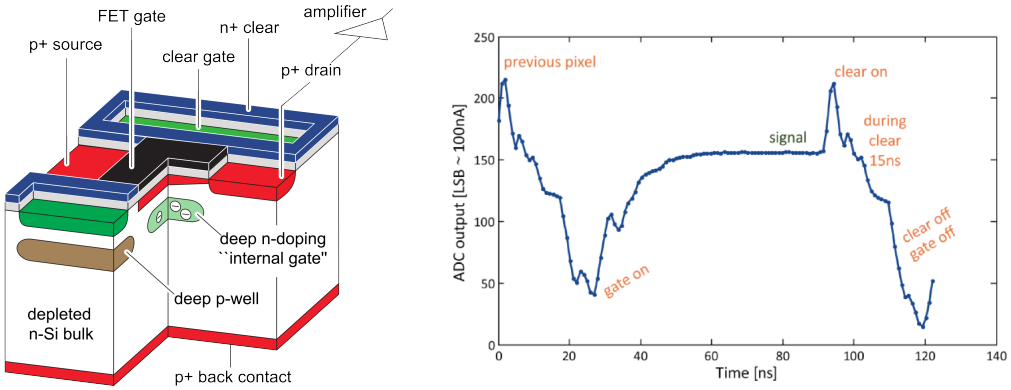

Figure 2: (left) DEPFET technology principle. (right) Single pixel current output as seen by the Drain Current Digitiser (DCD) with clear at the end of the cycle.

A dedicated operation mode has been developed in order to disable the PXD in a window of 300 ns when the bunches just injected in the ring transit near the IP. The particle losses of these bunches will produce background bursts in the detectors for hundreds of turns in the ring, corresponding to damping time of a few milliseconds. If the ionizing charge produced by this machine background is collected, the PXD dead time would result in around 20%, which is not acceptable. The PXD group has developed the so-called *gated-mode operation* of the detector in which the ionized charge is not collected in the internal gate, effectively disabling the PXD.

The PXD is composed of 8 ladders for layer 1 and 12 for layer 2 for a total of about 8M pixels. Each layer is composed of two modules with pixel sizes varying from $50 \times 55\,\mu m^2$ to $50 \times 85\,\mu m^2$ depending on the distance from the interaction point. The first produced module with the final pixel cell design and the final metallization is shown in Figure 4. The consequences of multiple scattering are minimized having layer 1 (2) just 1.4 cm (2.2 cm) away from the IP, thinning the sensitive area down to 75 µm and positioning most of the readout chips outside the sensitive area, for an average material budget of 0.2%. A peculiarity of a PXD module is that it is an *all-silicon module*: the active sensor, the mechanical support, and the substrate for the whole routing of metal interconnectivity to the readout chips is silicon.

4. The Silicon Vertex Detector

The four outer layers of the vertex detector are equipped with double sided silicon detectors on n-type silicon with AC coupled readout. The SVD has a peculiar lamp-shade geometry, shown in Figure 3, that minimizes the material crossed by forward tracks. The average material budget for perpendicular tracks is about 0.8%. The silicon thickness is between 300 and 320 µm and the strip pitch depends on the side and the sensor position, more details are reported in Table 1. The strip pitches on the $r-\phi$ side are smaller than the ones on the z side in order to improve the resolution on the transverse plane. Pitches are also increasing with the distance from the IP, since increasing multiple scattering relaxes the requirements on the single hit resolution.

The strips are read with the APV25 [3] chip, developed for the CMS experiment. Each chip reads 128 strips and can read several samples along the shaping curve (*multi-peak mode*). The

layer	sensor type	readout strips $r-\phi/z$ side	strip pitch $r-\phi/z$ side	number of sensors	approx. active area (mm^2)
4,5,6	large	768/512	75/240 μm	120	7030
4,5,6 forward	trapezoidal	768/512	50-75/240 μm	38	5893
3	small	768/768	50/160 μm	14	4738

Table 1: Technical specifications of the SVD sensors.

shaping time of 50 ns represents a gain of more than a factor 10 in speed if compared to the readout chip of the former Belle SVD, and moreover it allows to reduce the occupancy. An additional gain of around 8 in speed is obtained by fitting on FPGA the shaping curve sampled[1] at 40 MHz in the multi-peak mode: the precision on the estimation of the peaking time will be of the order of 3 ns. This time resolution is impressive for silicon detectors and it is one of the main feature of the SVD.

Although the SVD is more than 3 cm away form the IP, the higher machine background from SuperKEKB requires that the short strips of a single sensor are read individually, unlike the previous silicon vertex detectors of Belle and *BABAR*, otherwise the occupancy would be too high. The readout chips of the modules that face the non-tracking region are easily placed outside the sensitive region. For the other modules (one in layer 4, two in layer 5 and three in layer 6) the readout electronics must be placed inside the tracking volume. This is achieved with the *chip-on-sensor* origami concept that consists in having all the APV25 chips reading both sides of the sensor on one side of it and folding the pitch adapter to connect the strip of the other side to the corresponding readout chips. A photograph of an origami module is shown in Figure 3. This way both sides of each sensor can be read by a set of APV25 chips placed on top of the sensor, minimizing the strip occupancy. A second benefit of the origami concept is the effective reduction of the noise since strips and pitch adapter are short, hence the capacitance at the charge preamplifier input is reduced.

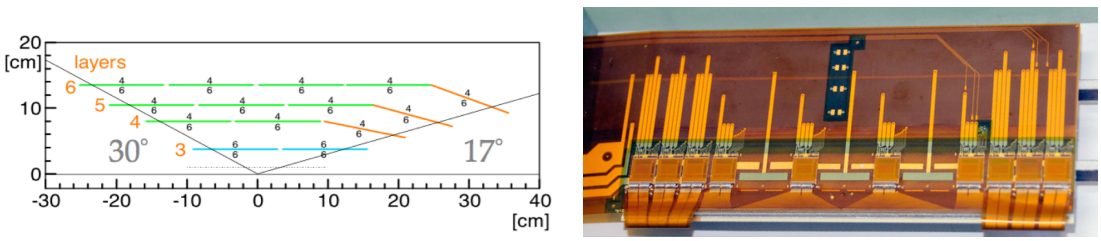

Figure 3: (left) SVD layout. (right) SVD Origami module, the readout chips are visible on top, as well as the folded pitch adapters, while the sensor is covered and it is not visible.

5. The System at Work

Four SVD modules and one small PXD module have been tested [4] with an electron beam of 2 to 6 GeV in a 1 T magnetic field at the DESY Laboratories, in Hamburg. The data acquisition

[1] 3 or 6 samples.

was performed by a *pocket* version of the *Belle II* DAQ, at a trigger rate of around 1 kHz. This was the first combined test of SVD and PXD modules and was a success from the detectors point of view, the DAQ and the tracking. The figure of merit of this achievement is the demonstrated correct functioning of the *Region of Interest* finding algorithm (ROI). The ROI finding algorithm consists in performing online tracking with the four SVD layers, extrapolating the tracks towards the PXD sensor planes and defining rectangular regions which should contained the fired pixels. Only the pixels inside the ROIs are further processed.

6. Conclusions

The *Belle II* Vertex Detector is composed of two systems with different characteristics, complementary to each other: the PXD is a very light detector and it will provide unambiguous 2D hits while the SVD will have an excellent time resolution. The VXD will allow an unprecedented precision in the determination of the primary and secondary vertices of B and charm meson decays.

Great achievements have been reached in the last months: the first DEPFET sensor with final pixel design and the first mechanically precise and electrically working ladder of SVD layer 5 have been built and are shown in Figure 4.

The VXD construction is proceeding. The SVD construction sites are all entering in production mode in order to start the ladder mount in April 2016 and finish the assembling in February 2017. The PXD group will start the main sensor production at the end of 2015 to have the PXD ready at KEK in April 2017. The PXD and SVD will be integrated at KEK in June 2017 and installed in April 2018, to be ready for data taking starting at the end of 2018.

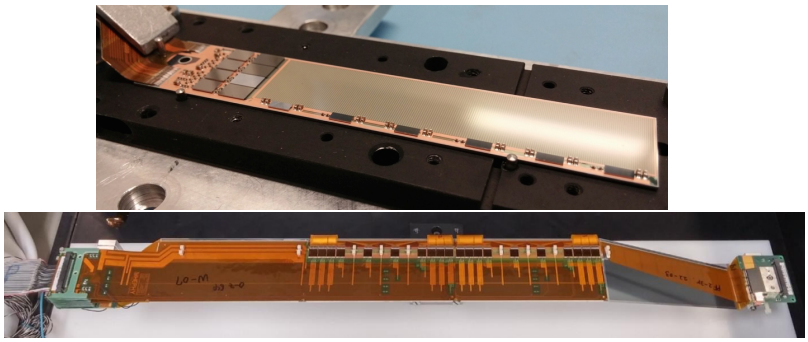

Figure 4: (top) A PXD module with final pixel cell design and the final metallization. (bottom) A mechanically precise and electrically functioning SVD layer 5 ladder. The two photographs have different scales, the shown SVD ladder is around 6 times longer than the shown PXD module.

References

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[3] M. French et al., *Nucl. Instrum. Meth.* A 466, 359 (2001).

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