Advanced Testing Techniques for ASICs and MCMs

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Abstract:

This paper sets out to discuss some of the following subjects associated with testing today's Mixed Signal, Multi Chip Module and Sub Micron ASICs. Testing during product development phases of engineering test and production test along with the economics of test, specifically the criteria needed when considering purchasing a specific type of tester and what tests are performed on the device under test. There will also be a description of the utilities available for device debug and an analysis of the testing challenges, specific tools and methodologies to provide solutions for the devices discussed in this paper.

Introduction.

Test has always been considered to be an unnecessary overhead during the product development phase, as a designer would argue that simulators provide sufficient fault coverage to test the most complex of device. This is not necessarily true when viewed from the test engineer's perspective as he would have converted "perfect" simulation files into his tester format only to find that due a process fault the device does not work. It is here that the detective work starts. His first samples will either be on a wafer, necessitating the use of a wafer prober, or in packaged form, probably assembled from visually good die. The type of tools he will need to use may be a Photo Emission Microscope to look for hot spots, an Electron Beam system (Ebeam) to analyze node voltages and a Focused Ion Beam system (FIB) to repair broken tracks or lay down new metal. Once all the problems are resolved in this product development phase, then the device is released for production, but again only after many different process runs at the extremities of the "recipe" and after exhaustive hot and cold testing and possibly "burn in" where the device is subjected to varying periods of extremities of hot (>150°C) and cold (<-55°C)

Economics of Test.

When considering the Economics of test some of the following factors come into play, such as tester type, tests to perform, and tester utilization. When deciding which tester to use it is always important to consider whether it is actually worthwhile buying a tester. It could possibly be better to subcontract test to a test house or a wafer fabrication suppliers test facility if only a few designs are done each year. Assuming it is worth buying your own tester, does its price fit your budget ?, is it easy to use ?, will you get a return on your investment ?, will you have to run it 24 hours a day?, does it need expensive

services such as air conditioning or refrigeration units to run? or can you program it off-line?, thus enabling many engineers to prepare test plans without actually using the tester. If the tester is a different type to other Automatic Test Equipment (ATE) then it is worth considering the ease of software program transfer from Tester A to Tester B, and whether a complete set of fixtures are required, or just a compatible mother board which accepts interchangeable device interface boards from either tester.

How Much Test?

There has all ways been a concern as to what tests should be performed and how much fault coverage they can achieve. Traditionally Functional tests have found most faults as they check the device as it would work in its typical operation. As devices and systems have become more complex then the need for Scan and Built in Self Test (BIST) methods are needed, however the disadvantage to this is that they consume extra silicon area, which designers are not too willing to give up. Extra silicon area means a higher chip cost, however this is still worthwhile as savings in field returns are almost eliminated if faults are found before customer shipment. Iddq is a more recent technique to find faults where the device is tested with a special set of vectors which are used to put it into a quiescent state and then monitor the supply current. A faulty gate oxide short is normally found using this technique. A monitor is required as it not only has to sink high chip currents when the device is operating normally, but also has to measure femto-amps when in a quiescent mode. Not one of these four techniques is better than the others as these methods complement each other to come closer to achieve that elusive 100% coverage.

Types of Test Equipment.

There are five types of test equipment which may be used :
System Test will test parts in the working environment they are destined for by using a dummy package with flying leads to the Device under Test (DUT). The extra leads could cause timing delays and it would be difficult to automate the test process with a handler.
Rack & Stack would utilise GPIB or VXI instrumentation with a fixed configuration controlled by a host computer for test. Although this would provide a better solution for test no automation would be possible.
Engineering Testers are small floorstanding testers, which have many versatile test sources, allowing simple reconfiguration. They have low running costs and are capable of automation of tests.
Production Testers are much larger than an engineering tester and require more elaborate services. Although they cost more, they have more resources per pin with good automation.
Home Brew Testers are designed in house, normally costing the same as an engineering tester, but at the cost of development time and could have support issues if their designers change jobs.

Typical Tests Performed

The following tests are normally performed to completely check device performance.
Continuity Tests check that the device is in contact with the tester by checking the presence of an protection diode; they are particularly useful when wafer probing
Functional Tests /Scan Tests are normally performed at a Low and High Vcc Level Power Consumption is measured when the device is either in a Static, Dynamic or Quiescent state
DC Parametric Tests check for Input and Output pin Leakage. Gross Pin Leakage Output Level. They require the use of a Parametric Measurement Unit (PMU) which is capable of either forcing voltage and measuring current (or vice versa) on the pin under test.
AC Parametric Tests check for Setup / Hold Timing on input pins and Propagation Delay on output pins.

Tools for Automatic Test

Pattern Conversion will allow conversion from a simulator output file (for example verilog .vcd format) to create a tester ready setup and pattern file.
Graphical User Interfaces make the tester easy to use through a series of windows that instantaneously show and allow modification of the test settings.
Graphical Programming makes test flow programming an easy task, with the use of icons (similar to subroutines) and wiring (program flow). This is a much easier than programming in more traditional languages such as "C", Pascal, Basic or Fortran.

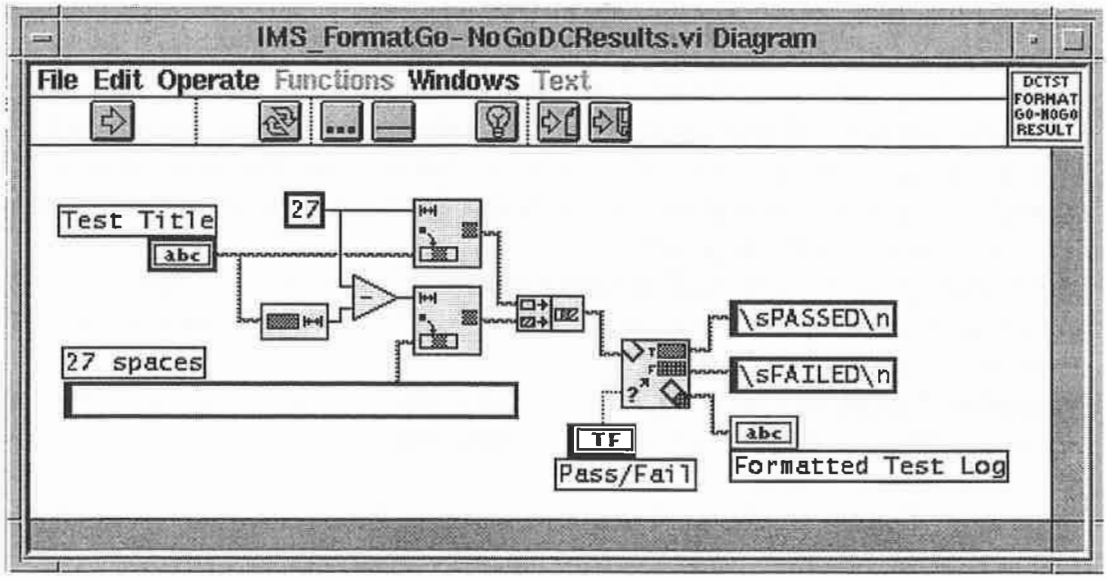

Figure 1 - Example of Graphical Programming Software

Macros allow test setups to be stored within the tester, thus eliminating unnecessary communications between a host computer and the ATE.

Test Sequencers give a graphical representation of the tests performed with the measured results, Pass/Fail and Failure Bin information.

Step	Step Title	P / F	O	Mode	Action Taken
1	Continuity	PASS	–	Normal	Continue
2	Loose Functional	PASS	–	Normal	Continue
3	Tight Functional	PASS	–	Normal	Continue
4	Voh–Vol	PASS		Normal	Continue
5	Iih–Iil	PASS	–	Normal	Continue
VDD	Vdd	PASS	–	Normal	Continue
SHMOO	Vdd vs Fmax	PASS		Normal	Continue
VIDEO	Signal Integrity	PASS	–	Normal	Continue
FullPattern	Vector Burst	PASS	–	Normal	Continue
Func350	350MHz	FAIL		Normal	Continue
Func300	300MHz	PASS	–	Normal	Pass 300MHz
Func250	250MHz		–	Normal	

Figure 2 - Example of Test Sequencer

Shmoo Plots are versatile flexible plotting utilities that show how a device reacts to different values of test parameters in 2-D plot. They may display different failure modes, first fail vectors and may be run in batch modes with the results sent to file.

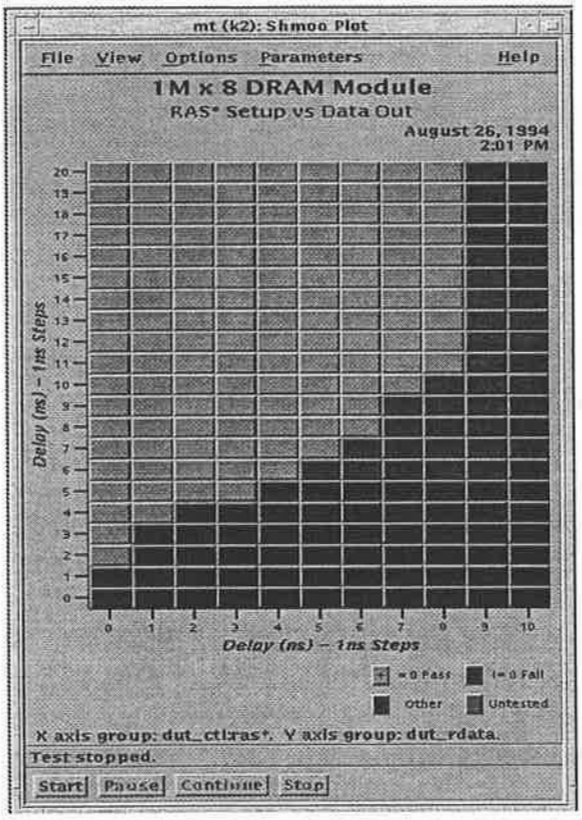

Figure 3 - Example of a Shmoo Plot

Off-line Programming not only provides an easy test program generation tool, but will also check for tester resource compatibility.
Conversion to Other ATE tools help when transferring test setups and patterns to other ATE.
Virtual Test gives the test engineer the ability to simulate the test environment with the DUT before it is even fabricated, which in turn reduces the test development time.

MCM Testing

Although an MCM provides a neat compact package with more functionality than a semiconductor device due to the ability to mix different technologies, large chips or just to incorporate components that would be restrictive to include on a chip, it is a complex device to manufacture and test. The important ingredients are fairly good die (FGD) to be put down on a known good substrate (KGS) which effectively creates a small equivalent printed circuit board (PCB). The key to testing is to use PCB test techniques such as Structural, Functional and Final test., however due to the value of components being used in the assembly process it is normally cost effective to rework faulty parts. The manufacturing process may be summarized in the following diagram (figure 4)

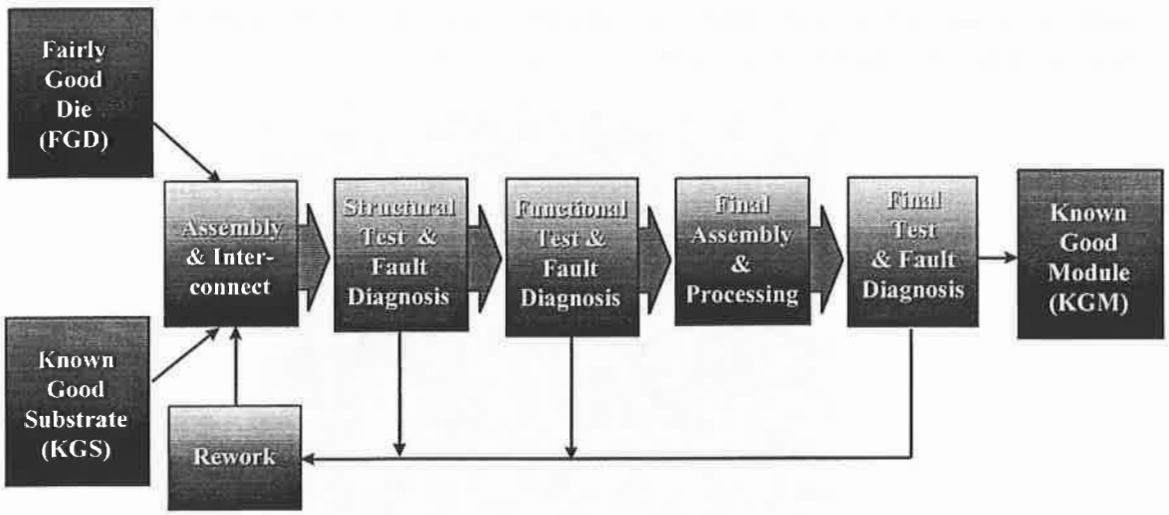

Figure 4 - Summary of the MCM Manufacturing Process

It is important that devices with Scan and BIST are used in an MCM, although this may not be possible, and special software is needed to compensate for the lack of testable devices.
The test generation process requires Netlist and Boundary Scan Data Library (BSDL) information which have to be analyzed to prepare a set of Serial Vectors (SVF) for test and a test analysis report (to give an indication of how much fault coverage). Once the MCM has been tested the test failures have to analyzed with Boundary Scan Map information to create a Fault Dictionary of where the failures are physically located on

the MCM, thus allowing repairs. This process is summarized in Figure 5. The important test tool needed is the ability to analyze long lengths of Scan Data by segmenting it into Frames and Clusters, thus making it easier to check the response from a known stimulus. The benefits from this technique are that the data is viewed logically, the errors are isolated and are interpreted much faster.

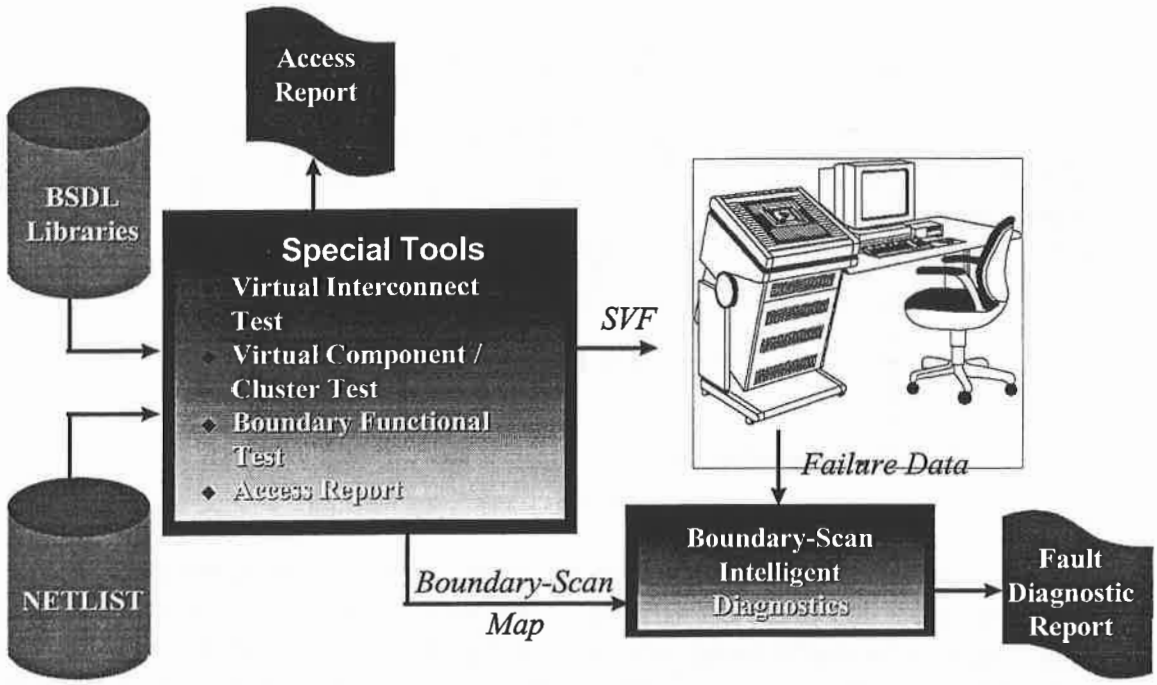

Figure 5 - Summary of the Fault Isolation Process in MCM Test

Some of the typical failures are due to wrong and or missing die, die internal failures, die input/output failure, interconnect opens or shorted and die interactions.
The testing methodologies may be summarized by the following descriptors : Interfaces (to other MCMs), Ingredients (of the MCM) Interactions and Interconnects (between die/components).

Sub Micron Testing

Sub Micron designs pose a different set of test problems due to the high speeds and lower supply voltages. As the device geometries are much smaller than older devices the gate delays and interconnect delays are becoming the same. Synthesis tools are needed in the design phase and similar tools are needed for test.
The two main test techniques used are :
Flexible Clocking - High Internal Clock speeds are achieved using a Phase Locked Loop (PLL) circuit and in order to analyze speed failures this PLL needs to be bypassed and the input clock has to have the special feature to provide up to 8 clocks per data cycle (with the added ability to provide odd or fractional clocks per data cycle). This clock should

also be capable of changing the delay and widths of this clock even down to a composite sub-cycle.

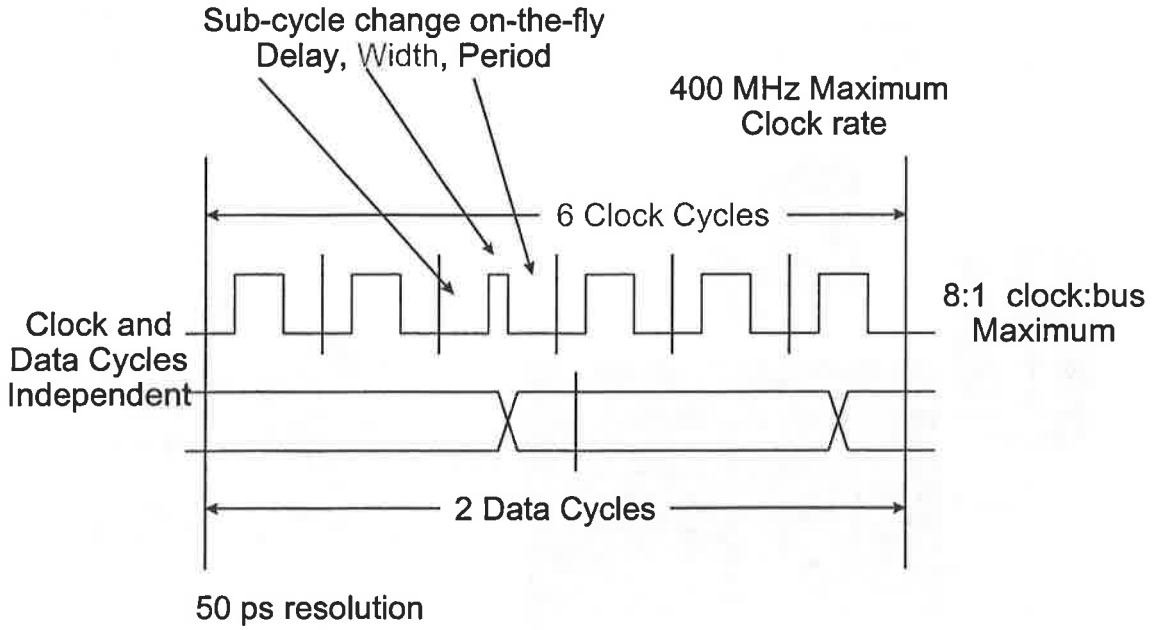

Figure 6 : Flexible Clock Characteristics

Cycle Stretch and Cycle Shrink - As there are now critical paths inside the device as gate and interconnect delays are the same there is a need to change the timing on a per cycle basis. This is achieved by being able to either stretch or shrink other pin timings on a per vector basis with the use of different timings or timesets. This provides useful timing information for the test engineer to create a timing fault dictionary to analyze failure mechanisms.

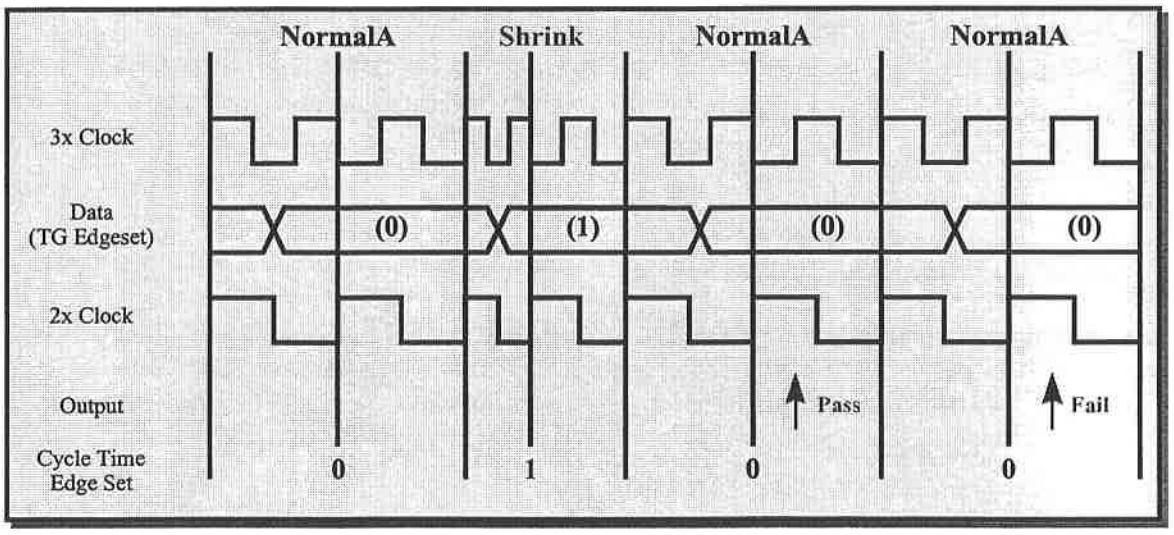

Figure 7 : Cycle Shrink Example

Tools - An important tool that is used is a Time Navigator which automates the manual process of creating timesets and timing search algorithms such as domino and ripple effects. Domino effects change the timing on successive cycles which causes the timing to be sped up (or slowed down) from a starting vector. Ripple effects also changes the timing on successive cycles but only changes cycle timing on one vector at a time.

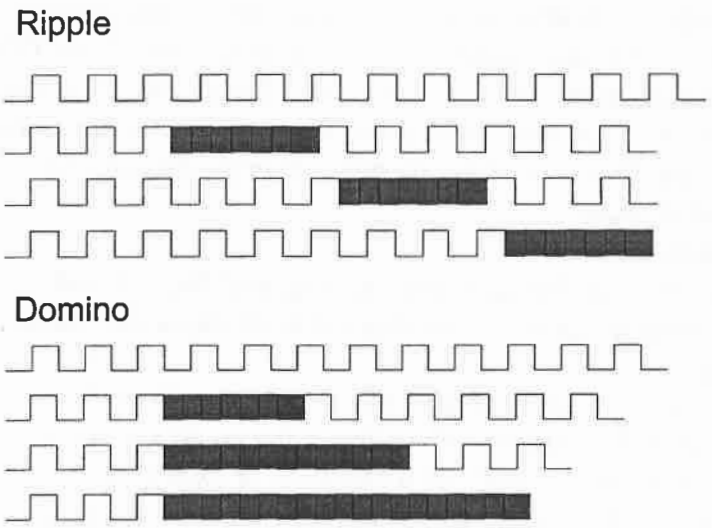

Figure 8 : Ripple & Domino Effects

Mixed Signal Testing

As semiconductor processes have become much easier to control, so it has been much easier to include analogue circuitry into the digital domain. The mixture of these two separate worlds has lead to a variety of mixed mode solutions in the fields of Multimedia, Datacommunications, Medical, and Telecommunications. When taking a typical Multimedia device such as a RAMDAC, there are many tests needed to check out its functionality for both Audio and Video Performance (see Figure 9)

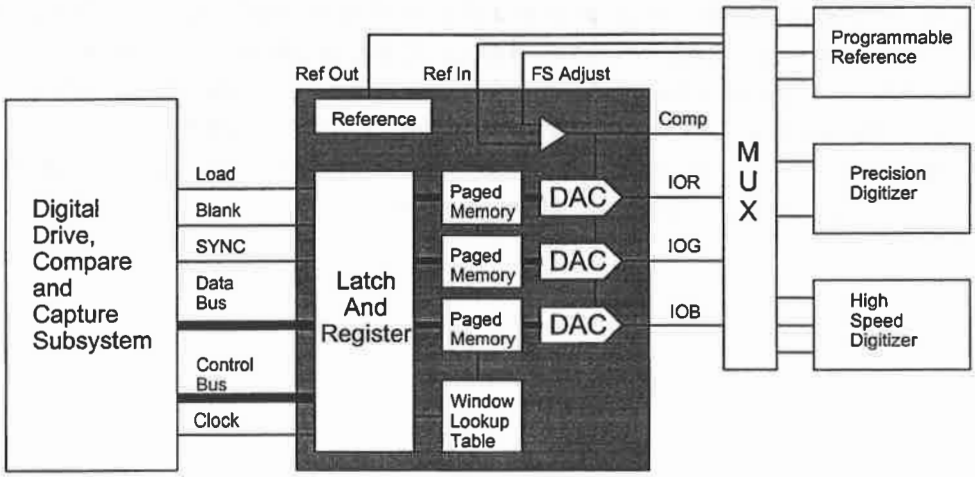

Figure 9 - Schematic of a RAMDAC Device

Typical Video Tests would be Glitch Energy, Gain Offset, DAC to DAC Matching, White and Blank Levels, Integral Non Linearity (INL), Differential Non Linearity (DNL),Least Significant Bit (LSB) Size, Rise, Fall and Settling Times.

Typical Audio Tests would be Full Scale I/O Voltage, Gain/Attenuation Step Size, Attenuation Step, Attenuation Span, Gain Step, Gain Span, Dynamic Signal Performance, Signal to Noise and Distortion (SINAD), Signal to Noise Ratio (SNR), Total Harmonic Distortion (THD), Spurious Free Dynamic Range (SFDR), Dynamic Range, Inter Channel Isolation, Frequency Response, Filter Characteristics, Transition Band, Stop Band, Stop band Rejection, Out of band Energy, Group Delay, and Power Supply Rejection Ratio (PSRR).

Test Requirements

Not only can test can be split into Analog and Digital, but also into Stimulus and Response. To cover all these possibilities the following tester features are required.

Analog Testing

The stimulus resources could consist of an Arbitrary Waveform Generator (AWG) and Reference Voltages for extreme DC voltages that could not be provided by the ATE. The response resources could consist of a Digitizer or Digital Storage Oscilloscope (DSO) , Network Analyzer and a Spectrum Analyzer. These type of instruments would either be available as a GPIB or VXI instrumentation depending on the performance required.

Digital Testing

The digital resources needed would consist of a high speed clock with the ability to provide up to 8 clocks per data cycle and be capable of speeds in excess of 200 MHz. The data stimulus and response section should also be capable of performing at speeds up to 200MHz.

Conclusions

Although design tools have advanced considerably over the years there is still a need for test to investigate all the fabrication defects created in the manufacturing stage of the production cycle, whether it be at naked die level or at packaged part. In order to survive in the competitive world of ATE, Tester Manufacturers have to work closely with Semiconductor Manufacturers to develop solutions for tomorrow's integrated circuits. Finally although test is sometimes the forgotten process in the manufacturing cycle when budgets are reviewed, there is still an important need for it as the consequence would be the need for expensive field repair or replacement.