



The Cluster Control Board of the JEM-EUSO mission

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Abstract: The Cluster Control Board (CCB) is one of the key elements of the JEM-EUSO read-out electronics, which manages the data received from eight units of the Photo Detector Module (PDM) of JEM-EUSO, performing data selection and transmission. To reduce the large amount of data produced at the detector level and to discriminate the good Extensive Air Shower (EAS) events from the spurious ones, a hierarchical trigger scheme over two levels has been developed. The first trigger level consists of three sub-levels which are implemented within the front-end Application Specific Integrated Circuit (ASIC) and the PDM electronics. The second trigger level is implemented in the CCB electronics. After the onboard processing of the data received from 8 PDMs at a rate of around 57 Hz, potentially good events are transmitted to the onboard CPU at the level of around 5 mHz. In this paper, we will firstly present the algorithm developed for the second trigger level, focusing on its implementation in hardware. The algorithm aims at distinguishing the unique patterns produced on the focal surface by the EAS from the ones produced by background events. It is based on the scan of a predefined set of directions, which covers the complete parameter space, to find good patterns associated with the EAS. The final set of directions has been carefully optimized to adapt the algorithm to the limited on-board computing power. To fulfill the requirement on the processing time, the algorithm was implemented in a Field Programmable Gate Array in order to make use of its parallel processing capabilities. After presenting the current architecture of the CCB and discussing the complex interfaces with the other elements of the read-out electronics, we will report on the performance of the laboratory model.

Keywords: JEM-EUSO, Cluster Control Board, detector, electronics

1 Introduction

The planned Extreme Universe Space Observatory (EUSO) - attached to the Japanese Experiment Module (JEM) of the International Space Station (ISS) - is a large Ultra Violet (UV) telescope to investigate the nature and origin of the Ultra High Energy Cosmic Rays (UHECR) by observing the fluorescence light produced in Extensive Air Showers (EAS).

The main instrument of JEM-EUSO is a super-wide $\pm 30^\circ$ Field of View (FoV) telescope, which will be able to trace the fluorescence tracks generated by the primary particles with a timing resolution of $2.5 \mu\text{s}$ and a spatial resolution of 0.07° (corresponding to about 550 m on ground), allowing to reconstruct the incoming direction of the UHECR with an accuracy better than a few degrees [1].

The Multi Anode PhotoMultiplier Tube (MAPMT) used as the basic detector element was developed by RIKEN in collaboration with Hamamatsu Photonics K.K. and has 64 channels in an 8×8 array.

As the electronics has to handle over $3.15 \cdot 10^5$ pixels, the Focal Surface (FS) has been partitioned into subsections

- the Photo-Detector Modules (PDMs) - and a multi-level trigger scheme has been developed. In the current baseline design, there are two trigger levels: the 'first level' trigger (L1), which is implemented within the PDM electronics and the 'second level' trigger (L2) which is implemented in the CCB electronics.

2 L2 Trigger Algorithm

2.1 Overview

The fluorescence light from EASs (induced by UHECRs) looks like a thin luminous disk, which travels ultra relativistically on a straight path through the atmosphere. As the EAS produces more particles, the luminosity of the disc will also increase until the shower reaches its maximum and then fades out. A typical proton induced shower with an energy of 10^{20} eV, will be detected as several photons per pixel and μs during a typical duration of tens to hundreds μs . As the detector has some exposure time for each image - the Gate Time Unit (GTU) - the fluorescence light will appear as a small spot, which moves on a straight line from image to image. The speed and the direction of this mov-

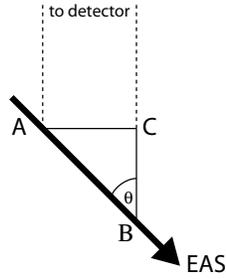


Figure 1: Kinematics of an EAS

ing spot is obviously depending on the incoming direction of the UHECR that is from the shower axis.

The principle of the L2 trigger algorithm is therefore trying to follow the movement of this spot over some predefined time, to distinguish this unique pattern from the background. In the case of an L1 trigger, the PDM electronics (see [2] for details) will send (together with the frame data) a starting point, which contains the pixel coordinates and the GTU which generated the trigger - also called 'trigger seed'. The L2 algorithm will then define a small box around this trigger seed, move the box from GTU to GTU and integrate the photon counting values. This integrated value is then compared to a threshold above the background and an L2 trigger will be issued if the threshold is exceeded.

It should be stressed, that an effective implementation of the L2 algorithm is constrained by the limited available computing power on board, due to power-, weight- and size-requirements and the space-qualification of the hardware.

Currently it is foreseen to have a total of 375 starting points for the integration, which are distributed equally over time and position around the trigger seed. Each integration will be performed over ± 7 GTUs for a predefined set of directions (see Section 2.2).

In order to follow the movement of the spot on the detector, the speed and the direction in terms of detector pixels has to be calculated.

We define in the following θ as the zenith angle ($\theta = 0^\circ$ means nadir direction of JEM-EUSO) and ϕ as the azimuth angle of the EAS ($\phi = 0^\circ$ means direction of the ISS movement). Since the EAS travels at the speed of light, the photons reaching JEM-EUSO from any point on the EAS are lagging behind the passing EAS-front by the time:

$$\Delta t = \frac{\overline{AB} + \overline{BC}}{c}$$

with c being the speed of light and $\overline{AB} + \overline{BC}$ as defined in Figure 1. Together with

$$\sin \theta = \frac{\overline{AC}}{\overline{AB}}, \quad \tan \theta = \frac{\overline{AC}}{\overline{BC}},$$

$$\tan \theta = \frac{\sin \theta}{\cos \theta} \quad \text{and} \quad \tan \frac{\theta}{2} = \frac{\sin \theta}{1 + \cos \theta}$$

it follows

$$\Delta t = \frac{\overline{AC}}{c \cdot \tan \frac{\theta}{2}}$$

as can be derived from Figure 1. If we define now Δx and Δy as the projections on the focal surface along x and y expressed in number of pixels and ΔL as the FoV at ground of a pixel in a time Δt (chosen as the GTU) we find

$$\overline{AC} = \Delta L \cdot \sqrt{\Delta x^2 + \Delta y^2}$$

and therefore

$$\theta = 2 \arctan \left(\frac{\Delta L}{c \cdot \Delta t} \cdot \sqrt{\Delta x^2 + \Delta y^2} \right) \quad (1)$$

$$\phi = \arctan \left(\frac{\Delta y}{\Delta x} \right) \quad (2)$$

2.2 Number of Directions

Due to the fact, that the incoming direction of the EAS is unknown, the approach of the L2 trigger algorithm is simply to try out a set of directions which covers the complete space ($\theta = 0^\circ \dots 90^\circ$ and $\phi = 0^\circ \dots 360^\circ$). The integrated count value will have a maximum when we 'hit' the (nearly) correct direction, because in this case the integrating box will follow the spot.

As the integration over the directions is a time consuming task, a trade-off between the number of directions and the available computing power has to be found. In addition, as the hardware only works on whole pixels, some directions will produce the same offsets Δx and Δy - for example, in the extreme case $\theta = 0^\circ$ (which means the shower axis is parallel to the optical axis of the telescope), the spot is not moving at all there is no need to integrate over different ϕ angles.

Therefore, a minimum set of directions (containing 67 θ - ϕ combinations in total) was selected and evaluated with simulations aiming to optimize the design according to the constraints mentioned above.

3 Cluster Control Board

3.1 Overview

In case an L1 Trigger is issued, the data of the ring buffers from 8 PDMs are transferred to the CCB and the L2 trigger algorithm is executed. The data from the PDMs are processed independently, as it is not intended to have a fixed geometrical relationship between the PDMs connected to one CCB. In case an L2 trigger is found within any of the 8 PDMs, the complete data are transferred to the mass memory module of the Mission Data Processor (MDP).

Due to the necessity for parallel processing and the need for a high number of input/output pins (for the eight data interfaces to the PDMs and the interface to the MDP, besides

various other interfaces for control and housekeeping) it is foreseen to implement the L2 trigger algorithm inside an Field Programmable Gate Array (FPGA) chip on the CCB. As a baseline, it is planned to use a radiation tolerant Xilinx Virtex-4QV FX-140 and as an advanced option the use of a radiation hard Virtex-5QV is currently under investigation (see [3] for the specification).

The current block diagram for the FPGA is given in Figure 2, which is basically the implementation of the L2 trigger algorithm. Besides the eight Linear Track Trigger (LTT) modules it is planned to use the microcontroller cores for 'low speed' purposes, such as the configuration of the LTT modules, housekeeping and the communication with the MDP.

In order to perform the necessary calculations as fast as possible, the hardware architecture of the trigger is highly pipelined and parallelized. As it is not possible to store the raw data completely in the internal RAM of the FPGA, the data will be written to an external memory upon arrival. Only the data necessary for the trigger calculation will be stored inside the FPGA to reduce the probably slow read/write access for the external RAM. A first data 'selection' will be done by the 'Data Allocator'-module. The data will then be passed to the '3x3 Sum'-module which performs the summation of the 9-pixels blocks in two stages (horizontal and vertical) for the whole frame which reduces redundant 3x3 summation to a minimum. The new frame generated this way is then trimmed to a 19x19 pixel frame around the seed and stored in the 'Frame Buffer' for ± 14 GTUs.

After the 'Frame Buffer' is filled completely (it contains the necessary information for the integration), the 'Address Generator' allocates the different 3x3 sums - depending on the starting point for the integration and the offsets for the various directions which are stored in a Look Up Table (LUT) - to the 'Accumulator'. After each direction-integration, the accumulated value is compared to the current maximum to select the overall maximum value and is then stored along with the information to which starting-point this value belongs ('Maximum Comparator'). When the integration process is finished for all starting points, the maximum value is compared to the trigger threshold ('Threshold Comparator') and an L2 trigger is issued if the threshold is exceeded. In this case the raw data buffer (external RAM) is sent to the mass memory module of the MDP, whereas the information at which pixel the maximum value was found, could be used by the MDP to calculate the pixel coordinates on the focal surface. This information then could be used as a target for the LIDAR to monitor the atmospheric conditions around the EAS (see [4] for more details).

3.2 Interfaces

The interface between PDM and CCB for the scientific data from the detector and for controlling/monitoring the PDMs is a critical part in the processing chain as many other

parts rely on the performance of this interface (e.g. the ring buffer on the PDMs, the implementation of the L2 algorithm and the dead-time of the instrument). In order to reduce the dead-time of the instrument, the event data (around 2.7 Mbit per PDM and event) has to be transferred as fast as possible within the hardware constraints. The current baseline is to implement a parallel bidirectional interface with 20 data channels running at 40 MHz. Due to the fact that the distance between the PDM and the CCB is about 1 m - as it is foreseen that the CCB is mounted on the back of the focal surface - it was decided to use the Low Voltage Differential Signaling (LVDS) standard which results in a more reliable interface, but doubles the number of lines needed. In order to reduce the weight of the harness, an advanced option is currently under investigation which uses a double buffer approach whereby a total of 4 data channels will be sufficient.

As a baseline for the interface between CCB and MDP (which will be controlled by an intermediate board - the Interface Data Acquisition (IDAQ) board) the SpaceWire standard was chosen due to its approved reliability. To reduce the overhead of the standard, a modified protocol will be studied as advanced option.

3.3 Results from the performance tests

To verify the correct operation of the 'Linear Track Trigger' module, a first simple test was developed where the 'PDM Interface' was replaced by a 'PDM Simulator' module. This module consists of a small Finite State Machine (FSM) and an 'Event Buffer' which is basically a large RAM, filled with the simulated data of an event generated by the EUSO Simulation and Analysis Framework (ESAF).

The data from the 'Event Buffer' are sent to the input of the 'Linear Track Trigger' module where it will be processed as described in Section 3.1. To have a more detailed look into the processing, the 'Accumulator', 'Maximum Comparator' and 'Threshold Comparator' are connected either to a ChipScope Virtual Input/Output (VIO) or an Integrated Logic Analyzer (ILA) module.

The output of the 'Accumulator' is sampled by the ILA module every time the integration of one direction is finished. This allows to compare every single integrated value with the ones coming from simulations and to verify the correct operation of the 'Linear Track Trigger'. Unfortunately, the sample buffer of the ILA module is limited (as it uses the internal RAM of the FPGA) and it was not possible (with this simple test) to store all 25125 integrator values. Therefore, only around 16000 integrator values could be recorded. But as all sampled values (including the overall maximum) are equal to the ones coming from simulation, it is assumed that this test was passed successfully - also due to the fact, that the correct behavior of the 'Linear Track Trigger' module was verified in advance with hardware simulations.

According to the current implementation, the decision of an L2 trigger could be performed within approximately 5

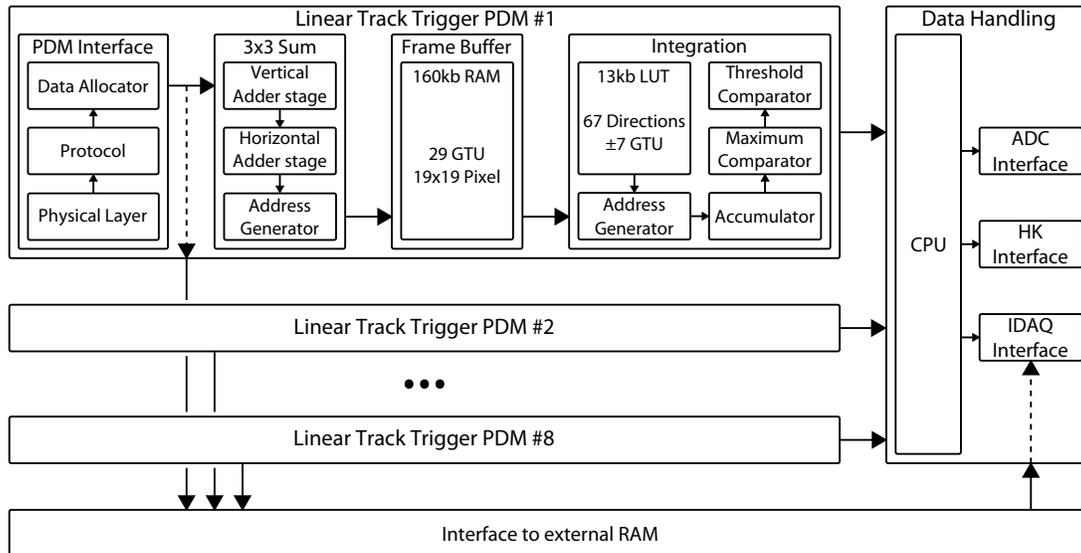


Figure 2: The current block diagram of the CCB FPGA. Most of the logic resources are needed for the eight 'Linear Track Trigger' modules which perform the L2 trigger algorithm and handle the data transfer from the PDM. As it is not possible to hold the data from all eight PDMs inside the FPGA RAM an interface to an external memory will be needed. Additionally, it is currently foreseen to use the integrated microcontrollers of the Virtex-4 FX140 to control and monitor the trigger modules and to handle the communication with the MDP and the housekeeping submodule.

ms. The time needed for the data transfer between PDM, FPGA and external RAM is not included in this number. It should be stressed, that the actual calculation time depends on the system clock of the FPGA, therefore, on the overall implementation. However, even if the system clock has to be reduced by a factor of 2 the calculation is still fast enough to meet the requirements, as 18 ms were allocated for the L2 trigger calculation.

4 Conclusion & Outlook

The developed hardware is still in phase A and a long way is necessary to reach the final space-qualified Cluster Control Board. The hardware implementation of the 'Linear Track Trigger' algorithm as L2 trigger is performing accordingly to the requirements. Based on the parallelization of the calculation process, the requirement on the processing time of the L2 trigger could be exceeded by a factor of 20. It should be stressed, that this value is highly dependent on the overall implementation of the CCB FPGA but at least the requirement was met.

In our current plan of the CCB development are the implementations of the interfaces to the Photo-Detector Module, to the Mission Data Processor and to the Housekeeping. We will then start the design of a first laboratory model of the CCB Printed Circuit Board. More information can be obtained from [5].

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