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Published by IOP Publishing for Sissa Medialab

Received: *November 15, 2016*
Revised: *January 8, 2017*
Accepted: *February 19, 2017*
Published: *February 28, 2017*

2017 JINST 12 P02020

LDQ10: a compact ultra low-power radiation-hard 4 × 10 Gb/s driver array

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Abstract: A High-speed and low-power VCSEL driver is an important component of the Versatile Link for the high-luminosity LHC (HL-LHC) experiments. A compact low-power radiation-hard 4 × 10 Gb/s VCSEL driver array (LDQ10) has been developed in 65 nm CMOS technology. Each channel in LDQ10 can provide a modulation current up to 8 mA and bias current up to 12 mA. Edge pre-emphasis is employed to compensate for the bandwidth limitations due to parasitic and the turn-on delay of VCSEL devices. LDQ10 occupies a chip area of 1900 μm × 1700 μm and consumes 130 mW power for typical current settings. The modulation amplitude degrades less than 5% after 300 Mrad total ionizing dose. LDQ10 can be directly wire-bonded to the VCSEL array and it is a suitable candidate for the Versatile Link.

Keywords: Analogue electronic circuits; VLSI circuits

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doi:10.1088/1748-0221/12/02/P02020

Contents

1 Introduction

At CERN, the next LHC upgrade (HL-LHC) will achieve higher beam luminosity compared to previous LHC, and then improve the statistical significance of the High Energy Physics(HEP). Consequently, the amount of experiment data generated by the detectors and the radiation levels will increase by tenfold in HL-LHC. This raises new challenges on ASIC development for data transmission systems, requiring higher data rate and reduced power consumption as well as better radiation tolerance [1–3].

The GigaBit Transceiver (GBT) and the Versatile Link, a 5-Gbps bidirectional optical communications link, has been developed and is now being mass produced the for Phase-I upgrade [1, 4, 5]. Due to the large number of channels in the future detectors required for data transmission, the power consumption of the chipset needs to be minimized. As part of the Phase-II upgrade program, the Low-power GBT (LpGBT) [6] and Versatile Link Plus (VL+) projects [7] aim at an overall power consumption smaller than 750 mW of the LpGBT chip (for one up-link) while pushing the data rate of the up-link to 10 Gb/s. The LpGBT chipset is currently being designed and implemented using a 65 nm CMOS process to achieve those targets.

A low-power and high-data-rate Laser Driver (LD) is an important on-detector component of the Versatile Link for the HL-LHC experiments. In 2015, we reported the design and measurement results of a low-power and radiation-tolerant 10 Gb/s VCSEL Driver (GBLD10+) [8]. The single-channel GBLD10+ consumes 31 mW and has a compact size of 380 μm × 1730 μm including the PADs. These features allow multiple of GBLD10+ chips to be assembled side by side in package, with each one directly wire bonded to a VCSEL diode.

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In this paper, we report the design and measurement results of a 4×10 Gb/s VCSEL driver array, the LDQ10, leveraging on the GBLD10+ design. At 10 Gb/s, each of the 4 channels in the LDQ10 consumes 32.5 mW under typical settings (4 mA modulation current and 6 mA bias current) and the total power consumption of the 4-channel LDQ10 is 130 mW including the digital control circuitry. It occupies a silicon area of 1.7 mm $\times$ 1.9 mm with a pitch of 250 um between each adjacent channel, allowing the LDQ10 to be directly wire-bonded to a quad-VCSEL array. Each channel has pre-emphasis capability to compensate for bandwidth and potential slow turn-on time of the VCSEL devices. Careful design and layout is employed to minimize the crosstalk, so that it has negligible effects on the driver performance. The LDQ10 was irradiated up to 300 Mrad showing little or no degradation off the performance.

2 Single-channel low-power 10Gb/s driver

We have successfully designed and demonstrated two low-power single-channel 10 Gb/s VCSEL driver ICs, GBLD10+ in 65 nm CMOS [8], and GBLD10 in 130 nm CMOS [9, 10].

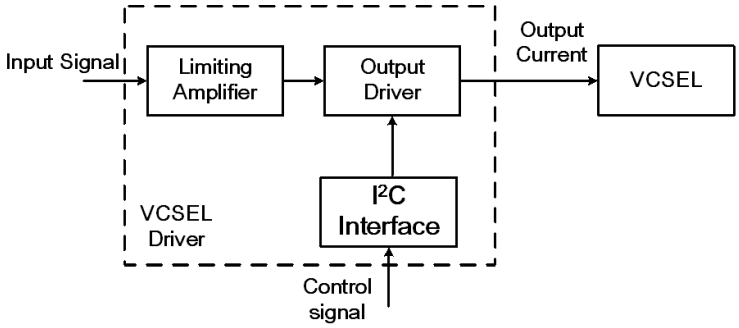
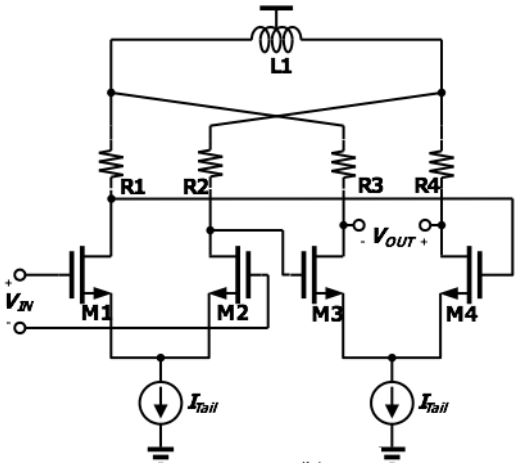


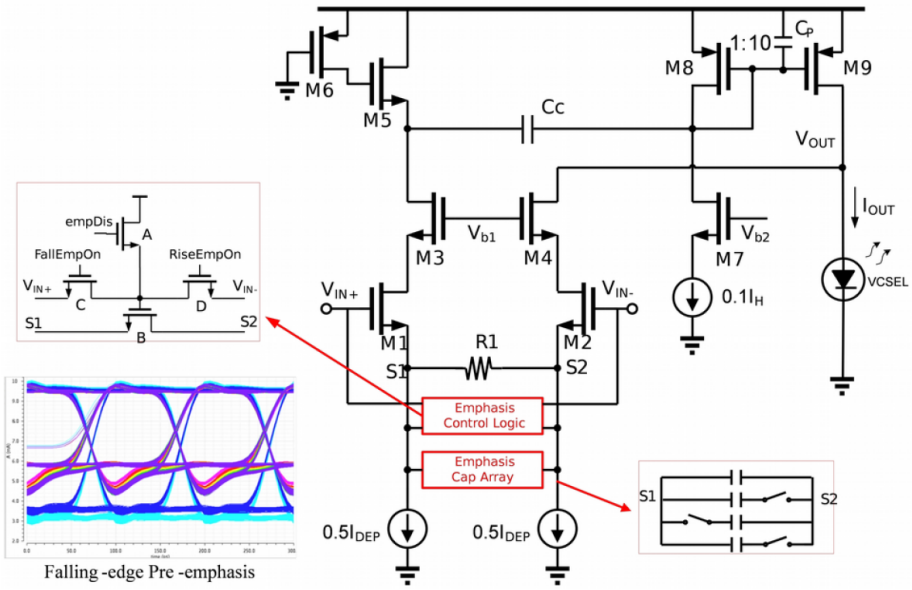
Figure 1. Circuit block diagram of GBLD10+.

A simplified block diagram of GBLD10+ is shown in figure 1. The main building blocks consist of a Limiting Amplifier (LA), an Output Driver (OD) and the I2C interface. The LA is powered by 1.2 V and provides more than 12 dB voltage gain for an input signal of 400 mV_{dpp} (differential peak to peak). The large signal swing at the LA output ensures complete switching of the modulation current by the OD. To meet the gain and bandwidth targets, as well as the stringent area requirement, a two-stage inductor-peaking topology is used. The traditional inductor peaking approach requires two inductors in a differential limiting amplifier stage, occupying a large die area. To minimize the area, we employed a topology that shares the inductor between two consecutive stages, as is shown figure 2(a) [8, 9, 11].

The OD is shown in figure 2(b) [10]. In order to reach a speed of 10 Gb/s, a feedforward path is built between the two branches by the coupling capacitor C_c. The high-frequency current roll off is neutralized by the compensation current generated by the feedforward path. In this design, we further boost the speed of the left branch by the "active inductor" load, which consists of transistors M5 and M6, to enhance the feedforward strength at high frequencies. An edge pre-emphasis function is also added at this stage to broaden the bandwidth and compensate the asymmetric falling/rising time caused by the turn-on delay of VCSELs [12].



(a)



(b)

Figure 2. Schematic diagram of the (a) LA and (b) OD.

3 4 × 10 Gb/s VCSEL driver array design

3.1 Driver array architecture

The block diagram of LDQ10 is shown in figure 3. It consists of four driver channels each working up to 10 Gb/s. Each channel provides bias and modulation current ranging from 0 to 12 mA and 0 to 8 mA, respectively, as is shown in figure 4. Here the bias current refers to the maximum current (the eye height) flowing into the VCSEL and the modulation refers to the AC amplitude (eye depth) of the current. The I^2C block controls the different functions of each channel, including the channel turn-on/off switches, the bias current, the modulation current, and the pre-emphasis configuration. All circuits are powered by 1.2 V for low-power operation except for the OD stage which is powered

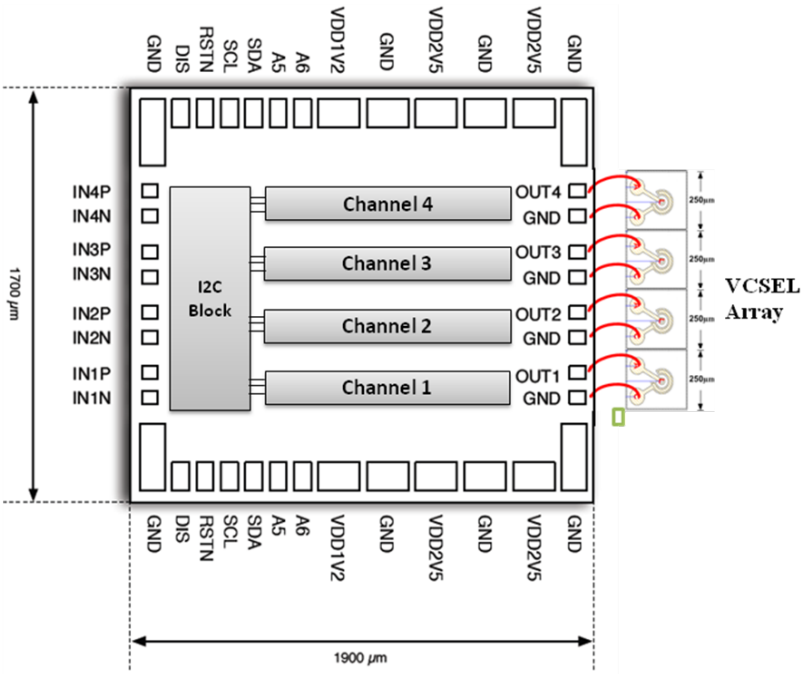


Figure 3. Driver array structure.

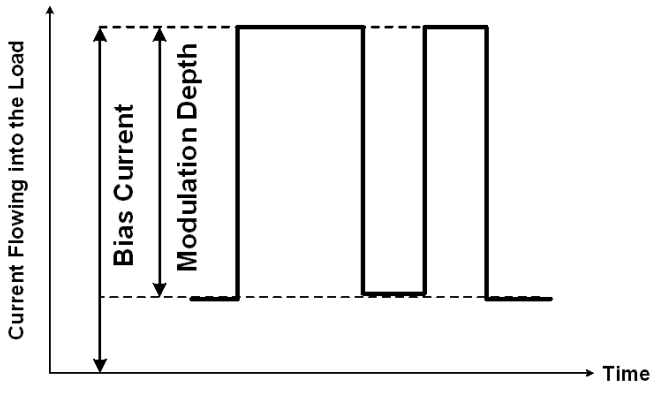


Figure 4. Bias current and modulation current definition.

by 2.5 V to accommodate the high turn-on voltage of VCSEL (typically 1.7 V). The transistors are biased carefully to guarantee no transistor works with more than 1.2 V. Each channel can be individually powered on/off to further save power consumption when needed.

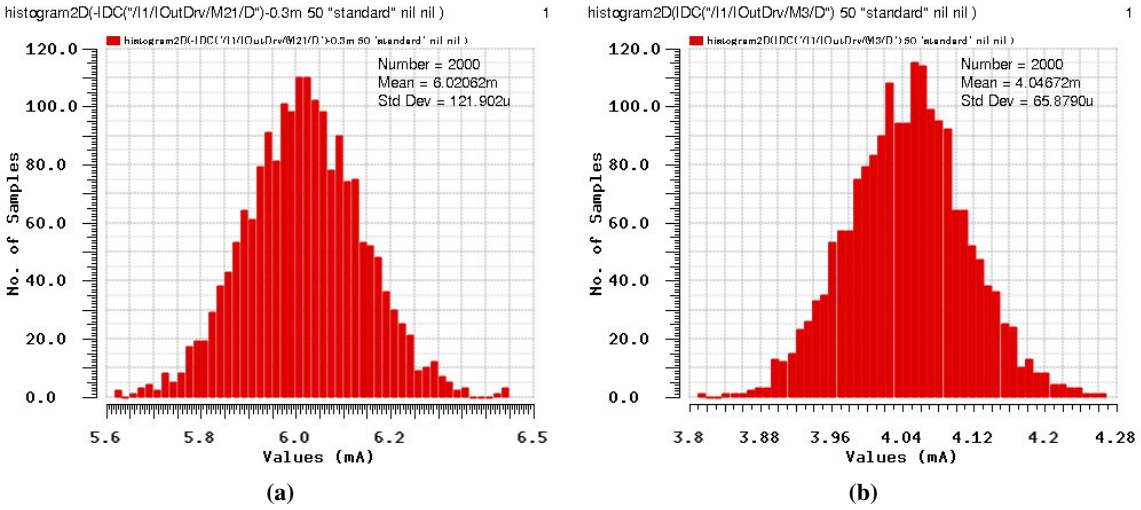
3.2 Input and output connection

Large on-chip pads and ESD parasitic capacitance may lead to reduction of bandwidth in the signal path. All these issues cast trade-offs on bandwidth, and ESD protection. In our design, standard ESD block is used. On both the data input and output of the VCSEL driver, small-sized pads ($60\,\mu\text{m} \times 45\,\mu\text{m}$) are used to reduce parasitic capacitance. The driver input is differential and contains a $100\,\Omega$ on-chip resistor, providing input impedance matching. At the output node, the

output pad is directly bonded to the anode of VCSEL device, while the cathode of VCSELs is bonded back to on-chip ground pads.

3.3 Monte Carlo simulations of bias current and modulation current

During chip fabrication, the process corners and device mismatch could lead to variation in both the bias and modulation current. In order to predict these variations, Monte-Carlo simulations of 2000 runs were performed and the results are shown in figure 5. The 3σ value of bias and modulation current is 0.36 mA and 0.2 mA, respectively, which is small compared to the nominal value (6 mA for the bias current and 4 mA for the modulation current). The design is thus robust against process variations and device mismatch.



(a) (b)

Figure 5. Monte-Carlo simulation (a) bias current (b) modulation current.

4 Testing results

Electrical, optical and irradiation measurements were performed to characterize the LDQ10. For electrical characterization, an Agilent JBERT N4903B was used for high-speed PRBS7 data generation and an Agilent DSA91204A Oscilloscope was used for output waveform measurements. When driving a VCSEL, the light signal was converted into an electrical signal by an Agilent 8163B and then measured in the oscilloscope. Figure 6 shows the electrical and optical testing boards which house the LDQ chip. Both board inputs are connected with on-board AC coupling capacitors and terminated by the on chip 100 Ω differential resistors. The output of the electrical board is AC coupled to a 50 Ω load resistor while that of the optical board is directly bonded to the VCSEL array.

4.1 10 Gb/s electrical measurement results

The eye diagram and jitter performance of LDQ10 was measured with PRBS 2^7-1 input data and BER of 10^{-12}. Figure 7 shows the 10 Gb/s electrical eye diagram with 4 mA modulation current and 6 mA bias current. The total jitter in the electrical eye diagram is 15.47 ps with an RMS random jitter component of 0.68 ps.

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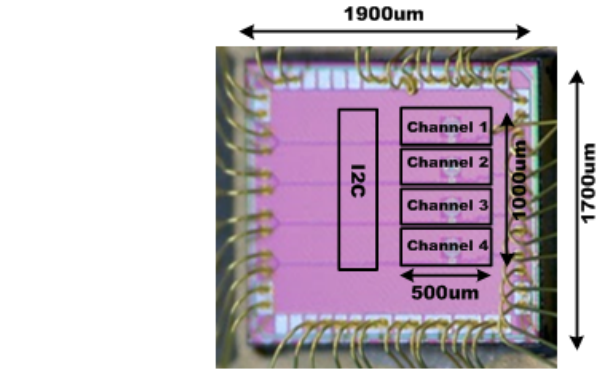
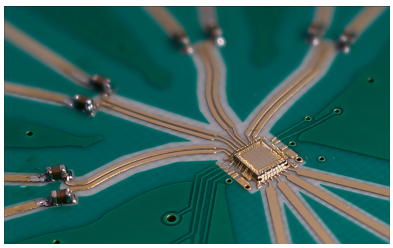
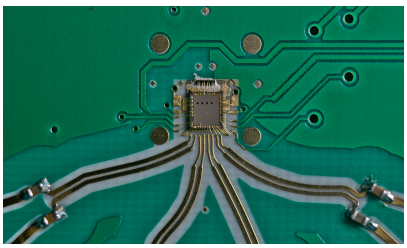


(a)



(b)



(c)

Figure 6. (a) Die photo (b) electrical testing board and (c) optical testing board.

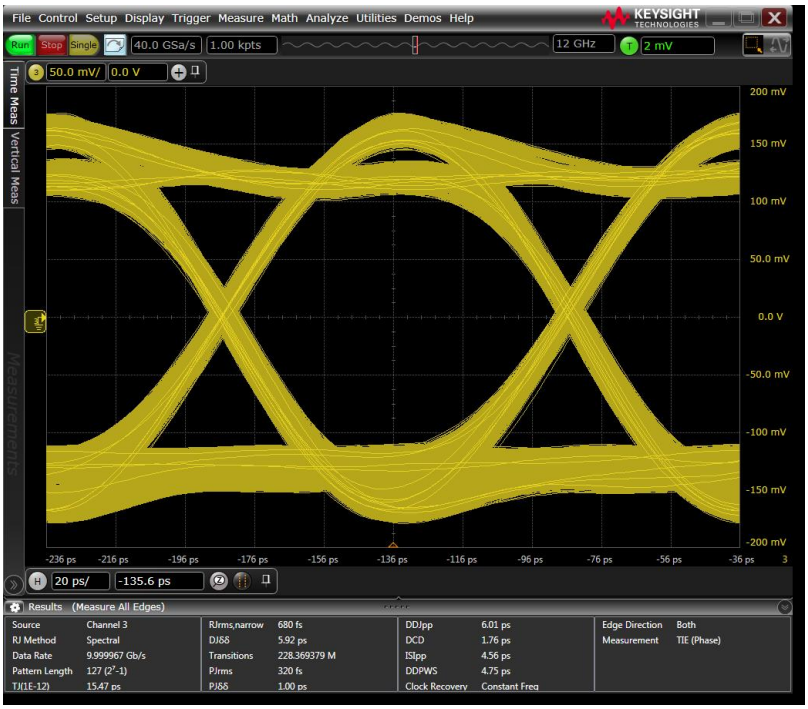


Figure 7. Electrical eye diagram.

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4.2 10 Gb/s optical measurement results

The optical board of LDQ10 is assembled with Philips Photonics ULM850-25-TT-N01xxU VCSEL array [13]. The eye diagram at 10 Gb/s is shown in figure 8, where the total jitter is 17.97 ps and RMS random jitter is 0.84 ps, demonstrating the good performance of LDQ10.

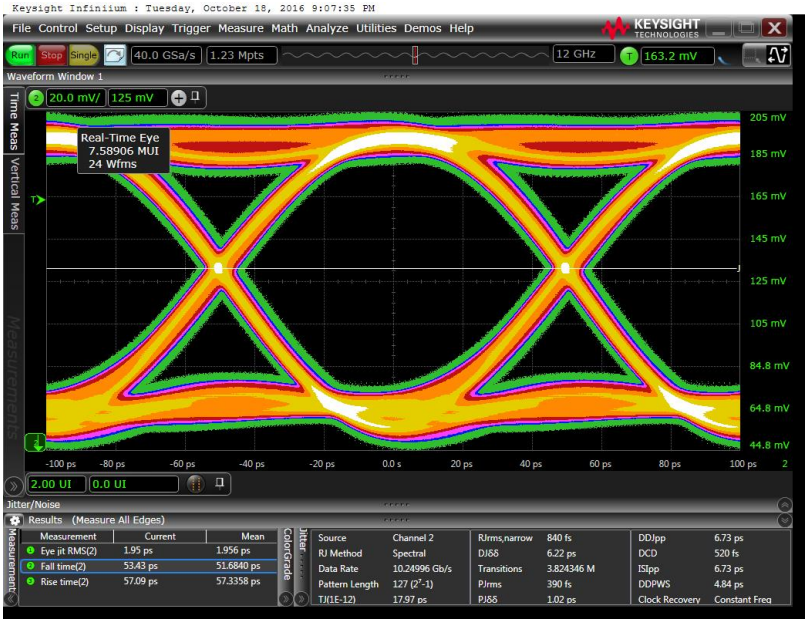

Figure 8. 10 Gb/s optical eye diagram with PRBS7 input data.

4.3 Crosstalk measurement results

Crosstalk among channels may increase the jitter and corrupt the eye diagram. The worst-case scenario for the channel under test happens when the other three channels are transmitting the same data but a different data sequence from the one being transmitted by the channel under test. In our design, a power/ground mesh with a large amount of on-chip decoupling capacitors was used to minimize the crosstalk effects. Figure 9 shows the comparison of performance between the scenario of only one channel being turned on and the worst-case scenario when all 4 channels are turned on. As evident from the results, the increase in the total jitter is less than 2 ps at the worst-case scenario compared to when only a single-channel is running. This demonstrates that the crosstalk has negligible effects on the driver performance.

4.4 Pre-emphasis measurement results

As mentioned in section 2, frequency-domain edge pre-emphasis is employed in LDQ10 to accommodate different parasitics and compensate for the VCSEL turn-on delays. When the bias current and modulation current are around optimum point, pre-emphasis has minimum effective on the performance. However, when the bias current and modulation current are much higher or lower than the optimal values, the pre-emphasis provides quite significant jitter improvement. Figure 10 shows the measured eye diagrams at 10 Gb/s with/without pre-emphasis. For figure 10(a) and 10(b), the bias current and modulation current are 7mA and 3.5mA, respectively. The total jitter is improved by 2.4 ps as shown.

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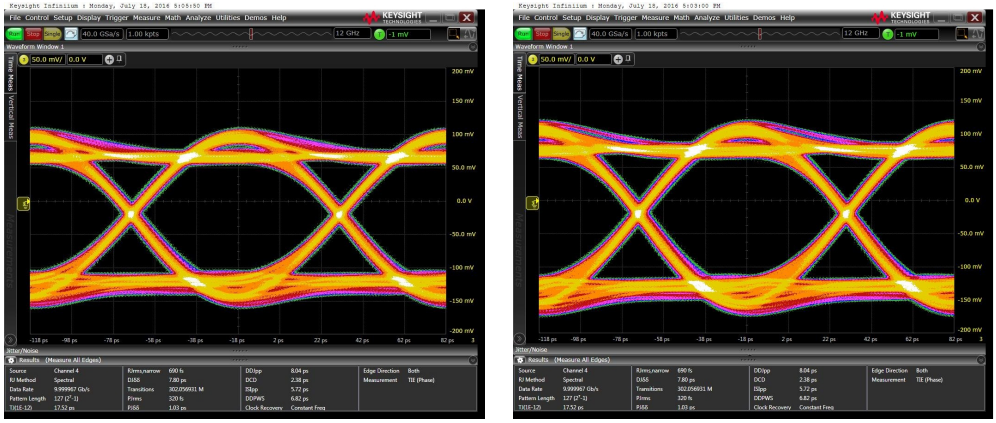

(a) (b)

Figure 9. 10 Gb/s/channel electrical eyediagrams of crosstalk meausrement (a) one channel turned on (b) four channels turned on under worst-case senario.

(a) (b)

Figure 10. 10 Gb/s optical eyediagrams with (a) no pre-emphasis (b) pre-emphasis on.

4.5 Measurement of output DC voltage sweep

Different VCSELs have a range of threshold voltages. Additionally, the forward voltages of VCSELs vary with different bias/modulation current. These characteristics require the driver to be able to operate under a wide range of VCSEL forward voltages. To demonstrate that the LDQ10 is capable of operating under large range of forward voltages, the DC output voltage was measured with a set up shown in figure 11. The output DC node was connected to a bias tee, providing different output DC voltages, simulating the conditions where VCSEL forward voltages are different. The output signal is AC coupled to the 50 Ω termination resistor of the oscilloscope. The performance of the driver is recorded with output DC voltages ranging from 1.6 V to 2.3 V, under 6 mA bias and 4 mA modulation current. The results show that the output modulation current varies less than 5 % when the output DC voltage varies from 1.6 V to 2.1 V. When the voltage exceeds 2.1 V and approaches 2.3 V, the modulation amplitude gradually decreased due to the reduction of the voltage headroom.

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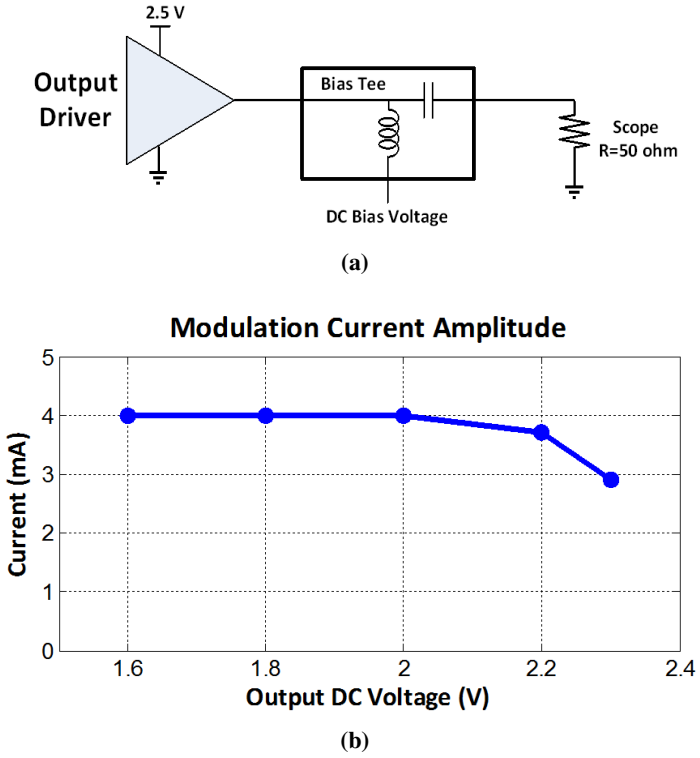


Figure 11. (a) Setup for output DC voltage sweep (b) effect of the output DC voltage on modulation current amplitude.

4.6 Irradiation measurement results

During the irradiation tests the chips were powered and X-ray irradiated for 3 days up to 300 Mrad dose with dose rate of 9 Mrad/hour. Plots of the total jitter and modulation depth vs. TID are displayed in figure 12. The change in these parameters under radiation dose up to to 300 Mrad is minimum. Plots of the supply current vs. radiation dose for one channel are shown in figure 13. The measurement results demonstrate the good radiation tolerance of the LDQ10 to ionizing radiation.

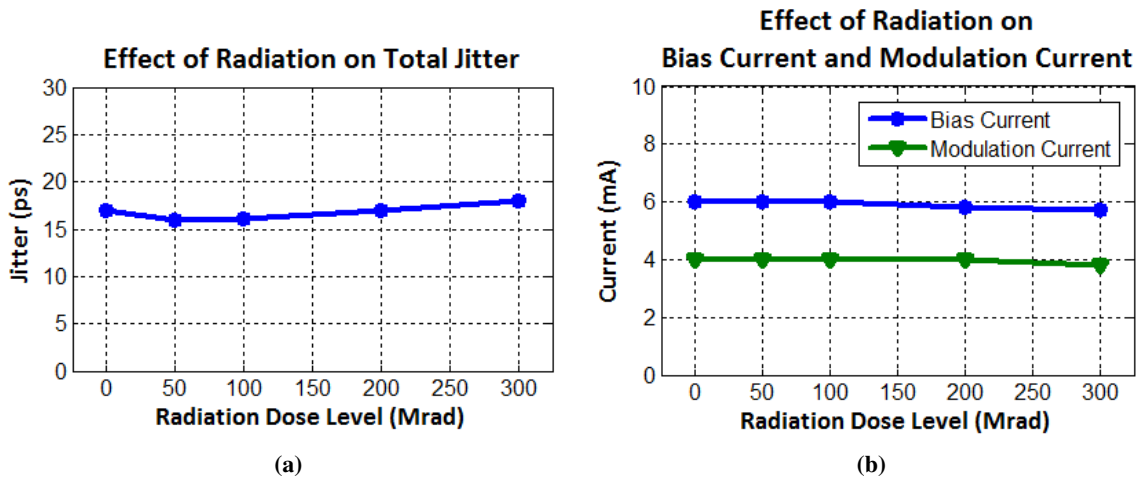
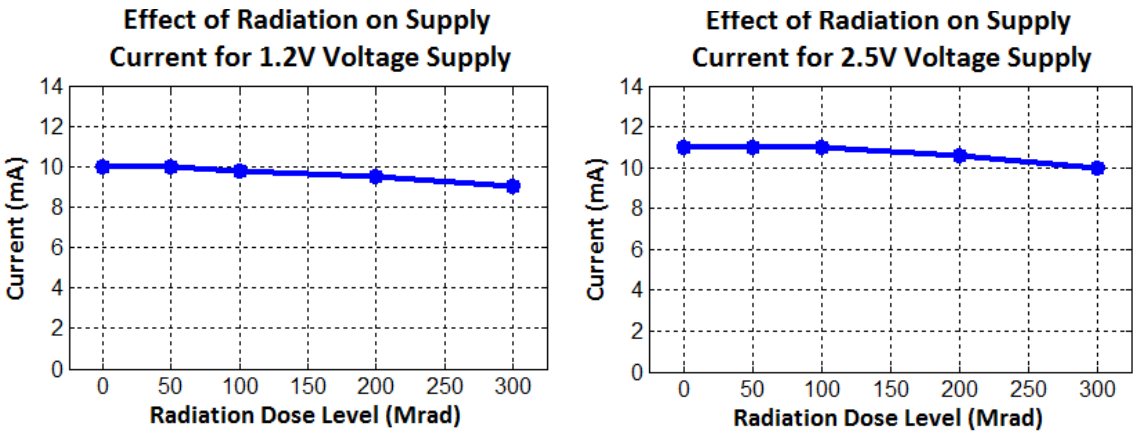


Figure 12. (a) Plot of total jitter vs. radiation dose, (b) plot of bias/modulation current vs. radiation dose.



(a) **(b)**

Figure 13. (a) 1.2V supply current vs. radiation dose, (b) 2.5V supply current vs. radiation dose.

Summary. A 4 × 10 Gb/s low-power VCSEL driver array (LDQ10) has been designed and implemented using a 65-nm CMOS technology. Various design techniques have been employed to increase the driver bandwidth, minimize the power consumption, make the silicon area compact, and minimize the cross talk among the channels. Edge pre-emphasis is also employed in the design to allow for bandwidth enhancement at the rising and/or falling edges of the data transitions. The LDQ10 occupies a silicon area of 1.7 mm × 1.9 mm with a pitch of 250 um between each adjacent channel, allowing the LDQ10 to be directly wire-bonded to a quad-VCSEL array. It consumes 130 mW when all channels are turned on under typical setting. Each channel can be individually turned on and off for further power saving. Extensive measurement results of the LDQ10 with VCSEL devices demonstrate good jitter performance at 10 Gb/s, negligible crosstalk effects, and tolerance to total ionization dose up to 300 Mrad.

Acknowledgments

The authors would like to thank DoE for the funding of project and acknowledge Francois Vasey, Jan Troska, Csaba Soos, Lauri Juhani Olantera, and David Porret at CERN for their valuable help in LDQ10 measurement setup and insightful discussions.

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