SPACIROC: A Front-End Readout ASIC for Spatial Cosmic Ray Observatory

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Abstract: The SPACIROC ASIC is designed for the JEM-EUSO fluorescence imaging telescope onboard of the International Space Station. Its goal is the detection of Giant Air Showers above a few 10^{19} eV, developing at a distance of about 400 km, downward in the troposphere. From such distance, most of the time, the number of the photons expected in the pixels is very weak, ranging from a few units to a few tens. For such running conditions, we propose a low-power, rad-hard ASIC which is intended for reading out a 64-channel Multi-Anode Photomultiplier. The two main features of this ASIC are the photon counting mode for each input and the charge-to-time (Q-to-T) conversions for the multiplexed channels. In the photon counting mode, the 100% triggering efficiency is achieved for 50fC input charges. For the Q-to-T converter, the ASIC requires a minimum input of 2pC. Moreover SPACIROC is required to have a low power dissipation which is around 1mW/channel. We will describe in details the architecture of this ASIC and how the required specifications are satisfied. SPACIROC is a result of the collaboration between OMEGA/LAL-Orsay, France, RIKEN, ISAS/JAXA and Konan University, Japan on behalf of the JEM-EUSO consortium.

Keywords: Front-End, ASIC, Low-power, DAQ

1 Introduction

The primary purpose of JEM-EUSO [1] mission is the detection of the Extensive Air Showers (EAS) created by the Extreme Energy Cosmic Rays (EECR $>10^{19}$ eV), inside the atmosphere. JEM-EUSO, which is a fluorescence telescope, looking downward, that should be installed on the JEM module of the International Space Station, will detect the fluorescent photons released by the EAS. By observing these phenomena from the upper side of the atmosphere, this telescope will be able to identify the EECR.

SPACIROC (Spatial Photomultiplier Array Counting and Integrating Readout Chip) was designed according to the requirements from the JEM-EUSO consortium. Multi-anode photomultipliers (MAPMT) are proposed to be the sensitive device of the JEM-EUSO observatory focal surface. SPACIROC [2] was designed to accommodate the readout of these MAPMTs. As JEM-EUSO is intended to track the fluorescent light, this ASIC is required to count the number of photons reaching each pixel of the MAPMTs. The secondary mission of SPACIROC is to measure the intensity of photon flux by performing charge to time (Q-to-T) conversion. The layout of SPACIROC is shown in figure 1. The final dimensions are 4.6 mm x 4.1 mm (19mm²) and it was submitted to the foundry in March 2010. The chip was developed using the 0.35µm SiGe process from AMS.

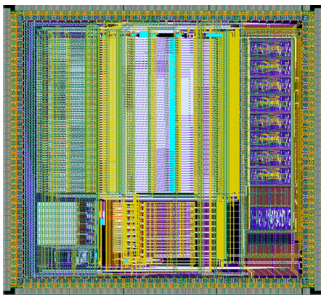

Figure 1 : SPACIROC layout

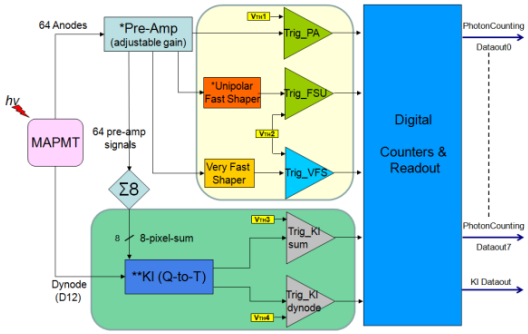

Figure 2: SPACIROC general architecture.

2 The ASIC

SPACIROC offers 64 inputs dedicated to the anodes of one MAPMT and 1 input for the last dynode. For the following, the MAPMT gain is assumed to be 10^6 in order to have 1 photoelectron (1 p.e.) around 160 fC.

2.1 Specifications

The specifications for the chip are the following:

- 64 channels preamplifier with independent gain (8-bit) adjustment.
- Photon Counting : 64 channels.
- Q-to-T converter : 1 channel for last dynode + 8 internal channels (multiplexed inputs).
- 100% trigger efficiency for charge greater than 50 fC (~1/3 p.e.).
- Q-to-T converter input range: 2 pC – 400 pC (12.5 p.e – 2500 p.e.).
- Power consumption : 1 mW/channel.
- 9 data serial outputs.

This circuit was designed for low-power spaceflight applications. SPACIROC is also radiation hardened by design against Single Event Latchup (SEL) and Single Event Upset (SEU).

2.2 Architecture

The general architecture of SPACIROC could be divided into 3 main blocks: the Photon Counting, the Q-to-T converter (called KI) and the digital part. The Photon Counting and KI are the analog section of this ASIC. The digital part of SPACIROC is used to count photon triggered pulses and to measure the photon intensity. The readout management are also implemented in the digital part. The architecture of SPACIROC is represented in figure 2. However figure 2 doesn't include the auxiliary components of the ASIC such as the bandgap reference, DACs and signals monitoring.

The 64 signals from MAPMT anodes are fed through the preamplifiers which offer adjustable gain to correct the gain non-uniformity of the MAMPT. The preamplified signals are fed to the Photon Counting and KI in order to transform these signals into discriminator pulses. These discriminator pulses will be made available at the inputs of the digital part for counting and measuring. Each mentioned block will be described in the following sections. The use of the word "trigger(s)" in the next sections will refer to the Photon triggered pulses on the outputs of the analog part.

3 Analog Design

3.1 Photon Counting

The 64-channel Photon Counting block is required to discriminate the preamplifier signal into trigger pulses. This operation is done in parallel for each channel. For this prototype, the ASIC offers three different discriminator outputs (Trig_PA,Trig_FSU and Trig_VFS) for each channel. The reason of having three different discriminators is to verify the performances of each triggering scheme under laboratory tests before choosing the design which represents the best trade-off between noise, speed and power consumption. Figure 3 shows the block diagram of the Photon Counting analog part.

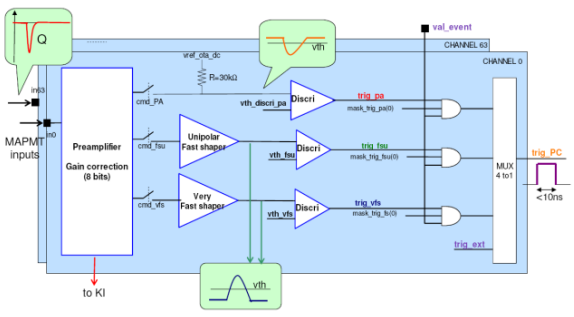

Figure 3: Photon Counting Architecture

The output for the first trigger design, which is called Trig_PA, is obtained from the preamplifier signal which is fed directly into a discriminator. Due to its simple architecture (a preamplifier and a discriminator), this design has the lowest power consumptions compared to the other trigger designs in the Photon Counting part. Estimated power consumption of Trig_PA analog part is 0.36mW/channel.

For the next two trigger designs (Trig_FSU and Trig_VFS), the preamplifier signal is fed to shapers before reaching the discriminators. The shapers will add more gain to the preamplifier signal. As for the second trigger design, Trig_FSU, a low-noise with adjustable-gain shaper called FSU from MAROC3 [3] chip is used. The output pulse of the Trig_FSU is obtained by comparing the FSU signal to a fixed threshold. The power dissipation for Trig_FSU is estimated at 0.56mW/channel.

For the last trigger design, Trig_VFS, a shaper is also used here. The shaper, which is known as VFS, has a larger gain and a faster shaping time compared to the FSU shaper. The output signal this design is obtained by discriminating the VFS signal. The power consumption for Trig_VFS is around 0.54mW/channel.

These three discriminator outputs are sent to the digital block via a 4-to-1 analog multiplexer. The fourth input of the multiplexer is for the external trigger signal which is used to test the digital block independently. Two 10-bit DACs are used in this block. One DAC is shared between Trig_FSU and Trig_VFS trigger designs as both designs will discriminate signals that have the same polarity and baseline. The other DAC is used for setting threshold in the Trig_PA trigger design because of the inverted polarity of the preamplifier signal at the discriminator input. Each trigger output could be masked independently as only one trigger could be used at one time.

3.2 KI

Another important feature of this ASIC is the ability to perform the Charge to Time (Q-to-T) conversion by measuring the signal duration over a fixed threshold. Q-to-T conversion is done by the 9-channel KI block. The first 8 inputs of the KI converters receive the pre-amplified signals of the MAPMT anodes. The pre-amplified signals are reorganised into the sum of every 8 neighbouring channels or pixels; hence the given name of 8-pixel-sum for this part. However, the 9th input of KI takes a signal coming directly from the dynode of the MAPMT. The gathered data on the dynode could be used for the MAPMT protection strategy (gain reduction against high photon flux) in the JEM-EUSO experiment. Figure 4 shows the general architecture of this converter.

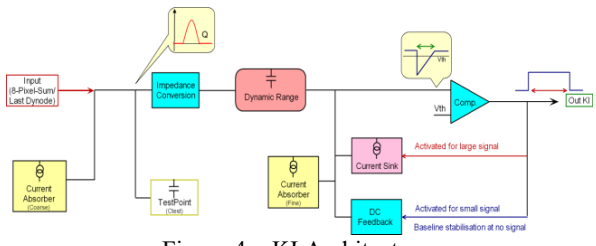

Figure 4 : KI Architecture

An impedance converter (Impedance Conversion) and a capacitive network (Dynamic Range) are used to transform the input current pulse into a voltage signal. The Impedance Conversion circuit will convert the low impedance input (~50Ω) of the KI part into higher impedance. The Dynamic Range circuit is used to scale the input dynamic range. The scaling is done via the ASIC configuration parameters in order to obtain the appropriate capacitance value for integrating the input signal. If the input signal is strong enough, it will produce a discriminator output, which in turn will deactivate the DC Feedback baseline and activate a variable gain current source (Current Sink). Once the current source takes over, the integrated signal length can be adjusted according to the selected current value. The 9-channel discriminator outputs can be masked individually or all at once. It is also possible to use external inputs for testing the digital part independently. This converter was designed in collaboration with RIKEN, Japan. The design is based on their KI02/03[4] chip.

3.3 Simulation results

The analog part of Photon Counting and KI were fully simulated. Figure 5 shows the simulations for the Photon Counting block. The injected charge are 1/3 p.e, 1 p.e and 10 p.e. The simulations results indicate that Photon Counting block could achieve 100% trigger efficiency starting from 1/3 p.e.

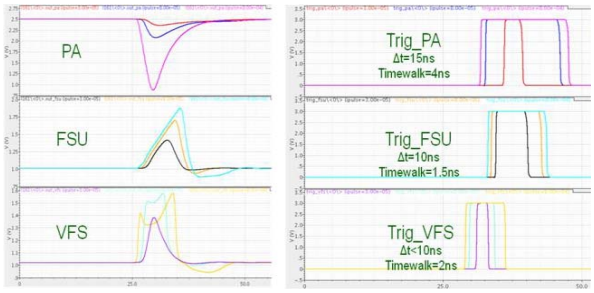

Figure 5 : Photon Counting simulations

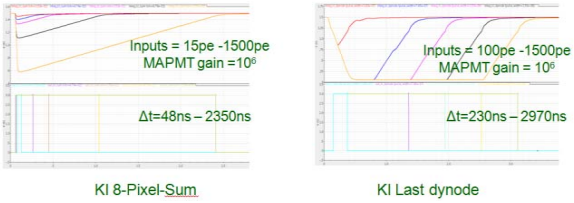

Figure 6 : KI simulations

The Figure 6 shows the simulations results of the KI block for the summed channels and the MAPMT dynode pulses. For the simulations, charges ranging from 15p.e. to 1500p.e. are injected into input of KI last dynode and 100p.e. – 1500p.e. are injected into the KI 8-pixel-sum inputs. The expected trigger widths could vary up to 2970 ns.

4 Digital Design

All the data acquisition and readout are done within a defined time slot which is call Gate Time Unit (GTU=2.5μs). This means that during every cycle of

GTU, the present data are acquired and the previously recorded data are sent out on the serial links.

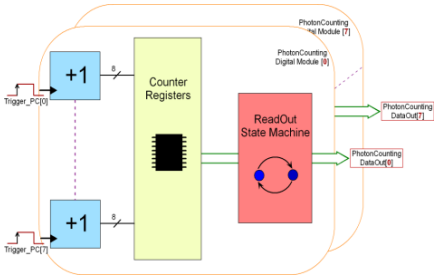

Figure 7 : Photon Counting digital

For the Photon Counting (figure 7), the digital part is organised into 8 identical modules. Each module will handle 8 triggers from Photon Counting analog part. The discriminator output's rising edge is used to clock an 8-bit counter which could operate up to 100 MHz. Each Photon Counting digital module will have 64-bit counters data and these data are transmitted on a serial data link. To summarise, 8 Photon Counting digital modules are required to manage 64 channels of Photon Counting and 8 serial links are used to send the counter data simultaneously.

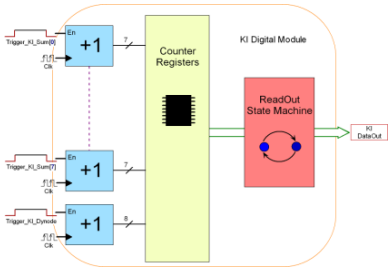

Figure 8 : KI digital

The digital part for the KI (figure 8) has the same architecture as the digital part for Photon Counting. However it has some minor differences for certain components. As the KI part has 9 channels, only one digital module is used. The KI discriminator outputs are sampled by the digital block system clock. The readout management program has been written differently so that it could accommodate a bigger channel number.

The digital part of SPACIROC was designed carefully in order to minimize area usage, to reduce power consumption and to increase the robustness of the system. Flip-flops in critical areas are implemented in Triple Modular Redundancy (TMR) configuration in order to mitigate the effects of SEU.

5 Measurements

The ASIC was received in October 2010 and extensive tests have been carried out. A test board (figure 9) and a Labview interface have been developed for testing SPACIROC.

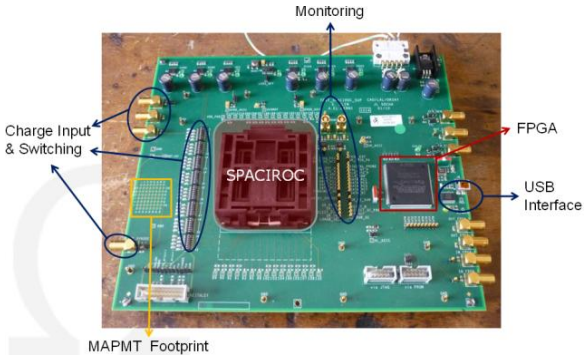

Figure 9 : SPACIROC test board

Test results have shown that the ASIC is working quite well and exhibits expected behaviours. Nearly all the important features are available and SPACIROC is capable of sending out data of Photon Counting and KI charge measurements.

6 Conclusions

To conclude, SPACIROC ASIC has been proven to work and exhibits good behaviour. Extensive tests are being carried out in order to characterise the chip completely. Current test results have shown that SPACIROC could achieve 30 ns double pulse separation and measuring input charges up to 1000 p.e. The measured power consumption under typical operating condition is around 1.1mW/channel. Further work on improving the chip is currently underway so that it could be ready for mass production.

References

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