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Weighting Mean Timers for High Energy Physics Electronics

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Weighting Mean Timers for High Energy Physics Electronics

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Abstract

A new family of electronics circuits, weighting mean timer, is presented in this technical memo. Weighting mean timers can be used in high energy physics experiment electronics to implement the "concurrence" condition in hardware trigger stage. Several possible architectures of weighting mean timers have been discussed.

1 Introduction

Weighting mean timer (WMT) is a new family of electronics circuits generating weighted mean time. Using weighting mean timers makes it possible to bring "concurrence", an essential event selection condition for nearly all high energy physics experiments, from data analysis stage to hardware trigger stage. This will significantly enhance the ability of the particle/nuclear physics experiment detectors.

1.1 Concurrence Condition

Concurrence condition requires that all tracks, hits in the detector are "in time" ones before further process. This is a necessary condition for the hits to come from the same event which is the basis of correct data interpretation. Concurrence condition is normally applied in data analysis stage today due to difficulties of algorithm implementation in hardware.

To search rare particle physics phenomena, experimentalists use high luminosity beams enabled by the modern accelerator technologies. In the high luminosity experiments the total event rate is so high that the probability of event overlapping is much greater than that in low luminosity experiments. To minimize system dead time and hence to use the high luminosity beam efficiently, fast hardware electronics devices are needed to implement the concurrence trigger condition.

1.2 Weighting Mean Timers for Concurrence Condition

Joining various attempts of hardware concurrence implementation[1, 2, 3], the development of WMT starts from a unique angle of arrival time manipulations with no cutting-edge technical difficulties in electronics. This makes it easier to build and test the WMT and eventually, to design multi-channel products with WMTs or to integrate WMTs in ASICs (application-specific-integrated-circuits).

The weighted mean time generated by WMT is a linear combination of two input times. Assume that the arrival times of the input signals are T_1 and T_2, respectively, then the time of a WMT output is:

$$T_a = \frac{(K_1 T_1 + K_2 T_2)}{(K_1 + K_2)} + T_d \tag{1}$$

where K_1 and K_2 are weight factors and T_d is a constant delay which is independent of T_1 and T_2. K_1 and K_2 are unequal in general, they may even have opposite signs.

2 Background: Demands in the Experiments

In any event selection condition where a linear combination of signal arrival times is required, one can use weighting mean timers to implement the hardware trigger. The linear combination normally represents an absolute time which could be event time or hit time with unknown variables such as particle speed or drift speed canceled. We will discuss a few examples here.

2.1 In Time Hits of Drift Chambers

The maximum drift time in drift chambers is normally several times larger than the beam crossing or beam bucket period in experiment systems. The signals seen at the chamber wires were created by the hits long and unknown time ago. It is very useful for a trigger system to find the real hit time. The "BANANA" module developed by University of Colorado for KTeV experiments at Fermilab is a device finding the in time hits[3].

To find the hit time on a chamber, at least two signals are required. If three or more signals from a hit are available, one may find a better result of the hit time by implementing appropriate linear combination.

Fig. 1(a) shows an example of using weighting mean timer to find in time hits on a two layer straw tube chamber.

Assume T_1 and T_2 are leading edge times of the signals from the tubes, then the

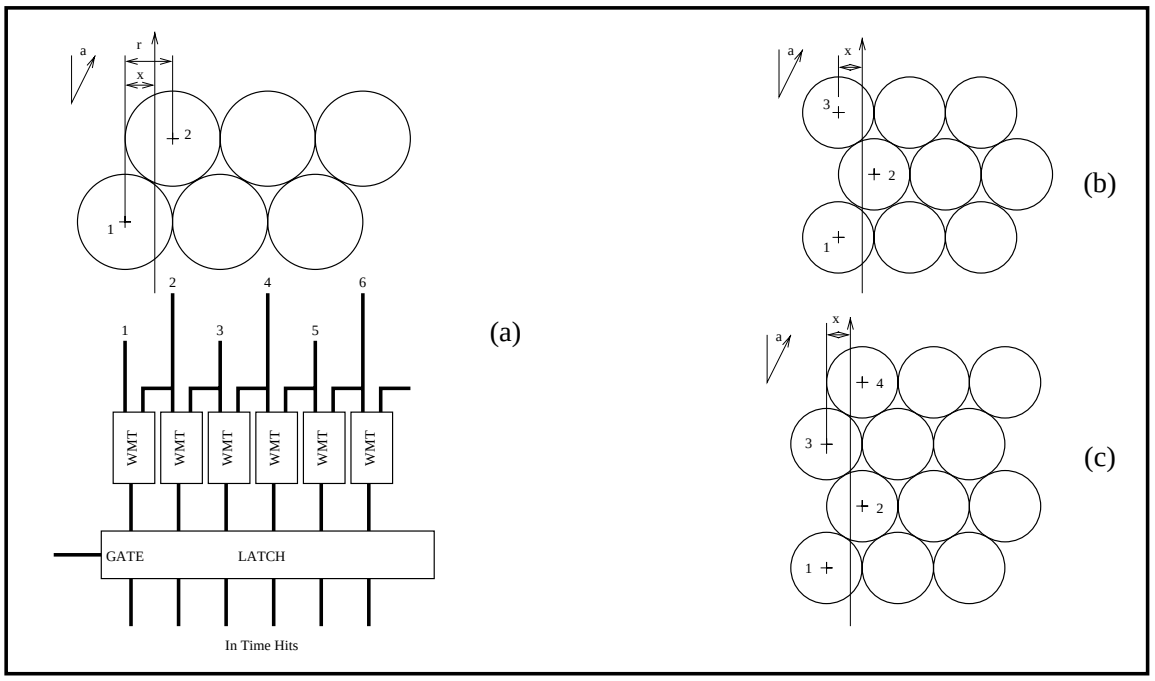

Figure 1: Weighting Mean Timers Used for "In Time Hits" in Drift Chamber System

hit time T_0 and the linear combination of T_1 and T_2 have the following relation:

$$\frac{T_1 + T_2}{2} = T_0 + \frac{r}{2v}\cos a + \frac{\sqrt{3}r}{2v}\sin a \tag{2}$$

where r is the radius of the chamber tube, v is the drift speed and a is the particle incident angle as shown in Fig. 1(a). The dependence on the transverse distance x is eliminated in Eq. (2) but the angular dependence is not. In fact, there is no enough information from the two arrival times to cancel it. The last term of Eq. (2) is the dominant part of the error. A 10° deviation in incident direction will generate an error about 15% of (r/v) in T_0

For the applications in which the deviation of a is small, one can extract the hit time by adding a weighting mean timer to each pair of the chamber signal. The outputs of the WMTs will be aligned according to the hit time. With a common gate, the in time hits can be latched for further trigger process.

The Eq. (2) has the same weight factors. If the non-linear drift speed is considered, one may use different weight factors to form piecewise fit.

The three layer straw tube configuration shown in Fig. 1(b) has enough information for all unknowns T_0, x and a in theory. A linear combination of three arrival times T_1, T_2 and T_3 will eliminate the transverse distance dependence and the dominant portion of the angular dependence:

$$\frac{T_2}{2} + \frac{T_1 + T_3}{4} = T_0 + \frac{r}{2v}\cos a \tag{3}$$

Although the dependence of a is not completely canceled (that requires non-linear operations), the error caused by the last term of Eq. (3) is small. A 10° deviation in incident direction will generate an error only 0.8% of (r/v) in T_0

The four layer straw tube configuration shown in Fig. 1(c) provides redundant information for extra check. But it may be too complicate for hardware trigger system. The linear combination providing hit time information is:

$$\frac{T_1 + T_4}{8} + \frac{3(T_2 + T_3)}{8} = T_0 + \frac{r}{2v}\cos a \tag{4}$$

which has the same angular dependence as Eq. (3).

2.2 In Time Hits in a Track

In an experiment set up shown in Fig. 2(a), a three-way coincidence of three hodoscopes, H_1 H_2 and H_3, identifies a particle track.

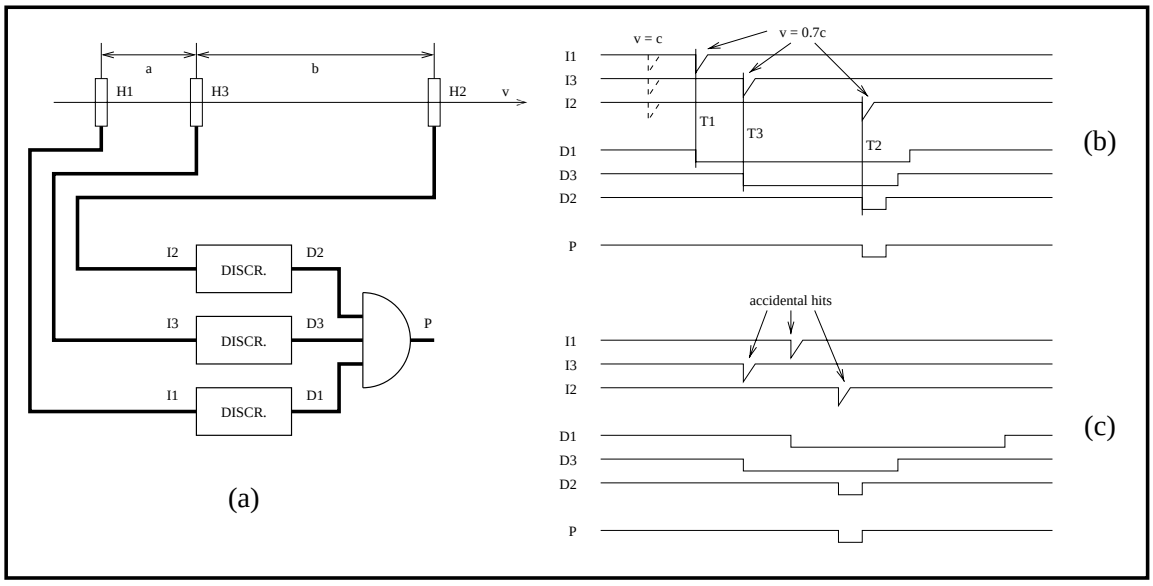

Figure 2: A Three-Way Coincidence Set Up Causing False Trigger

It is not a problem if the particles are all very high energy ones so that their speeds are very close to the speed of light c. Simply choose the cable linking the detectors to the discriminators so that the signals from H_1 H_2 and H_3 are lined up together as the dash line shown in Fig. 2(b).

However, if the energy of the particle is not so high, then its speed may be far from c. For example the speed of an $1GeV$ proton is only $0.7c$. To cover the low speed particles, one has to adjust the discriminator unit to output very wide pulses as shown in Fig. 2(b).

This will likely to cause false trigger in the high luminosity experiments. Consider an example shown in Fig. 2(c) which could be generated by the accidental hits of a slow particle in a beam bucket and a fast particle in next bucket. None of the particles satisfies the trigger condition, but a false trigger is generated due to large pulse width of the discriminator outputs.

One may solve this problem by using a weighting mean timer. Fig. 3(a) shows the connections.

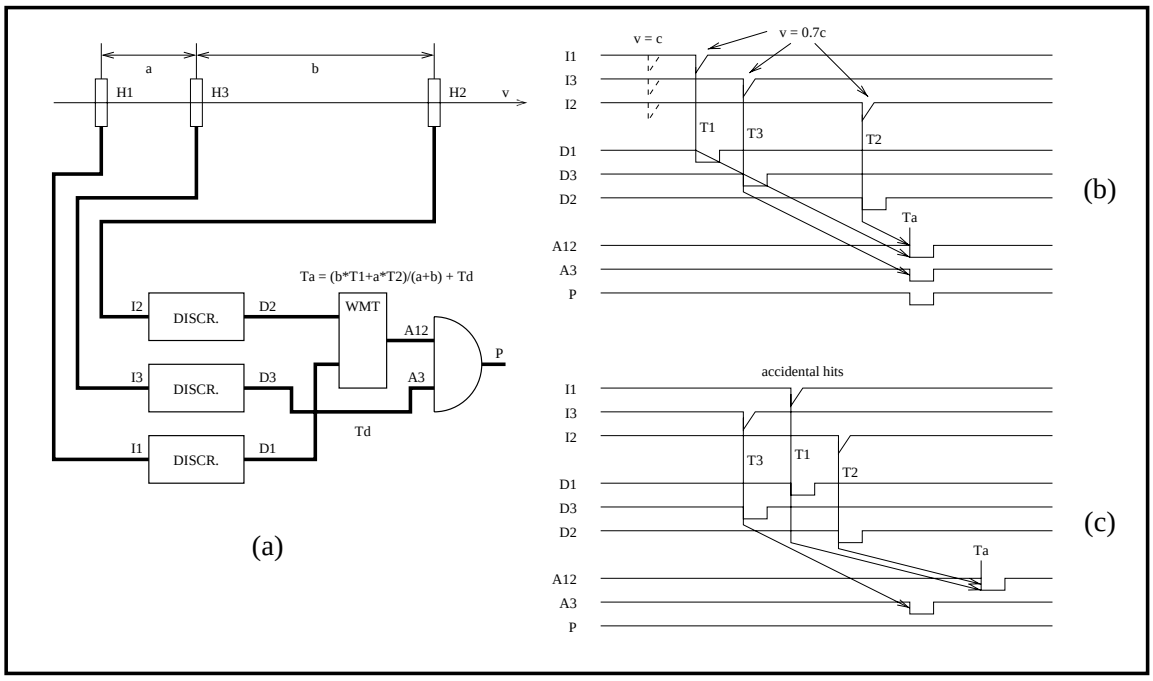

Figure 3: An Example of Weighting Mean Time Application Rejecting "Out of Time" Hits

The outputs of the discriminators can be adjusted to the minimum width. The output time of the WMT is:

$$T_a = \frac{(bT_1 + aT_2)}{(a+b)} + T_d \tag{5}$$

after the weight factors are appropriately chosen. The output of WMT, A_{12} and the delayed version of the discriminator, A_3 form a coincidence as shown in Fig. 3(b). The WMT keeps A_{12} aligned with A_3 for all particle speed v within a broad range even the width of A_3 is small.

This provides an "out of time" hit rejection which is not otherwise available in hardware. Fig. 3(c) represents the same hit set as in Fig. 2(c). The circuit correctly rejected the hit set which will generate false trigger in the old three-way coincident trigger circuit.

2.3 Starting Time of Tracks

Consider a simple experiment apparatus as shown in Fig. 4(a). A target or beam colliding point is at O and two hodoscopes, H_1 and H_2 are at x_1 and x_2, respectively. Assume a particle flies out of O at time T_0 with speed v and hits H_1 at T_1 and H_2 at T_2, then the arrival times have dependence on the unknown particle speed.

As an example, the time of flight over a distance of $20m$ may vary from $66ns$ to $95ns$ when the speed of the particle varies from 1 to 0.7 times of speed of light. This difference may be larger than the period of beam crossing or beam bucket.

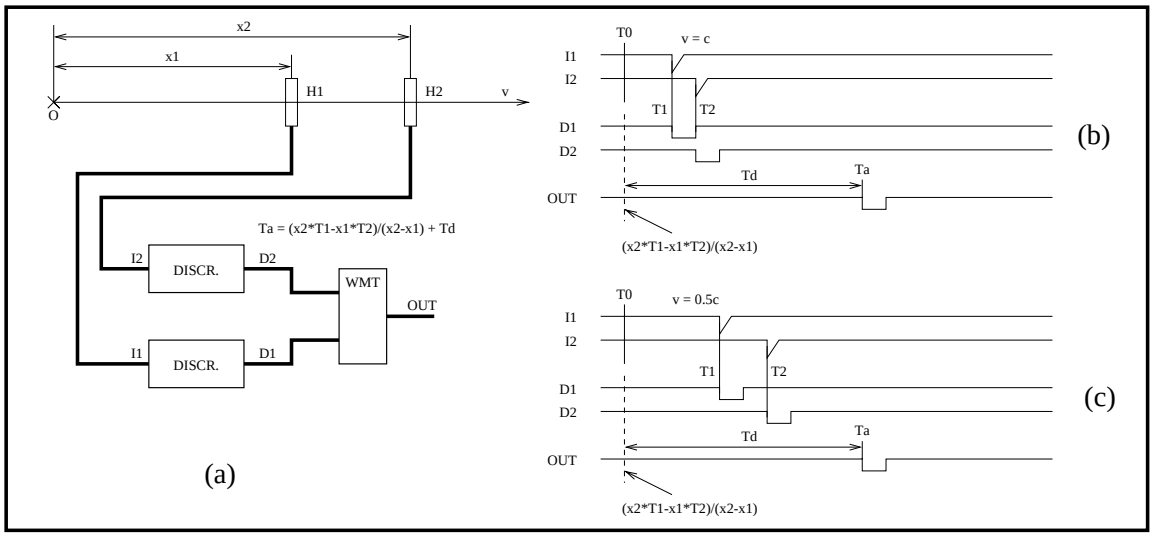

Figure 4: Weighting Mean Timers Used for Finding Event Time

To find the event time, we first write down:

$$\begin{aligned} T_1 &= T_0 + \frac{x_1}{v} \\ T_2 &= T_0 + \frac{x_2}{v} \end{aligned} \tag{6}$$

A linear combination of T_1 and T_2 will cancel the dependence on the particle speed:

$$\frac{x_2 T_1 - x_1 T_2}{x_2 - x_1} = T_0 \tag{7}$$

Note that the coefficients have different signs.

The linear combination can be implemented by using a weighting mean timer. With the weight factors chosen appropriately, the output time of the WMT is simply the event time plus a constant delay.

Fig. 4(b) shows signals created by a fast particle and Fig. 4(c) shows the ones for a slow particle. Although T_1 and T_2 sweep in a large range, the output time T_a is alway T_d after the event time T_0.

3 Technical Approach: Architectures of Weighting Mean Timers

In this section, we will discuss some circuits of the weighting mean timers.

3.1 Charge Sum Architectures of Weighting Mean Timers

The architecture presented in this section (see Fig. 5) employs a capacitor to store electric charge coming from current sources. The voltage change on the capacitor is detected by a comparator and the comparator changes the output logic level when the voltage change of the capacitor passes a threshold voltage.

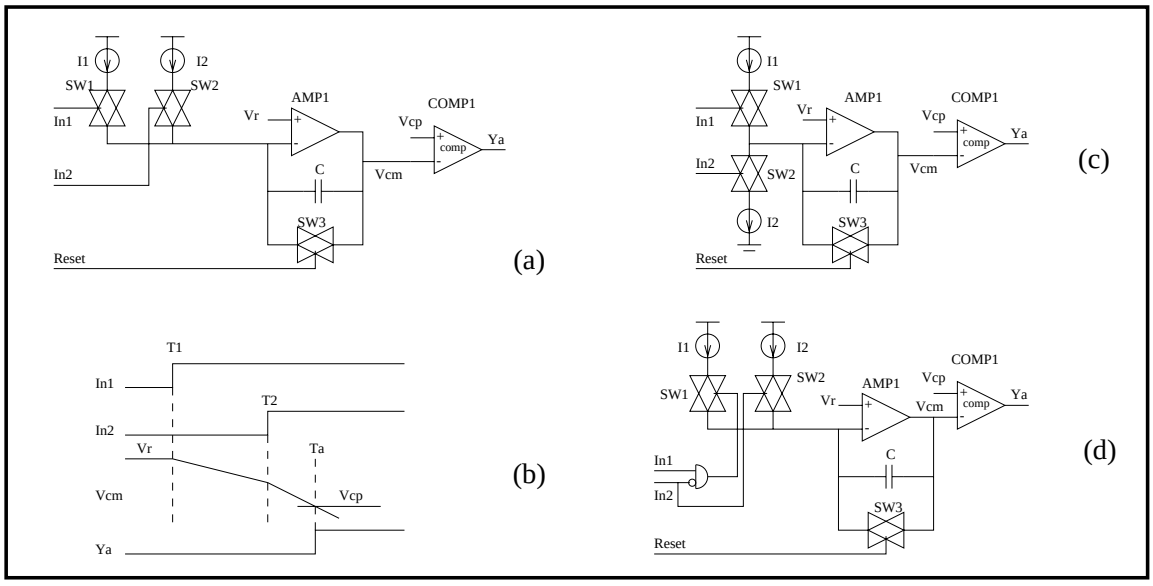

Figure 5: Charge Sum Architectures of Weighting Mean Timer: (a) Typical Circuit. (b) Timing Diagram. (c) A Circuit with a Negative Weighting Factor. (d) A Circuit with both Positive and Negative Weight Factors and Uses Single Type of Current Sources.

Now we will discuss the circuit of Fig. 5(a) for detail. The amplifier AMP1 and the capacitor C are used as an integrator. The circuit works after a reset pulse and switch SW3 brings the both ends of the capacitor to the same voltage. After reset, the output voltage of AMP1, $V_{cm} = V_r$. The threshold voltage V_{cp} of the comparator COMP1 is set to be lower than V_r. So the output of COMP1, Y_a is at "0" logic level. When In_1 goes active at time T_1, the current switch SW1 turns on and capacitor C is charged at current I_1. At T_2, In_2 goes active and C is charged at current $I_1 + I_2$. During charging process, V_{cm} goes lower and lower. When $V_{cm} = V_{cp}$, Y_a flips from low to high and this time, T_a is defined as the output time of the weighting mean timer (see Fig. 5(b)). The total charge on the capacitor C during this process is:

$$C(V_r - V_{cp}) = (T_a - T_1)I_1 + (T_a - T_2)I_2 \tag{8}$$

Therefore:

$$T_a = \frac{I_1T_1 + I_2T_2}{I_1 + I_2} + \frac{C(V_r - V_{cp})}{I_1 + I_2} \tag{9}$$

So, T_a is a weighted mean time of T_1 and T_2 with weight factor $K_1 = I_1/(I_1 + I_2)$ and $K_2 = I_2/(I_1 + I_2)$. Both K_1 and K_2 are positive. The delay of the mean timer, T_d is the last term of the Eq. (9).

The weight factors of circuit of Fig. 5(c) have different signs. The total charge in C for this circuit is:

$$C(V_r - V_{cp}) = (T_a - T_1)I_1 - (T_a - T_2)I_2 \tag{10}$$

When $I_1 > I_2$, the output time of the mean timer is:

$$T_a = \frac{I_1T_1 - I_2T_2}{I_1 - I_2} + \frac{C(V_r - V_{cp})}{I_1 - I_2} \tag{11}$$

In this case, $K_1 = I_1/(I_1 - I_2) > 0$ and $K_2 = -I_2/(I_1 - I_2) < 0$.

The circuit in Fig. 5(c) can also operate in another mode, in which: $I_2 > I_1$ and V_{cp} is set $= V_r$. After In_1 becomes active at T_1, V_{cm} goes lower than V_r and Y_a is "1". However, after T_2, V_{cm} goes backward since $I_2 > I_1$. When V_{cm} goes back to V_r (which $= V_{cp}$), Y_a turns to "0" and this falling edge defines T_a. For this mode, the capacitor C is charged first and then discharged and the final total charge on C is 0:

$$0 = (T_a - T_1)I_1 - (T_a - T_2)I_2 \tag{12}$$

One may find the output time of the mean timer is:

$$T_a = \frac{-I_1T_1 + I_2T_2}{I_2 - I_1} \tag{13}$$

The weight factors, $K_1 = -I_1/(I_2 - I_1) < 0$ and $K_2 = I_2/(I_2 - I_1) > 0$.

The advantage of this mode is that the output time T_a does not depend on any voltage setting. This may improve the stability of the operation. However, the output of the comparator Y_a may be undefined after reset since the both inputs of

the comparator is at the same voltage. So some additional logic may be required to regulate the logic level.

If a weighting mean timer is required to be able to operate at both same sign and different sign modes for the weight factors, Fig. 5(d) is a circuit for this requirement. The current switch SW1 opens only during T_1 to T_2. The total charge then can be written:

$$C(V_r - V_{cp}) = (T_2 - T_1)I_1 + (T_a - T_2)I_2 \tag{14}$$

Therefore:

$$T_a = \frac{I_1 T_1 + (I_2 - I_1)T_2}{I_2} + \frac{C(V_r - V_{cp})}{I_2} \tag{15}$$

By adjusting I_1 and I_2, one may obtain either $K_2 > 0$ or $K_2 < 0$.

The charge sum scheme allows a design of WMT with more than two inputs. In other words, a WMT with N inputs can be designed so that the output time:

$$T_a = k_1 T_1 + k_2 T_2 + ... + k_N T_N \tag{16}$$

where T_1 to T_N are the input times and k_1 to k_N are weight factors. It is true that:

$$k_1 + k_2 + ... + k_N = 1 \tag{17}$$

A WMT with 3 or 4 inputs is an ideal device for the drift chamber trigger with 3 or 4 signal wire layers.

3.2 Digital Delay Line Architectures of Weighting Mean Timers

Delay lines have long history being employed in mean timers[1, 2]. In this section, WMTs using controlled digital delay lines will be discussed. (see Fig. 6)

Fig. 6(a) shows a circuit of weighting mean timer with positive weight factors. The input signals In_1 and In_2 are sent through two delay lines whose delay per tap is t_1 and t_2, respectively. Assume that the delay lines have M sections and the leading edges meet at the i-th tap, and the output Y_a is generated at time T_a, then T_a can be written:

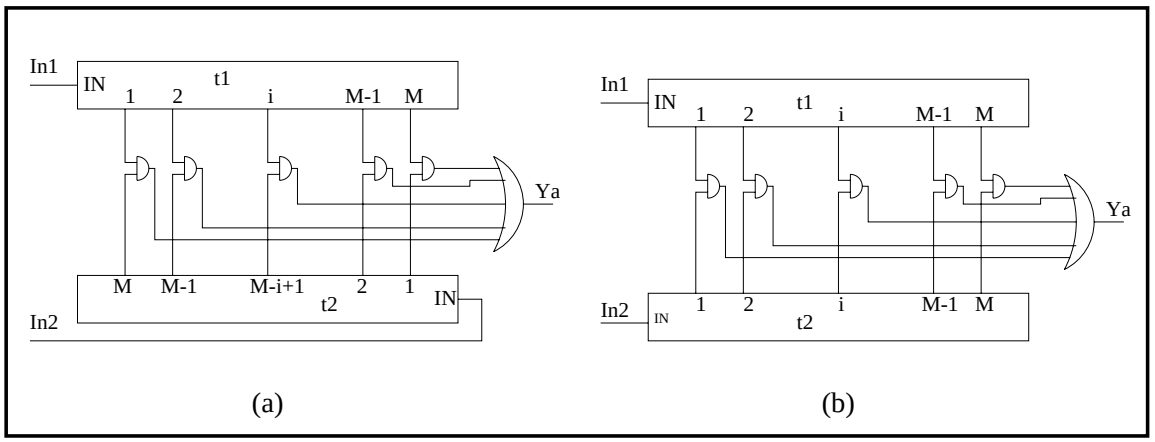

Figure 6: Digital Delay Line Architectures of Weighting Mean Timer: (a) WMT with Both Positive Weight Factors. (b) WMT with a Negative Weight Factor.

$$\begin{aligned} T_a &= T_1 + i\ t_1 \\ T_a &= T_2 + (M - i + 1)t_2 \end{aligned} \tag{18}$$

Eliminate the dependence on i, one has:

$$T_a = \frac{t_2 T_1 + t_1 T_2}{t_1 + t_2} + \frac{t_1 t_2 (M+1)}{t_1 + t_2} \tag{19}$$

It can be seen that the weight factors $K_1 = t_2/(t_1 + t_2)$ and $K2 = t_1/(t_1 + t_2)$. If the two delay lines are identical, then the weight factors both become 1/2. This is the case of "normal" mean timer.

The circuit in Fig. 6(b) shows a weighting mean timer with a negative weight factor. The input signals propagate in the two delay lines at the same direction. Consider the $t_1 > t_2$, i.e., signals propagate faster in the second delay line than in the first one. The leading edge of In_2 starts later than the one of In_1. When the leading edge of In_2 catches the one of In_1, one may write:

$$\begin{aligned} T_a &= T_1 + i\ t_1 \\ T_a &= T_2 + i\ t_2 \end{aligned} \tag{20}$$

After eliminating i, one has:

$$T_a = \frac{-t_2 T_1 + t_1 T_2}{t_1 - t_2} \tag{21}$$

From Eq. (21), one can see that the weight factors of this mean timer have different signs.

3.3 Counter Architectures of Weighting Mean Timers

In this section, we will discuss weighting mean timers based on a counter and a switchable oscillator. The block diagram is shown in Fig. 7.

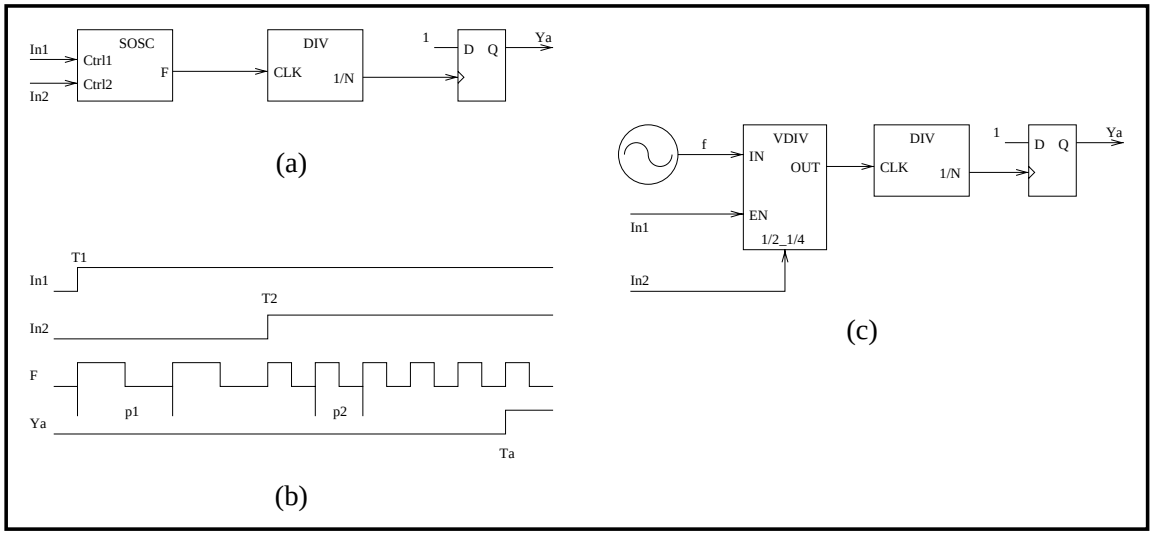

Figure 7: Counter Architectures of Weighting Mean Timer: (a) Typical Block Diagram. (b) Timing Diagram. (c) Block Diagram for 1/2 Weight Factors.

The switchable oscillator SOSC in Fig. 7(a) has two control inputs. When In_1 becomes active at T_1, the SOSC outputs clock signal at frequency $1/p_1$ (p_1 is the period of the oscillation). The divider counts the clock cycles. After In_2 becomes active at T_2, the period of the output of SOSC changes to p_2. The divider continues counting at the new rate until the total number of cycles is N, the divider then outputs a leading edge which turns Y_a on. The N of the divider is normally chosen to be integer power of 2, such as 16, 32, 64 etc. The divider does not have to be synchronize devices, but rather, low cost asynchronize schemes with high speed devices at early stage can be used in this design. One may also choose a high frequency commercial pre-scaler as the divider.

Now we will discuss the principle of the operation. The counter counts at a rate of $1/p_1$ from T_1 to T_2, and at a different rate of $1/p_2$ from T_2 to T_a. The total number of counts is N (see Fig. 7(b)). Therefore, approximately:

$$\frac{T_2 - T_1}{p_1} + \frac{T_a - T_2}{p_2} = N \tag{22}$$

One may find T_a from the above:

$$T_a = (\frac{p_2}{p_1})T_1 + (1 - \frac{p_2}{p_1})T_2 + p_2\ N \tag{23}$$

This is a weighted mean time with weight factors $K_1 = p_2/p_1$ and $K_2 = (1-p_2/p_1)$. When $p_2 < p_1$, both K_1 and K_2 are positive, while when $p_2 > p_1$, K_2 becomes negative.

The advantage of this architecture is that N can be very large. In fact, increasing of a flip-flop will double the counting range. Therefore, this is an economical scheme when the mean timer is required to operate over a large timing range.

For a "normal" mean timer with $K_1 = K_2$, one chooses $p_2 = p_1/2$. In this particular case, one may use the design shown in Fig. 7(c). The variable divider VDIV can be implemented using two J-K flip-flops. When In_1 is active, the VDIV is enabled and the output frequency is the input frequency divided by 4. After In_2 goes active, the dividing factor of VDIV becomes 2. This circuit is suitable for the applications such as finding "in time" hits of drift chambers. The weight factors are precisely 1/2 due to the digital structure of the circuit. An oscillator with high stability may be used in this circuit to improve the performance.

4 Summary

In high energy physics experiments, weighting mean timers can be used in trigger systems with chamber signals as trigger sources. Another type of applications is finding event time or hit time in the systems with signals generated by slow particles.

The weighting mean timers based on charge sum principle should have good time resolution and relatively long total delay. However, careful analog circuit design is required. The delay line scheme has much less analog circuits and fit CMOS ASIC well. But the total delay can not be very long. The weighting mean timers using fast counters are ideal for applications with very long total delay. The pure digital design requires very minimum efforts. But the time resolution is not very good.

Different architectures of the weighting mean timers and their combinations can be chosen for different applications.

References

[1] J. Chapman and J. Mann, Digital Mean Timers for the Straw Tube Tracking System at SDC, *IEEE Transactions on Nuclear Science*, **40**, 794, (1993).

[2] Y. Arai et al., A Modular Straw Drift Tube Tracking System for the Solenoidal Detector Collaboration Experiment, Part I. Design, *Nuclear Instruments and Methods*, **A381**, 355, (1996).

[3] P. Mikelsons et al. (Colorado Group of KTeV at FNAL), Banana: A Drift Chamber Coincidence Trigger Subsystem, to be submitted to: *Nuclear Instruments and Methods*, (1998).

[4] C. Ljuslin et al., An Integrated 16-channel CMOS Time to Digital Converter, *IEEE Transactions on Nuclear Science*, **41**, 1104, (1994).

[5] J. Christiansen, An Integrated CMOS 0.15 ns Digital Timing Generator for TDC's and Clock Distribution Systems, *IEEE Transactions on Nuclear Science*, **42**, 753, (1995).