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(MISC)

EXPANSION OF THE READY-SYNC FUNCTIONS OF THE IBM 1800 COMPUTER

INTRODUCTION

The IBM 1800 utilizes external synchronization to enter or output digital information. In the case of digital input, the IBM 1800 can perform digital input addressing by generating a "ready" signal which is transmitted to an external customer device. The external device provides a "sync" pulse which initiates entry of digital input data into the Processor-Controller and removes the "ready" signal until completion of data entry.

Similarly, output data can be extracted from the Processor-Controller. A "ready" signal is transmitted to the customer's external device. The external device provides a "sync" pulse which causes the P-C to initiate action on an output point and to remove the "ready" signal.

Since the IBM 1800 may use a single "ready" output which must be shared by multiple user data sources, some means for selecting the desired user data source must be provided. Similarly, since the IBM 1800 can output digital data to multiple users (displays for example), some means must be provided to channel output data "ready" signals to the desired destination. Consequently a GATED (READY) · (SELECT) FANOUT and a SYNC FAN-In have been developed to permit the "ready"-"sync" functions to be shared by multiple users.

GATED (READY) · (SELECT) FANOUT

The circuit diagram of the GATED (READY) · (SELECT) FANOUT is shown in Fig. 1. The IBM ready signal specifications follow:

1. Down Level - 12 volts
2. Up Level + 0.0 to - 0.5 volts (indicates ready condition)
3. Output Impedance ~ 1000 ohms

The fanout device accepts the "ready" input at J7. Output selection is affected by closing a grounded-emitter N-P-N transistor switch in the IBM 1800 connected to one of the control terminals P2A, P2B, - - - P2F. Assume for example that a "ready" signal of 0 volts is applied at J7 and P2-B is selected. If the ready input is at ground potential, the base of transistor Q7 can rise to a voltage sufficiently positive so that base current flows from Q8 through R23 into the collector of Q7. Since the base of Q2 is approximately 6 volts and Q8 acts as a saturated transistor switch, approximately 5 volts appears across resistor R24. Consequently a current of 33 milliamperes is available at the collector of Q1. Since only 25.6 milliamperes are required across R6 to raise the voltage level to 0 volts, an additional 7 milliamperes are passed to ground through diode CR3. The voltage at output J2 is therefore caught at + 0.6 volts approximately. One could avoid using catching diodes CR2 through CR7 by letting the resistance of R24 be 180 Ω. However, the use of catching diodes minimizes the tolerance requirements on the power supplies and components.

The unselected outputs are essentially open-circuit at P2A, P2C, - - - P2F . Consequently, the transistor bases of Q1, Q3, Q4 - - - Q6 are at + 12 volts. The unselected transistors are back-biased, and no collector current flows through them. Therefore the unselected outputs appear to the output loads as voltage sources of - 12 volts with an output impedance of 470 ohms.

The unit is packaged in a standard double width NIM package. The selected "ready" outputs, J1 - - - J6, and the "ready" input, J7, are BNC connectors on the front panel. The "select" controls are applied through connector P2 on the rear panel. Individual control line pairs are brought out on the rear panel on barrier strips TB1 and TB2.

SYNC FAN-IN

The specifications for the IBM 1800 "sync" signal are as follows:

1. Up Level — - 0.5 volt to + 0.5 volt dc

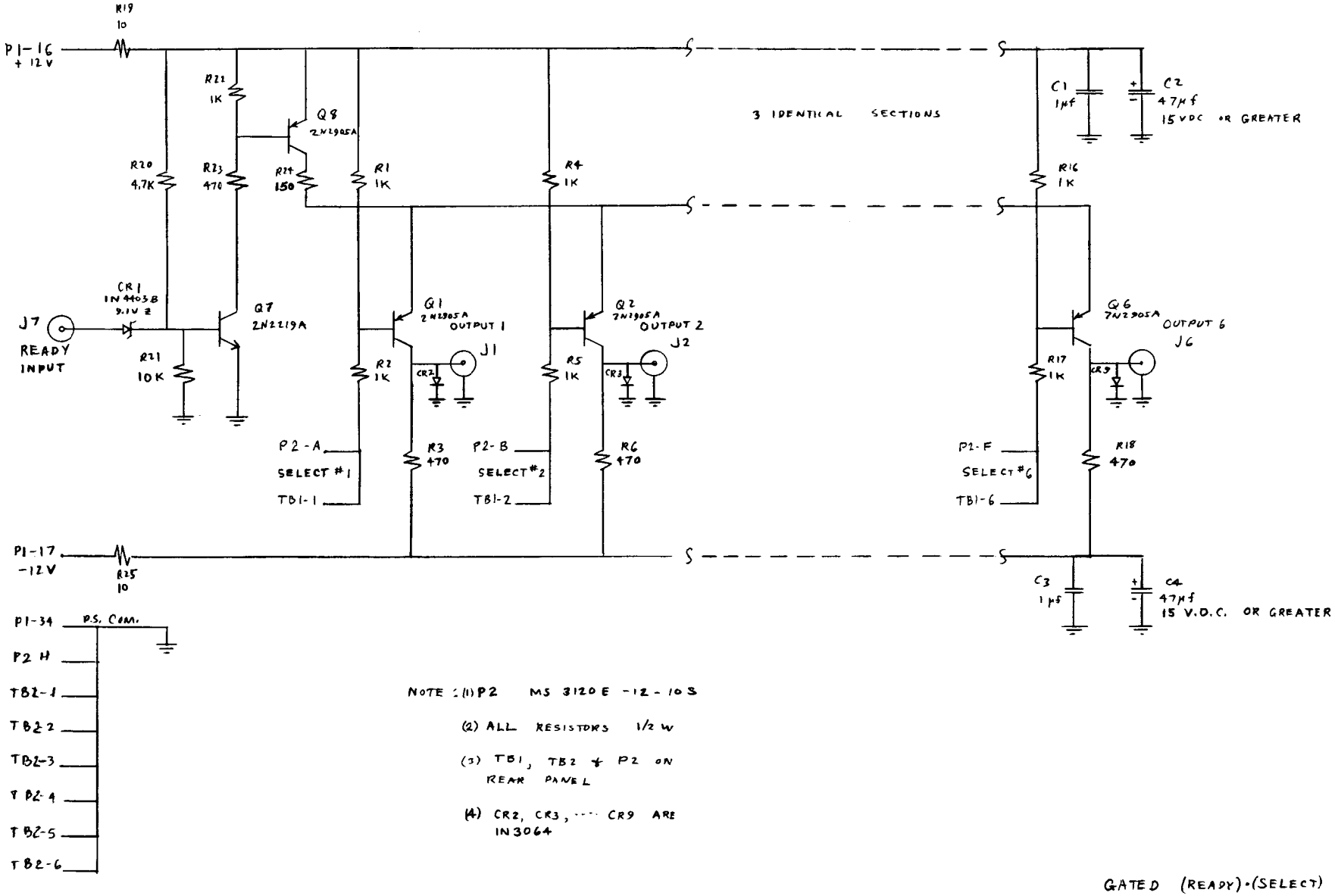
   The data channel starts on a positive going transition

2. Down Level - 6 vdv to - 18 vdc

3. Current Requirements 30 mA (maximum)

Given any one of six "sync" inputs, it is desired to "OR" the inputs and provide a buffered output. This function is accomplished by the circuit shown in Fig. 2. Transistors Q1 through Q6 together with Q7 function as part of a differential amplifier. When a - 12 vdc signal is applied at each of inputs J1, J2 - - - J6, the voltage across R8 is established by the voltage at the base of Q7. Since the base of Q7 is maintained at -5.6 vdc, the voltage across R8 is approximately 24 - (5.6 + 1.4) = 17 volts. However, if the voltage at one of the inputs is raised to zero volts, the drop across R8 increases to (17 + 5.6) = 22.6 vdc. When a down level is applied to all inputs, Q7 conducts; and a voltage of - 2.5 volts is applied to the base of Q8. The circuit built around Q8 and Q9 acts as a non-inverting saturating amplifier. Consequently, if all inputs are at the down level, the output at J7 is approximately - 11.5 vdc. If one of the inputs is at the up level, Q7 is cut-off and the output at J7 appears as a voltage source of 0 vdc with an output impedance of 520 ohms.

The unit is packaged in a standard single width NIM package. Inputs J1 - - - J6 and output J7 are BNC connectors mounted on the front panel.



NOTE : (1) P2 MS 3120 E -12-10S

(2) ALL RESISTORS 1/2 W

(3) TB1, TB2 & P2 ON REAR PANEL

(4) CR2, CR3, ···· CR9 ARE IN3064

GATED (READY)·(SELECT) FANOUT

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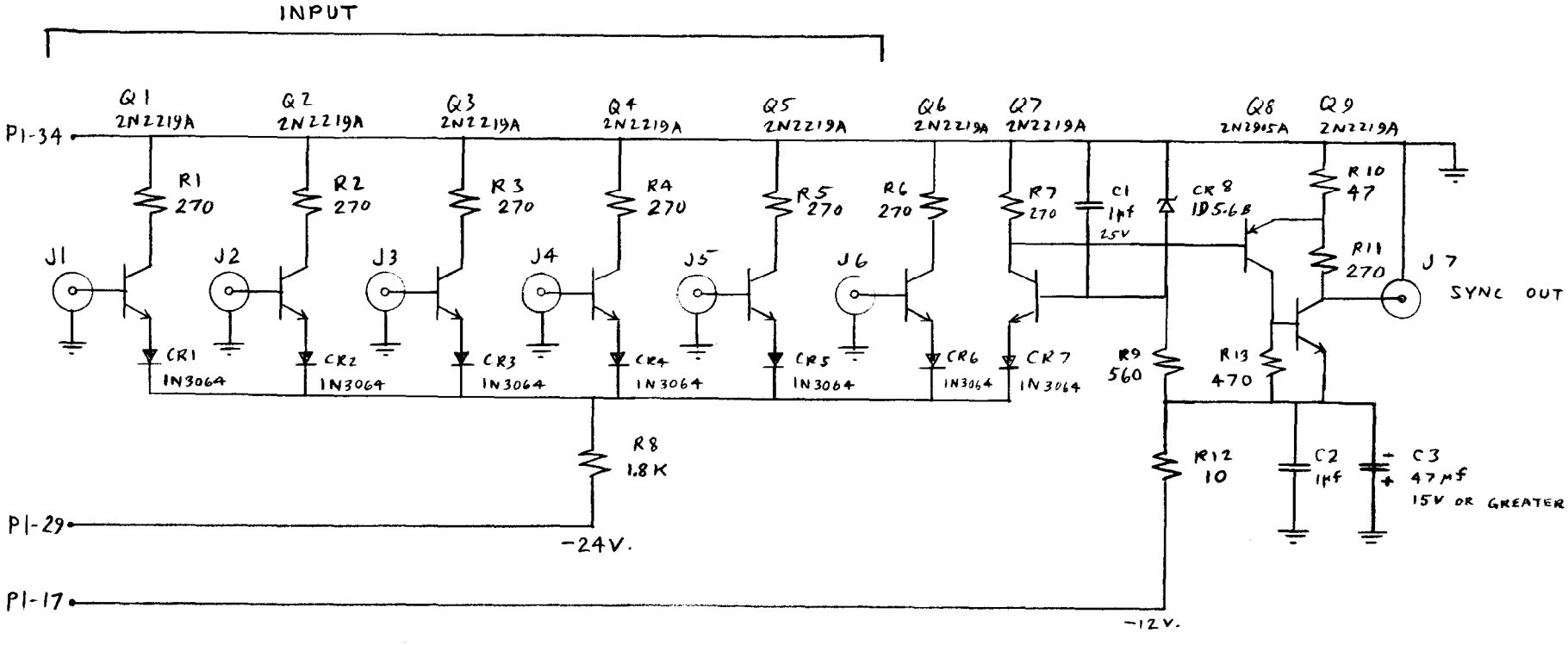
Fig. 1



NOTE: ALL RESISTORS 1/2 W

SYNC FAN-IN

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Fig. 2