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ATLAS Phase II Letter of Intent: Backup Document

Final Report: Phase-2 Tracker Upgrade Layout Task Force

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Abstract.

The mandate of the Upgrade Layout Task Force was to develop a benchmark layout proposal for the ATLAS Phase-2 Upgrade Letter of Intent (LOI), due in late 2012. The work described in this note has evolved from simulation and design studies made using an earlier "UTOPIA" upgrade tracker layout, and experience gained from the current ATLAS Inner Detector during the first years of data taking. The layout described in this document, called the LoI-layout, will be used as a benchmark layout for the LoI and will be used for simulation and engineering studies described in the LoI.

1. Introduction

From approximately 2022, the high luminosity upgrade of the LHC, HL-LHC, is expected to operate for a period of about 10 years. The HL-LHC will deliver (leveled) peak luminosities of $L_{peak} \geq 5 \times 10^{34}$ $cm^{-2}s^{-1}$ and accumulate an integrated luminosity of $L_{int} \sim 3000$ fb^{-1}. Assuming a 25 nsec bunch spacing, the mean number of interactions per bunch crossing (pile-up) will be $\langle\mu\rangle \sim 140$, with distribution tails exceeding 200 interactions. The separation of primary vertices in such collisions is at the millimeter level. In addition to requirements of robust operation, efficient readout and tolerance to both the integrated radiation dose and accumulated activation, the physics goals of the ATLAS experiment at the HL-LHC require that the tracking performance (for example the track reconstruction efficiency, the track momentum resolution, and the flavor tagging efficiency) of the tracking detector (ITK) is superior to that of the existing ATLAS Inner Detector (ID) at existing levels of pile-up.

The LoI-layout presented in this document has evolved from extensive simulations and engineering design work, over several years, based on the so-called UTOPIA layout [1]. The LoI-layout will be implemented in the ATLAS Athena simulation framework using Geant4 [2] for detailed performance studies in view of the LoI, including physics processes relevant to HL-LHC operation. At the same time, it will be used as the basis for detailed engineering studies, service optimizations, etc.

The LoI-layout will also allow performance comparisons with any new novel layout ideas, including the Alpine [3] and Conical [4] pixel layouts that are discussed as future options in the LoI. Finally, future advances in detector technology can be evaluated in the context of this layout.

The Phase-2 Tracker Layout Task Force was formed in November 2011, with the mandate to provide a realistic layout for the LoI by the ATLAS Upgrade Week [5] of March 2012. To facilitate this work a Requirements Document [6] was approved by the ITK Steering Committee in February 2012. This document summarizes the criteria, requirements and constraints motivating layout choices, as much as possible independently of any specific technology. The aim of this document was not only to state relevant facts and requirements, but to make design choices more "measurable". As much as possible engineering constraints and technical requirements were taken into account.

A layout, called the “Cartigny layout”, was presented at the Upgrade Week [7], and subsequently

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reviewed by several ITK working groups. Based mainly on practical engineering constraints, the layout was slightly modified to the design presented in this document (the LoI-layout).

The design process utilized simple design drawings and an analytic ray-tracing model [8] to estimate the main performance numbers. In this model, the track error matrix is evaluated for tracks as a function of p_T and pseudo-rapidity $|\eta|$. The program is supplied with a tabulated magnetic field (B_r and B_z) on an r-z grid, as well as idealized active or passive cylindrical, conical and disk material layers. In the case of active layers, the sensor resolutions in r-ϕ and z are provided. The model takes account of multiple scattering in the material layers.

A simulation of the LoI-layout using Geant4 was not possible within the timeline of the Task Force. Simulation studies, together with a detailed engineering and design work and an optimization of both the service routings and material, will be made for the LoI in the coming months. That work will lead to further refinements of the LoI-layout presented here, that will be included in future versions.

The LoI layout is described, together with relevant notation and a table of active dimensions, in Section 2. The tracker design is then motivated and justified in subsequent sections.

2. The LoI Layout

Figure 1 shows a drawing of the LoI layout.

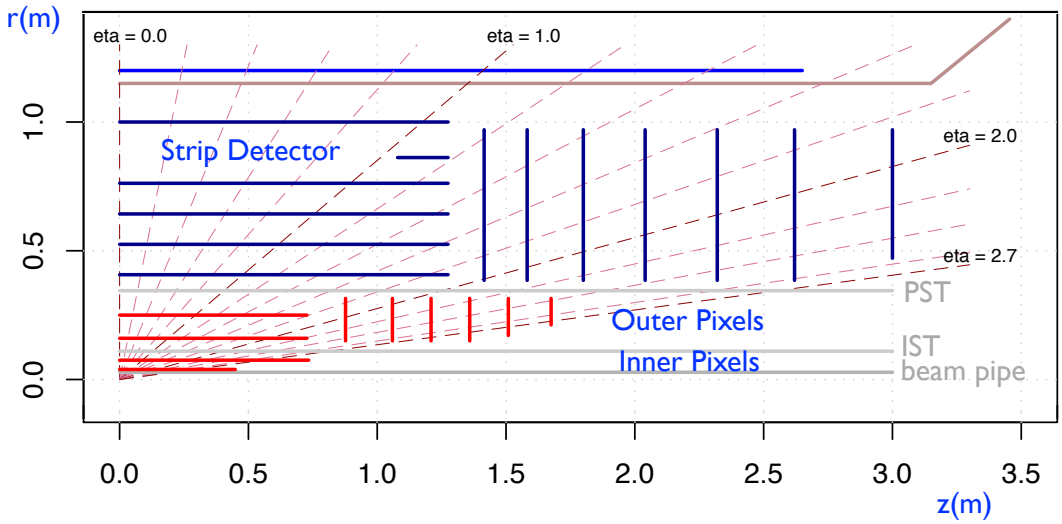


Figure 1. A quarter panel radius (r) vs. z projection of the proposed LoI layout that will be used for detailed Geant4 simulations and engineering studies (see text).

The pixel (red) and silicon micro-strip (blue) sub-detectors are independent. The pixel sub-detector has four barrel layers with 6 pixel disks in each end-cap. The two inner pixel barrel layers are separately removable and supported on an Inner Support Tube (IST) of inner radius R_{IST} = 110 mm. The full pixel detector is supported on a Pixel Support Tube (PST) of inner radius R_{PST} = 345 mm. The strip sub-detector has 5 barrel layers, and in addition a barrel "stub" to maintain hermeticity at the barrel-forward boundary. The layout is complemented by 7 disks in each end-cap. Each strip layer or disk has back-to-back sensors that provide 2 hits with a nominal 40 mrad stereo angle. Tables 1 and 2 list the mean active radial and longitudinal boundaries for each layer and disk of the pixel and strip sub-detectors.

The layout was guided by the requirement of at least 14 hits, including at least 4 pixel hits, in the range $|\eta| < 2.5$.

The layout was also constrained by the external decision of the ITK Steering Committee that the inner 2 pixel layers, as well as the full pixel detector, should be independently replaceable and fully accessible. This imposes the IST and PST support tubes, and constrains the cable routing.

Table 1. a) The mean active radius and active ½ – length for each pixel barrel layer of the LoI layout. b) The inner and outer mean active radii for each pixel disk, as well as the mean active longitudinal position along the beam-line (|z|)

Pixel Barrel		
Layer	**Mean active radius (mm)**	**Active ½ - length (mm)**
L0	39	456.5
L1	75	747.0
L2	160	722.8
L3	250	722.8

(a)

Pixel End-cap			
Disk	**Active radius (mm)**		<z> active (mm)
	Inner	**Outer**	
D1	150.1	315.0	877.0
D2	150.1	315.0	1059.0
D3	150.1	315.0	1209.0
D4	150.1	315.0	1359.0
D5	170.6	315.0	1509.0
D6	212.4	315.0	1675.0

(b)

Table 2. a) The mean active radius and active ½ – length for each silicon micro-strip barrel layer of the LoI layout. b) The inner and outer mean active radii for each micro-strip disk, as well as the mean active longitudinal position along the beam-line (|z|)

Strip Barrel		
Layer	**Mean active radius (mm)**	**Active ½ - length (mm)**
L4	407	1275
L5	525	1275
L6	643	1275
L7	762	1275
L8	1000	1275
Stub	862	1079 – 1275

(a)

Strip End-cap			
Disk	**Active radius (mm)**		<z> active (mm)
	Inner	**Outer**	
D1	385.0	970.0	1415.0
D2	385.0	970.0	1582.0
D3	385.0	970.0	1800.0
D4	385.0	970.0	2040.0
D5	385.0	970.0	2320.0
D6	385.0	970.0	2620.0
D7[1]	471.0	970.0	3000.0

(b)

3. Performance Requirements for the Phase-2 Tracker

The performance document [6] used knowledge of the existing tracker performance, as well as detailed simulations using the UTOPIA layout [1]. As a result of those considerations, the following general conclusions were reached:

a) To maintain pattern recognition capabilities in a high-pileup environment and to allow for robustness against limited detector defects:
   - At least 14 hits should be maintained for $|\eta| < 2.5$, including gaps between the barrel and end-cap regions, and for primary interactions in the range $|z_{int}| < 150$ mm (this motivates the barrel "stub"): this is the requirement for what is termed "full hermeticity" in this note;
   - At least 4 pixel hits are required to allow segment reconstruction and extrapolation to the

[1] The increased inner radius of this disk (one inner module) is motivated by the integrated non-ionising (NIEL) radiation. A radius of 385 mm will be assumed for most simulation studies.

silicon strips;

- Limited stand-alone tracking capability should be maintained in the forward region ($2.5 < |\eta| < 2.7$), based on the pixels, to allow for combined muon tracking;
- An optimized pixel granularity (to be determined from detailed Geant4 simulations) is needed to aid high-p_T track association to primary vertices (up to 200 primary vertices within a bunch-crossing length of σ_Z ~5 cm), and to maintain secondary-vertex and b-tagging capabilities at the level of the existing tracker (including the IBL) despite the existence of a larger radius beam-pipe and higher pileup;
- At least 5 stereo space points (10 silicon micro-strip layers) are required to allow robust track reconstruction for a detector with 4 pixel layers. This offers limited back tracking capabilities for conversions, and allows bremsstrahlung recovery. In both the bending and non-bending planes, the accuracy of the stereo track extrapolation to the EM (and hadronic) calorimeters should match the reconstructed calorimeter cluster centroid accuracy;
- The track reconstruction efficiency and track momentum resolution is required to be at least at the level of the existing ATLAS ID, in a high-pileup environment, and superior to ATLAS for the 2-track separation within high-E_T jets: this implies a low material budget noted below, a larger dimension of the pixel system and acceptable detector granularities in the inner layers of the strip detector (nominal specifications for the occupancy are < 0.4% for individual pixel elements and < 2.5% for individual strip elements, discussed below and to be verified by simulation);
- The ability to align with tracks, and the ability to adequately constrain weak alignment modes is essential; it is assumed that the tracker stability and position reproducibility after thermal or magnetic cycling can be maintained at least at the level of the current tracker.

b) No total material budget specifications were listed in [6], but the following aims were noted to significantly reduce the total material as compared to the existing ATLAS ID. For the preliminary performance studies the following assumptions were made (to be refined):

- It is important to minimize the material of the detectors and their support structures, subject to the stability constraints noted above. Including the sensors, readout electronics, electrical services, cooling pipes and mechanical supports, the following material is targeted, averaged over the active sensor surface: < 1.5% X_0 per layer for inner pixel layers, < 2% X_0 per layer for outer pixel layers, < 2.5% X_0 for inner short strip layers and < 2% for long outer strip layers;
- Passive service material, both inside and outside the detector acceptance, is dominant and must be minimized. Simulation studies of service layouts are crucial for both the detector occupancy and secondary interactions/conversions. In particular, with no formal specification, an aim is to remove all passive services (excepting cable buses and cooling lines attaching the modules) within $|\eta|=1$.

The following issues were not considered at this stage in the layout:

a) Activation, in particular for the inner pixel layers and disks, may be a major concern. In the absence of detailed simulations, and a better understanding of the detector materials, possible activation concerns were not considered in the layout.

b) Possible influences of the layout due to a possible hardware level-1 track trigger were not considered, as the layout could, depending on the chosen technology, become significantly more complex.

c) The expected individual strip occupancy for inner strip barrel modules exceeds the qualitative limits of ~1% used for ATLAS studies, and 2.5% for the specifications in [6], assuming default barrel strips of 74.6 μm x 23.6 mm. An optimization of the barrel strip granularity requires full simulation, and for the LoI, 17.7 mm barrel strips are being simulated [9] (see Section 7). In the case of inner disk modules, the situation is even worse. For this reason, much shorter strip lengths are being studied in [9].

d) Similarly, the pixel granularity and shape, especially for inner layers, needs to be optimized: for the performance studies of this layout, a nominal granularity of 50 x 250 μm^2 was used for all layers. It is assumed that for the two innermost pixel layers a much reduced pitch will become available.

4. External Requirements affecting the Phase-2 Tracker

The LoI layout has been influenced by several external constraints imposed by the existing detector envelope, and by general considerations of cost, access, maintenance, and initial engineering feasibility (for example service routing).

a) The inner envelope of the ITK is determined by the beam pipe radius and bake-out cladding. The current envelopes are, as shown in Table 3:
   - R_{inner} (beam pipe) = 28 mm;
   - R_{outer} (beam pipe) = 33 mm;
   - $<R_{L0}>$: Mean active radius of inner pixel barrel layer 0 $<R_{L0}>$ = 39 mm

Table 3: Assumed outer radii of the beam pipe and pixel support structures, and the outer active envelope, in the LoI layout.

	Outer Radius (mm)
Beam Pipe	33
Inner Support Tube (IST)	110
Pixel Support Tube (PST)	345
Mean active radius barrel strip layer, R_{barrel}	1000
Active outer strip disk radius, R_{EC}	970

b) The outer envelope of the ITK is defined by the service routing and the overall ITK support structure. The current engineering envelopes are:
   - $<R_{barrel}>$ Mean active radius of outer barrel strip layer $<R_{barrel}>$ = 1000 mm;
   - $<R_{EC}>$ Mean active radius of outer EC strip disks $<R_{EC}>$ = 970 mm.

   The aim is to maximize the track lever arm for momentum measurements. For the same reason, the last strip disk is placed at |z| = 3000 mm, the constraint being imposed by service routing.

c) The requirement that the full pixel detector should be removable in a short shutdown effectively separates the pixel and strip tracking envelopes, since a Pixel Support Tube (PST) is required, and all pixel services must be routed within that envelope. The requirement that the inner 2 pixel layers are replaceable implies the need of an Inner Support tube (IST) and service routing for those layers within that envelope. As shown in Table 3, the current outer radii of the IST and PST are respectively:
   - R_{IST}(outer) = 110 mm; and
   - R_{PST}(outer) = 345 mm

   R_{IST} is determined by the requirement that the inner 2 pixel layers may need replacement during the operating lifetime of the HL-LHC, without removing the full pixel detector. R_{PST} is determined by several factors, the most important being the need to maintain an acceptable occupancy. Other less tangible factors include the expected pixel cost.

d) The constraints (subject to engineering changes) imposed to allow service routing are shown in Table 4.

e) The services – the material budget, the placement of patch panels and manifolds, and the

service routing – are crucial constraints to the layout, and only limited realistic simulations using the UTOPIA layout were available. Two possible service routings of the pixel services have been identified for urgent simulation and engineering studies. Option A of Figure 2 places the passive outer pixel barrel and disk services at larger radius, reducing the traversed material. Option B, subject to the optimized placement of patch panels and manifolds, minimizes the passive service material inside the detector acceptance but increases the material traversed in the forward direction.

Table 4: Clearances between active barrel and disk layers for service routing, or for engineering supports.

STRIPS	Distance (mm)
Minimum separation between barrel layers	100
Active gap between barrel layer and end-cap disk (mean active δz)	140
Gap between PST and end-cap disk inner radius (active radius)	40
Gap between PST and barrel layer inner radius (mean active radius)	70
PIXELS	
Active gap between barrel layer and end-cap disk (mean active |δz|)	150
Gap between PST and end-cap disk outer radius (active radius)	30

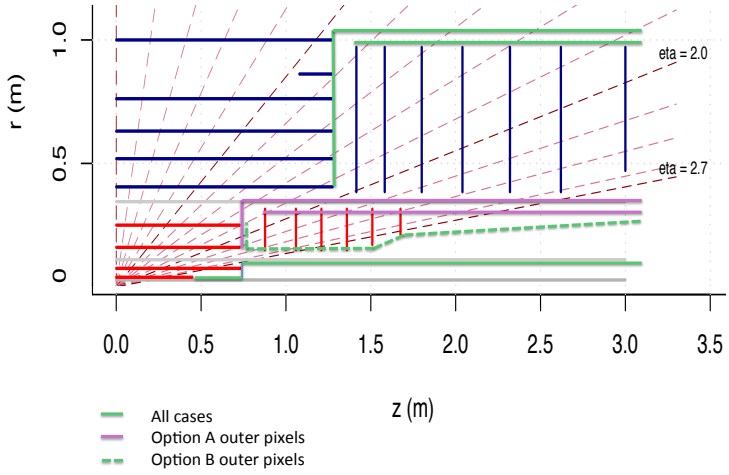


Figure 2. Possible service layouts for the outer pixel layers.

5. Constructing the Pixel and Strip Layouts

Taking account of the above performance requirements and engineering constraints, the pixel layout is driven by the requirement of hermeticity subject to the positions of the IST and PST, their radial clearances, and the clearance between the barrel and disk pixel layers. Two pixel barrel layers are constructed inside the IST and two layers are constructed between the IST and PST. The inner pixel radius is minimized subject to engineering constraints ($<R_{L0}>$ = 39 mm) and the outer pixel radius is determined by the PST radius and the hermeticity requirement between L3 and D1 ($<R_{L3}>$ = 250 mm). The forward pixel disks are then adjusted to achieve hermeticity and the requirements that inner layers reach $|\eta|$ = 2.7.

As noted in Section 3, the PST radius is determined primarily by the limit to the occupancy at high

pile-up of the inner micro-strip modules for D1-D7.

An attempt is made to maintain equal |z|-spacing between pixel disks, and to reduce the track distance between successive hits. The |z| positions are then iterated to match the position of strip disks, keeping the number of hits above 14 at all $|\eta| < \sim 2.5$.

The default pixel size for the LoI layout is 50 x 250 μm^2. However, based on experience with the current pixel detector and first simulation results from UTOPIA, there are indications that small pixel sizes would be beneficial:

- to account for the loss of impact resolution due to the larger radius of L0 compared with the IBL;
- to improve the accuracy of track association to selected primary vertices, possibly implying a change of (local) z pitch especially in the EC regions;
- indications of shared hits deteriorating the 2-track resolution and b-tagging efficiency near the core of hadronic jets.

Smaller pixel sizes (25 x 125 μm^2) are being implemented in Geant4 simulations to optimize the pixel granularity, taking into account clustering effects etc. only available in the full simulation [9].

The silicon strip detector consists of five strip barrel layers (L4–8) and 7 disks (D1–7). In addition, a barrel "stub" is introduced to ensure the required hermeticity in the region of the barrel – end-cap gap.

The radius of L4 is determined by the PST clearance, and the detector occupancy, estimated to be ~1.5%/mm^2 at the selected R4 radius (R_{L4} = 405 mm). The situation is even worse for the inner modules of D1-D6. For this layout study, the default strip granularity for barrel micro-strip layers L4 – L6 is (74.6 µm x 23.6 mm). The default granularity for the layers L7 and L8, as well as the "barrel stub" is (74.6 µm x 47.2 mm). However, shorter strips are being considered for L4, and are being simulated in [9]. Similarly, an optimization of the inner module strip length of D1-D7 will be made [9].

Each of L4-L8 and D1-D7 are double layers with a stereo angle of 40 mrad., to allow reconstructed space-point |z| resolutions (barrel) and |r| resolutions (disks) of ~760 µm for an individual layer. By alternating the stereo angle in successive layers, the effective z (r) - resolution becomes ~550 µm per layer.

The current mean active radii of the layers have been modified slightly from the optimized design to ensure 4-fold azimuthal symmetry of the barrel layers, assuming a 10^o tilt angle of the barrel modules (respectively 28, 36, 44, 56, and 72 for each layer, and 64 for the "stub"). The barrel ½ - length of 1275 mm allows for 13 strip modules to ensure full barrel hermeticity to $|\eta| > 1$. The strip disk positions (and also the pixel positions) have then been slightly changed accordingly.

Full hermeticity is achievable using 6 micro-strip disks, but this results in un-equally spaced disks and sharp "saw-tooth" variations of the momentum resolution. In the Cartigny layout, this was alleviated using several "disklets", but these were not favoured for engineering reasons. A 7^{th} disk was introduced to partially recover the excellent momentum resolution obtained using the disklets. The disk separations were initially chosen the minimize the saw-tooth variations, and then modified slightly.

The approximate area for the different pixel and micro-strip layers and disks is shown in Table 5.

Table 5. Approximate active silicon surface for the barrel region, and for each of the pixel and strip end-caps (labeled as A and C).

Pixel and Strip Barrel	
Layer	**Area (m^2)**
L0	0.22
L1	0.69
L2	1.46
L3	2.28
Total pixel	**4.65**
L4	12.98
L5	16.63
L6	20.22
L7	24.42
L8	32.04
Stub	4.25
Total strip	**110.54**
Total barrel	**115.19**

Pixel and Strip End-cap	
Pixel	**Area (m^2)**
D1–D4	0.241
D5	0.220
D6	0.170
Total pixel (A+C)	**2.708**
Strip	**Area (m^2)**
D1–D6	4.981
D7	4.518
Total strip (A+C)	**68.81**
Total end-cap	**71.52**

6. Preliminary Performance Evaluation of the LoI Layout

6.1 Preliminary Material Estimate

The expected material (units of radiation length X0) is shown for the LoI layout in Figure 3a). A comparison is made with the existing ATLAS layout in Figure 3b). The following should be noted:

- The ATLAS material estimate is "as built", to be compared with the estimate material budget for the LoI layout is "as projected";
- For the LoI layout, the material budget, although increasing, is well understood for tracks of $|\eta| < 1.0$, in the impact range $|z| < 150$ mm.
- The reduced material budget of the LoI layout is largely due to multiplexing of the electrical services, both high-voltage and low-voltage, and reduced on-detector material following from the "baseline" CO_2 cooling.

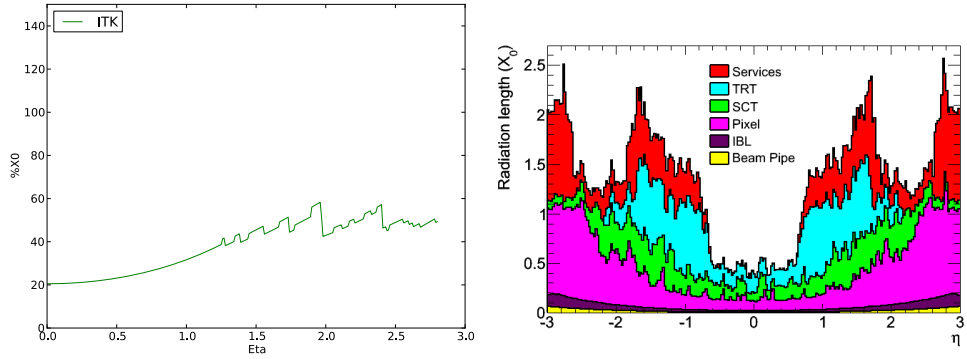
6.2 Hermeticity and Number of Hits

Figures 4 a) and b) show respectively: the number of pixel hits as a function of $|\eta|$, for tracks having a longitudinal vertex position -150 mm, 0 mm and + 150 mm; and the number of strip hits as a function of $|\eta|$. In the region $2.0 < |\eta| < 2.7$, at least 4 pixel hits are traversed. The importance of this for the vertex association of muons in the range $|\eta| > 2.5$ needs to be assessed by full simulation. Also the forward pixel granularities need to be assessed.

Figures 5 a) and b) show respectively: the total number of silicon layers traversed as a function of $|\eta|$; and the total number of pixel or stereo space points reconstructed. Although the full hermeticity requirement of 14 hits is not achieved at $|\eta|$ ~2.5, the performance is expected to be maintained because of the increased number of pixel hits.

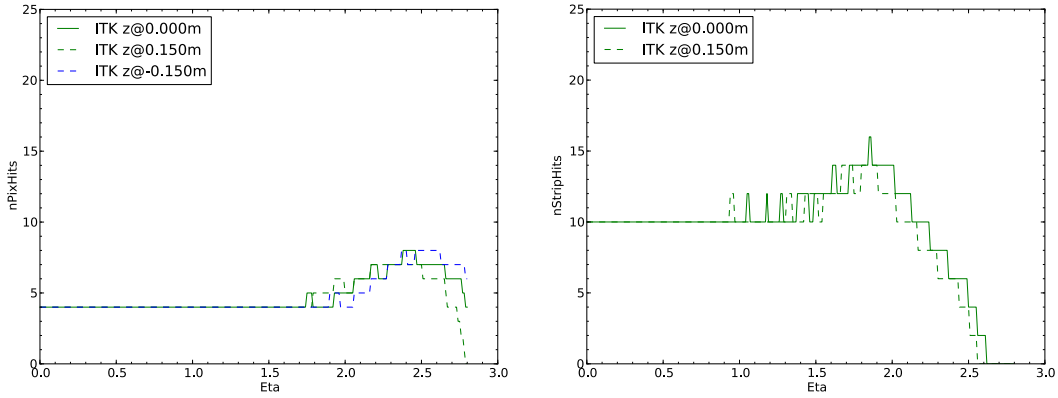
6.3 Impact Parameter Resolution

No performance plots of the transverse and longitudinal mean impact resolution are shown in this document, since these quantities will be determined by the material of the inner pixel layers, the pixel granularity, and the event complexity. The performance will be evaluated by [9], but a requirement is that it should be superior to that of the existing ATLAS detector including the IBL, despite the larger inner radius (this implies reduced granularity).



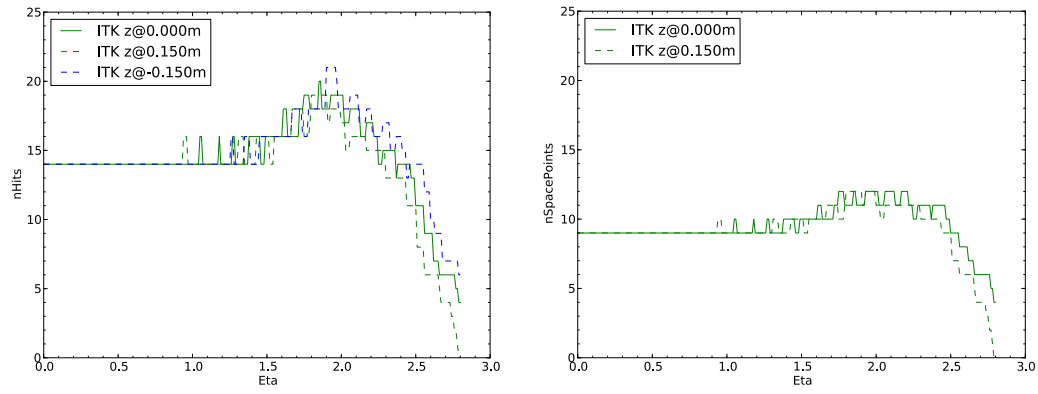
(a) (b)

Figure 3. a) The estimated material budget, expressed as a % X_0, as a function of |η|. b) The as-built material budget, expressed in units of X_0, for the existing ATLAS ID. The absolute scale of the figures should not be directly compared since the passive material implementation of (b) is more complete, in particular at the barrel end-cap transition. However, a striking comparison is the larger barrel |η| range in (a).



(a) (b)

Figure 4. a) The number of pixel hits as a function of |η|, for tracks with z-vertex with respect to the centre of the ITK of z = -150 mm, z = 0 mm and z = 150 mm. b) The number of micro-strip hits as a function of |η|, for tracks with z-vertex z = 0 mm and z = 150 mm.



(a) (b)

Figure 5. a) The total number of silicon layers (pixel or micro-strip) traversed as a function of |η|, for tracks with z-vertex with respect to the centre of the ITK of z = -150 mm, z = 0 mm and z = 150 mm. b) The total number of pixel or stereo micro-strip space points as a function of |η|, for tracks with z-vertex z = 0 mm and z = 150 mm.

6.4 Momentum Resolution

Figure 6 compares the nominal transverse momentum resolution as a function of |η|, assuming the nominal pixel and silicon micro-strip granularities, for the LoI layout. The results are compared with that from the existing (ATLAS + IBL) detector, assuming the same simplifications of the ray-tracing program [8] (optimistic with respect to measured data). Nevertheless, a 30% improvement of the p_T-resolution is estimated, with respect to the existing ATLAS detector. Ongoing GEANT simulations should give a more accurate comparison with respect to the existing ATLAS detector.

The deteriorated p_T-resolution in the forward direction is due to:

- The reduced outer active radius of strips D1-D7 (R_{outer} = 970 mm) as compared with L8 ((R_{outer} = 1000 mm);
- The drop-off of lever arm at the outer radius of successive disks, giving the saw-tooth effect;
- The combined effects of reduced integrated magnetic field B_{int} (lever arm) and non-uniformity of the B-field at large z, in particular beyond the outer radius of D7 (placed at z=3000 mm to maximize the lever arm as a function of |η|.

Material effects also deteriorate the resolution with increased |η|, in particular for $\pi^{\pm}$ and $e^{\pm}$.

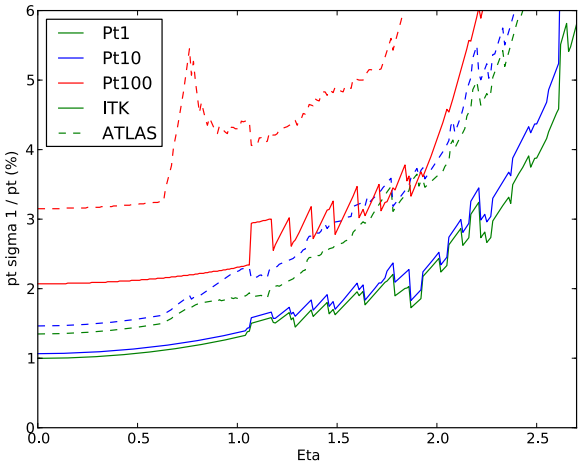


Figure 6. Inverse p_T-resolution using [8], measured as a function of |η| for the LoI layout, and comparison with the inverse p_T resolution of the existing ATLAS experiment including the IBL.

6.5 Distance between hits

A major concern for the existing ATLAS tracker is for tracks in the forward region (|η| > 2), where the large track extrapolation between the pixel and micro-strip disks – in the presence of passive service material – can result in an increased track fake rate. An effort has been made in the LoI layout to increase the number of pixel hits in this region (discussed above), and to reduce the maximum extrapolation distance between successive pixel or micro-strip disks. Engineering efforts will also aim to reduce the passive service material. Figure 7a) shows the maximum distance between the pixel and strip sub-detectors, expressed as a function of the track |η|. Figure 7b) shows the difference of this maximum extrapolated distance, and that of the existing ATLAS detector. The results of Figure 7 are a significant improvement with respect to the existing tracker.

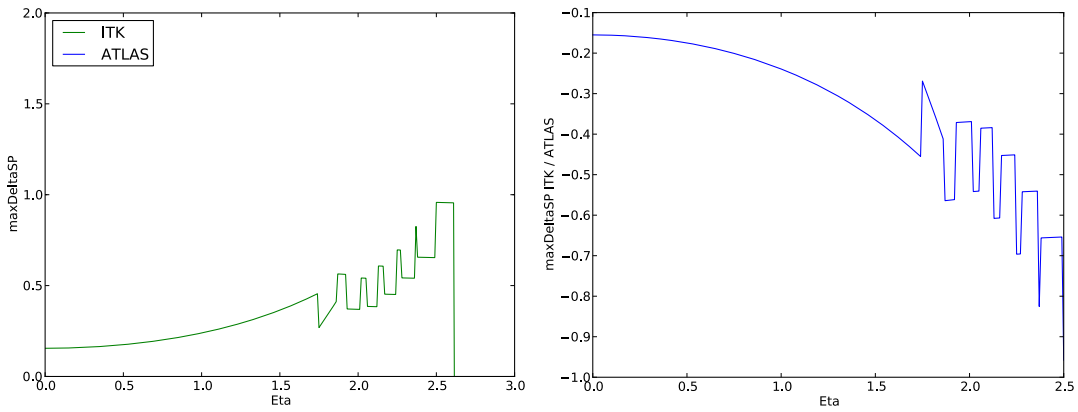


Figure 7. a) Maximum distance between the pixel and silicon strip layers (L_M), measured as a function of the track $|\eta|$. The vertical scale is measured in metres. b) The difference (L_M (ITK) – L_M(ATLAS). The results of Figure 7 are a significant improvement with respect to the existing tracker.

7. Limitations of the LoI-layout

The LoI layout fulfills the design requirements of the ITK detector. The layout is not, however, complete. In particular, the layout is independent of the details of module layout: sensor granularity, module placement, module overlaps for alignment, structural stability, service routing etc. that will determine the ITK performance.

An optimization of these issues requires a full Geant4 Athena simulation [9] for relevant physics channels.

Nevertheless, the following comments are relevant.

a) Other pixel layouts are being considered, for example [3] and [4]. For this reason, the pixel and strip sub-detectors have been optimized semi-independently, allowing the replacement of the pixels by some other layout, and allowing direct performance evaluations of the layouts. In a final engineering design, this independence is not mandatory.

b) The possible implications of a hardware Level-1 track trigger have not been considered in the LoI layout.

c) There has been considerable engineering criticism of the barrel "stub" from the silicon strip "stave" community, because of the lack of modularity of that design (largely because of the stave technology currently baselined). Suggestions have been made to replace the barrel "stub" by either an additional pixel layer inside the pixel PST, or by the addition of a sixth barrel layer. No detailed comparisons of these 2 options have been made. Using the existing technologies, the cost increase would be similar for each solution.

d) The major concern of the LoI layout concerns the occupancy, and the deterioration due to radiation damage, of the inner strip barrel layer (L4) and the inner modules of the strip disks D1-D7. A powerful argument exists for replacing L4 by a pixel technology if technical developments permit, because of the sensor granularity.

e) A second major concern is the activation of inner pixel barrel and disk regions. This has not been considered and may influence the design at a later stage.

An attempt has been made in the layout to maintain limited tracking capability in the range $2.5 < |\eta| < 2.7$. Depending on the physics case, it may be useful to extend the pixel coverage to $|\eta| < 3.0$, to allow better sensitivity to VBF Higgs production. This could affect the IST choice.

8. Conclusions

The ATLAS ITK Layout Task Force has presented in this note the proposed LoI layout of the ATLAS Phase 2 Inner Tracker (ITK) upgrade. The layout potentially fulfills the performance requirements of the proposed upgrade.

The LoI layout has taken account of comments by the ITK detector and engineering communities, but has not at this stage been fully implemented into a Geant4 simulation of potential Phase 2 physics processes, not has it been fully engineered.

References.

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[4] S. Burdin et al., *Conical pixel layout,* backup document for the Phase II ITK Upgrade.

[5] ATLAS Upgrade Week, Stanford, March 2012, see http://www.slac.stanford.edu/exp/atlas/events/2012/AUW/

[6] A. Clark et al., Performance Specifications of the Phase II Tracker Upgrade, ATLAS Note ATU-SYS-FP-0001, May 2012. See http://edms.cern.ch/cern.ch/document/11217189

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[8] N. Hessey, *IDRES program*, see http://www.nikhef.nl/~r29/upgrade/idres.html.

[9] LoI Layout in Geant4 Athena simulation. (Peter, what is the best reference)