CMS CALORIMETER TRIGGER RECEIVER SYSTEM

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Abstract

The CMS level-1 calorimeter trigger electronics is designed to identify signatures for high-energy electrons, photons, neutrinos and jets. The calorimeter regional trigger system receives and processes 1.2 Gbaud digital serial data transmitted from the calorimeter readout electronics on copper cables and transmits the results for further processing at 160 MHz. The heart of this system is the Receiver Card, which uses the new generation of Gigabit Ethernet receiver chips on dedicated mezzanine cards that convert serial data to parallel data. This data is then deskewed, linearized, summed and further processed on the main Receiver Card before transmission on a high speed point-to-point backplane for subsequent processing by cards that sum energies and identify electrons and jets.

1. CMS TRIGGER OVERVIEW

The CMS detector for the Large Hadron Collider (LHC) [1] presents an extraordinary challenge for its trigger and data acquisition system. Its trigger system must carefully sift the 40 MHz data to retain only interesting physics signals at 100 Hz level while discarding the well-known QCD background. The CMS trigger is implemented in two physical levels, one based on custom electronics and the other relying upon commercial processors. The level-1 system uses only coarsely segmented data from calorimeter and muon detectors, while holding all the high-resolution data in pipeline memories in the front-end electronics, to produce a trigger decision in 3 μs. Level-1 triggered events at a 75 kHz rate are sifted further in higher levels of triggers implemented as software filters.

The CMS level 1 trigger decision is based in part upon local information from the level 1 calorimeter trigger about the presence of physics objects such as photons, electrons, and jets, as well as global sums of E_t and missing E_t (to find neutrinos) [2].

For most of the CMS ECAL, a 5 x 5 array of PbWO4 crystals is mapped into trigger towers. In the rest of the ECAL there is somewhat lower granularity of crystals within a trigger tower. There is a 1:1 correspondence between the HCAL and ECAL trigger towers. The trigger tower size is equivalent to the HCAL physical towers, .087 x .087 in η x ϕ. The ϕ size remains constant in $\Delta\phi$ and the η size remains constant in $\Delta\eta$ out to an η of 2.1, beyond which the η size increases.

As shown in Figure 1, the CMS level-1 calorimeter trigger starts with a basic 3 x 3 sliding-window electron algorithm [3] that involves two separate cuts on the longitudinal and transverse isolation of the ECAL energy deposit. The first electron cut involves the hit tower HCAL to ECAL energy ratio, H/E. A second cut is placed on the HCAL transverse energies in the nearest eight towers surrounding the hit tower.

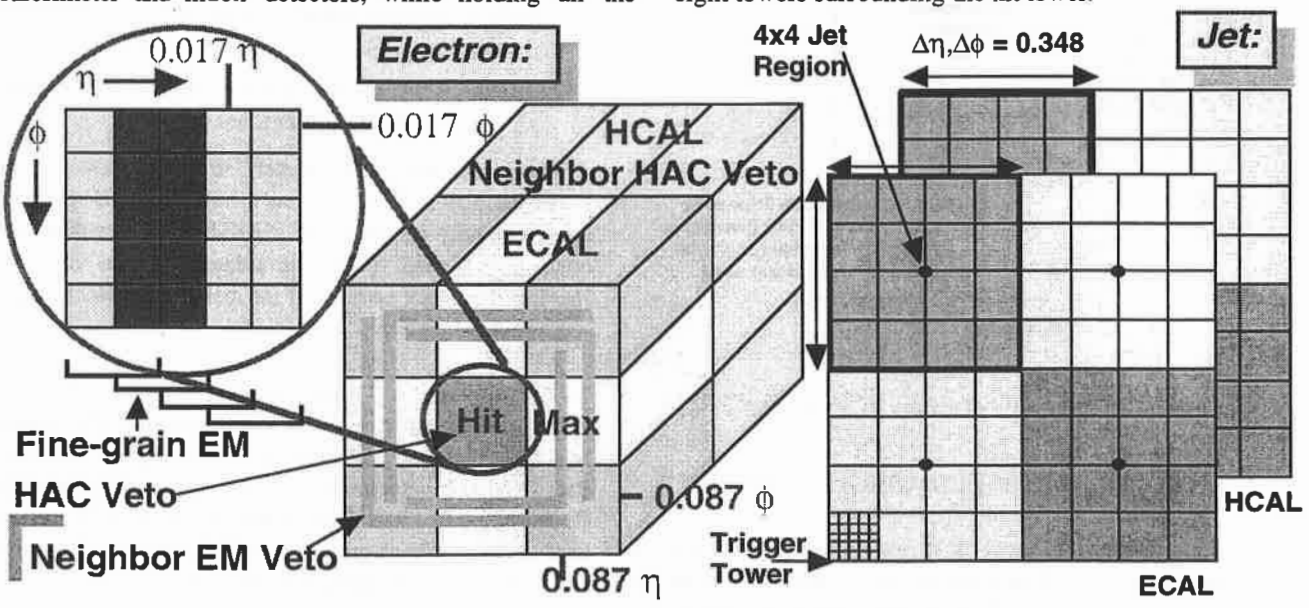

Figure 1. Calorimeter Trigger Algorithms.

Additional trigger cuts are imposed to permit lower E_t thresholds. An ECAL transverse isolation cut considers all four 5-tower corners of the 3x3 window and requires that at least one of them be below a programmable cutoff. The act of checking all four 5-tower corners ensures that the candidates depositing energy in any corner of the central tower do not self-veto due to leakage energy. Another cut is based on a summary of the energy found in the ECAL crystals before summation in trigger towers. A "fine-grain" electromagnetic isolation bit is set and transmitted with the trigger tower energy if the maximum energy found in a pair of strips of five crystals represents a large fraction of the total energy found in the 25 crystals summed in a single ECAL trigger tower. An electron found in a region where this bit is set can be triggered with a lower threshold.

As shown in Figure 1, jet triggers are based on sums of ECAL and HCAL transverse energy in non-overlapping 4x4 trigger tower (0.35 η x 0.35 ϕ) regions. Results of detailed simulation of both electron and jet algorithms have shown good performance on the CMS physics signals [4].

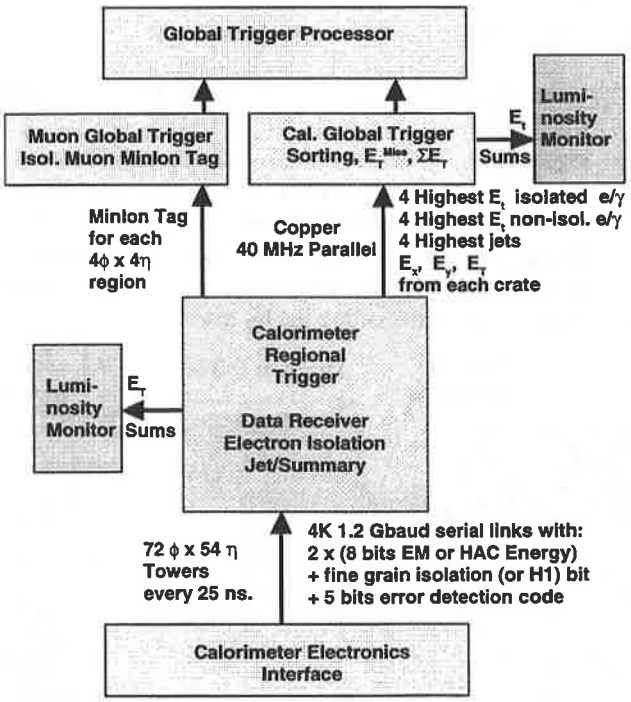

Figure 2. Overview of Level 1 Calorimeter Trigger

2. CALORIMETER TRIGGER HARDWARE

The calorimeter level 1 trigger system, shown in Figure 2, receives digital trigger sums from the front end electronics system, which transmits energy on an eight bit compressed scale. The data for two HCAL or ECAL trigger towers for the same crossing will be sent on a single link in eight bits apiece, accompanied by five bits of error detection code and a "fine-grain" bit characterizing the energies summed into the trigger towers. For ECAL, this is the "fine-grain" electromagnetic isolation bit. In HCAL, this bit is set based on the ratio of energy in the first and second longitudinal HCAL sections.

The calorimeter regional crate system uses 19 calorimeter processor crates covering the full detector. Eighteen crates are dedicated to the barrel and two endcaps. The remaining crate covers both Very Forward Calorimeters.

Each calorimeter regional crate transmits to the calorimeter global trigger processor its sum E_t, E_x and E_y. It also sends its 4 highest-ranked isolated and non-isolated electrons and 4 highest energy jets along with information about their location. The global calorimeter trigger then sums the energies and sorts the electrons and jets and forwards the top four calorimeter-wide electrons and jets, as well as the total calorimeter missing and sum E_t to the CMS global trigger.

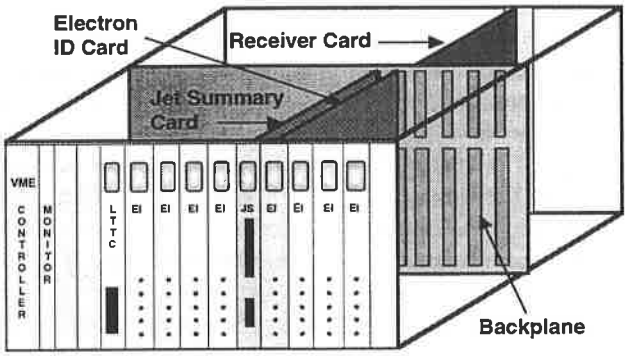

Figure 3. Schematic view of a typical Calorimeter Level 1 Regional crate.

The regional calorimeter trigger crate, shown schematically in Figure 3, has a height of 9U and a depth approximately of 700 mm [5]. The front section of the crate is designed to accommodate 280-mm deep cards, leaving the major portion of the volume for 400 mm deep rear mounted cards.

The majority of cards in the Calorimeter Level 1 Regional Processor Crates, encompassing three custom board designs, are dedicated to receiving and processing data from the calorimeter. There are eight rear-mounted Receiver cards, eight front-mounted Electron Identification cards, and one front-mounted Jet Summary card for a total of 17 trigger-processing cards per crate.

The Receiver Card synchronizes the input data and passes it through look-up tables to separately linearize the energies into the number of bits needed for electron identification and energy triggers. Data in parallel form is shared with the neighboring crates at 80 MHz. The entire system operates in lock step after this stage at 160 MHz. The energies are then summed in 4 x 4 trigger tower regions. The crate is built on a central "backplane" which provides data sharing at 160 MHz. Data for electron identification logic, which includes both the data, received on the serial cables and that received on inter-crate cables, are transferred to the Electron Identification cards plugged into the front-side of the ``backplane". The 4 x 4 sums are transferred to Jet/Summary card plugged into the center of backplane on the front-side of the crate.

The Electron Isolation card implements its algorithm in a custom integrated circuit. The candidate electrons are ranked and top candidates are passed to the Jet/Summary card. The Jet/Summary card sorts the electron and jet candidates in the crate to output the top four candidates of each kind on a cable to the global trigger. It also calculates sums of E_x, E_y and E_t for transmission to the global calorimeter trigger cards, which sort objects and sum energies from their inputs to obtain the final output of the calorimeter trigger which is used together with the muon trigger data to provide the final trigger decision.

3. RECEIVER CARD SYSTEM

The Receiver card is the largest board in the crate. It is 9U by 400mm. The design is optimized to forward data for further processing only at appropriate resolution and only on a need-to-know basis. Figure 4 shows the rear side of the Receiver Cards. It receives the calorimeter readout data from copper cables, and converts from serial to parallel format.

The Receiver Card receives the 8-bit non-linear E_t and 1-bit fine-grain ECAL or HCAL ID data from 32 ECAL and corresponding HCAL trigger towers for a total of 64 input channels per card. The same technology is employed for both HCAL and ECAL. Each input copper link carries 2 channels of either HCAL or ECAL data in one 24-bit frame per 25-nsec crossing. The frame contains 2 9-bit data words for the two towers, with each data word containing the 8 bits of energy and the single bit of identification information. Each frame also contains 5 bits of error detection code, which are used for error logging and to zero problem channels that can cause high spurious trigger rates. The 24-bit word is then 8/10 bit encoded, resulting in a 1.2 Gbaud serial link.

The data is brought in on 20-m non-halogenated cables of the type presently being developed for 1000Base T Ethernet. Four links are incorporated into a single cable that is connected into one of eight mezzanine cards, each of which contains a single Vitesse VSC7214 4-channel Interconnect Chip. The mezzanine cards contain circuitry for on-board cable and connector equalization. The data is already synchronized across the HCAL and ECAL and transmitted on equal length cables, so only a limited phase adjust is required. The tower geometry in the ECAL and HCAL is designed to match and the ECAL and HCAL tower mappings on the cables also match so that correlating the two calorimeters is straightforward.

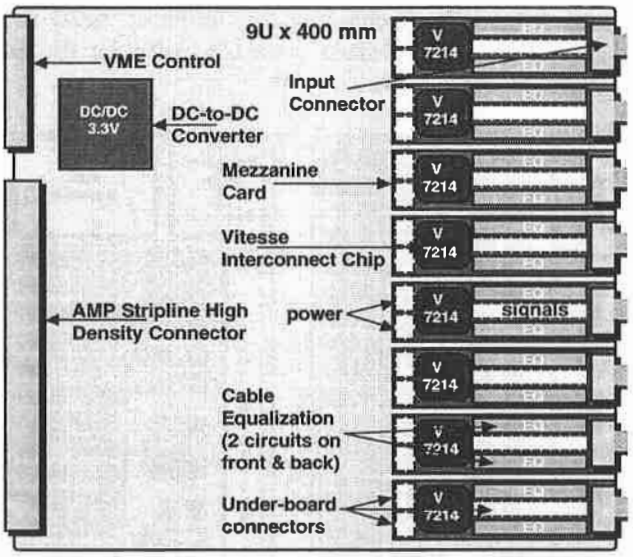

Figure 4. Rear side of the Regional Calorimeter Trigger Receiver Card.

Figure 5 shows the front side of the Receiver Card that contains the circuitry to synchronize the incoming data with the local clock, and check for data transmission errors. The data emerges from the Vitesse 7214 as 120 MHz TTL and is brought to the front side for processing by the Phase ASIC. It deskews the data, checks the error detection code, and multiplexes the data out at 160 MHz ECL. The Receiver Card then outputs an error bit for each 4 x 4 region of input towers. The Phase ASIC also provides test vectors for board and system checkout.

The Phase ASIC is designed to receive four channels of parallel data from the Vitesse Receivers. Each channel of data arrives at 120 MHz eight bits wide in 3 cycles for each 25 ns bunch crossing. This provides a 24-bit frame at 40 MHz that contains the 18 bits of data described above and 5 bits of error detection code, with one bit in reserve. A block level diagram of the ASIC is shown in Figure 6. The single clock for four channels is derived from the Vitesse Receiver. Data is transmitted from each Receiver channel along with two status bits and an error bit. The status can be used to determine whether the link is in

setup mode or data transmission mode. The input stage of the Phase ASIC is a 44 bit wide FIFO that is six frames deep. The FIFO accommodates minor phase shifts between the transmitter and local clocks. The FIFO is followed by a circuit, which sets the proper phase between the incoming data and the local bunch-crossing clock. Once properly phased, the data and error bits can be separated into 18 bits of data (two channels) and 5 bits of Hamming code. The Hamming code is recomputed from the data and compared with the received Hamming code bits. The data leave the Phase ASIC at 160 MHz in two data channels with 9 bits apiece, and one error channel, also 9 bits. The technology for the Phase ASIC is the same Vitesse 0.6 μ GaAs process as used for the Adder ASIC described below.

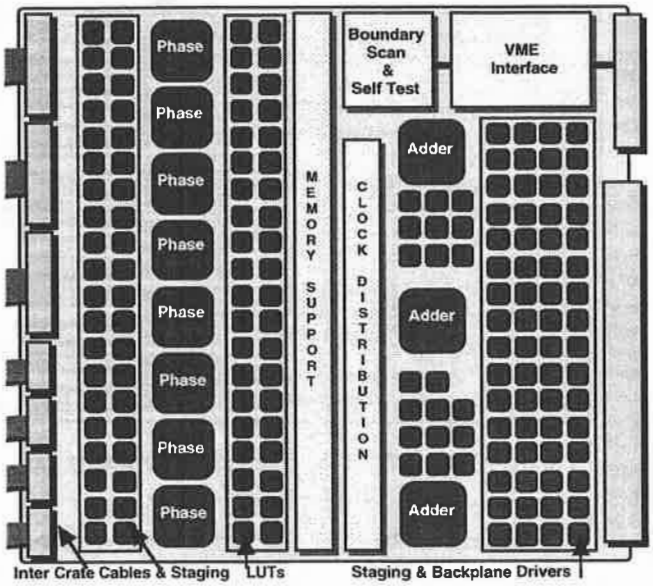

Figure 5. Front side of the Regional Calorimeter Trigger Receiver Card.

In order to achieve maximum utilization of board space, all the logic following the Phase ASIC is run at 160 MHz. This high data rate provides a factor of 4 reduction in component volume. A significant savings is also realized by placing the multiplexing circuitry, necessary to convert the 40 MHz data flow into 160 MHz, at the output stage of the Phase ASIC. After synchronization, each of the Error Detection Codes is checked against the data. If an error is detected a single bit is set, one for each incoming channel, and appended to the original EDC code. These EDCs, along with their error bits, are transmitted out of the ASIC at 160 MHz.

The rest of the Receiver Card linearizes the ECAL and HCAL E_t using 160 MHz memory lookup tables and prepares data for subsequent processing by the Electron Identification Card (EIC). It stages this information and the neighbor tower data to the EIC over a high speed point to point 160 MHz backplane described below. It also linearizes the ECAL and HCAL E_t on an 8-bit scale and uses the Adder ASIC[3] to make 4x4 sums for jet and missing E_t triggers.

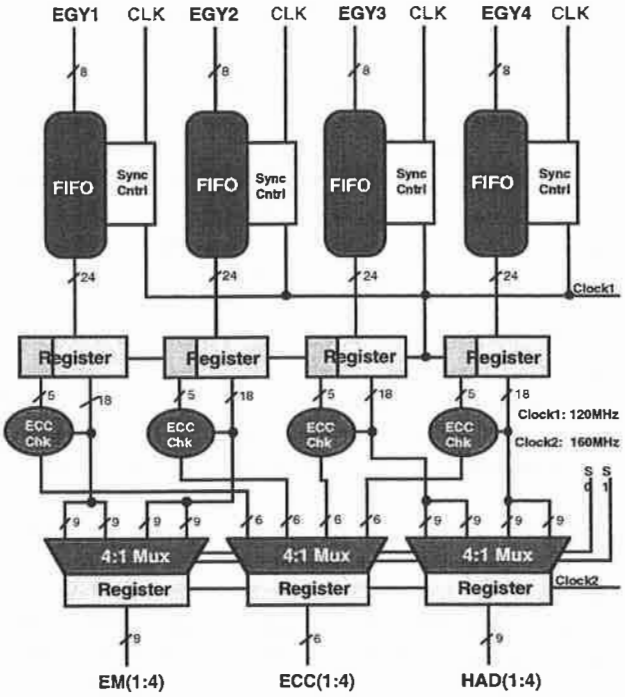

Figure 6. Block level diagram of the Phase ASIC.

The Adder ASIC is designed to add 8 11-bit numbers (including the sign) in 25 nsec, while providing bits for arithmetic and input overflows. It has been produced by Vitesse in 0.6 μH-GaAs, consists of approximately 11,000 cells, uses 4 W and has been tested to 200 MHz, considerably above the 160 MHz requirement.

The Receiver Card also ORs the ECAL fine-grain EM ID and HCAL Muon ID bits separately for each 4x4 region. It then stages the 4x4 region data to the Jet/Summary cards. There are a number of lookup tables and adder blocks on the front of the Receiver Card. The lookup tables translate the incoming information to transverse energy on several scales. The energy summation tree begins on these cards in order to reduce the amount of data forwarded on the backplane to the Jet Summary card. Separate cable connectors and buffering are also provided for inter-crate sharing. The Receiver card also has separate lookup tables to provide linearized 8-bit ECAL transverse energy, and H versus E comparison bits, for the electron/photon algorithm. These data are staged to both the cards within the crate at 160 MHz on the backplane, and to the neighboring crates on cables at 80

MHz. The prototype Receiver Card has recently been manufactured and is under test. Figure 7 shows a photograph of the front side of the completed card.

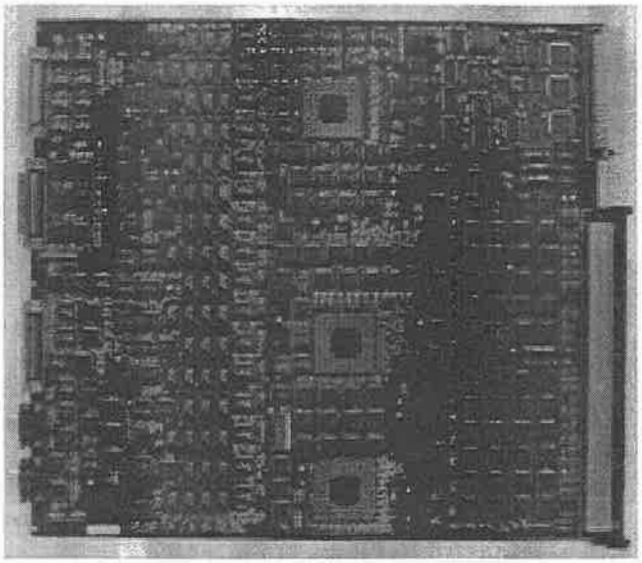

Figure 7. Photograph of the front side of the prototype Receiver Card

The backplane[6] is a single 9U-high printed circuit board with front and back card connectors. The top 3U of the backplane holds 4 row (128-pin) DIN connectors, capable of full 32 bit VME. The first two slots of the backplane use three row (96-pin) DIN connectors in the P1 and P2 positions with the standard VME pinout. Thus, a standard VME module can be inserted in the first two stations. The form factor conversion to the remaining slots is performed on the custom backplane.

The bottom 6U of the backplane, in the data processing section of the crate, utilizes a single high-speed controlled-impedance connector for both front and rear insertion. The design is based around a 340-pin connector, by AMP Inc. to handle the high volume of data transmitted from the Receiver cards to the Electron Identification and Jet Summary Cards. There are 1419 differential 160 MHz point-to-point links on the backplane between the various cards. The backplane is constructed with six ground and power planes and seven signal layers.

In order to test the feasibility of operation at high frequency we built a complete prototype backplane, which can house up to eight Receiver and Electron Isolation card pairs, a Clock card and a Jet/Summary card. The layout of this prototype backplane is shown in Figure 8. The figure shows the read side of the backplane projected onto the front, revealing both front side and rear side connectors. Results from testing clock signals on the backplane show rise and fall times of 0.8 ns from 20% to 80% height with full ECL signal levels even when measured at the farthest card slot. This performance meets the requirements of 160 MHz operation of the backplane.

4. CONCLUSIONS

The construction and test of the CMS regional calorimeter trigger Receiver Card, Backplane and associated ASICs that implement the Level-1 trigger algorithms represent and important step towards demonstrating the feasibility of the trigger design.

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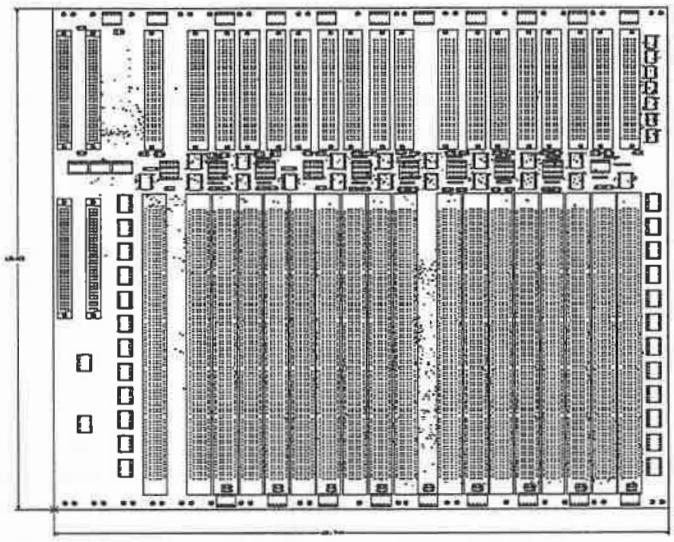

Figure 8. Layout of the backplane

5. REFERENCES

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[3] W.H. Smith *et al.*, CMS Calorimeter Trigger Implementation and Performance, *Proceedings of the Second Workshop on Electronics for LHC Experiments*, Balatonfured, Hungary, September, 1996.

[4] S. Dasu *et al.*, CMS Level-1 Calorimeter Detailed Simulation, CMS Note 1998/027, and references therein.

[5] J. Lackey *et al.*, CMS Calorimeter Level 1 Trigger Conceptual Design, CMS TN/94-284 (1994).

[6] W.H. Smith *et al.*, High Speed Data Processing for the CMS Calorimeter Trigger, in *Proceedings of the Third Workshop on Electronics for LHC Experiments*, London, England, September, 1997.