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Development of Low-Power Small-Area L-2L CMOS DACs for multichannel readout systems

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ABSTRACT: The design and measurements of 8-bit DACs based on L-2L ladder architecture are presented. The main design goals were low power consumption and low area. Such features are needed for DACs trimming parameters in each channel of a multichannel readout system. The PMOS and the NMOS based DACs are studied, for wide range of biasing conditions, in two operation modes — as a current generator and a current divider. The NMOS and PMOS prototypes occupying respectively 0.034 mm^2 and 0.043 mm^2 are fabricated in 0.35μm CMOS technology and tested. The measurements show full functionality with the maximum INL and DNL errors below 0.4 LSB. The measured DAC power consumption is about 80μW.

KEYWORDS: VLSI circuits; Analogue electronic circuits

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1 Introduction

In multichannel readout systems of high energy physics experiments digital to analog converters (DACs) are commonly used to control various parameters like discriminator threshold voltage or current/voltage bias. The systematic and the random mismatches of CMOS technologies force the use of trimming DACs to obtain a uniform channel to channel behavior in a multichannel ASIC. For these reasons a DAC with moderate (6–8 bits) resolution, a low power consumption and a small die area, is one of the basic building blocks requested in the multichannel readout system. The goal of this paper is to design 8-bit DACs conforming to these specifications.

In section 2, the operation principle of L-2L DAC, with a particular attention to mismatch and offset effects, is discussed. Section 3 describes the design of the proposed NMOS and PMOS based DACs. The measurements results are presented in section 4.

2 L-2L DAC architecture

2.1 Binary weighting principle

For any bias condition the drain current of MOS transistor is proportional to its width-to-length ratio. Based on this statement it can be shown that any series-parallel connection of identical transistors can be treated as one transistor with equivalent aspect ratio, as shown in figure 1. Since the main branches of circuit in figure 1 are equivalent the current is equally divided between the branches [1, 2].

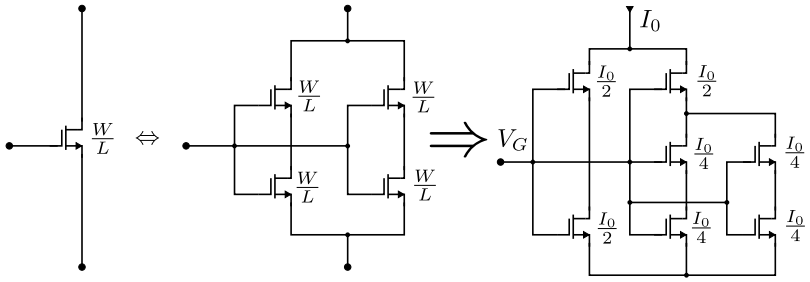

Figure 1. Principle of current division and L-2L ladder design.

2.2 Short channel effects

In modern deep submicron CMOS processes the *short channel effect* is an important factor which affects the drain current of MOSFETs. The most important short channel effect in designing L-2L ladder is the *carrier velocity saturation* (CVS). The effect becomes significant for devices with reduced channel length, for which the proportionality between carrier velocity and longitudinal electrical field vanishes (see expression (2.1)). To reduce this effect the device should work in deep linear region or should have long enough channel [2].

$$\mu_{sat} = \frac{\mu_0}{\sqrt{1+\left(\frac{\mu_0 V_{DS}}{L v_{sat}}\right)^2}} \tag{2.1}$$

2.3 Mismatch effects

The most important limitations of DAC resolution come from the mismatch effects. The mismatch is caused by the fluctuations of polysilicon shape, doping, or gate oxide thickness. Based on Pelgrom model [3, 4] the dispersion of transistor current can be written as:

- for saturation region

$$\sigma(I_d) = \sqrt{\frac{A_\beta^2}{W \cdot L} + \left(\frac{2 \cdot 100\% \cdot A_{V_{th}}}{V_{od}}\right)^2 \cdot \frac{1}{W \cdot L}}, \tag{2.2}$$

- for linear region:

$$\sigma(I_d) = \sqrt{\frac{A_\beta^2}{W \cdot L} + \left(\frac{100\% \cdot A_{V_{th}}}{V_{od} - \frac{1}{2}V_{ds}}\right)^2 \cdot \frac{1}{W \cdot L} + \left(100\% \cdot \frac{\Delta V_{ds}}{V_{ds}}\right)^2}, \tag{2.3}$$

where $V_{od} = V_{gs} - V_{th}$ is overdrive voltage.

One can see that the main way to minimize transistor mismatch is to increase the device area and/or to increase the overdrive voltage. For the devices working in linear region any variance in drain-source voltage can also seriously deteriorate the performance of current division. For this reason any input offset of amplifier, setting the potential of drain/source node, can be a serious limitation of L-2L DAC resolution.

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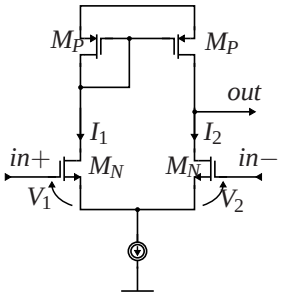

Figure 2. Circuit used in offset analysis.

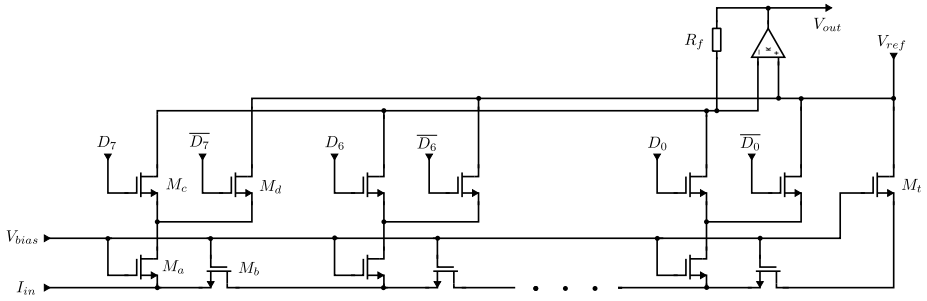

Figure 3. Schematic diagram of proposed DAC.

2.3.1 Amplifier input offset

The input offset of differential amplifier (figure 2) has two components. The first one comes from threshold voltage mismatch in the input pair, while the second from current mismatch in the load. Using the Pelgrom mismatch model one can obtain following expression for the input offset of differential amplifier.

$$V_{offset} = V_{gs_1} - V_{gs_2} \approx \sqrt{\sigma^2_{V_{th_N}} + \frac{I^2 \cdot \sigma^2_{I_P}}{gm^2_N} + \frac{V^2_{od_N} \cdot \sigma^2_{\beta_N}}{4}} \tag{2.4}$$

For the minimum offset one would need a high transconductance of the input pair working with low overdrive voltage, and a large area of the load devices working with high overdrive voltage.

3 L-2L DAC implementation

The proposed NMOS version of L-2L DAC core is shown in figure 3. A complementary circuit is implemented for the PMOS version. The proposed DAC is designed to test the L-2L architecture and can work in two different modes: as a current generator and a current divider. In the first mode the node I_{in} (see figure 3) is shorted to ground (or V_{dd} for PMOS version). For this mode the current generated by the ladder depends strongly on biasing conditions (V_{bias} in saturation region, V_{bias} and V_{ref} in linear region). The transistors M_c and M_d work as switches [5]. The default bias conditions are set in order to obtain the least significant bit (LSB) current equal 25 nA (LSB voltage step

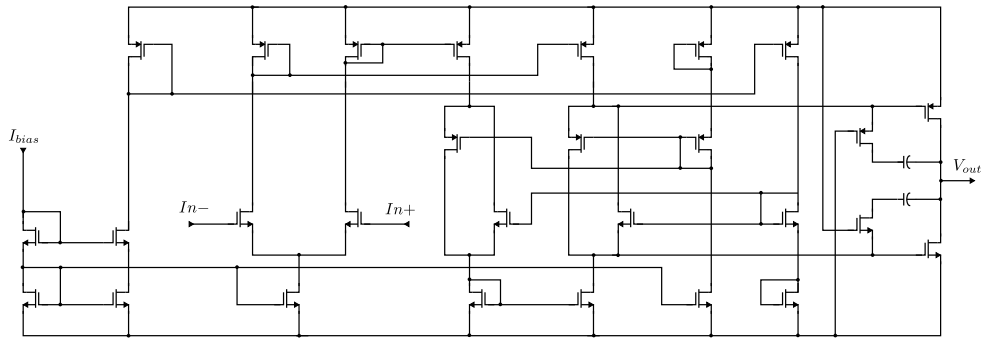

Figure 4. Schematic diagram of output amplifier.

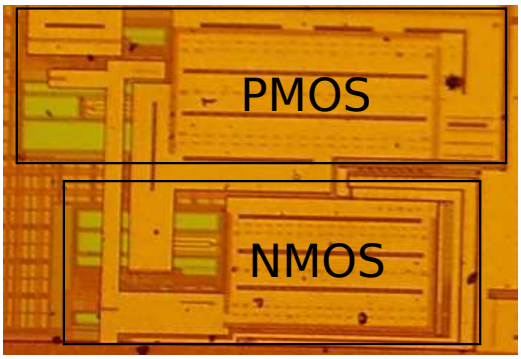

Figure 5. Micrograph of fabricated prototypes.

about 0.5 mV) what corresponds to V_{bias} about 1.2 V for the NMOS and 1.45 V for the PMOS ladder respectively. In the current divider mode the LSB current was fixed to constant value and the ladder linearity was investigated in different biasing conditions.

3.1 Output amplifier

Due to the relatively high current generated by the L-2L ladder in the current generator mode at maximum gate potential ($V_{bias} = V_{dd}$), a two stage class AB output amplifier was designed. The schematic diagram of the output amplifier is shown in figure 4. The first stage is based on an operational transconductance amplifier (OTA) while the second output stage uses the *floating current source* [6] bias. To ensure stability, a classical Miller compensation technique with nulling resistor is used. The simulated key parameters are: open loop gain 109 dB, gain-bandwidth product 2 MHz, input offset 2 mV, and noise rms 0.1 mV.

4 Measurements results

The first prototypes of PMOS and NMOS DACs were fabricated in a two-poly four-metal 0.35 μm CMOS technology. The dimensions of DAC cores are 340×125 μm^2 for the PMOS version and 295×116 μm^2 for the NMOS version respectively. The chip micrograph is shown in figure 5. The

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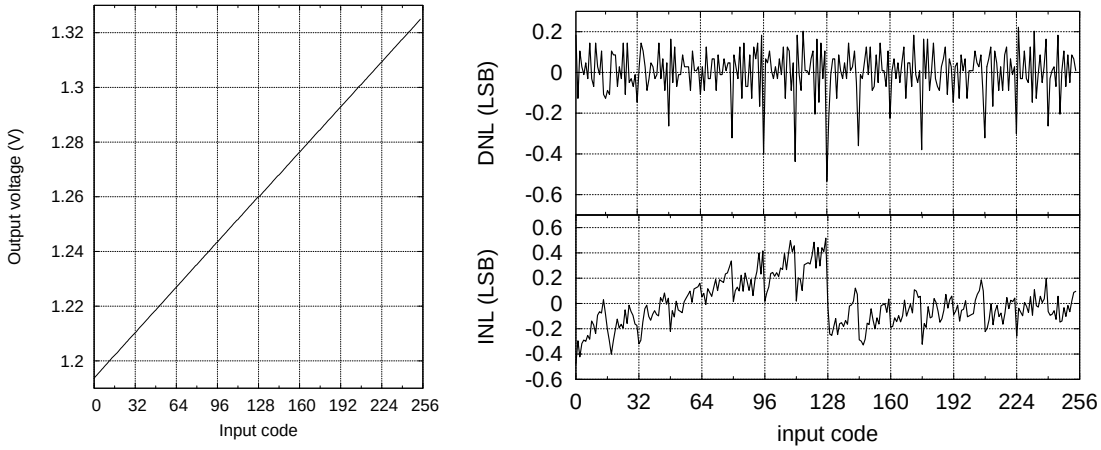

Figure 6. Nonlinearities of NMOS DAC at default biasing conditions.

measured DAC power consumption at default settings is around 80 μW. It is similar for the NMOS and the PMOS version since it comes mainly from the output amplifier which consumes around 60 μW. The DAC performance was verified over a wide range of biasing conditions in two modes of operation, as a current generator and current divider. Because of the foreseen DAC applications, only the static measurements of linearity were done. The Tektronix AWG2021 arbitrary waveform generator was used as pattern generator and the Agilent B1500 semiconductor analyzer to generate all bias potentials and to measure the DAC output voltage.

4.1 Current generator mode

In this mode of operation four DACs were tested. In figure 6 the linearity measurements, i.e. the transfer curve and the INL, DNL errors, performed for the NMOS DAC, at default biasing conditions, are presented. It is seen that both INL and DNL stay within 0.5 LSB. The NMOS DAC linearity was verified over a wide range of biasing potentials and similar INL and DNL errors were obtained. The NMOS DAC works correctly for the gate potential V_{bias} in the range 1.2-2.8 V and for the V_{ref} in the range 1-2 V. The LSB value for these biasing conditions changes from 0.5 mV (for $V_{bias} = 1.2V$) to 4.2 mV ($V_{bias} = 2.8V$) which corresponds to the LSB current range 25-210 nA.

Similar measurements were performed for the PMOS DAC version. Typical linearity results obtained at default biasing conditions are shown in figure 7. The INL and DNL errors stay well within 0.5 LSB. The measurements were repeated changing the biasing conditions, i.e. V_{bias} in the range 0.1-1.4 V and V_{ref} from 0.5 to 2.5 V, and similar INL and DNL errors were obtained. The LSB step corresponding to these biasing conditions changes from 0.5 mV ($V_{bias} = 1.5V$) to 2.2 mV ($V_{bias} = 0.1V$). These values of LSB step correspond to currents in the range 25-110 nA.

4.2 Current divider mode

The performance of the prototype DACs was also verified in the current divider operation mode. The measurements were done both for the NMOS and the PMOS DAC, in the current range 12-200 nA per LSB. In figure 8 the nonlinearity errors obtained for the NMOS and the PMOS DAC are

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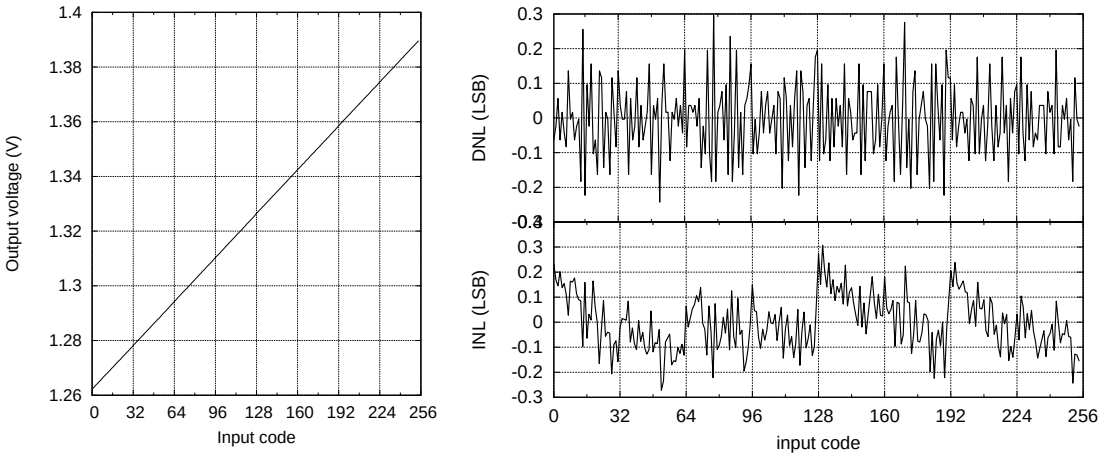

Figure 7. Nonlinearities of PMOS DAC at default biasing conditions.

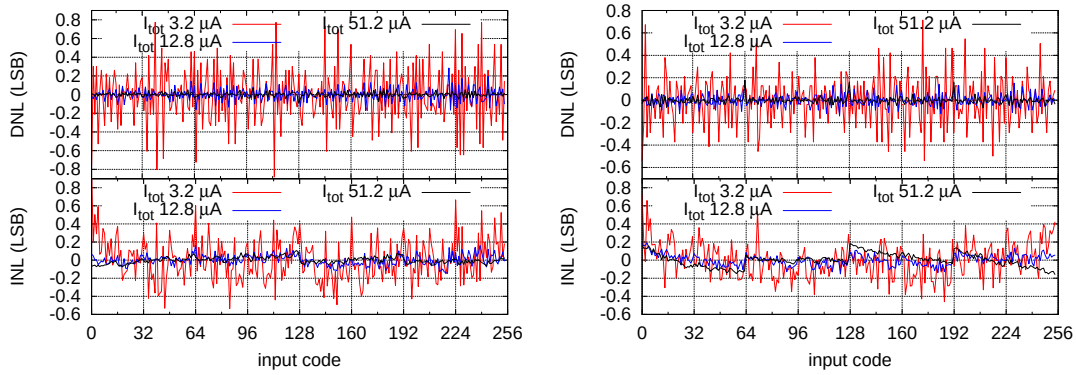

Figure 8. DAC nonlinearities in current divider mode for three value of divided current (NMOS — left, PMOS — right).

shown for different currents. It is seen that the maximum INL and DNL values are below 0.7 LSB and much lower in average.

4.3 DAC performance vs power supply

Lastly, the DAC performance was studied as a function of supply voltage. It was verified that the DACs sustain good linearity for supply voltage down to 1.7 V. Typical INL and DNL errors for NMOS DAC measured at 1.7 V supply voltage are shown in figure 9. In fact the only limitation (except the transistor threshold voltage) to scaling of supply voltage in this architecture, is the correct operating point of the output amplifier.

5 Summary

Two general purpose low power (80 μW) small size (~ 0.04 mm^2) 8-bit L-2L DACs were designed, fabricated and tested. A very good linearity was found for the NMOS and the PMOS DAC version,

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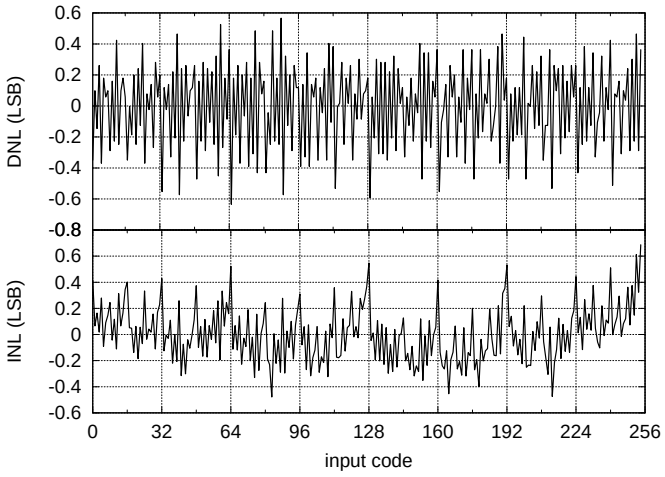

Figure 9. DAC nonlinearities for 1.7 V of supply voltage.

operating in two different operation modes, i.e. the current generator and the current divider mode. It confirms that the L-2L architecture is a very attractive choice for DACs in CMOS technologies. The obtained low power and area match well with DAC requirements in a multichannel readout system, where fine tuning of various parameters (e.g. thresholds) in every channel, is often needed. In the near future the developed circuits and architectures are foreseen to be implemented in such multichannel readout system.

Acknowledgments

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