

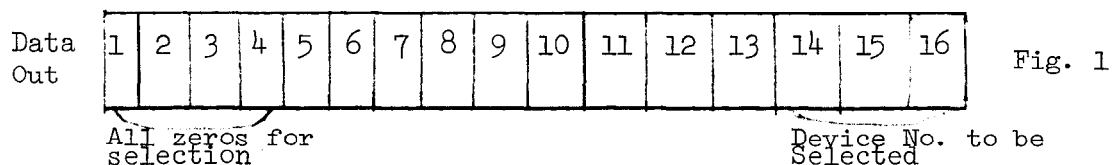
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## DEVICE SELECTOR

### General

The purpose of the Device Selector is to connect up to seven devices to the IBM 2701 Parallel Data Adapter via one common interface. It includes a computer simulator and a peasant clock.

The terms output and input are always in respect to the computer or 2701. An output or input word consists of 16 bits or two bytes of 8 bite.



A device may be selected by sending the 1st output word with zeros in the 4 most significant places and the Device No. in the 3 least significant places. One device can only be deselected by selecting another device. The following device numbers have been allocated:

No.	Device
0	No device
1	Hummingbird I
2	Hummingbird II
3	Not yet connected
4	Peasant clock
5	Display 22 1/2
6	Not yet connected
7	Switch registers

Fig. 2

### Principles of operation

There are two modes of operation: Computer and Simulator. The first switch on the right hand side of the top row is the Off Line switch. When operated it sets the Computer/Simulator FF in the simulator position if the computer WS or RS lines are not up. In this position, no data or control

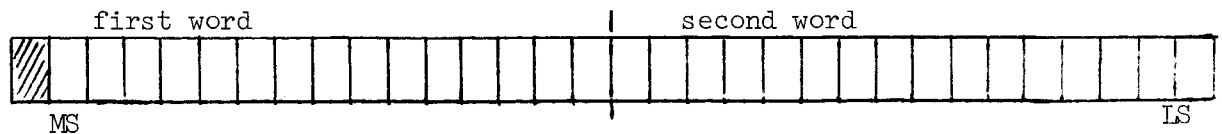


The first switch on the left hand side of the top row is the single/continuous switch. If this switch is down the simulator will stop after every OUTPUT/INPUT cycle, if up it will allow a new cycle to start. The next three switches are used to specify the number of words to be sent to a device. Up to seven words of 16 bits may be sent, that's why there are seven rows of 16 switches each. The rows are numbered 1 - 7. There are three lamps on the top row which indicate the number of words which are sent to the device. The MF switch on the right hand side should be in the up position whenever there is a Move Film operation during an output cycle. Start and "CLR" are momentary switches and operate when pushed down. To START means to initiate an OUTPUT cycle and "CLR" means to clear all registers and control FF's. Normally clear will only be used after switching on. Below the seven switch rows there are 16 indicator lamps which display the input from the selected device. In the same way the bottom row displays the output from the computer or simulator, depending which one is selected. There are more control lights displaying the control signals going to the devices. They are "RS" = Read Select, "WS" = Write Select, "RG" = Read Gated, "WG" = Write Gated, "WC = 0" (Word Count = zero), "O/P = Output Parity (this signal not used). There are also three lamps which display the number of the selected device. An example will illustrate the use of the device selector. Let us assume that we want to test the Hummingbird II. We want to scan from line zero to line 64. We accept X coordinates laying between 32 and 256. We want to move film 15 positions forward. We want to read with threshold 7 and density 2 (read every 2 lines) and do this test continuously. On fig. 3 is shown the set up to achieve this. We send seven words as follows:

Word	Hexadecimal value					Significance
1	0	0	0	2		Select HB II
2	7	0	0	0		Clear
3	2	0	4	0		YF = 64
4	3	0	2	0		XS = 32
5	4	1	0	0		XF = 256
6	5	0	0	F		MF = 15 steps
7	6	7	2	0		Threshold = 7, Density = 2

We see that it is not necessary to send a YS = 0 because the clear already takes care of this.

Device No. 7 is the simulator itself. Upon selection the contents of the 7 switch rows may be read. In this case the number of rows to be read are specified by the three switches marked WORDS TO SEND on the top row. Device No. 4 is the so-called Peasant Clock. Like No. 7 the only output to the device is the selection word. The clock itself consists of a 31 bit 100  $\mu$ s counter. This counter can be read by two input words as follows:



The output cycle resets the word selection "FF", so that the first read order will get the most significant part first with a zero in the sign position.

## Technical Description of the Device Selector

The Device Selector input consists of 16 Output-Data lines + Parity and 5 Control lines from the 2701 Parallel Data Adapter. An Output line is true, when at +3v and false, when at 0v. DEC W 520 Comparators have been used for levelconversion. See Fig. 4 for the Output logic. The outputs of the levelconverters are the inputs of 'and' gates, which are enabled when the keyswitch on the control panel is in the Computer position. If the position of the switch is the Simulator, another set of 'and' gates are enabled, which have Output Data and Control Signals from the Simulator at the inputs. The outputs of both gate sets are 'or-ed' together. The 16 Data lines are connected to Bus Drivers (R 650), the output from the drivers is going to all the Devices, which are connected. Some of the data lines are used in the Device Selector itself, which will be explained later.

The Output Control signals are: Write Select (WS), this signal is true (down) as soon as the computer starts the Output cycle and remains true during the whole cycle.

Write Ready (WR) only goes true, when data is available at the 16 Output-Data lines.

Wordcount=0 (WC=0) goes true after the computer has sent the last Output word, but strangely enough the WR also goes true during the WC=0. We 'and' the WS, WR and  $\overline{WC=0}$  in the Device-Selector. The result of this operation is called Write Gate (WG).

The Input Control signals are: Read Select (RS), similar to the WS. Read Ready (RR) only goes true, when the computer is ready to accept data from the device.

WC=0 is also used during the Input cycle, it goes true when the computer cannot accept any more data, but the RR goes true at the same time. We 'and' RS, RR and  $\overline{WC=0}$ . The result of this operation is called Read Gate (RG). WG, RG and WC=0 are connected to all the Devices via Bus Drivers.

We know that a Device may be selected by the first Output word, when this word has zeros in the 4 most significant places and the Device # in the 3 least significant places. (see General Description). The selection takes place in the Selection Decoder (see Fig. 4), which consists of 3 FF register, which is sampled only during the presence of the first Output word, and a Decoder with 8 Outputs of which 7 are used (Device 0 does not exist). The 7 Outputs are the Selection Signals (SEL 1-SEL 7), which are connected to the Devices via Bus Drivers. ( Except for Device # 7, which is a part of the Simulator as we will see later)

The Input logic is shown on Fig.6. It consists of 7 rows of 'And/Or' gates of 20 gates each ( DEC RL41's are used ). One row consists of 16 Data signals and 4 Control signals from one Device. One row has only Data signals (Device # 7). There are also 4 Control signal inputs from the Control-panel (see Fig.3) The Outputs from all 'And/Or' gates is fed into 20 Level Convertors which convert the DEC levels of -3v and 0v into IBM levels of +3v and 0v ( DEC WO61's are used ). The inputs to the Level Convertors are 'And' gates. One input of these gates is only true when the Computer/Simulator FF is in the Computer position.

The Timing of the Output and Input Cycles is shown on Fig.5.

### Technical Description of the Simulator

If the Computer/Simulator FF is in the position Simulator no Data and Control signals can go to the Computer. Thus the computer is completely isolated.

The Simulator itself consists of a Control signal generator, a Word generator and a Word selector. (See Fig. 7.)

The Control signal generator consists of 4 FF's, every output represents one of the Control signals: WS, WR, RS, RR.

The Word generator consists of 7 rows of 16 switches with relative logic. Each row represents one Output word.

The Word selector allows only one row to be selected at one time.

It consists of a three bit counter and a binary to octal Decoder.

If the counter is zero the 1st switch-row is selected.

The output of the counter is also compared with the output of a three bit switch-register on the Control-panel (Words to send).

This comparator will produce the  $WC = 0$  signal upon coincidence.

When we push the CLR switch on the control-panel, the counter and the Control FF's will be reset. If we now push the START switch the Simulator will initiate an Output cycle. Both WS and WR will be set and the selected Device may take the Data from the first row. The WR will be reset by a DD signal from the Device, the same signal will advance the counter of the Work-selector by one, and the WR will be set again 2.4 usecs later (this delay is based upon the Computer delay between consecutive words). This sequence will go on until the counter has the same value as the switch-register when a  $WC = 0$  will be sent. The EOR signal from the Device will reset the WS FF after a delay of 180 usecs (the only significance of this delay is that it creates a waiting period before the Read cycle starts). The WS going to zero will set the RS FF in the case that the Move Film switch (MF) on the control panel is in the normal down position. If this switch is up, the RS FF can only be set by the Interrupt from the device, which only happens after a Move Film instruction has been sent to one of the scanners. The

RS going to one will set the RR FF. This FF will be reset by a DD signal from the Device.\* Like during the output cycle this FF will be set again 2.4 usecs later. The same will happen when the next DD signal comes. The input cycle can only be terminated by the Device EOR signal, which will reset the RS FF after 180 usecs. The RS going to zero will set the WS FF in the case that the Single/Continuous switch (S/C) is in the normal down position. If this switch is up, the WS FF can only be set by pushing the START switch on the control-panel. It means that in this case there will be one Write and one Read cycle, every time we push the START switch. Finally an End of File signal from the Device will reset the WS FF. (See Fig. 7.)

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\* The data coming from the Device is not fed into the Simulator, it is only displayed in a set of 16 lamps on the control-panel.



## ENGINEERING NOTE

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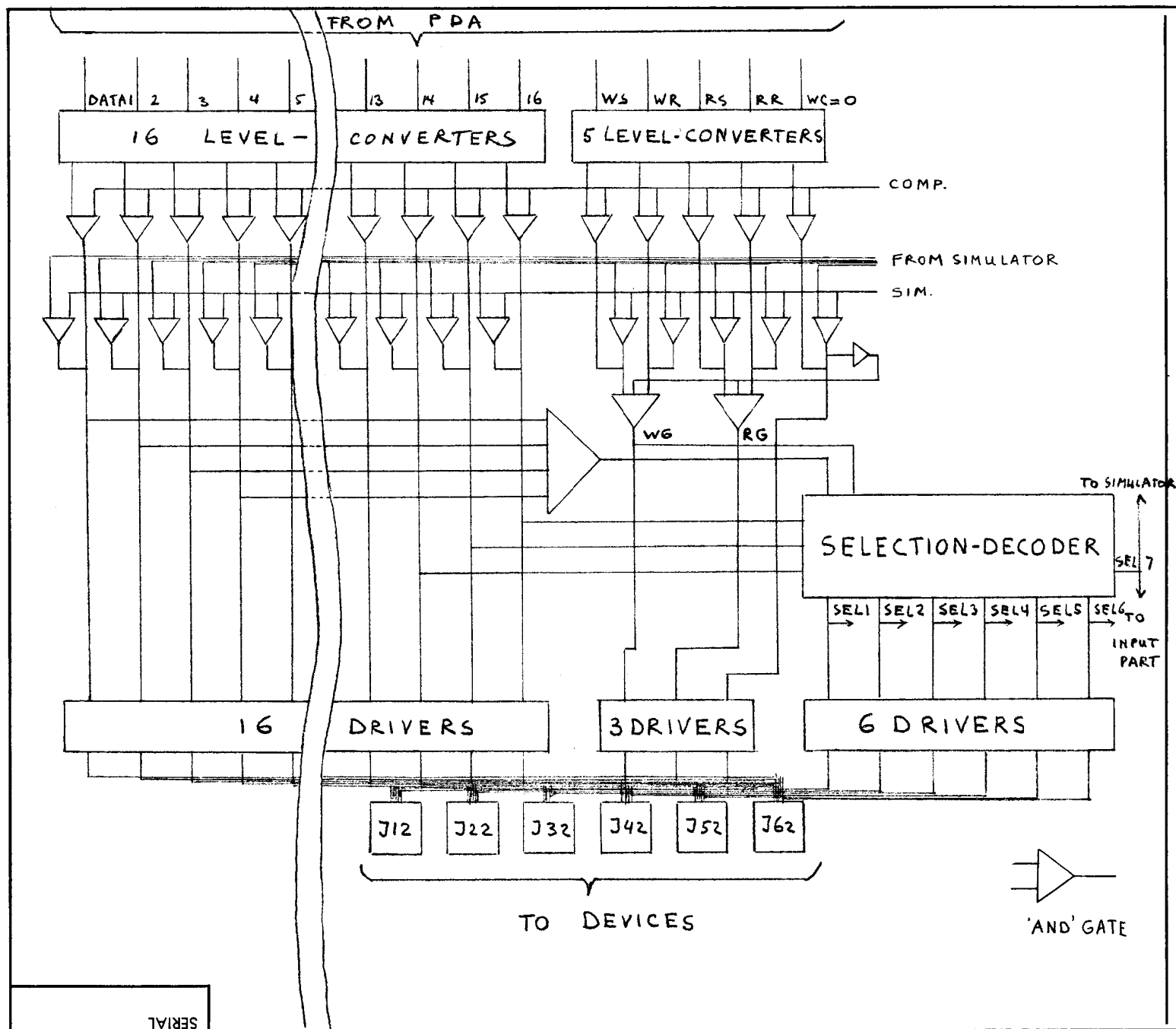
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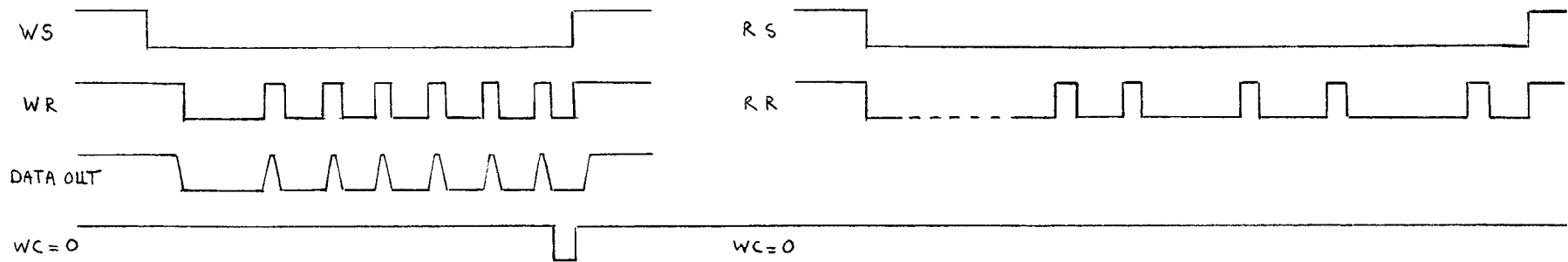
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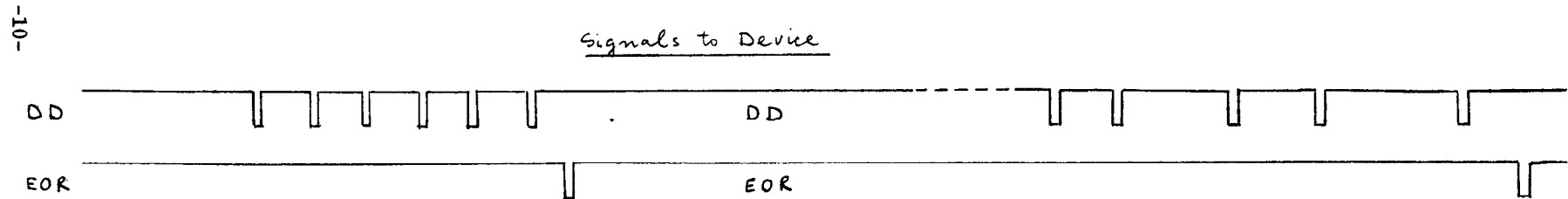
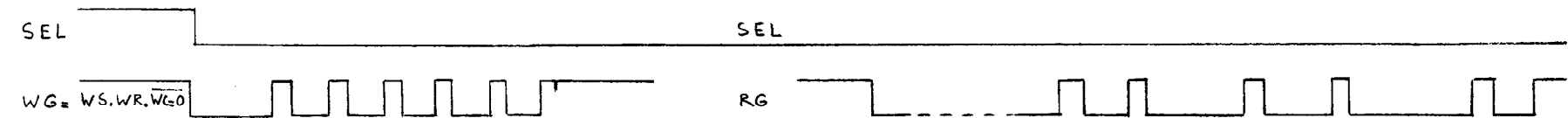
PROJECT-JOB Device Selector

TITLE Fig. 4





Signals from Computer PDA



Signals from Device

WRITE

READ

↔  
5μS

TIMING DIAGRAM DEVICE SELECTOR  
INTERFACE

Fig.5

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TITLE Fig. 6

