Development of a Technological Prototype of Silicon-Tungsten Electromagnetic Calorimeter for ILD

Vincent Boudry[*] **on behalf of the ILD SiW-ECAL development group**

Laboratoire Leprince-Ringuet - École polytechnique, CNRS/IN2P3
Palaiseau, F-91128 France
E-mail: Vincent.Boudry@in2p3.fr

The specific conditions of the International Linear Collider offer perfect conditions to use improved reconstruction techniques, based on Particle Flow Algorithms. They require Highly Granular Calorimeters. Recent advances in Monte-Carlo simulation, integrated electronics, large composite structures associated with the power-pulsed working mode of the collider allow for high-density, triggerless, almost dead-zone free calorimeters. The R&D efforts concerning the Silicon-Tungsten option of the ILD experiment near the ILC will be here summarised.

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[*]Speaker.

1. Introduction

1.1 ILC & ILD

The International Linear Collider (ILC) is an electron-positron accelerator whose construction is nowadays being envisaged in the North of Japan. Despite high centre of mass energies ($250 - 500\,\mathrm{GeV}$ in stages, upgradable to $1\,\mathrm{TeV}$) and high luminosity ($0.8 - 3 \cdot 10^{34}\,\mathrm{cm^{-2}s^{-1}}$), the environment is relatively background free. The main one – pair production – being easily canalised in the beam pipe by a high magnetic field. As the beams will be pulsed at $5\,\mathrm{Hz}$ in short trains of $1300 - 2600$ bunches with a comfortable separation ($350 - 700\,\mathrm{ns}$ for a total length of $1\,\mathrm{ms}$), it was decided to develop high-granularity calorimeters integrating a fully embedded readout electronics with local zero-suppression, local storage and delayed readout. To avoid thermal dissipation it should run in power-pulsed mode, with a typical duty cycle of $1\,\%$.

1.2 Constraints on the detectors

The typical physics channels exploited, be they Higgs or top quark production, will generate jets of energies between 40 and $100\,\mathrm{GeV}$. As a touchstone for performance evaluation of various detectors and reconstruction software options, the separation of events with pairs of WW and ZZ was selected. In practise, a single Jet Energy Resolution (JER) of $\sigma(E_{\mathrm{jet}})/E_{\mathrm{jet}} \lesssim 3.8\,\%$ is required. This about a twice a good as the performance reached with the LEP detectors [1].

One innovative way to achieve this goal is to use the Particle Flow Algorithms (PFA) [2], in which every particle in a jet is individually reconstructed and measured using the best information available: tracks for charges particles ($65\,\%$ in energy of a typically jet), ECAL for the photons ($25\,\%$), and the calorimeters for the neutral hadrons, $\mathrm{h^0}(10\,\%)$. Using the complete PFA framework PandoraPFA [3], it has been demonstrated [4] on fully simulated data samples that this goal can be obtained using:

- a state-of-the-art TPC with a resolution of $\delta P_{\mathrm{T}}/P_{\mathrm{T}} \sim 5 \cdot 10^{-5} P_{\mathrm{T}}$,

- a precision vertex detector ($\sigma_{x,y,z} \sim 10\,\mathrm{\mu m}$) and

- Electromagnetic and Hadronic Calorimeters (ECAL and HCAL) with average single particle resolution ($\sigma E_\gamma / E_\gamma \sim 16\,\% / \sqrt{E_\gamma}$ and $\sigma E_{\mathrm{h^0}}/E_{\mathrm{h^0}} \sim 50\,\% / \sqrt{E_{\mathrm{h^0}}}$).

This requires in turn to separated the contributions of individual particles in calorimeters, making them imaging or highly granular devices.

1.3 Imaging Calorimetry

With nowadays technology a 1000 fold increase in granularity w.r.t. current standard calorimeters (such as e.g. the ones in the LHC experiments). A gain by a factor of two in JER w.r.t. to pure calorimetric measurement has been obtained. Advanced software techniques might allow to even go further (see the contribution by N. v. d. Kolk at this conference).

Practical imaging calorimetry in a full size detector such as the ILD brings many challenges combining:

- Mechanics to provide modular self-supporting structure with minimal dead materials, deformations and non-homogeneity;

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- (Micro-)Electronics to provide reliable low-noise, low-power Very Front End (VFE) readout chips (ROC) fully embedded in the detectors, over large surfaces;

- Instrumentation to provide high quality, yet not too expensive, sensors;

- Thermics for the proper self-cooling of the devices.

The entanglement of those aspects requires an iterative procedure of prototype building, testing and improvement, with a constant vigilance on physics performances, cost, quality and industrialisation issues. Last but not least the performances can only be assessed using PFA algorithms, and are as such a non-trivial combination of hardware and reconstruction software.

1.4 The Si-W ECAL of ILD

The CALICE collaboration[1] main purpose is to foster the R&D on imaging calorimeters, by sharing experience and means to develop and test prototypes and techniques. Among various options kept for the ECAL of the ILD experiment, the Silicon-Tungsten ECAL (SiW-ECAL) is the most compact and advanced one. It features large highly-resistive Silicon PIN diodes, finely segmented ($5 \times 5\,\text{mm}^2$), directly glued on PCB's holding the ROC. The PCB's are stitched together by glued flat connectors. Sided by a Kapton film carrying the High Voltage (HV) on one side and by a Copper thermal drain on the other side, they are assembled on both sides of an H-shaped support holder composed of a Tungsten core wrapped in a carbon fibres. Such a structure is dubbed a SLAB. Up to 15 SLAB's (for 30 sensitive layers) will be inserted in a large ($140 - 180 \times 90 \times 30\,\text{cm}^3$) composite Tungsten-Carbon Fibre structure, ensuring a total of 24 X_0.
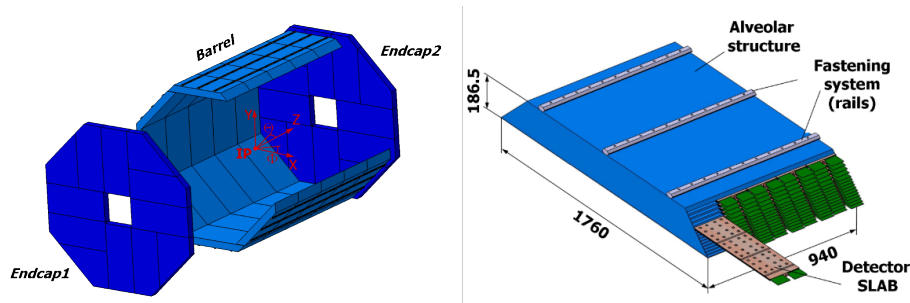
Figure 1: Structure of the ECAL in ILD (Left); Holding structure of the SiW-ECAL in the barrel (right).

1.5 The Prototypes of Si-W ECAL

A so-called *physical prototype* was build in 2005, and extensively tested in beam test campaign until 2011. This device strongly inspired the PAMELA satelite [5].

A second prototype is being build; as a technological test-stand, it will fully integrate an embbeded electronics, using the SKIROC2 analogue/digital ASIC [6, 7] featuring auto-triggering, a 14-bit signal dynamics, partial zero suppression, a memory for 15 events and power-pulsing for 64 channels. The pixel size will be $\sim 5.5 \times 5.5\,\text{mm}^2$ inside a tower of 15 single layered SLAB's. One of the SLAB will be a long one to test the readout over large surfaces, wile all the other ones

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[1]https://twiki.cern.ch/twiki/bin/view/CALICE/WebHome

will be instrumented only over a surface of $18 \times 18\,\text{cm}^2$. Beside the validation of the techniques used, its building will also help to establish procedures and develop preliminary semi-automated test benches for mass production.

Among all the aspects addressed by the technological prototype, recent advances were reached in Thermic & Mechanical studies, in the preparation of the assembly of elements, in the Silicon wafer optimisation and finally on the optimisation of global parameters. Those 4 items will be described in this article. The Acquisition and VFE Electronics aspects are detailed in F. Gastaldi and Ch. de la Taille contributions to these proceedings.

2. Thermal & Mechanical studies

Barrel structure model: A complete prismatic composite Tungsten–Carbon fibre structure similar to the one designed for the barrel of ILD has been realised in December 2011. It features 3 rows of 15 alveoli (see fig. 2). The last 5 are thicker to accommodate SLAB's with a double amount of Tungsten (4.2 mm) w.r.t. the first 10 SLAB's (2.1 mm). The same amount of Tungsten is found between the alveoli in the two sections.

Its dimensions ($55.2 \times 149.1 \times 20.5\,\text{cm}^3$) and weight ($\sim 700\,\text{kg}$) are close to the ones of the ILD (between 60 % to 95 % depending on the final dimensions). The building process has been from the start-on designed for industrialisation: the Carbon-Fibre alveoli are produced with a single dimension, then cut to fit in the mould and assembled with the Tungsten plates in an autoclave under vacuum. This structure will be used as a support for the technological prototype to be tested in beams.
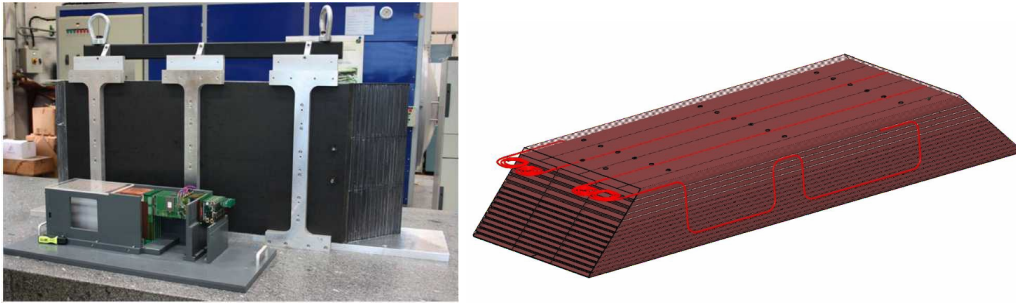

Figure 2: Structure for the ECAL prototype with a stack of short SLAB's (left); CAD design of barrel structure with the FBG (right).

Metrology: Some of the alveoli and the structure have been equipped with Fibre Bragg-Grated (FBG) to measure their deformations. The deformation of the single alveolus under transversal stress has been properly reproduced by finite element analysis (FEA). The metrology using 3D measuring arm machine (FARO) of the structure has show a small deformation (max: 5.28 mm) at the centre of the upper part of the structure. This point will have to be improved for final production.

ILD ECAL: In ILD the ECAL barrel has the form of a solid octagonal cylinder. The 8 staves are composed of 5 modules, hold by 3 rails onto the HCAL. Each modules (corresponding to one Tungsten-Carbon structure) contains 5 towers of 15 SLAB's (equipped with Scintillator or Silicon

sensors). In the current design (as described in [8]) its internal radius is $R_{\text{min.}} = 1808\,\text{mm}$, its external one $R_{\text{max.}} = 2020\,\text{mm}$ for a half-length of $Z_{\text{half}} = 2348\,\text{mm}$. These numbers might be reduced by 20 to 30 % after optimisation, as well as the number of towers and layers. Extensive FEA calculus have shown a maximum deformation of the loaded structure below 0.1 mm. The
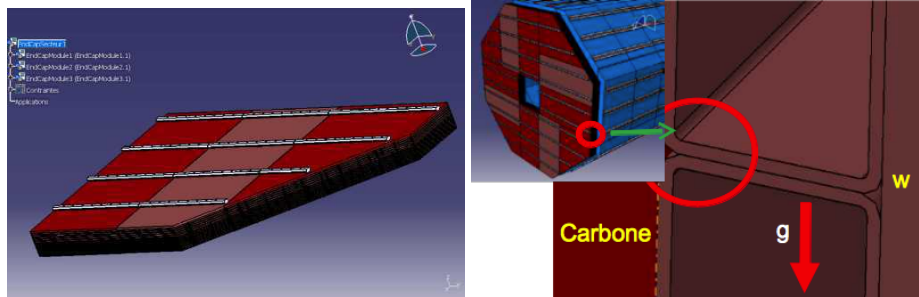
Figure 3: Structure of the ECAL Endcaps in ILD (Left); Region of maximal constrains in the holding structures (right).

Endcaps are composed of 4 quarters, around a central square aperture with a side length of 800 mm, each segmented in 4 Tungsten-Carbon fibre structures holding 4 towers.

Endcaps alveoli study: The alveloli of the ECAL Endcaps are for many aspects more challenging than the barrel ones: longer structure and SLAB's (up to 250 cm long), working under a maximal transverse constrains due to the weight and seismic vibrations (tuned for North Japan). An extra ply in the structure would increase the dead gaps between two SLAB's, which might be avoided by a better estimation of the constrains.

Recent improved FEA calculations[2] have been performed on the wall of the alveoli: they have indicated a maximum displacement below 0.1 mm for a constrain below 160 MPa. They have been compared with shearing test on specimen realised using the standard procedure. They were tested in monotonic charge and discharge, then to the breakdown.

Preliminary results hint a safety margin of ~ 3.2 with respect to the stress induced on the largest module (2.5 m – 25,5 kN), which might not be enough to handle the "seismic issues" (as presented at the ILD'13 meeting in Krakow [9]). Fatigue and progressive shearing measurement shows a reduction in stiffness which is predictable during the integration phase. It will require to keep deformation below 0.35 mm or to increase the number of plies of each alvealus.

Many studies are still needed: to improve the cohesion (e.g. extra inter-coat adhesive layer w.r.t. the barrel, optmisation of the draping for long moulds, ...), to test a compete structure (destructive tests of demonstrator of the barrel module), to simulate a complete endcap structure and reevaluate of the impact of the dead zones on physics.

Thermal studies: With a duty cycle of 1 % such as allowed by the ILC running mode, existing VFE electronics (SKIROC2) yielding 0,205 W per Wafer and a dedicated (still to be designed) interface electronics at the end of each slab radiating 0.3 W, one expects a total consumption of the ECAL barrel of $\sim 4.5\,\text{kW}$. Thermal simulations have shown that an internal passive cooling with a heat sink at the readout end of the SLAB's could hold up-to 10 times the heat load. With the design

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[2]using ANSYS APDL, SAMCEF and ANSYS ACP.

close to the current one, an isolated ECAL barrel module would experience a thermal gradient of $\Delta T = 2.2\,^{\circ}\mathrm{C}$ and an Endcap module of $\Delta T = 6\,^{\circ}\mathrm{C}$.

3. Assembly: Quality tests & preparation of large production

The feasibility a Highly-Granular Calorimeter depends largely on a conception allowing the mass production of high quality elements. Depending on the final dimensions of the detector (being re-discussed) a complete ECAL in ILD would feature up-to 64 modules of 30 layers, for a grand total of 9,600 SLAB's, 75,000 sub-units, 300,000 Silicon wafers (for $\sim 2500\,\mathrm{m}^2$), 1.2M chips and 77M electronic channels. Hence, a great care has been taken in the design for all items to increase the use of replaceable elements and allow quality checks before and after every assembling operation. As an examples the barrel structure is made of identical alveoli cut at the right dimension before assembly and the SLAB's are mostly made of identical and interconnected Active Sensor Units (ASU) holding the electronics on one side and the Silicon sensors on the other one (see fig 4).
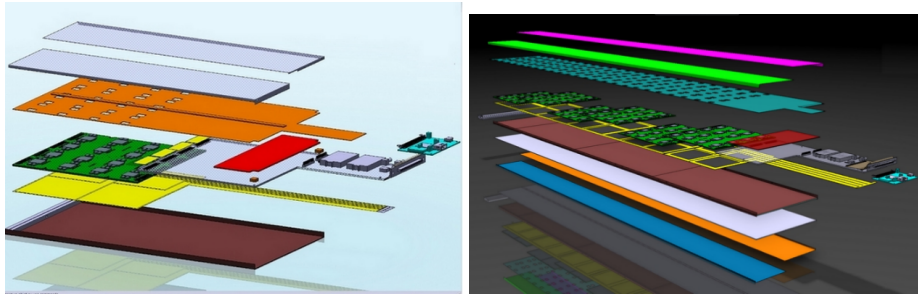
Figure 4: Left: Exploded view of a short SLAB (holding a single ASU); an H- (or U- for prototyping) shaped cradle made of W plates wrapped by Carbon fibres supports the ASU (Green PCB with yellow Wafers glued on them) connected to a terminal adaptor board (SMB, in Grey) carrying the power-buffering elements and interfaces. A thermal drain made of Copper (Orange) and a thin shielding (top) protect the sensitive elements. The bias voltage is brought by a long Kapton film. Right: View of a long slab with 7 ASU's interconnected by flat Kapton films.

ASU design: The VFE ASIC's will be tested using standard micro-electronics techniques after encapsulation as well as the PCB's.

The PCB's design is being finalised after a long process of trial and error approach. The 8th version featuring 4 BGA-packaged chips (256 channels) was used for a testbeam in 2012 [10] and allowed to validate most of the design. The 9th version allowed to test the readout of 16 chips and 2 options of clock distribution. It displayed a good flatness (needed to avoid stress on the Silicon wafers). At the time of writing electric tests are on-going. Version 10 will be the final version to be produced for the prototype and testing in beam in 2015. It is 1.2 mm thick and accepts thinned version of the BGA-packaging.

Meanwhile development on the original – more aggressive – design of the PCB's continues: aiming at having bump-bonded chips onto the PCB's, it is mechanically challenging. An improved version will soon be produced.

The interconnection format to other ASU's and to the adaptor board has been thoroughly tested. It was verified that in a strong magnetic field (2 T) the power-pulsing operation had no significant effect on the contact resistivity [11].

ASU test bench: A versatile test-bench has been realised which allows to validate a complete PCB (1024 channels) with or without Silicon wafers. A PVC platform holding a SMB card connected to the DAQ system is extruded to leave space optionally for a HV Kapton film and wafers, a thick PMMA[3] fastening up to 1024 test probes using calibrated springs, and shielding. The PCB to-be-tested comes on top in contact with the array of springs, with a monitored force. It is connected to the SMB by mechanical contacts.

The device has been designed to serve as well as a R&D station, as a basis for the qualification of the PCB for the prototype and as basis for later mass-test bench for the ILD-ECAL.

Gluing station: The gluing of 4 wafers onto a PCB is done by depositing calibrated dots of conductive glue on every readout pad. It is a complex process which involves the global and local flatness of the board, for the correct estimation of the amount of glue needed. The parallelism of the edges conditions the positioning of the wafers (the goal is $\sim 100 \, \mu$m).

After a semi-automated positioning and gluing tested on the ASU's used for the 2012 beam tests, the gained experience translated into improvement on the use of specific pumps for a dry and clean vacuum, on cleaning of the PCB and a differentiated positioning of the glue dots at the edge of the PCB to prevent short-cuts. A fully automated chain combining the dot deposition and wafer positioning is under conception, to be completed by a readout test bench to characterise the newly formed ASU's.

Assembly Bench: Finally the ASU's have to be assembled into full SLAB's. The development of a set of specifications to assure proper assembly of ASU's (Tolerances of PCB, H or U cradle) is being defined: as an example mechanical stress on wafers during interconnections is been investigated.

Two stations are being investigated: one for the interconnection, the second for the assembly. They will be be combined and automatised.

4. Wafers

The silicon sensors, high resistivity $(3 - 4 \, \mathrm{k\Omega m})$ PIN diodes, are the basis unit the ECAL: in term of total cost (for about one half), but primarily for its dimension, so as to maximise the yield of square wafers drawn from cylindrical ingots[4]. The sensors are segmented in an array of cells, with dimension ranging from $10 \times 10 \, \mathrm{mm}^2$ for the physical prototype to $5.5 \times 5.5 \, \mathrm{mm}^2$ for the technological prototype. The size and number of cells is adjusted to the dimension of the wafer and the capacity of the readout ASIC's. The "Guard Rings" (GR) are structures implemented near the edge of the sensors to gradually dampen the bias voltage and avoid leakage currents (or breakdown) through the defects of the edges. It was discovered during the beam test of the physical

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[3]Poly(methyl methacrylate)

[4]Whereas an hexagonal shape would optimise this yield, a square shape is preferable in terms of mechanics, reduction of dead space and mass production of the components.

prototype of the ECAL with high energy electrons, that a percent coupling between the guard ring and the readout cells resulted in so-called "square events", in which all the peripheral cells were responding.

An R&D program [12] is on-going on the GR aiming at reducing the peripheral dead-zone, limiting its coupling to external cells, and provide a non-proprietary techniques to open-up the wafer-producer park. The use of segmented GR to reduce the capacitive coupling and of "edge-less" techniques are investigated. These studies are mainly done in the scope of the French-ANR[5] program CALIIMAX in relation with Kyushu U. and Hamamatsu (HPK) as well as with various European producers.

Recently a batch of sensors without GR, thanks to laser edging, and slightly higher resistivity was provided by Hamamatsu. The dimensions and layout (surface of $90 \times 90 \, \text{mm}^2$ segmented in 256 cells of $5.5 \times 5.5 \, \text{mm}^2$ for a thickness of $320 \, \mu\text{m}$) are identical to the old one. Capacity-Voltages (C-V) curves show a lower bias voltage ($30 \, \text{V}$ vs. $65 \, \text{V}$) needed to stabilise the capacitance. From Intensity-Voltage (I-V) measurements, reduced absolute leakage currents ($31 \, \text{nA}$ vs. $48 \, \text{nA}$ for $120 \, \text{V}$ bias voltage were found. Thanks to earlier stabilisation a lower bias voltage could be used, yielding leaking current of $21 \, \text{nA}$ at $60 \, \text{V}$. More details can be found on Tatsuhiko Tomita's poster at this conference.

Several designs of segmented GR have been realised and implemented on so-called baby wafers ($\sim 3 \times 3 \, \text{cm}^2$ segmented in an array of 3×3 cells). To test the coupling of the GR with the border cells, charges are injected in the bulk in a corner of the wafer with the help of a pulsed Nd:YAG laser ($1064 \, \text{nm}$, $1.5 \, \text{ns}$) focused on a $20 \, \mu\text{m}$ spot. The cells are readout by a dedicated DAQ system. Whereas for 1 GR design, the signal more or less scales with the length of the outer rim of the cells (i.e. corner cells receive twice as much as side cells, except for the cell opposite to the injection spot), the segmented GR show a very strong relative reduction of coupling. A future batch of baby wafer will feature meshed electrodes on the pixels (now fully metallised), so as to allow charge injection – and calibration – inside a pixel.

A second laser test bench is now available with similar characteristics (wavelength of $1056 \, \text{nm}$, $1 \, \text{ns}$ pulse width) injecting the equivalent of 700 MIP. It is mounted on a flexible test bench allowing the readout of a free standard-sized wafer connected by an array of springs to a prototype PCB and acquisition. Preliminary results show a coupling between 0.4 to 0.5 % for side cells. It scales with the length of the rim: doubled for corner cells and double-sized ones, quadrupled for double-sized corners ones. The system will be improved to reduce noise and PCB bending (preventing now all channels to be connected).

5. Issues & near future:

The DESY test beam of the current set-up allowed to demonstrate an excellent potential, e.g that a signal/noise ratio (MPV of MIP signal / noise dispersion) of up-to 14 is feasible. It was also very useful to reveal several issues: frequent post-triggering of the ASIC's, some noisy channels, lack of external triggering, a small non-linearity. The charge injection on test bench also showed some dispersion of the signal w.r.t. the memory depth in the ASIC's. All these effects are now

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understood and will be solved or improved by the next version of the PCB's, either by changing the routing or better decoupling.

The technological prototype will be completed in 2015 and tested that year with high energy beams.

6. Acknowledgements

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