Characterization of a new HV/HR CMOS Sensor in LF150nm Process for the ATLAS Inner Tracker Upgrade

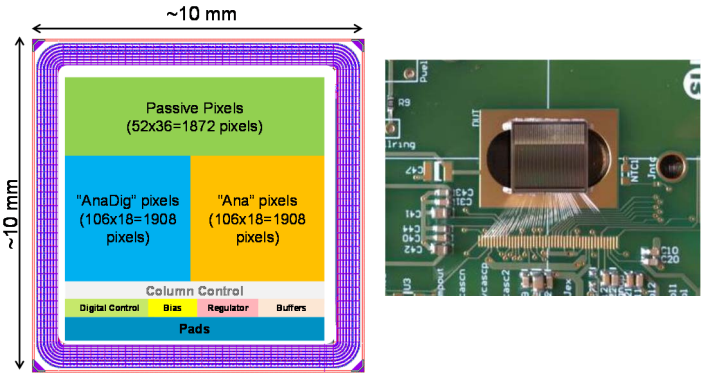
Y. Degerli, *Member, IEEE*, F. Balli, M. Barbero, S. Bhat, P. Breugnon, Z. Chen, M. Elhosni, S. Godiot, F. Guilloux, C. Guyot, T. Hemperek, T. Hirono, F.J. Iguaz, H. Krüger, M. Lachkar, J. Liu, J.P. Meyer, A. Ouraou, P. Pangaud, P. Rymaszewski, A. Rozanov, P. Schwemling, M. Vandenbroucke, and N. Wermes

***Abstract*–A HV/HR CMOS detector prototype called LF-CPIX, has been designed in LFoundry 150nm technology. The front-end electronics has been implemented using both NMOS and PMOS transistors, inside the charge collection diode, with a pitch of 250 µm x 50 µm. This demonstrator is an implementation of a matrix of smart pixels where the diode is composed by a Deep Nwell, and P-type substrate is used as a depleted sensor. Three types of pixels have been developed: passive pixels, analog-digital pixels, analog pixels. The analog pixels can be connected to the FE-I4 IC, which is the present readout IC of the innermost ATLAS pixel layers. The different versions of the LF-CPIX demonstrators are described, characterization of the different pre-amplifiers flavors with external injection signal and ^{55}Fe source are presented for the digital pixels. Finally radiation hardness results are discussed.**

I. Introduction

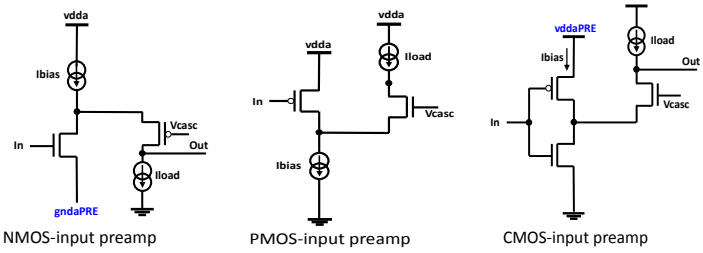
THE Large Hadron Collider (LHC) upgrade planned for 2026 calls for developing new type of sensors to replace the ATLAS Inner Tracker. For this upgrade, the HV/HR CMOS technology has been studied because of its low price, the limitation of the scattering (reduction of the material budget) and the good tracking precision (small pixel sizes). In addition, the charge collection by drift allows a high radiation tolerance and a good time resolution. Fig. 1a shows the architecture of the LF-CPIX sensor chip designed in LFoundry (LF) 150 nm HV process. Fig. 1b is the photography of a fabricated chip. In this chip, there are three pixel types: passive, analog-digital and analog pixels. Passive pixels are simple collection diodes, analog-digital pixels feature an integrated preamplifier and a discriminator together with a 4-bit threshold tuning DAC, and analog pixels feature only the analog front-end. Moreover, in these pixels three different preamplifier types have been used in the Charge-Sensitive Amplifier (CSA) part of the front-end: NMOS-input, PMOS-input and CMOS-input (see Fig. 2). The supply of the CMOS-input preamplifier (vddaPRE) is generated by an on-chip regulator. A detailed description of this chip can be found in [1]. According to the Cadence software simulations, less noise and faster response are expected with the CMOS-input preamplifier thanks to the combined gains of the 2 transistors.

Two versions of the LF-CPIX chip have been designed, called V1 and V2. The guard-rings of the LF-CPIX_V2 chip have been optimized in order to increase the breakdown voltage of the sensor's bias [2].



(a) (b)

Fig. 1. a) Architecture of LF-CPIX demonstrator chip designed and fabricated in LF150nm HR/HV CMOS process, b) Photography of the LF-CPIX chip.



(a) (b) (c)

Fig. 2. Preamplifier flavors implemented in the CSA's of LF-CPIX demonstrator: a) NMOS-input, b) PMOS-input, and c) CMOS-input.

II. In-Lab Tests

A. Tests without Source

The first parameter measured on LF-CPIX chips is the breakdown voltage (BV). During these measurements, the High Voltage (HV) (or BackBias voltage) is applied to the two

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Y. Degerli, F. Balli, M. Elhosni, F. Guilloux, C. Guyot, F.J. Iguaz, M. Lachkar, J.P. Meyer, A. Ouraou, P. Schwemling, M. Vandenbroucke are are with CEA-Saclay, IRFU, 91191 Gif-sur-Yvette Cedex, France (e-mail: yavuz.degerli@cea.fr).

M. Barbero, S. Bhat, P. Breugnon, Z. Chen, S. Godiot, P. Pangaud, A. Rozanov are with Centre de Physique des Particules (CPPM), 163 Avenue de Luminy, Marseille, France.

J. Liu was with CPPM, Marseille. He is now with Shandong Univ., China.

T. Hemperek, T. Hirono, H. Krüger, P. Rymaszewski, N. Wermes are with Physikalisches Institut der Universität Bonn, Nussallee 12, Bonn, Germany.

outer P-Well guard-rings. Fig. 3 shows the BV measured on two different LF-CPIX chips without backside processing. As expected, the BV of the LF-CPIX_V2 chip (~216V) is higher than the BV of the LF-CPIX_V1 chip (~130V).

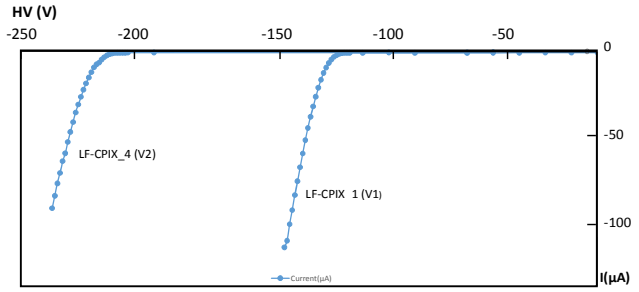

Fig. 3. Reverse bias currents measured on two versions of LF-CPIX chip (The HV is applied on the two outer P-Well guard-rings). The breakdown voltages extracted from these measurements are respectively -130V for the LF-CPIX_V1 and -216V for the LF-CPIX_V2.

Then the front-end response of LF-CPIX chips has been calibrated using an external injection pulse. The gain and input referred noise values measured on a LF-CPIX_V2 chip are shown in Fig. 4 for the analog-digital pixel sub-arrays with three preamplifier flavors (HV=-80V, gndaPRE=0V, Vinj =0.5V). Note that as the extracted gain and noise values depend on the injection capacitance value, the design value of this capacitance (Cinj=2 fF) has been used in these measurements. As seen in this figure, the pixels with PMOS preamplifier show unexpected higher gains than the two others, leading also to smaller input referred noise values.

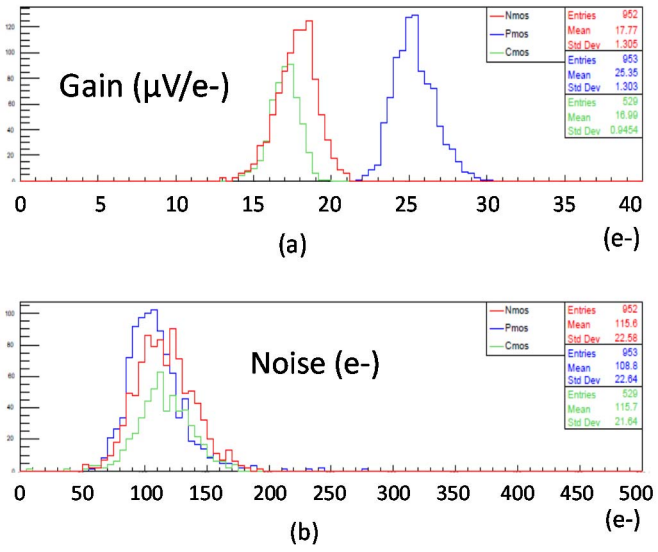

Fig. 4. a) Gain and b) input referred noise distributions estimated from injection pulse for the pixel sub-arrays with the three different preamplifier types for a LF-CPIX_V2 chip (HV=-80V, gndaPRE=0V, Cinj=2fF, Vinj=0.5V).

Then, for the three pixel flavors, the input referred noise values for different HV values have been measured. Fig.5 shows the results for the same LF-CPIX_V2 chip without backside processing. The noise values are almost constant below -80V, probably indicating that the diode is fully depleted. The PMOS-input preamplifier shows globally less noise than the two other flavors.

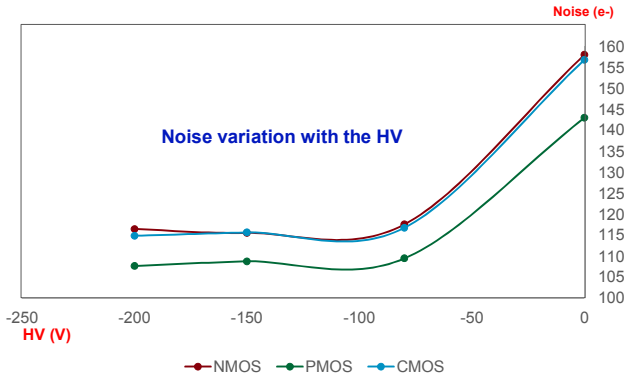

Fig. 5. Measured variation of the noise with the HV for a LF-CPIX_V2 chip (HV=-80V, gndaPRE=0V, Cinj=2fF).

The next step is the reduction of the threshold dispersion across the pixels thanks to a 4-bit DAC implemented inside each pixel. The thresholds of the pixels with the three preamplifier flavors have been measured before and after tuning. The threshold values have been extracted from S-curves obtained by varying the external pulse amplitude. Fig. 6 shows the distributions of the threshold values before and after tuning for the CMOS-input flavor. Note the reduction of dispersion after tuning.

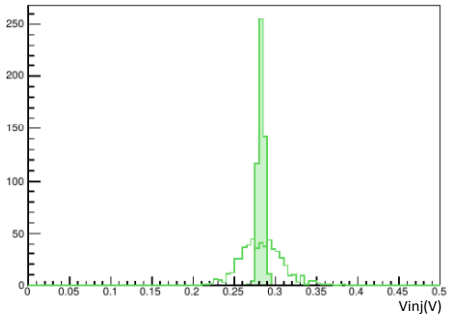

Fig. 6. Threshold distributions obtained for the CMOS-input pixel flavor before and after tuning.

The noise and threshold dispersion values for the three pixel flavors are summarized in Table I. The threshold dispersions reduce after tuning, but less effectively for the PMOS flavor. The overall noise performances improve after tuning.

TABLE I. THRESHOLD DISPERSIONS AND NOISE VALUES OBTAINED FOR THE THREE PIXELS FLAVORS BEFORE AND AFTER TUNING

PIXEL FLAVOR	TH. DISP. (e-)		NOISE (e-)	
	BEFORE TUNING	AFTER TUNING	BEFORE TUNING	AFTER TUNING
NMOS	612	229	206	147
PMOS	405	297	158	132
CMOS	411	140	172	152

To understand the reasons of the inefficiency of the tuning for the PMOS flavor, the gains of the pixels as a function of the injection signal amplitude have been checked. Fig. 7 shows the gain variation of the pixels. Indeed, the gain of the PMOS flavor depends strongly on the amplitude of the injection signal. This issue needs to be investigated further.

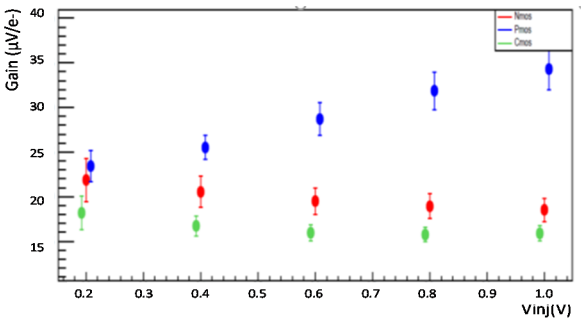

Fig. 7. Estimated gains as a function of the amplitude of the injection pulse for the three different preamplifier types for a LF-CPIX_V2 chip (HV=-80V, gndaPRE=0V, Cinj=2fF). Note the strong variation of the gain for the PMOS flavor.

B. *Tests with ^{55}Fe Source*

In order to calibrate the gains of the pixels, a ^{55}Fe source has been used. A typical spectrum obtained on one pixel is shown in Fig. 8. Table II shows the gain values measured on several pixels. These gain values have to be considered as qualitative and give only an idea of the global gain, since the real gain of the analog chain of the chip (buffers etc.) is not known precisely. Note that there is no significant difference between the gains of the three pixel flavors (which confirms the hypothesis that the gain of the PMOS flavor is overestimated with the injection signal). However, one can estimate the real value of the injection capacitance from these measurements. The estimated value from these measurements is ~2.1 fF, close to the design value of 2 fF.

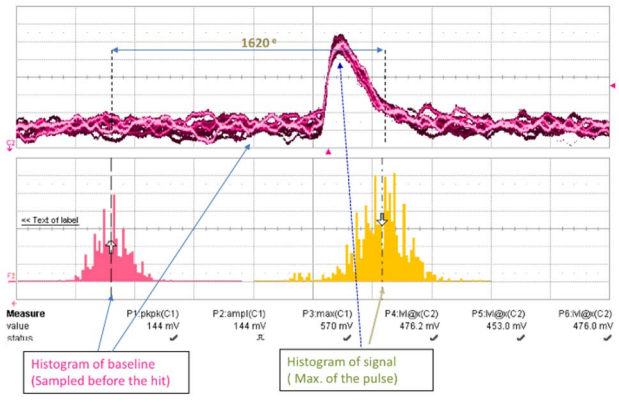

Fig. 8. Response of the pixel to an ^{55}Fe source and typical signal and noise histograms obtained on a LF-CPIX_V2 chip (HV=-80V). The value of the injection capacitance estimated from these measurements is Cinj=~2.1 fF.

TABLE II. GAINS MEASURED ON DIFFERENT PIXELS

	CMOS	PMOS	NMOS
Gain (µV/e-)	15.03	13.45	12.77
	14.32	12.60	13.51
	14.41	14.59	12.60
	13.70	14.94	12.09

III. IRRADIATION RESULTS

The LF-CPIX chips have been irradiated at CERN-PS with protons during the 2017 summer at room temperature. A total dose of 149 MRad has been reached. Table III summarizes the noise and threshold dispersion results for the CMOS-input pixel flavor of a LF-CPIX_V2 chip without backside processing (different than the chips presented in previous sections). The noise values are significantly higher after irradiation due to the increase of the leakage currents. By moderately cooling (-17 °C) the irradiated samples, the noise values become closer to the pre-irradiation values. Very similar noise and threshold dispersion behaviors have been observed for the NMOS-input and PMOS-input flavors.

TABLE III. MEASURED NOISE AND THRESHOLD DISPERSION VALUES BEFORE AND AFTER IRRADIATION UP TO 149 MRAD. FOR A LF-CPIX_V2 CHIP

PIXEL FLAVOR	TH. DISPERSION (e-)			NOISE (e-)		
	BEFORE IRRAD. (ROOM TEMP.)	AFTER IRRAD. (ROOM TEMP.)	AFTER IRRAD. (-17°C)	BEFORE IRRAD. (ROOM TEMP.)	AFTER IRRAD. (ROOM TEMP.)	AFTER IRRAD. (-17°C)
CMOS	476	501	428	161	467	184

IV. CONCLUSIONS

The LF-CPIX chips designed and fabricated in LF 150nm HV process have been characterized in laboratory conditions and then irradiated at CERN with protons. Among all the LF-CPIX chips tested, the CMOS-input preamplifier based pixels show the most stable performances but the in-time efficiency of these pixels must be measured.

The preliminary results are very promising and show that the depleted sensors developed in the LF150nm process are good candidates for the outer layer of the ATLAS inner tracker upgrade. The LF-CPIX chip is also the basis of a monolithic demonstrator (LF-MONOPIX) designed and produced in the same process [3].

REFERENCES

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