KEK Preprint 99-14

BELLE Preprint 99-1

Development of the Central Trigger System for the BELLE detector at the KEK B-factory *

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Abstract

In this paper, we describe the design and development of the central trigger system (GDL) for the BELLE detector at the KEK B-factory. The GDL consists of four types of single width 6U VME modules (ITD, FTD, PSNM and TMD) which are designed using the programmable logic techniques of Xilinx FPGA and CPLD. Individual and combined performance tests of these modules are done and it is confirmed that the GDL functions as expected.

PACS numbers : 07.50.Ek keywords : Trigger system, FPGA

*submitted to NIM-A.

1 Introduction

The KEK B-factory (KEKB)[1] is an asymmetric e^+e^- collider operating at the $\Upsilon(4S)$ resonance with the aim to study the CP violation in the B-meson system with the BELLE detector[2]. The goal luminosity is 10^{34} cm^{-2}sec^{-1}. The cross-sections and expected trigger rates are listed in Table 1 for various physics processes. The cross-section of $B\bar{B}$ events, which are the primary interest of the B-factory experiment, is reasonably small and a high trigger efficiency should be achieved for these events, while the uninteresting events with large rates should be suppressed. The Bhabha and $\gamma\gamma$ events are important for luminosity measurement and detector calibration. We prescale these events since the cross-sections are so large. The two-photon process trigger needs to be restricted because of the large cross-section and the topological resemblance to beam background events in the low p_t region. After the suppression of these events, the trigger rate is $\sim$100 Hz from physics events.

Because of the high beam current of the B-factory, severe beam backgrounds are expected. Based on the simulation study, we expect $\sim$ 100 Hz from beam related backgrounds, which leads to $\sim$200 Hz total trigger rate. The beam backgrounds are dominated by the spent electrons and positrons. The rates are very sensitive to the actual accelerator conditions and it is difficult to make a reliable estimation. Therefore, the trigger system is required to be robust against unexpectedly high beam background rates. The trigger conditions should be flexible so that background rates are kept within the tolerance of the data acquisition system (max. 500 Hz), while the efficiency for interesting physics events is kept high. It is important to have redundant triggers to keep the efficiency high even for varying conditions. The BELLE trigger system has been designed and developed to satisfy these requirements. The trigger system is composed of two parts: the trigger systems of the individual components of the BELLE detector and the central trigger system, called the Global Decision Logic (GDL). This article reports on the design and

development of the BELLE GDL.

In section 2, a brief description of the BELLE detector and the trigger system is provided. Section 3 describes the role of the GDL and its components. Section 4 describes the hardware development and performance of the individual components of the GDL and in section 5 describes the performance of the GDL system.

2 The BELLE Detector and Trigger System

Fig. 1 shows the BELLE detector. It consists of the following detector components from the inside to outside: Surrounding the beam pipe, three layers of double-sided Silicon Vertex Detectors (SVD) are placed to measure the decay positions precisely. Charged tracks are measured by the Central Drift Chamber (CDC) which has 50 layers of stereo and axial wires. The three innermost layers have cathode strips to provide position information along the beam axis (z axis) for the trigger. Threshold type Aerogel Čerenkov Counters (ACC) and Time-of-Flight counters (TOF) are used for particle identification. Trigger Scintillation Counters (TSC) provides trigger signals taking a coincidence with the TOF. An Electro-magnetic Calorimeter (ECL), which consists of 8880 CsI(Tℓ) crystals, measures the energy of photons and electrons. A superconducting solenoid magnet provides a 1.5 T field for momentum measurement of charged tracks. The iron return yoke plates are instrumented with 14 layers of resistive plate counters (RPCs) between the plates, which serve as K_L and muon detectors (KLM). The Extreme Forward Calorimeter (EFC), placed in front of the final focusing quadrupole magnet, measures the luminosity and is also used for tagging particles in the very forward region.

Fig. 2 shows the schematic view of the BELLE trigger system. As mentioned before, it is composed of the sub-detector trigger systems and the GDL. The sub-detector trigger system is based on two categories: track triggers and energy triggers. The CDC and

TSC/TOF are used to provide the trigger signals from charged particles. The CDC provides r-ϕ and r-z track trigger signals. The ECL trigger system provides triggers based on total energy deposit and cluster counting of crystal hits. These two categories of triggers provide sufficient redundancy. The KLM trigger provides additional information on muons and the EFC triggers are used for tagging two photon events as well as the Bhabhas. The sub-detectors process event signals in parallel and provide the trigger information to the GDL, where all the information is combined to characterize the event type.

Considering the beam crossing rate of 509 MHz ($\sim$ 2 nsec interval) with the full bucket operation of KEKB, a "Fast trigger and Gate" scheme is chosen for the BELLE trigger and data acquisition system. The latency of the trigger system is set to 2.2 μsec to match the SVD readout system (sample and hold scheme with 2.5 μsec shaping time). In order to maintain the 2.2 μsec latency, each sub-detector trigger signal is required to be available at the GDL input by a maximum latency of 1.85 μsec (timing adjustments are done at the input of GDL, as described later). As a result, the GDL is left with a fixed 350 nsec processing time to form the final trigger signal.

3 Global Decision Logic (GDL)

The configuration of the Global Decision Logic (GDL) is shown in Fig. 3. The GDL takes up to 48 trigger signals from sub-detectors and makes global correlations among them. It provides up to 48 types of event trigger signals. It is designed to function in a pipelined manner with a 32 MHz clock in order to avoid dead time losses and it takes 350 nsec to generate the final trigger signal. The functionality of the GDL is shared by several types of modules as shown in Fig. 3:

- Input Trigger Delay (ITD):
  Adjusts the timing of input trigger signals to meet the latency of 1.85 μsec.

- Final Trigger Decision (FTD):
  Performs the global trigger logic, correlating the information from sub-detector triggers.

- Prescale and Mask (PSNM):
  Prescales the high rate input triggers for calibration/monitoring purpose and disable the unused triggers from the FTD.

- Timing Decision (TMD):
  Generates the final trigger signal at 2.2 μsec latency based on the timing information of the "timing triggers" from the TSC and ECL.

The timing decision logic uses a 64 MHz clock to provide 16 nsec ($\pm$ 8 nsec) timing accuracy. The 32 MHz and 64 MHz clocks are made from the accelerator RF signal (subdivision to 1/16 and 1/8 frequencies, respectively) and hence the trigger signals from the GDL are synchronized to the beam crossing. The final trigger from the GDL provides the timing for the ADC gates and TDC stops. The trigger signals at each step of the GDL are sent to the scalers to monitor the rates and dead time. They are also fed into FASTBUS multi-hit TDCs (LeCroy 1877S) to record the timing so that the timing and logic of the GDL can be verified.

4 GDL Modules

The ITD, FTD, PSNM and TMD serve as the components of the GDL. These are designed as single width 6U VME modules. These modules extensively use the Xilinx Field Programmable Gate Array (FPGA) and Complex Programmable Logic Device (CPLD)

chips [3] in order to provide sufficient flexibility in the system. In this section we describe the hardware design and performance tests of the individual modules.

4.1 Input Trigger Delay (ITD) Module

As mentioned above, the timing of each sub-detector trigger signal has to be adjusted properly in order to make a global correlation at the FTD. The timing of the TSC and the ECL timing signals should also be adjusted correctly. The task of the timing adjustments is performed by the ITD module. The ITD latches the input sub-trigger signals by the system clock (sub-triggers with 32 MHz and timing signals with 64 MHz) and delays them so that the sub-trigger signals and the timing signals are valid at the FTD and TMD inputs at t = 1.85 μs.

The ITD module is designed as a general purpose programmable pipeline delay module. It takes 16 channel ECL level inputs and provides the delayed outputs in both ECL and TTL levels at the front panel with 2.54 mm pitch 17 pair flat cable connectors. This module offers programmable delays ranging from 0 to 31 in units of the clock cycle for each channel. It can select either external (NIM level/ECL level) or internal (50 MHz) clocks. The delay logic is implemented in 4 Xilinx FPGA (XC3130-125PC68) chips. The delay values are set and read out either via VME bus from the CPU board or from the front panel switches. The picture of this module is shown in Fig. 4 (left).

The delay logic for all the channels has been realized with a shift register chain as shown in Fig. 5 for a single channel. The delay is given by the number of shift registers in the signal path which are switched on/off by the contents of the delay counter register in a binary manner. We tested the module and verified its function with the clock frequency up to 85 MHz for all the delay values. The jitter of the delayed output signals were measured to be less than 350 psec in R.M.S. for all the delay values. From these tests, we concluded that the ITD can safely function in a pipeline with the 64 MHz and 32 MHz

GDL clocks.

4.2 Final Trigger Decision (FTD) Module

The FTD makes global correlations of the 48 sub-detector trigger signals. The correlation logics are usually combinations of AND, OR, and VETO (NOT). It is essential to keep enough flexibility in the correlation logic to take care of any needs.

We designed the FTD module as a universal logic unit board where the user logic is downloaded to the Xilinx CPLD chip (XC95108-15PQ160). The CPLD features fixed pin-to-pin delay and in-system programmability. The module contains 96 TTL level I/Os at the front panel with 2.54 mm pitch 17 pair flat cable connectors. These I/O lines are connected to the I/O pins of the CPLD chip and can be used either as inputs or outputs depending on the logic loaded. The board has two clock sources connected to the CPLD clock pin, external (NIM level) and internal (32 MHz). The logic on the CPLD can be loaded via the VME bus from the CPU board. It also contains another CPLD (XC95108-7PC84) to implement the VME interface circuit. Its logic is pre-loaded from a PC via serial port lines. The schematic along with a picture of this module is shown in Fig. 6. We use this module with the I/O configuration of 48 inputs and 48 outputs.

We tested the module loaded with the trigger logic planned for the actual experiment. The signals were latched at inputs and outputs in the CPLD logic to form a two-stage pipeline. Input pulses asynchronous to the clock were fed to each input channel while other inputs were kept constant. The latency from the input to output was measured with system clock frequencies between 25 and 95 MHz.

The latency distributions for different clock frequencies are shown in Fig. 7. When the pipeline works correctly the latency distribution should stay within one clock period with a tiny spread due to the jitter as indicated in the figure. The figure shows the module works successfully up to 80 MHz (12.5 nsec clock period). We concluded that the FTD

can work with a 32 MHz clock quite safely.

4.3 Pre-scaler and Mask (PSNM) Module

The Pre-Scaler and Mask Logic (PSNM) prescales or masks the input signals. To implement the PSNM logic, we use the universal logic board (Fig.4 (right)) which was developed for the level 2 trigger in the KEK PS E162 experiment [4]. This module [5] has a total number of 64 TTL level I/Os with 2.54 mm pitch 17 pair flat cable connectors at the front panel. It has 3 clock sources, external (2 NIM level inputs) and internal (40 MHz). It makes use of four Xilinx FPGA chips (XC3190A-09PP175) for user logic implementation.

We implement 4 channels of prescale and mask logic in one FPGA chip, and one module handles 16 channels. The logic for each channel consists of a programmable synchronous counter and a register to store the prescale value. The counter counts the number of input pulses and compares with the prescale value stored in the register. When the counter output matches to that of the prescale value, the terminal count bit in the synchronous counter is set and becomes available as the output signal. Setting the prescale factor to 0 masks out the corresponding channels. The pre-scaling factors for individual channels are set and read out by a VME CPU board.

Due to the size of the logic resources inside the FPGA chips, the maximum prescale factor per channel is limited to 255 (8 bit counter). Two PSNM modules are cascaded to provide a maximum prescale factor up to 65025 (255^2). We use 6 modules for the 48 output signals from the FTD. This module with the PSNM logic was tested with clock frequencies between 25 and 50 MHz. We found that the system can work properly up to 34 MHz. Because of the complicated synchronous counter logic and larger gate array size of the chip compared with the ITD, the maximum usable clock rate is slower than that for the ITD. Since the PSNM will be used with a 32 MHz system clock in a more stable cooling environment than the test bench, we conclude that this module can function

safely.

4.4 Timing Decision (TMD) Module

The TMD decides the timing of the trigger signal from the GDL for triggered event based on the timing signals from TSC and ECL.

The TMD module design is based on the FTD module, modified to handle the ECL level I/Os for better timing performance. The module contains a total of 64 TTL level I/Os connected through 2.54 mm pitch 17 pair flat cable connectors, and 8 ECL inputs and 8 ECL outputs with 2.54 mm pitch 8 pair flat cable connectors at the front panel. Two Xilinx CPLD chips are used in this module to take care of the VME interface logic (XC95108-7PQ160) and the TMD timing logic (XC95108-10PQ160). It has the following clock sources: external (2 NIM and 1 ECL level), internal (64 MHz). The timing decision logic is downloadable via the VME bus. The schematic along with a picture of this module is shown in Fig. 8.

This module asserts the final trigger at t = 2.2 μsec with trigger type information. A logical OR of the 48 PSNM outputs (cue signal) is formed at the TMD. As a timing source, the TSC is better than the ECL because of its small jitter ($\sim$5 nsec) compared to that of the ECL ($\sim$100 nsec). Therefore, the TSC timing signal has higher priority than the ECL timing signal. Furthermore, when timing signals are not available from the TSC or the ECL, TMD generates the final trigger from the cue signal. Hence the final trigger timing is categorized into 3 types: trigger type 0 corresponds to the timing from the TSC timing signal, trigger type 1 corresponds to the timing from the ECL timing signal, and trigger type 2 corresponds to the timing of the cue signal.

Upon the detection of the leading edge, the timing signals are put into shift registers; the TSC signal into 22 steps shift-register with the 64 MHz clock and the ECL signal into 11 steps with the 32 MHz clock, to make a 350 nsec time delay. The arrival of the timing

signal at the TMD input is interpreted as t = 1.85 μsec. When the timing signal reaches the last step of the shift register, the time is t = 2.2 μsec (1.85 μsec + 0.35 μsec), and the final trigger is generated.

The timing decision logic is implemented as a state machine which is shown in Fig. 9. The state machine consists of 3 states: STDBY, DECISION and LFT (Latching Final Trigger). It is driven by the 64 MHz clock. STDBY is the default state, waiting for the cue signal. After detecting the cue signal, the logic transits to the DECISION state to decide the final trigger timing. When the timing is decided, it transits to the LFT state and the final trigger is issued. At the transition to the DECISION state, an internal timer is started which counts for 512 nsec. In the DECISION state the logic follows the sequence below within one 64 MHz clock cycle.

1. Check if the leading edge of the TSC timing signal has reached the last step of the shift register. If it is true, the final trigger is issued with trigger type 0 (FT0), and the logic transits to the LFT state.

2. Else, check if the leading edge of the TSC timing signal has already arrived at the TMD. If true, the logic goes back to the DECISION state stopping the internal timer.

3. Else, check if the leading edge of the ECL timing signal has reached the last step of the shift register. If true, the final trigger is issued with the trigger type 1 (FT1), and the logic transits to the LFT state.

4. Else, check if the leading edge of the ECL timing signal has already arrived at the TMD. If true, the logic goes back to the DECISION state stopping the internal timer.

5. Else, check if the internal timer has counted up to 512 nsec. If true, the final trigger

is issued with trigger type 2 (FT2), and the logic transits to the LFT state.

6. Else, the logic goes back to the DECISION state, *without* stopping the internal timer.

In the LFT state, the final trigger is kept active for at least four 16 MHz clocks and then the logic transits to the STDBY state. This completes one trigger cycle.

This timing decision allows the jitter of sub-detector triggers to be up to 512 nsec, which may happen for the CDC trigger due to large drift time. This value can be changed by loading the TMD logic with a different counter value.

Like the other GDL modules the functionality of this module was tested with a clock up to 95 MHz. It was found that the state diagram logic could function properly up to 75 MHz. Since we use this module with a 64 MHz clock, we conclude that it can function quite safely.

5 GDL System Test and Results

When all above modules are assembled as the "GDL" system, they should work as a part of the pipelined processor. The 32 and 64 MHz clocks, which are made from the RF signal, are given to all the modules as the external clocks in order to make them work synchronously.

The signal flow in the GDL is illustrated in Fig. 10. Here we assume the trigger and the timing signals are produced from the ITD at T=1.85 μsec with clock 0. They are latched at the FTD at clock 1 and the output of the combinatorial logic from the FTD (C = A and B in this figure) is available at clock 2. Then it is latched by the first PSNM (PSNM1) at clock 3 and the output is available at clock 4. The second PSNM (PSNM2) will latch this signal at clock 5 and the output is available at clock 6. This signal is fed

into the TMD input and is latched as the cue signal. The leading edge of this cue signal starts the state logic inside TMD. It issues the final trigger with the proper timing (22 $\times$ 64 MHz clocks after the arrival of the TSC signal or 11 $\times$ 32 MHz clocks after the ECL signal).

In the combined test of all the GDL modules, we verified the performance of the above pipeline scheme. A bench setup was prepared as shown in Fig 11. We used trigger patterns from a Pulse Pattern Generator (PPG) that was developed by the KEK electronics facility. The PPG has a 16 bit $\times$ 4K depth data RAM which can be loaded with any arbitrary binary pattern through the VME bus and it can be run continuously to get 16 periodic ECL level outputs with one depth per clock. Different PPGs were used to generate patterns to mimic the sub-detector trigger and timing signals realistically. The rates and widths of the timing signals are 250 KHz and 46.9 nsec for the TSC, 312.5 KHz and 250 nsec for the ECL respectively. The rate of the sub-detector trigger signals was kept at 10 KHz with a width of 100 nsec. The sub-detector trigger signals followed the path ITD $\rightarrow$ FTD $\rightarrow$ PSNM $\rightarrow$ TMD, whereas the timing signals were sent to the TMD directly. Multi-hit TDCs were used to record the input and output hit patterns and timing information at each stage of the GDL pipeline.

The result of this combined test is shown in Fig. 12. The top plot shows the trigger output from the FTD. The time t = 0 in this plot corresponds to the clock 0 of Fig. 10 and this timing is assumed as t = 1.85 μsec in the average. The outputs of the FTD are fanned out by the first stage of the PSNM. Therefore this signal appears around 125 nsec (clock 4). The second stage of the PSNM takes 2 more clocks and provides the output signals around 187.5 nsec (clock 6), which is shown in the second plot from top. The cue signal is latched at the TMD around 20 nsec after it leaves the PSNM module which is shown in the third plot. After this signal is detected inside the TMD logic, the STDBY state transits to the DECISION state as shown in the fourth plot. As described

before, the TMD logic checks for the presence of the timing sources (TSC and ECL) in the DECISION state and the final trigger is issued either 350 nsec after the TSC timing (FT0) or 350 nsec after the ECL timing (FT1) or around 500 nsec from the DECISION state (FT2), which are shown in plots 5, 6 and 7 respectively. From this result we confirmed that the entire GDL system based on the pipeline works reliably as expected.

6 Conclusion

The central trigger system (GDL) of the BELLE experiment has been designed and constructed. The functionality of the GDL is distributed among several single width 6U VME modules, which are called ITD, FTD, PSNM and TMD. Individual and combined performance tests of these modules are done in a realistic way close to the actual experimental conditions and the GDL was confirmed to work as expected. The GDL was successfully in use for cosmic-ray data taking of the BELLE detector.

Acknowledgments

We are deeply thankful to all the members of the DAQ/Trigger group for their generous help, cooperation and valuable suggestions at each step of the development of the GDL. Our sincere thanks go to Mr. Nagano of Xilinx corp. for his valuable suggestions regarding the usage of Xilinx CPLDs in the GDL. We are very much thankful to Mr. M. Miyazawa of GND company for his help and cooperation in making the PCB layout and fabrication of all the GDL modules in time. We would like to acknowledge and thank the members of the KEK electronics facility, Mr. S. Shimazaki, Mr. M. Ikeno and Mr. T. Murakami for their help and valuable suggestions. One of us (A.M.) would like to thank The Japan Science Society for financial support by the Sasakawa Scientific Research Grant.

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Table 1: Total cross section and trigger rates with $\mathcal{L} = 10^{34}$ cm^{-2}sec^{-1} from various physics processes at the $\Upsilon(4S)$. $^{(a)}$ prescaled by factor 1/100. $^{(b)}$ with restricted condition ($p_t \geq 0.3$ GeV/c).

Physics Process	Cross section (nb)	Rate (Hz)
$\Upsilon(4S) \to B\bar{B}$	1.15	11.5
Hadron production from continuum	2.8	28.
$\mu^+\mu^- + \tau^+\tau^-$	1.6	16.
Bhabha ($\theta_{lab} \geq 17^\circ$)	44.	4.4 $^{(a)}$
$\gamma\gamma$ ($\theta_{lab} \geq 17^\circ$)	2.4	0.24 $^{(a)}$
2γ processes ($\theta_{lab} \geq 17^\circ$, $p_t \geq 0.1$ GeV)	~ 15	~ 35 $^{(b)}$
Total	~ 67	~ 96

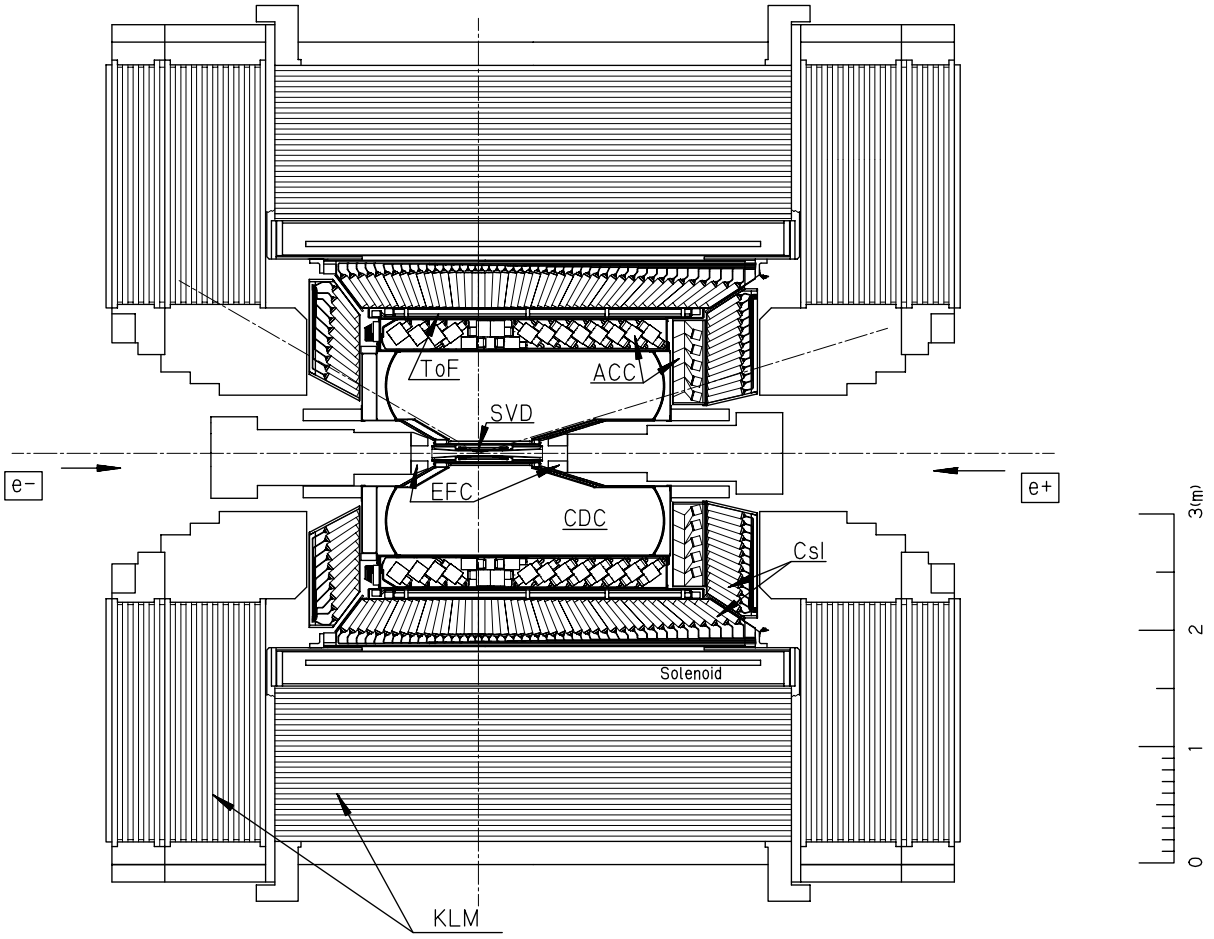

Figure 1: The BELLE detector.

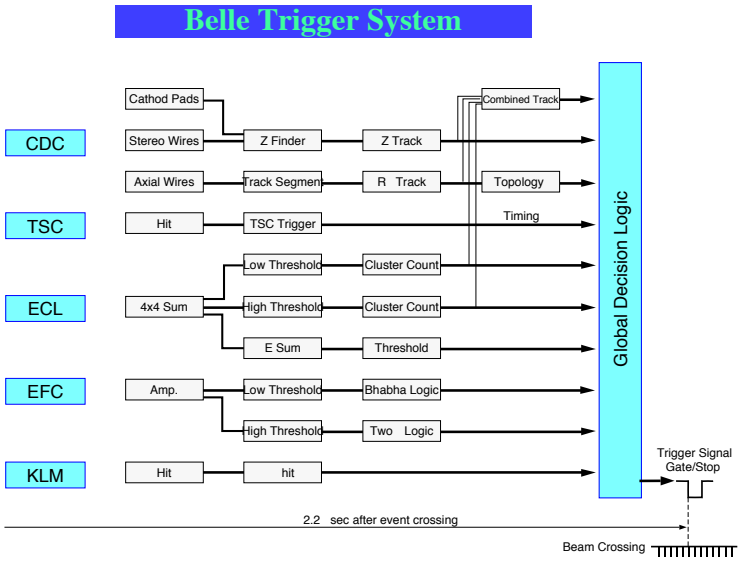

Figure 2: The trigger system for the BELLE detector.

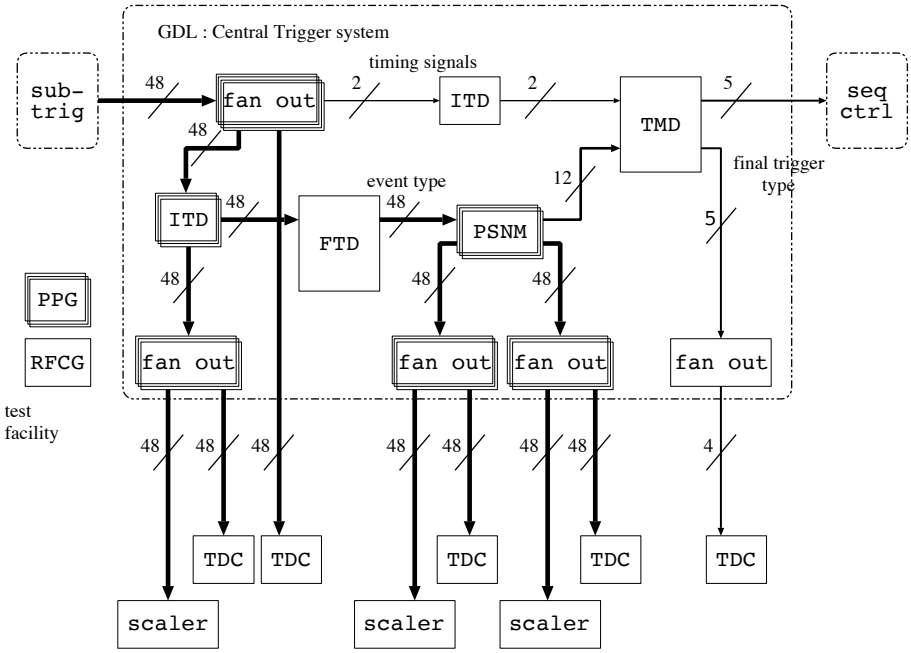

Figure 3: Schematic Design of the GDL.

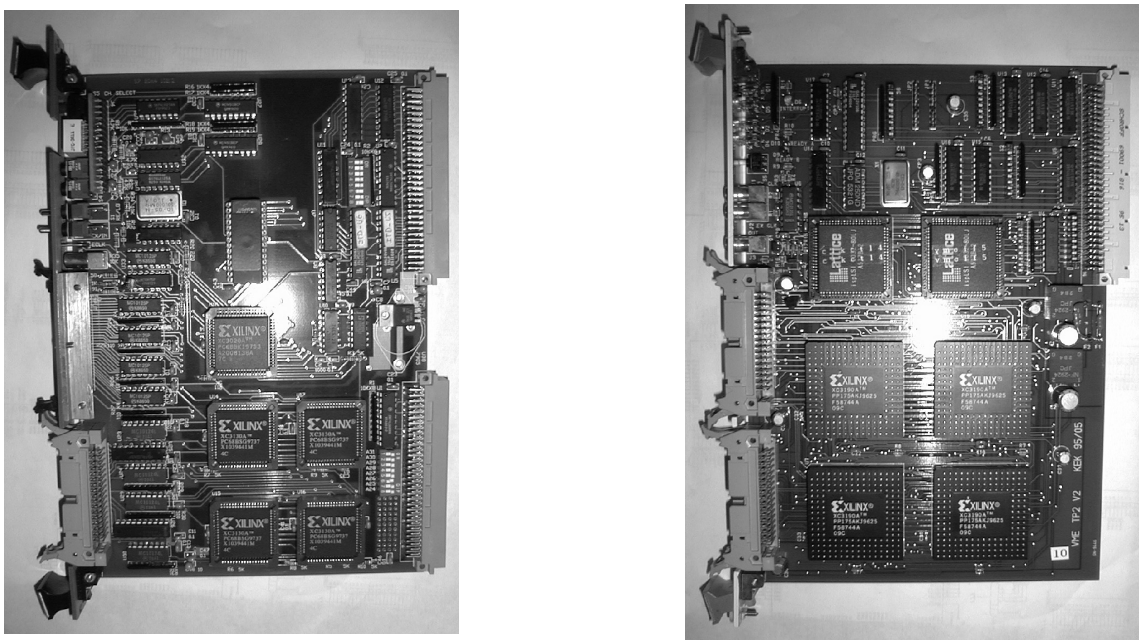

Figure 4: Picture of modules (left) ITD and (right) PSNM

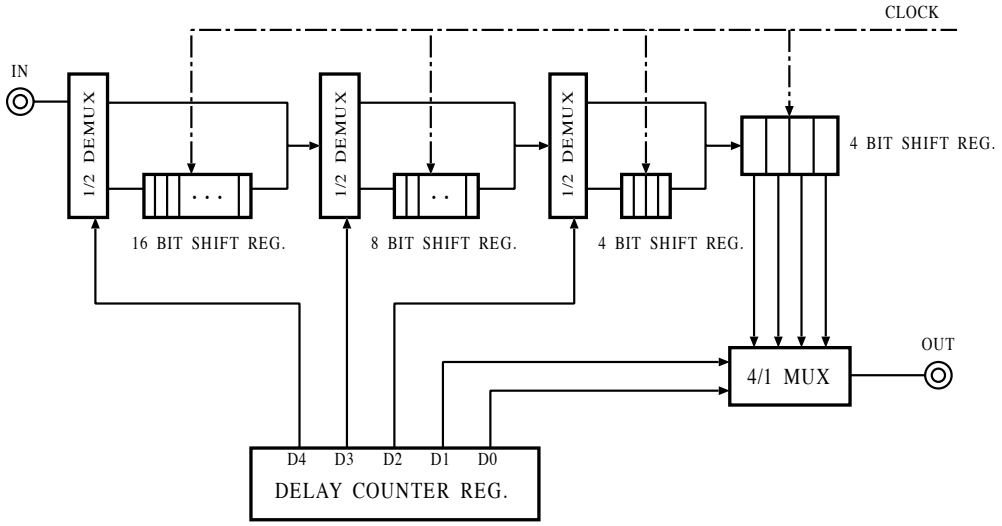

Figure 5: Input Trigger Delay Logic

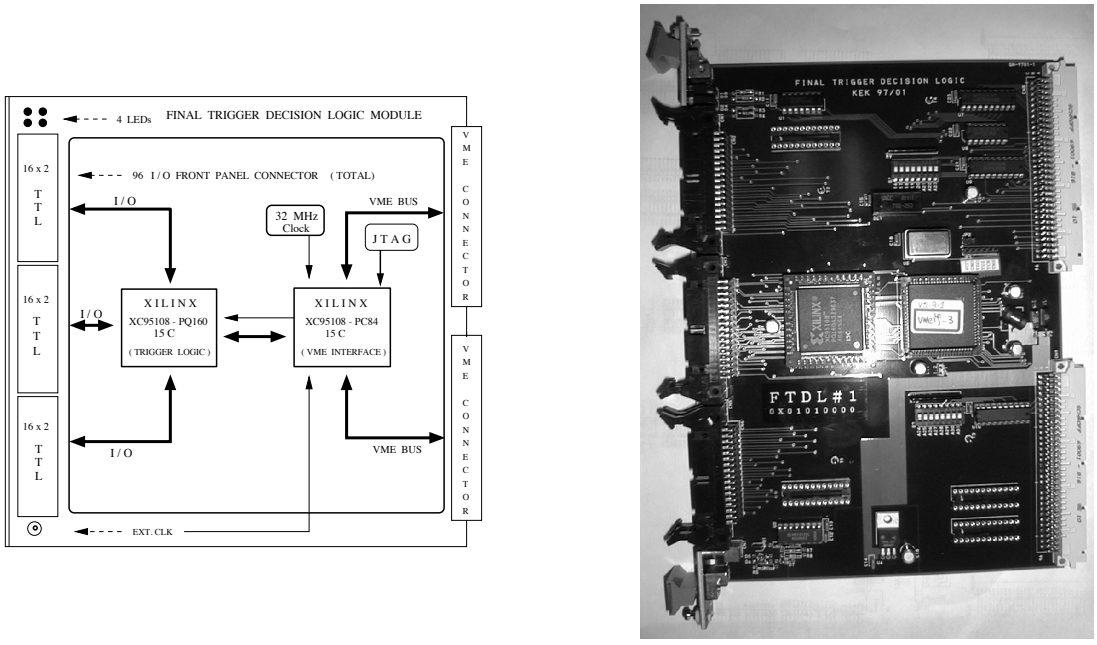

Figure 6: FTD Module (left) Schematic and (right) Picture

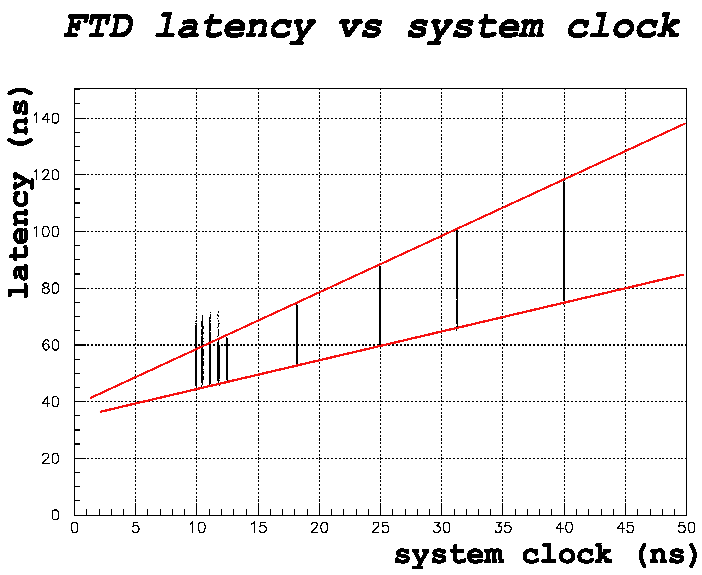

Figure 7: FTD latency distribution

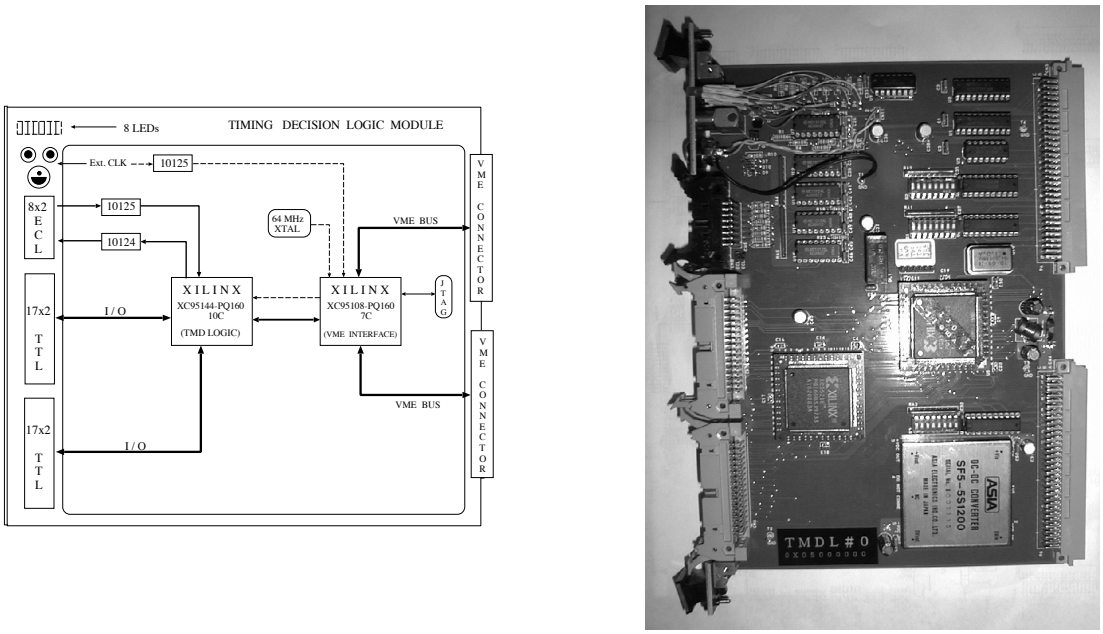

Figure 8: TMD Module (left) Schematic and (right) Picture

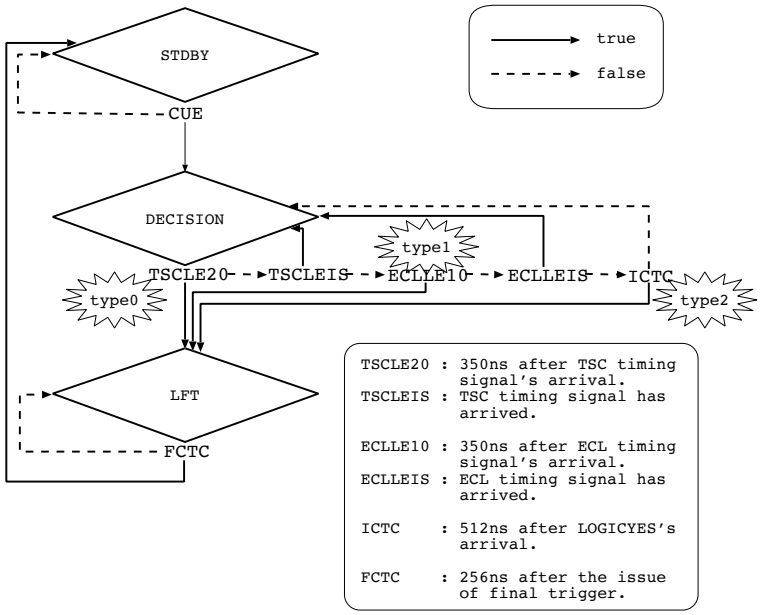

Figure 9: State Diagram of Timing Decision

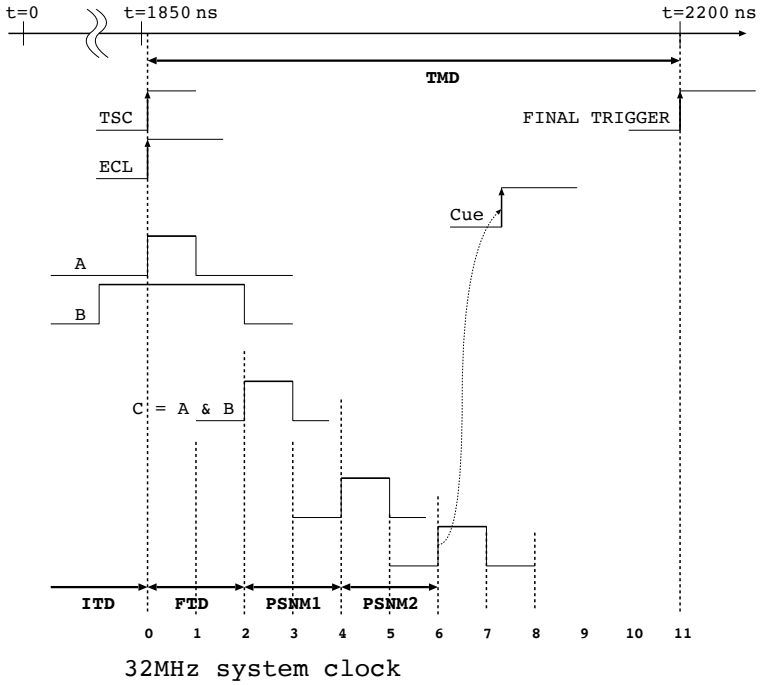

Figure 10: Timing chart of the GDL: digit 0 to 11 represent the number of the GDL system clock (32MHz).

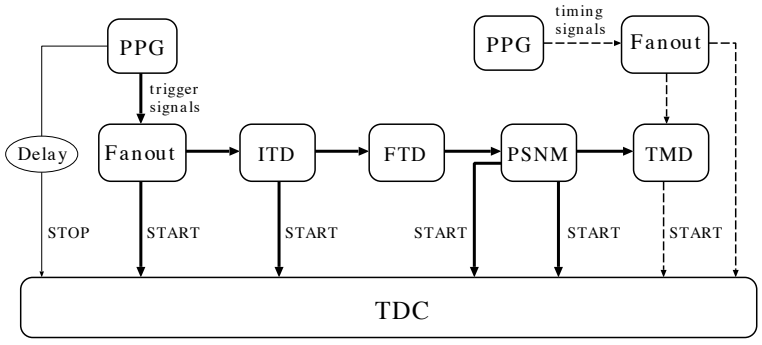

Figure 11: GDL system test bench setup

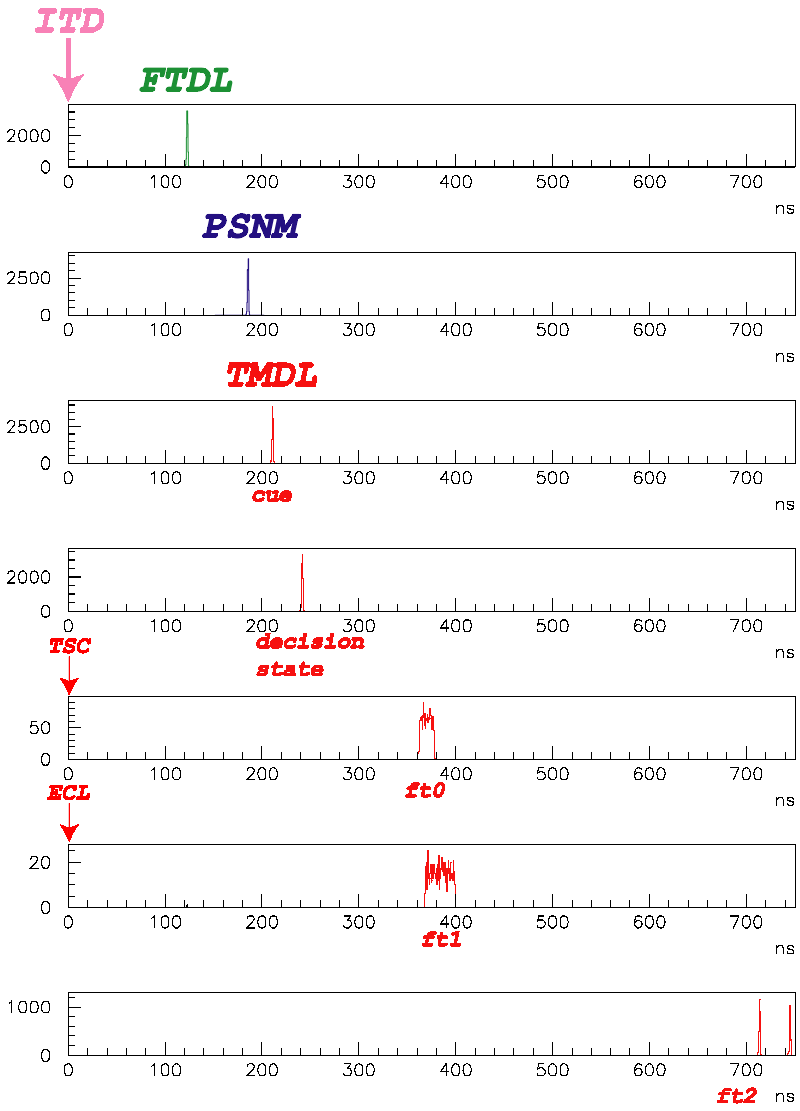

Figure 12: GDL system test result