Design and Development of Low Voltage Distribution Board for CBM-MUCH Experiment

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Introduction

Increasing demands for high position resolution and high rate capabilities of a tracking detector, led to a more complex and densely packed electronics, which require more and more power in confined space. These systems are self-triggered to meet the rate requirements of the present experiments, and so there is very stringent requirement on noise levels. In such systems power consumption and space is always a big issue to address. A GEM-based tracking system is planned to be used for muon tracking in the proposed CBM experiment[1][2] at FAIR. The density at the station 1 is very high with pad size 3 *mm* × 3 *mm* pads. This Muon Chamber will be movable system hence a careful design of low voltage distribution is needed for optimized performance and less cable count for ease of operation. To minimize the cable load, 48V is planned to be taken as the input the Low Voltage Distribution Board (LVDB) which will be located near the detector.

Functional Description of LVDB

The LVDB is an active system which divides a single channel high power low voltage (LV) into a several low power LV channels as per the requirement. The LVDB has mainly 8 channels with each channel having output voltage of 3.3V and current rating 1.2A. The LVDB has over current protection and monitoring facility of voltage and current for each channel using FPGA vertex-5 board.

The block diagram of LVDB is shown in Fig.1.In this LVDB 48V further stepped down to 5V using a DC to DC SMPS type convertor. Reason for choosing the SMPS is reduced size, low power loss on the convertor to avoid excess heat generation on the board. The prototype design has been tested for 2 channels. The block diagram in Fig.1 shows 8 channels for which the PCB is being fabricated and will be tested. The number of channels for each LVDB may vary depending on final requirement.

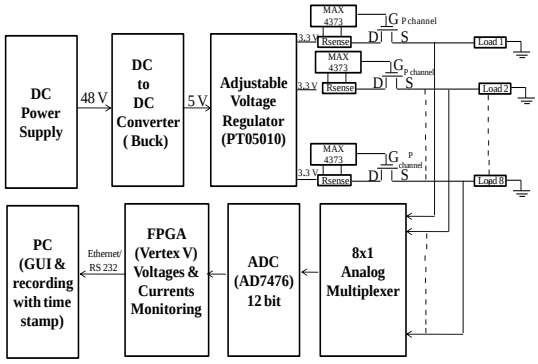


Fig.1 Block Diagram of LVDB

The LVDB is to be operated in confined area with no cooling facility, so the circuit has been designed with very low power dissipation of 90 mW, using DC to DC converter (PTH 05010). The design of final layout is evolving and final version may have two boards with 2 DC to DC converters: one to convert 48V to 5V and other 5V to 3.3V.

GEM[3] is a gaseous detector with operating voltage of around 3.5KV and hence there is always a possibility of sparks and unwanted glitches in the system. At times they may impair the electronics load. In such cases, the segmentation of the power supply of the electronics will be helpful in isolating faulty channels. In LVDB all output channels are protected from over-current and if one of the electronic channel draws over-current, that particular LVDB channel will be shut down keeping rest of its channels in working state. This minimizes the data loss due to unexpected glitches in the system.

Fig. 2 shows the basic building block of the over current protection circuit of the low voltage

distribution circuit [4] using MAX4373, sense resistors, control logic and switching elements. MAX4373 is a low cost, micro power IC containing high side current sense amplifier, band gap reference and a comparator with latch. The current sense resistor is connected in series to the load, so the resistance chosen should be as low as possible to minimize the voltage drops and must be very stable.

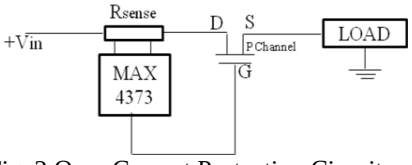


Fig. 2 Over Current Protection Circuit

Prototype testing and Circuit performance

In LVDB we use DC to DC converter (PTH05010) as a voltage regulator. The test results of this voltage regulator is as shown in Fig. 3 and Fig.4. In Fig.3 the voltage regulation of DC to DC converter is decreasing with increase the load current and voltage regulation is about 0.2%. In Fig.4 shows, how the efficiency varies with load current, it can be seen that it is nearly 85% to 90% at desired output voltage and current.

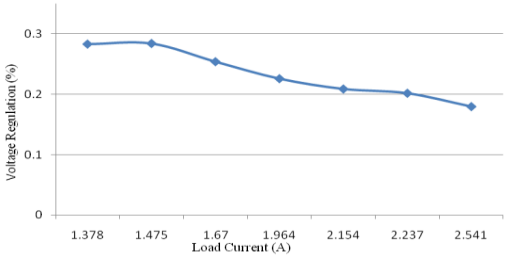


Fig.3 Load Current vs Voltage regulation

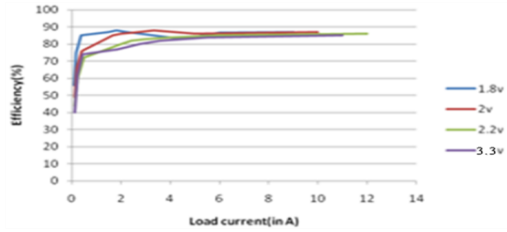
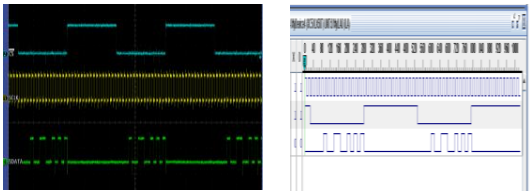


Fig.4 Load Current vs. Efficiency for different regulated voltage

Monitoring and Control

The LVDB handles large number of channels that are required in the actual experiment, so it is essential to monitor the status of each channel and control them to achieve this purpose. One FPGA based system is under development for online monitoring and storage of the output voltages and currents of LVDB. Several components like ADC and data reading block of FPGA has been designed and tested.

Fig.5 (a) shows a screen shot of the waveform captured by scope. In Fig.5 (a) blue waveform is chip selection clock, yellow waveform is serial clock and green waveform is serial data of 12 bit ADC (AD7476). Fig.5 (b) shows the PC screen capture of the waveform captured by JTAG port of FPGAVertex-5 board using Chipscope-pro. This data will be finally readout via Ethernet or RS232 interfaces.



(a) (b)

Fig.5 Output results of ADC (AD7476) and Chipscope-pro readout from Vertex-5 board

Future plans

Control of different parameters of the LVDB includes, remote controlled monitoring of voltage and current, switching on and off and reset of individual LVDB channels will be added to the present design.

The details of design report will be presented.

References

[1] http : //www.gsi.de/ f orschung/ f air experiments/CBM/index e.html

[2] A.K. Dubey, et. al, http : //dx.doi.org/10.1016/ j.nima.2012.10.043

[3] F. Sauli et al., Nucl. Instrum. and Methods A 386 (1997) 531

[4] Low Voltage Distribution for ALICE Photon Multiplicity Detector, Proceedings of DAE Symp on Nucl. Phys., Vol55(2010) page 762-763