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# HIGH PRECISION RF CONTROL FOR SRF CAVITIES IN LCLS-II

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## ABSTRACT

The unique properties of SRF cavities enable a new generation of X-ray light sources in XFEL and LCLS-II. The LCLS-II design calls for 280 L-band cavities to be operated in CW mode with a $Q_L$ of $4 \times 10^7$, using Single-Source Single-Cavity control. The target RF field stability is 0.01% and 0.01° for the band above 1 Hz. Hardware and software implementing a digital LLRF system has been constructed by a four-lab collaboration to minimize known contributors to cavity RF field fluctuation. Efforts include careful attachment to the phase reference line, and minimizing the effects of RF crosstalk by placing forward and reverse signals in chassis separate from the cavity measurement. A low-noise receiver/digitizer section will allow feedback to operate with high proportional gain without excessive noise being sent to the drive amplifier. Test results will show behavior on prototype cryomodules at FNAL and JLab, ahead of the 2018 final accelerator installation.

## INTRODUCTION

LCLS-II is an X-ray Free Electron Laser (FEL) under construction at SLAC, driven by a superconducting RF Linac [1]. The electron beam quality will directly translate to the quality of the X-ray beams produced in undulators and used for scientific research in the end stations; hence strict requirements have been placed on the stability of the accelerating cavity fields. An initial stability goal of 0.01° in phase and 0.01% amplitude has been set for the main Linac, composed of 280 nine-cell 1300 MHz superconducting cavities [2].

Plans for the RF controls for the 1.3 GHz cavities have been described elsewhere [3] [4] [5] [6]. It is based on mainstream digital LLRF technology, and incorporates many ideas developed for LBNL's NGLS proposal [7]. The controls use a Single Source Single Cavity (SSSC) architecture, where each cavity has a dedicated amplifier. SSSC has enormous value for simplifying control of narrow-band SRF cavities, It is also a sensible choice for a CW machine, where Solid-State Amplifier technology has approximately matched Klystrons in price, and they are considered easier to operate and maintain.

The LLRF subsystem of LCLS-II is itself a four-laboratory collaboration: LBNL for architecture, FPGA hardware and RF DSP programming, and ADC/DAC hardware development; Fermilab for downconverters, upconverters and piezo drivers; JLab for interlocks, stepper controls, and power supplies; and SLAC for LO distribution, MO and PRL, global control system integration, commissioning, transition to operations, and project management.

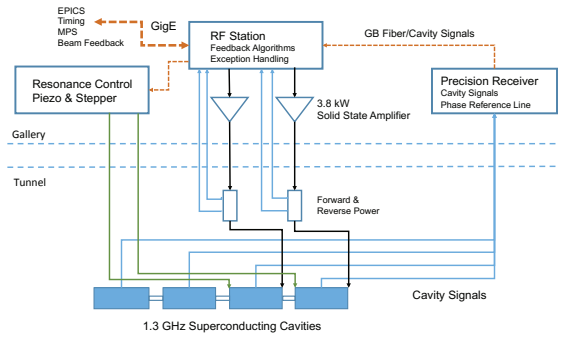


Figure 1: System hardware configuration supporting half of a cryomodule (one of two RF Station chassis shown).

## SYSTEM DESIGN

Each rack (supporting four cavities) includes a separate Precision Receiver Chassis (PRC), linked only by optical fiber to two RF Control Chassis (RFS), as shown in figure 1. This density of rack equipment matches the civil layout of the accelerator, where one LLRF rack is cabled to one penetration to the tunnel. The physical separation between PRC and RFS maximizes isolation between the critical stabilized cavity signals and the wildly fluctuating forward and reverse monitoring channels. Preliminary measurements show that this separation has succeeded, in that the measured isolation is at least 125 dB.

The system bypasses some of the usual compromises in choosing an IF by means of an unusual split-LO design, where a low-frequency IF (20 MHz) is used for RF downconversion, and a higher-frequency IF (145 MHz) is used for RF upconversion.

The downconversion IF is 7/33 of the ADC clock rate, yielding near-IQ sampling [8]. The low downconversion IF is good for selecting low-$1/f$-noise amplifiers, and for reducing crosstalk. The 94.3 MHz ADC clock rate is high enough that the whole 9-cell $TM_{010}$ passband (1274-1300 MHz) fits in the first Nyquist zone. The high upconversion IF allows commercial four-section tubular filters with 45 MHz bandwidth to remove the undesired sideband after mixing.

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Separating transmit and receive signals in the frequency domain has the added advantage of removing a perennial source of crosstalk from the drive back to RF inputs. There is a small additional complication of needing to generate the upconversion LO; the numbers have been chosen so that a simple divide-by-eight of the downconversion LO produces 165 MHz, which is mixed with the LO and filtered (using another tubular filter) to generate the 1155 MHz upconversion LO.

## LOW NOISE ANALOG/RF DESIGN

An RF Downconverter circuit board uses a 1320 MHz LO, distributed to each of the racks, to generate a 20 MHz IF for digitization. This board uses careful RF design and to achieve typically -90 dB channel-channel crosstalk. It also acts as an LO distribution module for the chassis.

The system's digitizer board [9] is based on the AD9653 four-channel ADC. Its 94.3 MHz sampling clock is derived by dividing the 1320 MHz LO by 14. The digitizer board uses FMC connectors to attach to the FPGA carrier, although it does not adhere to standard mechanical outlines. This board includes two channels of DAC output that synthesize the 145 MHz output used for field control. It also has features that are selected for clean chassis integration in this application, keeping the number of connectors and boards to a minimum.

Both the digitizer and RF downconversion hardware are mounted on a 6 mm aluminum plate to keep their component temperatures stable. They also both use low-noise LDO voltage regulators to avoid injecting noise from power supplies into the signal path. Those low-noise regulators use a capacitor to filter the voltage reference at audio frequencies; non-piezoelectric capacitors are used to avoid picking up environmental mechanical noise (e.g., fans).

Differential phase noise of a completed RF chassis was measured using a 1300 MHz source passively split to two input channels. After digital downconversion, filtering, and decimation, long data traces were saved for analysis. One such resulting differential phase noise power spectrum density plot is shown in figure 2. Between $1/f$ and white noise, power integrals diverge for both low and high frequencies. The final use case with beam-based feedback running (see below) will effectively apply a 1 Hz high-pass filter to this noise; therefore this measured noise can have such a filter applied to it. That curve's low-frequency integral then converges, so it's legitimate to plot the cumulative noise starting at DC. Such a plot is shown in figure 3.

## DRIFT

Weak stability requirements have been set for drift, since instrumentation measuring the high-repetition rate beam will be able to detect drifts in energy and phase of each of the four Linac sections. Attaching this instrumentation to the RF controls is one form of beam-based feedback (BBF). Initially this feedback will operate at the software level, but there is a possibility to upgrade that to a low-latency dedicated-fiber

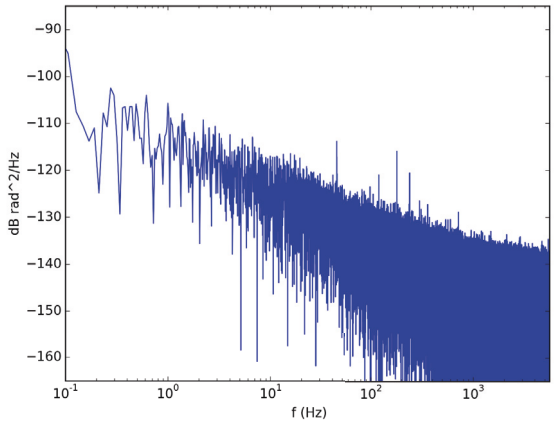


Figure 2: Chassis differential phase noise power spectral density at 1300 MHz.

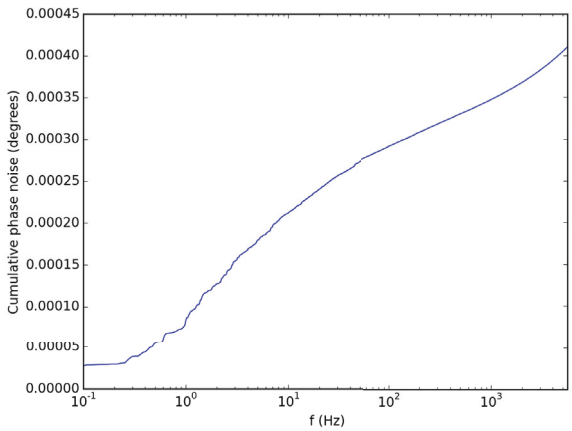


Figure 3: Chassis cumulative differential phase noise.

system, if the project finds evidence that will improve beam quality.

To ease commissioning and improve operability of the machine, many anti-drift techniques have been designed-in. Foremost among these is a phase-averaging reference line, based on earlier designs at SLAC and Fermilab [10], but with the averaging implemented digitally. The installation plan also calls for length-matching the cavity and reference cables in the low energy section of the machine, to compensate for temperature-sensitive electrical length in those *circa* 13 m cable runs.

For both reliability and drift reduction, the control chassis will be installed in racks that are thermally isolated from the service gallery. That gallery is dusty and is known to experience 30°C temperature swings. Using air circulated over a heat exchanger to temperature-stabilized water, the temperature inside the rack should fluctuate less than 4°C.

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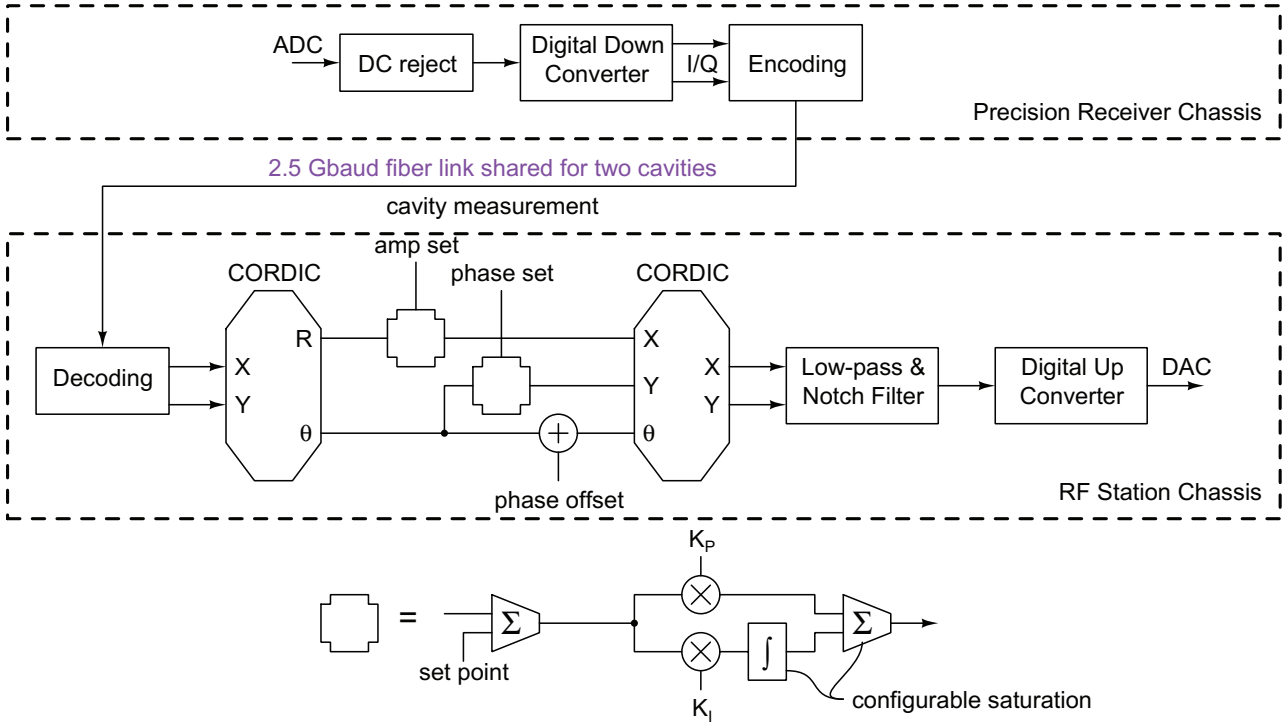


Figure 4: Simplified block diagram of DSP path for field control loop.

## DSP

The core of the DSP design is a Self-Excited-Loop (SEL), which has well understood [11] advantages for operating very narrow-band SRF cavities. Our flexible digital implementation, see figure 4, allows conceptually simple selection of amplitude-locked or not, and phase-locked or not, by adjusting clip limits on the PI controllers for amplitude and phase. The actuator for the phase loop is the reactive (imaginary) component of the drive signal, such that the amplitude loop has no response to cavity detuning. An example of this process working on a cold cavity will be shown later in this paper.

The real and imaginary clip limits will, in the end, be set to align with the power capabilities of the SSA, the fundamental power coupler's $Q$, beam current, and the allocated peak microphonic detuning. The latter is currently set by the project to ±10 Hz.

An input Digital Down Converter (DDC) section converts the IF (7/33 of the ADC sampling rate) to complex number (I and Q) form by means of two-sample FIR filter. Mathematically, two successive ADC samples (with DC offset removed) $y_n$ and $y_{n+1}$ are converted to I and Q according to

$$\begin{pmatrix} I \\ Q \end{pmatrix} = \frac{1}{\sin\theta} \begin{pmatrix} \sin(n+1)\theta & -\sin n\theta \\ -\cos(n+1)\theta & \cos n\theta \end{pmatrix} \begin{pmatrix} y_n \\ y_{n+1} \end{pmatrix} ,$$

where $\theta$ is the phase step between samples, $2\pi \cdot 7/33$ in this case.

The 145 MHz output (203/264 of the 188.6 MHz DAC clock) is synthesized from the computed I and Q drive values.

The last step before upconversion is a combined low-pass filter and notch filter. The low-pass filter is needed to restrict the noise bandwidth sent to the SSA, adjustable to trade off against group delay of the feedback path. The output noise of the system, before limiting by this filter, is defined by broadband ADC noise multiplied by the proportional feedback term, possibly as high as 65 dB. The notch filter is used to avoid exciting the $8\pi/9$ cavity passband. The two filters are combined to minimize the extra delay added by the notch filter.

The gain ($z$-transform representation) of the IIR filter implementing this low-pass and notch combination is

$$\frac{a_1}{1 - z^{-1} - b_1 z^{-2}} + \frac{a_2}{1 - z^{-1} - b_2 z^{-2}}$$

where $a_1$, $b_1$, $a_2$, and $b_2$ are all complex coefficients. A plot for the specific values used in testing, where the low-pass bandwidth was set to 200 kHz and the $8\pi/9$ mode was -752 kHz from center, is shown in figure 5. Note that the notch is shown on the high side, since this filter processes IF, which is frequency inverted compared to the RF.

## TESTING

Prototype LCLS-II cryomodules are in testing at Fermilab and JLab, and prototypes of the RF control system have also been installed there. A photo of one such LCLS-II rack is shown in figure 11. This rack will control and monitor four cavities; it includes three RF chassis, each with six 1300 MHz inputs. Each test facility also has its own set of RF controls; RF splitters have been installed on each cavity's forward, reverse, and probe ports, so that both controllers

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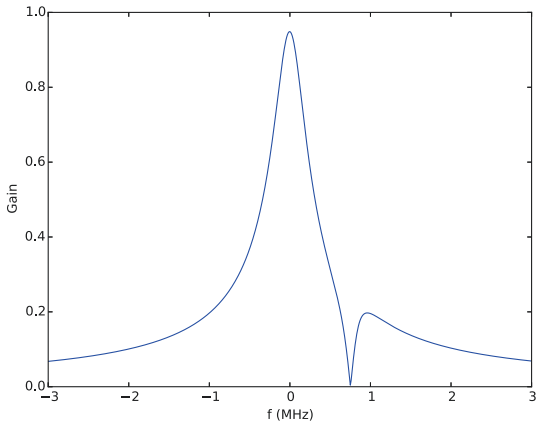


Figure 5: Combined low-pass and notch filter frequency response.

can simultaneously monitor the state of the cavity. This situation is ideal for development and debugging, including the ability to make out-of-loop measurements.

We have demonstrated automated routines running on a general-purpose computer (connected by Ethernet to the rack of FPGAs) bringing a cavity on from scratch. By setting up and analyzing pulsed waveforms, the routines measure such properties as the cavity bandwidth, resonance frequency, SEL phase offset, and plant gain. This gives one-button turn-on to CW closed-loop operation. SEL capabilities allow centering the cavity tune (at the operational gradient) to be considered as a leisurely second step.

Figures 6 through 8 show the digital SEL popping in and out of resonance tracking mode; these data were taken at a time when the cavity static tuning was slightly off. In 0.3 seconds, the system briefly entered resonance-tracking mode six times. The largest phase deviation of the cavity during any of these times was 7.3°. The apparent overshoot and non-ideal transitions between phase-locked and resonance-tracking "modes" (really determined by whether or not the imaginary drive terms has clipped) are an artifact of the waveform recording. That recording only has a bandwidth of 2.8 kHz, but the transitions happen on the 1 $\mu$s time scale. Note that the cavity gradient stays completely fixed during this time, because the amplitude loop continues to operate. Constant field amplitude gives constant Lorentz forces, and therefore no internal excitation of detuning excursions.

The locus of forward drive complex numbers shown in figure 7 nicely shows the vertical line understood by resonance theory for a fixed cavity vector. Once the imaginary part of the drive reaches its clipping threshold, the phase moves freely, and and the locus follows a fixed radius circle.

In-loop phase error measurements are effectively zero, 0.00013° rms over the frequency band 0.1 Hz to 2.8 kHz, while the feedback was generating reactive drive for microphonics suppression of 4.4° rms.

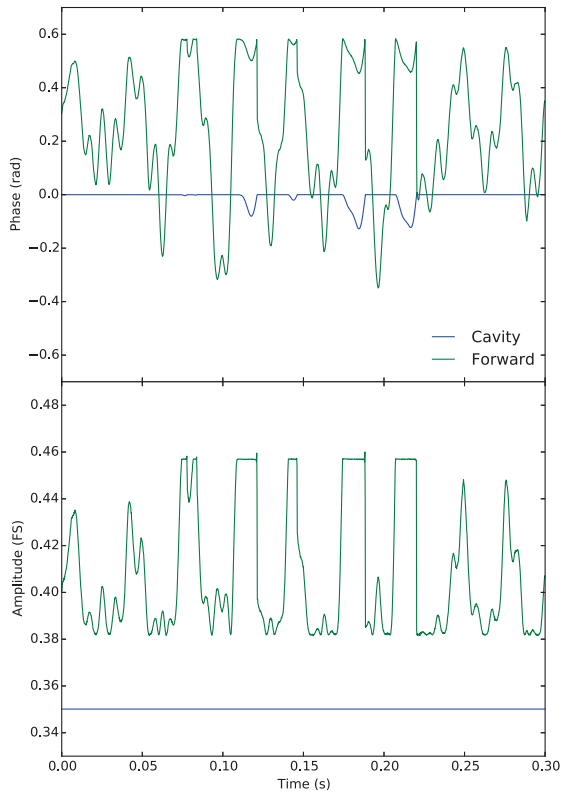


Figure 6: SEL operations with ordinary time axes.

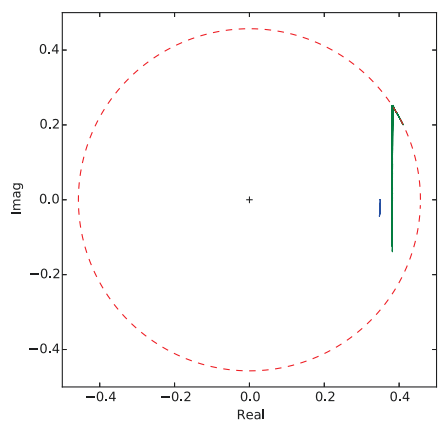


Figure 7: Locus of SEL operations in the complex plane.

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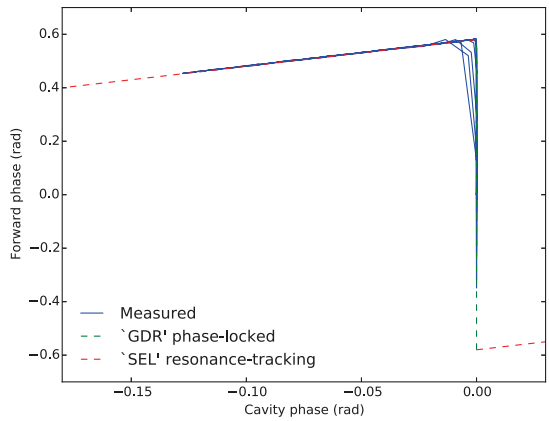


Figure 8: Connection between cavity and drive phase during SEL operations.

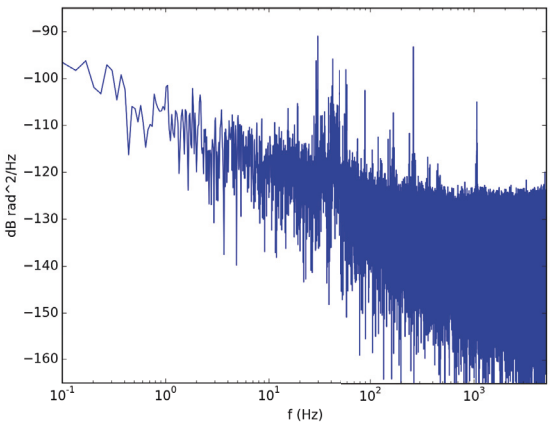


Figure 9: Out-of-loop phase noise power spectrum density.

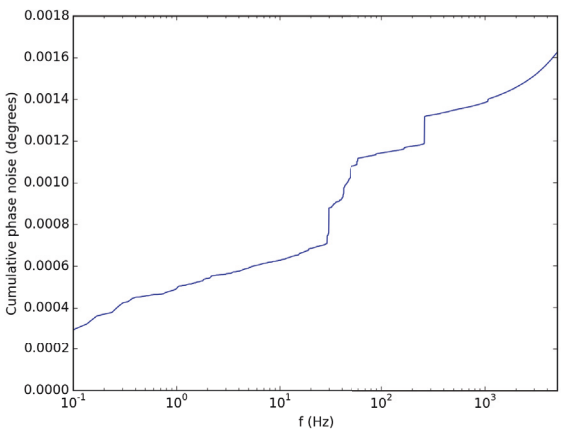


Figure 10: Out-of-loop cumulative phase noise.

Figure 11: Prototype Chassis installed at the FNAL CMTS.

Out-of-loop phase error measurements were taken by the FNAL LLRF system measuring in parallel. Those results are shown in figure 9; the overall phase error is 0.0016° rms over the frequency band 0.1 Hz to 5.0 kHz. A cumulative plot, integrated up from 0.003 Hz, is shown in figure 10. The FNAL data acquisition system has larger white noise and crosstalk than the LCLS-II system, and similar $1/f$ noise. Consequently, this measurement should be considered an upper limit, and the actual performance is still unknown. It's possible to extrapolate some bench measurements to a cavity run at -5 dBFS, to get 0.0005° rms above 1 Hz for a 20 kHz closed-loop bandwidth, but that is not verified.

Actual cavity field variations in the final accelerator will necessarily be larger than the noises quoted above. Cable length variations (including those inside the cryomodule), beam loading, phase reference line contributions, and the ever-elusive unknown unknowns will add to the system errors.

The system stability and transient response was checked for a large number of P and I gain settings, known as a gain scan. Figure 12 shows one such response.

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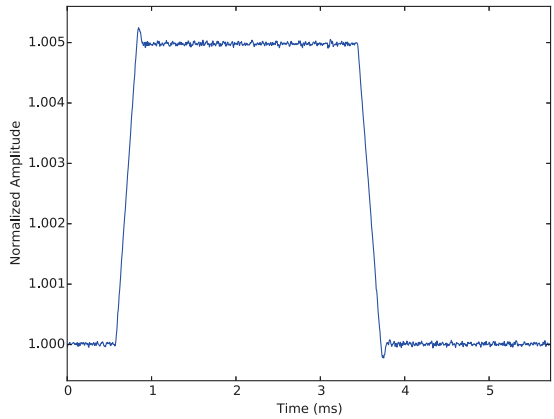


Figure 12: Amplitude loop response to 0.5% setpoint modulation.

## RESONANCE CONTROL

A low-noise digital-input piezo driver has been built, tested, and installed in a resonance control chassis, visible in figure 11 as the chassis second from the top. It (and the piezo actuator in the cryomodule) has demonstrated the ability to tune the cavity both statically and dynamically. When powered on and set to a static value, the detuning noise of its cavity does not measurably increase, thus verifying that the design has met system noise goals.

A detuning computer has been incorporated into the cavity control logic. It tracks the analog state equation to give a live estimate of the $Q$ and detune frequency of the cavity. Based on measurements $M_K$ and $M_V$ of the drive and cavity vectors, and a complex calibration constant $B$,

$$a = \frac{1}{\vec{M}_V} \cdot \left[ \frac{d\vec{M}_V}{dt} - B\vec{M}_K \right]$$

is computed as the exponential coefficient of the cavity equation; therefore $-1/\Re(a)$ is the time constant, and $\Im(a)$ is the detune frequency in $s^{-1}$. This equation holds for every operating mode of the controller, and is useful as long as the cavity field measurement is large enough to not suffer from dividing two very small numbers. Information from the real part of $a$ may become one source of quench interlock. Detune information will be sent to the resonance control chassis, initially just for low-frequency correction of helium pressure drifts.

There are ongoing experiments by Fermilab microphonics experts to develop DSP code and supporting software that can actively suppress narrow-band source terms by using the piezo actuator. The LCLS-II LLRF hardware has the capability to incorporate that functionality once it is understood.

Stepper motor drivers are also included in the resonance control chassis. These drivers take special attention because the motors are cryogenic. Even if microstepping is used for smoothness of motion, the drive currents have to be set to zero—implying that the motor is resting on a full-step—when the motor is not actively moving. The stepper motors are also essential for parking the tuners in a safe state for cavity warm-up.

## 3.9 GHZ

Sixteen 3.9 GHz cavities in two cryomodules will also be part of the final LCLS-II accelerator. These harmonic cavities are critically important for manipulating the curvature of the bunches in longitudinal phase space. While the phase stability requirements have been specified as the same as given for the 1.3 GHz systems, in time domain this is three times more stringent.

A 3.9 GHz down- and up-conversion strategy has been planned that shares infrastructure and resources with the 1.3 GHz systems. The FPGA and digitizer hardware, and even the ADC and FPGA clock rates will be identical to that used in the 1.3 GHz systems. A 3920 MHz LO will be used for downconversion to the same 20 MHz IF. A two-stage upconversion process will start with a synthesized 60 MHz IF. Frequency triplers will be used to attach the phase reference line to the PRC reference inputs. Initial prototypes of these RF chains have shown promising results in bench tests.

## PLANS

With clear evidence from cryogenic cavity tests that the prototype LCLS-II LLRF system meets critical performance specifications, the system is ready for its Final Design Review. The system's production and installation will follow shortly thereafter. SLAC will lead that effort, with support from the other collaborating laboratories. During the system's checkout and commissioning phase, the technical responsibilities of each lab within in the collaboration will be migrated to SLAC via a Lead, Mentor, and Consult transition plan.

LCLS-II as a whole may not achieve final performance goals until some time after first light and the transition to operations. LLRF performance optimization and software maturation will continue as the operating beam current increases and performance expectations rise.

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