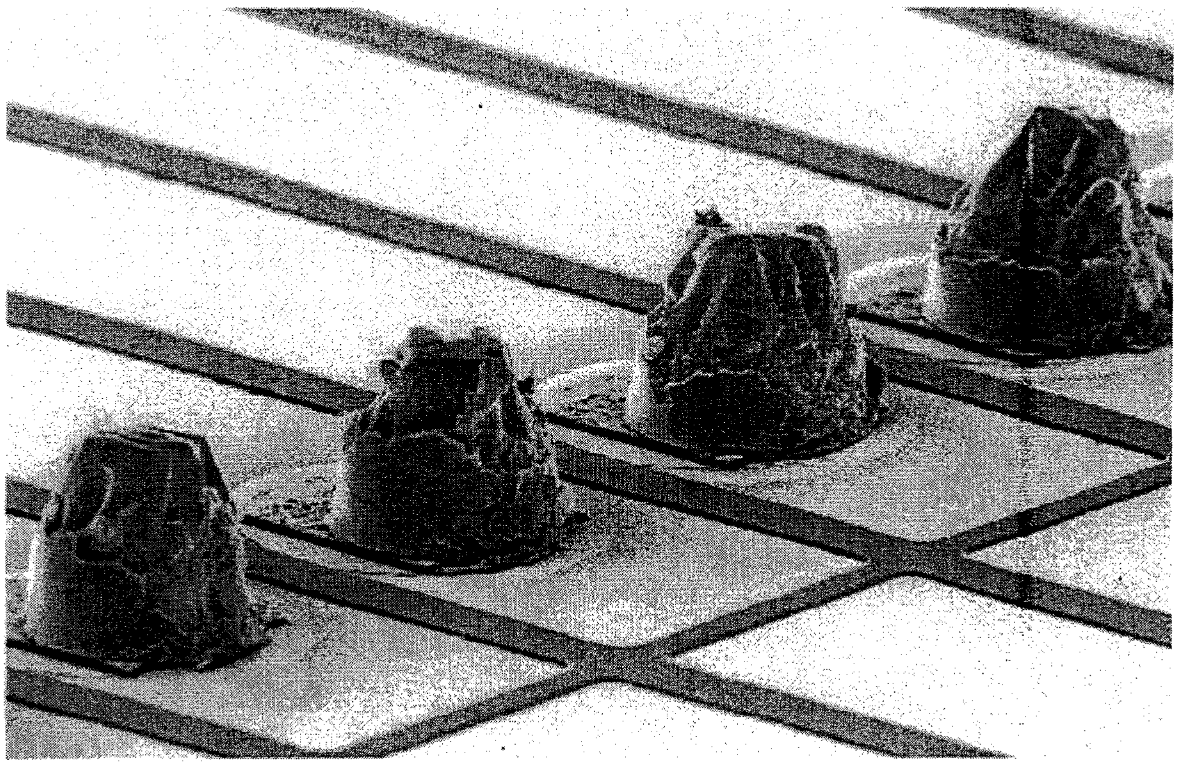
Fermilab-CONF-98/196

Proceedings of PIXEL98 - International Pixel Detector Workshop



May 7-9, 1998
Fermi National Accelerator Laboratory
Batavia, Illinois

Editors
David F. Anderson
Simon Kwan

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Distribution

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Preface

Experiments around the globe face new challenges of more precision in the face of higher interaction rates, greater track densities, and higher radiation doses, as they look for rarer and rarer processes, leading many to incorporate pixelated solid-state detectors into their plans. The highest-readout-rate devices require new technologies for implementation. The PIXEL98 Workshop (Fermilab, May 7-9, 1998) reviewed recent, significant progress in meeting these technical challenges. Participants presented many new results; many of them from the weeks – even days – just before the workshop.

Brand new at this workshop were results on cryogenic operation of radiation-damaged silicon detectors (dubbed "the Lazarus effect"). Other new work included a diamond sensor with 280-micron collection distance); new results on breakdown in p-type silicon detectors); testing of the latest versions of read-out chip and interconnection designs; and the radiation hardness of deep-submicron processes.

Approximately 100 attendees from all the major high-energy physics efforts throughout the world, over half from non-U.S. institutions, came to Fermilab for the meeting. Simon Kwan of Fermilab chaired the international and local organizing committees for the workshop.

Given the scale of the detector systems and the technologies involved, solving the technical problems requires close collaboration with industry. Finding solutions for bump-bonding (the assembly of readout chips to sensors), multiple chip assembly, radiation-hard electronics, and advanced material use all require joint industry-laboratory effort. Thus, the active participation of industry, particularly with bump-bonding/flip-chip capability, was a highlight of the workshop. The vendors participated in the formal presentations and in a less formal poster session and reception on the workshop's first evening.

Despite differences in physics goals and experiment environments among participants, the themes of precision spatial resolution, two-dimensional information for pattern recognition, high radiation tolerance, large amounts of data, and low mass emerged as key factors.

Two groups with experience running large scale tracking systems of silicon pixels (DELPHI and WA97/NA57), four groups planning to use large tracking systems (ATLAS, CMS, ALICE, and BTeV), and one group planning to use pixel detectors in hybrid photon detectors (LHCb RICH) gave presentations in a systems requirements session. The extremely clean Omega signal, extracted by WA97 without kaon identification from events often containing more than 50 tracks reconstructed in a 5 cm x 5 cm telescope, provided a dramatic demonstration of the pattern recognition power of pixel detectors.

The full-to-bursting session on readout electronics included ten presentations. Most of the talks described progress made by groups designing readout systems for the LHC experiments. There, the pixel detectors and readout schemes are very different: rectangular pixels vs. square pixels; "binary" vs. "digital" vs. "analog" readout. CMS also plans to use an (octal) analog encoding scheme to reduce the pin count and number of bus lines required to transmit inherently digital information, such as pixel addresses. However, some similarities are emerging, notably leakage-current tolerance provided by a nonlinear, synthetic resistor in the preamplifier feedback circuit and the use of a three-bit DAC to provide cell-to-cell discriminator threshold trimming. Much of the hallway conversation outside the meeting room focused on the possibility that standard CMOS processes with "deep submicron" (0.25 micron and below) feature size may be inherently radiation hard; and on the continued mystery of the increased noise seen by many groups after bump bonding.

A session on detectors focused on radiation damage and techniques to mitigate its effects. An overview of the physics of radiation damage in silicon detectors by Zheng Li (BNL) opened the session. Vittorio Palmieri (Bern) presented just-completed work on the resurrected operation at cryogenic temperatures of very radiation-damaged silicon detectors (the Lazarus effect) and on the cryogenic operation of silicon as an ionization chamber with ohmic contacts. William Trischuk (Toronto) presented results on a diamond sensor with 280 micron collection distance, a new record, and a bump-bonded diamond pixel detector. New work was also presented on p-type silicon detectors (Gino Bolla, Purdue), and on progress on the first fabrication run of 3-dimension detectors by Sherwood Parker (Hawaii). The meeting highlighted the differences in guard-ring structures in the CMS and ATLAS prototypes.

The session on bump-bonding included presentations from four vendors. These talks covered the basics of bump bonding, techniques used, pros and cons of indium versus lead-tin solder, flip-chip mating, and results on failure rate. Results from ATLAS and CMS on the yield rate for their prototype module assembly studies were also presented.

An interconnection and data readout session featured talks from ATLAS, CDF and CMS. The talks ranged from flexible circuit and optical data transmission technology developments (Mark Bailey of New Mexico and Pat Skubic of Oklahoma on the first of these, and Yi-Cheng Liu of Academia Sinica on the second) to control circuits (Robert Stone of Rutgers). The results for multilayer circuits on flexible plastics, in particular, showed new successes. Peter Gerlach (Wuppertal) described the unique ATLAS plan for combining some of the flexible-circuit and control-chip functions.

The infrastructure session focused on the fabrication, design, and cooling of the ALICE, ATLAS, and CMS pixel detectors. A number of talks featured the use of light-weight carbon composite materials for structure and cooling. Work on evaporative cooling for ATLAS is well advanced and looks promising. The close of the session featured a comprehensive presentation of the alignment and performance of the SLD CCD pixel detector by Glen Crawford (SLAC).

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Sensor development: D. Anderson, *Fermilab*, Z. Li, *BNL*
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Interconnection and data readout: K-H. Becks, *Wuppertal*, S. Schnetzer, *Rutgers*
Bump bonding: G. Grim, *UC Davis*, M. Campbell, *CERN*

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Participants Email Addresses

ALAM	Saj	msa90@cnsvax.albany.edu	University at Albany
ANDERSON	David	dfa@fnal.gov	Fermilab
ANTINORI	Federico	federico.antinori@cern.ch	INFN - Sezione di Padova
APPEL	Jeffrey	appel@fnal.gov	Fermilab
ARTUSO	Marina	artuso@suhep.phy.syr.edu	Syracuse University
ATAC	Muzaffer	matac@fnal.gov	Fermilab
BAILEY	M.	mwb@fnal.gov	University of New Mexico
BARBOSA	Ademarlaudo	laudo@novell.cat.cbpf.br	CBPF
BARNETT	Bruce	bab@jhu.edu	Johns Hopkins University
BARSOTTI	Edward	barsotti@fnal.gov	Fermilab
BECKS	Karl-Heinz	becks@wpcl1.Physik.uni-wuppertal.de	University of Wuppertal
BENJAMIN	Doug	dbenjamin@fnal.gov	CDF/TTU - FNAL
BINTINGER	David	davidb@lbl.gov	Lawrence Berkeley National Lab
BORTOLETTO	Daniela	bortoletto@purdd.physics.purdue.edu	Purdue University
CAMPBELL	Michael	michael.campbell@cern.ch	CERN
CANCELO	Gustavo	cancelo@fnal.gov	Fermilab
CANTATORE	Eugenio	eugenio.cantatore@cern.ch	CERN
CHARLES	Eric	echarles@slac.stanford.edu	University of Wisconsin
CHERRY	Michael	cherry@phunds.phys.lsu.edu	Louisiana State University
CHEUNG	Harry	cheung@fnal.gov	Fermilab
CHIEN	C.-Y.	cyc@jhup.pha.jhu.edu	Johns Hopkins University
CHRISTENSEN	Maja	maja@fnal.gov	Fermilab
CHRISTIAN	David	dcc@fnal.gov	Fermilab
CRAWFORD	Glen	gdc@slac.stanford.edu	SLAC
CREMALDI	Lucien	cremaldi@fnal.gov	
D'AMBROSIO	Carmelo	carmelo.d'ambrosio@cern.ch	CERN
DARBO	Giovanni	darbo@ge.infn.it	INFN
DEMARIA	Natale	lino.demaria@cern.ch	CERN

DOWNING	Robert	rwd@fnal.gov	Fermilab
EINSWEILER	Kevin	einsweiler@lbl.gov	Lawrence Berkeley National Lab
FORMENTI	Fabio	fabio.formenti@cern.ch	CERN
GABATHULER	Kurt	kurt.gabathuler@psi.ch	Paul Scherrer Institut
GAGLIARDI	Guido	gagliardi@infnge.ge.infn.it	Universita' di Genova
GENAT	Jean-Francois	genat@in2p3.fr	Universite Paris 6
GERLACH	Peter	peter.gerlach@cern.ch	University of Wuppertal
GILCHRIESE	Murdock	gilg@lbl.gov	LBNL
GRIM	Gary	gpgrim@ucdavis.edu	University of California, Davis
GUIDI	Guido	info@caen.it	C.A.E.N. SpA
HALLEWELL	Greg	GREGH@CPPM.IN2P3.FR	Centre de Physique des Particules de Marseille
HOFF	James	jimhoff@fnal.gov	Fermilab
HONSCHEID	Klaus	kh@mps.ohio-state.edu	Ohio State University
HOPMAN	Pablo	pih@lns62.lns.cornell.edu	Cornell University
HUMPSTON	Giles	giles.humpston@gecm.com	GEC-Marconi Materials Technology Ltd
KAGAN	Harris	kagan@mps.ohio-state.edu	Ohio State University
KARIM	Zaheed	eekarim@usthk.ust.hk	HKUST/AIT
KLEMPT	Wolfgang	wolfgang.klempt@cern.ch	CERN
KUHL	Thorsten	kuhl@physik.uni-bonn.de	Universitaet Bonn
KWAN	Simon	swalk@fnal.gov	
LAI	Adriano	adriano.lai@ca.infn.it	UNIVERSITA' DI CAGLIARI
LANDER	Richard	lander@ucdhep.ucdavis.edu	UCD
LI	Zheng	zhengl@bnlarm.bnl.gov	Brookhaven National Lab
LIU	Yi-Cheng	liu@fnal.gov	Academia Sinica, Taiwan
MAESTRO	Paolo	maestro@galileo.pi.infn.it	Unversity of Pisa and INFN-Pisa
MANI	Sudhindra	mani@ucdhep.ucdavis.edu	University of California, Davis
MANN	Lawrence	mannl@advceramics.com	
MEKKAOUI	Abder	mekkaoui@fnal.gov	Fermilab
MILLER	William O.	womiller@hytecinc.com	
MORANDO	Maurizio	Morando@pd.infn.it	University of Padua

PALMIERI	Vittorio	vittorio.palmieri@cern.ch	University of Berne
PARKER	Sherwood	sher@slac.stanford.edu	Lawrence Berkeley National Lab
PAULY	Louise	lpauly@ibm.net	
PELLETT	Dave	pellett@ucdhep.ucdavis.edu	University of California, Davis
PICCIOLO	Carol	carol@fnal.gov	Fermilab
REAY	Bill	reay@phys.ksu.edu	Kansas State University
RENARD	Stephane	n/a	TRONICS
RUBEN	Andreas	sales.us@wiener-d.com	
RUSS	James	russ@fnal.gov	
SAHU	Saroj K.	sahu@uhheph.phys.hawaii.edu	Univ. of Hawaii
SAZAMA	Cynthia M.	sazama@fnal.gov	Fermilab
SCHNETZER	Stephen	steves@ruthep.rutgers.edu	Rutgers University
SEIDEL	Sally	seidel@hepv1.phys.unm.edu	University of New Mexico
SELLER	Paul	seller@rl.ac.uk	Rutherford Lab
SELLINGER	Diane	sellinger@fnal.gov	Fermilab
SELOVE	Walter	ws@upenn5.hep.upenn.edu	University of Pennsylvania
SENYO	Katsumi	senyo@fnal.gov	Fermilab
SHEAFF	Marleigh	sheaff@fnal.gov	University of Wisconsin
SHIPSEY	Ian	shipsey@purdd.physics.purdue.edu	Purdue University
SKUBIC	Pat	skubic	University of Oklahoma
SNOEYS	Walter	walter.snoeys@cern.ch	CERN
SPIEGEL	Leonard	lenny@fnal.gov	Fermilab
STONE	Sheldon	stone@suhep.phy.syr.edu	Syracuse University
STONE	Robert	stone@physics.rutgers.edu	Rutgers University
STROLOGAS	John	strolog@hepux5.hep.uiuc.edu	University of Illinois at Urbana-Champaign
TRISCHUK	William	jtrischuk@fnal.gov	University of Toronto
TSUKAMOTO	Toshio	ttoshio@cc.saga-u.ac.jp	Saga University
TUMER	Tumay	tumay.tumer@ucr.edu	University of California
WESTER	William	wester@fnal.gov	Fermilab
WHITMORE	Julie	jaws@fnal.gov	Fermilab
WOLF	Juergen	wolf@izm.fhg.de	FhG-IZM
YAREMA	Raymond	yarema@fnal.gov	Fermilab

ZIMMERMANN	Sergio	zimmer@fnal.gov	Fermilab
ZIOCK	Hans-Joachim	ziock@lanl.gov	Los Alamos National Lab

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Construction and Performance of the WA97/NA57 Silicon Pixel Telescope

E.Cantatore representing the CERN WA97, RD19 and NA57 collaborations
CERN/EP, Geneva

Abstract

The silicon pixel telescope installed in WA97 has gradually upgraded from the first 72k pixel plane tested in 1993 to the present 13 planes telescope, which was successfully commissioned in the first run of NA57 (1997).

This 1.1 million channel detector is described along with some of its important characteristics, such as the spatial resolution (~12um) and the time resolution (16ns r.m.s for the Omega3 planes). Special emphasis will be put on the construction of the telescope and on how various procedures and systems ensured reliable operation of this detector.

In the high track multiplicity environment of central Pb-Pb interactions, where any other kind of detector would fail, the pixel telescope provided in the last four years of runs the precise measurements needed to achieve the physics goals of the WA97 experiment.

Introduction

The WA97 [1] and NA57 [2] experiments study strange and multi-strange baryon and anti-baryon production in central Pb-Pb collisions at CERN SPS. The extremely high multiplicity of such events yields a large number of simultaneous hits in the sensitive apparatus (fig.1). Pixel detectors were chosen as tracking devices in this environment for their high spatial resolution and their unambiguous two-dimensional information [3].

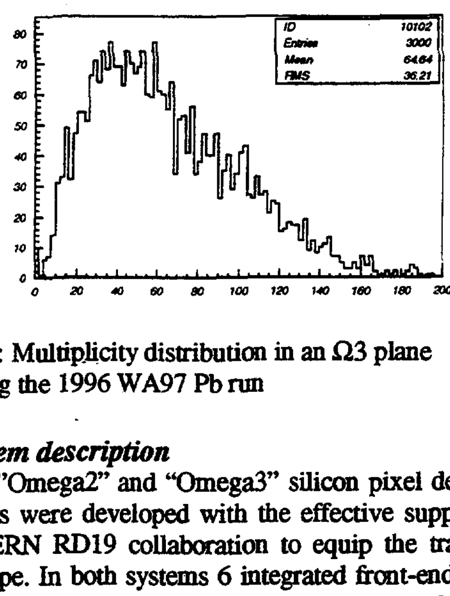

Fig.1: Multiplicity distribution in an $\Omega3$ plane during the 1996 WA97 Pb run

System description

The "Omega2" and "Omega3" silicon pixel detector systems were developed with the effective support of the CERN RD19 collaboration to equip the tracking telescope. In both systems 6 integrated front-end/read-out chips are bump bonded to a silicon detector segmented in pixels. Several of these modules, called "ladders" are assembled on a thin ceramic carrier to form an "array". Two arrays, suitably staggered, cover hermetically an area of 5×5 cm^2 and form a "plane". The tracking telescope is built from several planes aligned one after the other on a mechanical frame.

In the Omega2 system the pixel size is 75×500μm^2, and each pixel electronic cell contains a charge preamplifier, a discriminator with adjustable threshold, a delay element and a coincidence unit. The output is recorded in a flip-flop that can be read out through a shift register [4]. Each Omega2 front-end/read-out chip contains 1006 sensitive cells and 16 cells connected to an electric test input.

The Omega3 chip consists of 2032 sensitive cells sized 50×500μm^2. Two flip-flops per cell allow to test and mask each channel individually, so that Omega3 chips can be fully tested at the wafer level. Three additional bits per pixel control a tunable delay line that can be used to finely adjust the timing of the different cells [5]. Thanks to the introduction of this distributed digital control a very accurate time resolution (6ns r.m.s. after tuning the delay lines) was achieved with the $\Omega3$ chips [6].

The carrier on which $\Omega3$ ladders are assembled is manufactured on a ceramic support and consists of five conductive Al layers separated by Al_2O_3 dielectric. Its overall thickness is about 400μm. The carrier was designed in order to provide good decoupling and low impedance connection to the power supplies [7].

The telescope which was successfully commissioned in the 1997 proton run of NA57 consists of seven $\Omega2$ and six $\Omega3$ planes, for a total of 1 092 240 channels. It contains 84 $\Omega2$ ladders, coupled to 504 readout chips and 48 $\Omega3$ ladders, bonded to 288 readout chips.

Each array in the telescope is read out by a VME system, consisting of two PCBs equipped with programmable logic (LCAs) and standard CMOS and TTL ICs. One card, the "motherboard", is directly connected to the array, via a flexible epoxy PCB. The

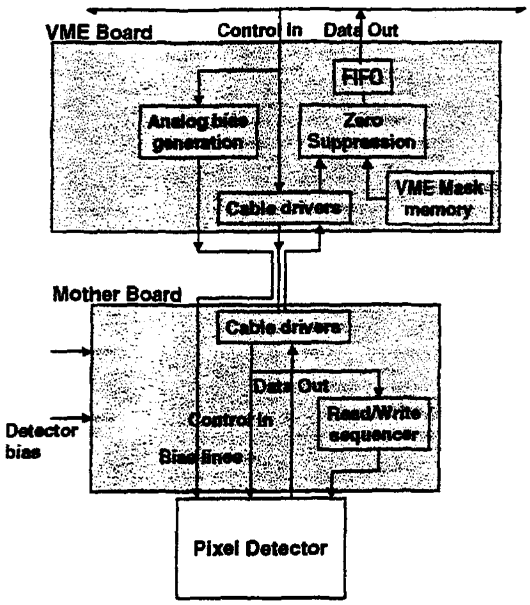

Fig.2: Block diagram of the Ω3 VME system

motherboard is then connected to the VME card, located in the control room, through a 30m 100 twisted pair cable. A block diagram explaining the functions of both cards is shown in fig.2.

The Ω3 VME system provides a bi-directional link between the VME bus and the pixel array. This allows to download the values of the different control registers in the pixel chips and to read out the data coming from the detector.

The readout frequency is 4MHz, due to the low speed of the programmable logic. Two chips are read out in parallel to form a 32bit data word which complies with the VME standard. Each card can read an array (49 152 pixels) in ~400μsec, suppressing the words that contain only zeros. A FIFO provides a buffer between the detector system and the VME bus.

A second level of masking and 5 DACs which provide the analogue bias currents for the integrated electronics are also included in the VME board.

To ensure reliable operation of the telescope during data taking, a cooling and a slow control system were also designed and implemented inside the NA57 spectrometer. . .

We observed that local heating of the detector by the integrated readout electronics can cause a significant rise in the leakage current. This increases electronics noise, so that more channels become permanently active and the temperature tends to rise further. This dangerous thermal runaway can effectively be counteracted by cooling the detectors. A simple scheme, in which each Ω3 plane is fluxed with ~10l/h of 5-10°C N_2 proved to be effective in reducing the frequency of the runaway (which was observed only once in the week of commissioning run of NA57).

The slow control system (fig. 3) provides the detectors bias for all the planes and the power supply for the Ω3 integrated electronics [8]. All leakage currents and the power consumption of the Ω3 arrays are constantly monitored. If any of the currents exceeds its preset value, the array affected by the fault is switched off and an alarm is sent to the shifter, who can start an automatic recovery procedure, or call the expert.

A graphic interface developed under Labview provides an easy way to check all the parameters, to keep a logbook of their history and to change the defaults.

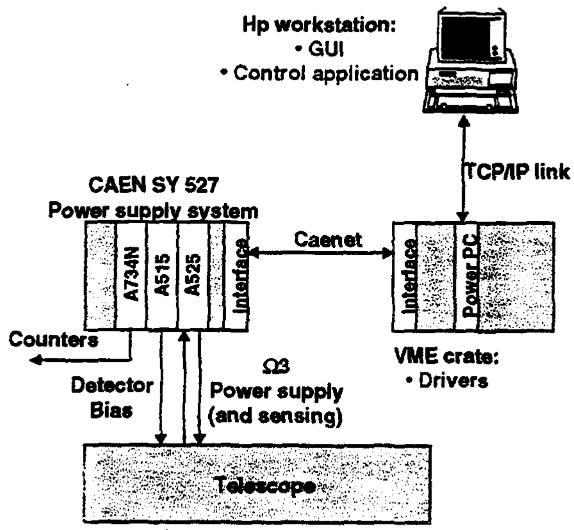

Fig.3: Block diagram of the NA57 slow control system

Telescope production

Several phases of manufacturing and testing have to be properly performed in order to produce the pixel detectors used in WA97/NA57.

Ω3 chips are tested at wafer level by means of a fully automated tester developed "in house". This system integrates a VME processor, the Ω3 VME readout, an automatic probe station controlled via GPIB, a set of DACs and ADCs and a CAMAC Programmable Delay Generator [9]. It is able of running a full functional test of the Ω3 chip in ~100s , checking the following parameters:

- value of the analogue bias currents
- functionality of all control registers
- tristate operation of the output buffers
- response of the front end to the electrical test
- number of "blinking"[1] pixels
- minimum and maximum internal delay

[1] Pixels that exhibit a non-poisson noise distribution and have to be masked during normal detector operation are referred to as "blinking"

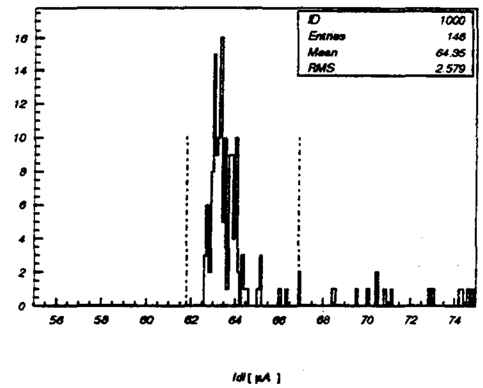

Fig. 4: Distribution of the delay control current (Idl) on one Ω3 wafer

In order to pass the test each chip must have perfect digital and I/O functionality, fewer than 128 pixels not responding to the test pulse and fewer than 300 blinking pixels. Moreover, all the analogue bias currents have to stay within one σ from the mean value measured on the whole wafer.

Figure 4 shows, for example, the distribution of the delay control current on a Ω3 wafer [9]. The lines represent the one σ cut level.

Known good die are flip-chip bonded by means of Sn-Pb solder bumps to the detector ladders [10].

The quality of the bump bonding is checked by means of a second probe test. The detector on top of each chip is exposed to a Sr^{90} source and 0.5 to 1×10^6 random triggers are recorded, in order to produce a source profile. Fig. 5 shows the results of such a test on a Ω3 ladder: the six chips and the shadow of the needle used to bias the detector backplane are clearly visible. Only detectors with a bonding yield better than 95% are selected for assembling onto the ceramic carrier.

The completed array undergoes a severe final test. All chip registers are tested again, blinking pixels are located and masked and a VME level mask is also generated. The threshold of each pixel is estimated electrically [6] and the bias currents are tuned to ensure 100% particle detection efficiency for a 300μm detector (max. threshold <9000e⁻ [11], [12]). The array is exposed to a Sr^{90} source to check the bump bonding quality after the mechanical and thermal stresses induced by manufacturing. Fig.6 shows the source profile recorded on a Ω3 array with very good bonding yield. The delay of each pixel is finally tuned in order to optimise time resolution [6].

Telescope performance

After masking blinking pixels the spurious hit rate of the Ω2 part of the telescope measured in the WA97

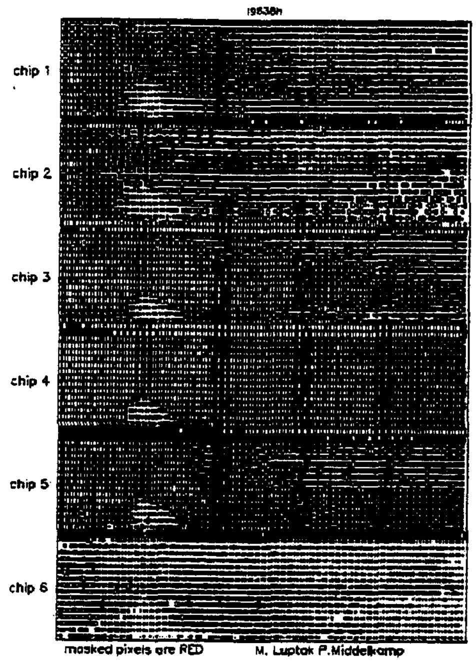

Fig.5: Ladder test with a Sr^{90} source. Chips are contacted one a time for the test. This cause pixels on the edge colums to be floating and thus more noisy.

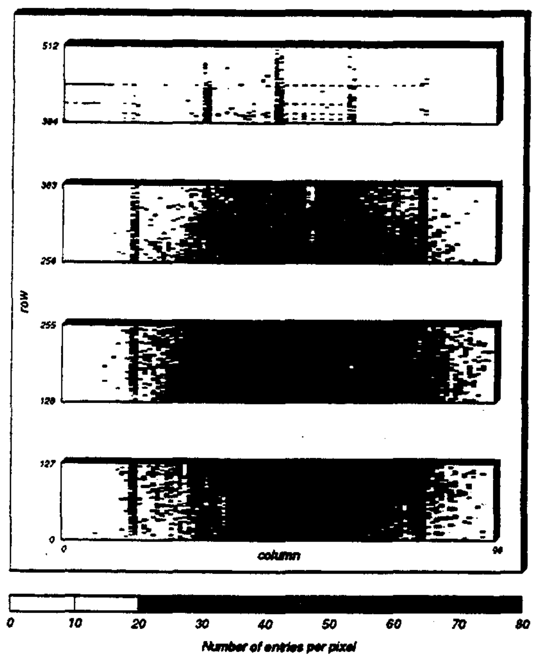

Fig.6: Profile of a Sr^{90} source seen by an Ω3 array. Two millions random triggers were recorded.

spectrometer is $<10^{-10}$ [11]. Taking into account all dead areas and the chips damaged after the array assembly[2], the efficient detector area is 95% for the Ω2 planes and 93% for the Ω3 detectors. Power consumption is 1.1W/array for the Ω2 and 1.8-2.3W/array for the Ω3 system. The consumption per pixel is practically the same in the two detectors. Full efficiency is achieved in both Ω2 and Ω3 detectors for a bias voltage ≥30V [12], [13]. The measured spatial resolution for all the tracks is 23μm in the Ω2 planes [14] and 12μm in Ω3 detectors [12]. The timing resolution of the Ω3 system, measured with both electric stimuli and high energy particle beams is 6ns r.m.s for a single chip and 16ns r.m.s for an array, after tuning the delay adjust registers.

Figure 7 shows the proton beam profile recorded by an Ω3 plane in the NA57 experiment. For more extensive and detailed information on the performance of both the Ω2 and Ω3 systems, the reader can refer to references [6] and [11] - [14].

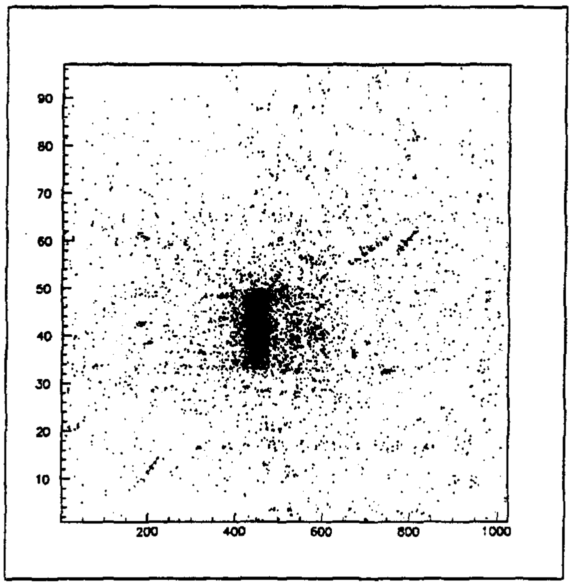

Fig.7: Proton beam profile recorded by an Ω3 plane during the 1997 NA57 run.

Conclusions

Both the Ω2 and the Ω3 pixel system proved to be precise and reliable tracking detectors during four years of operation in WA97 and NA57. They also demonstrated to be capable of handling very high multiplicity events that would have caused any other detector system to fail.

[2] Chips can be damaged while assembling the arrays by Electro Static Discharge or by errors in the mechanical handling

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The Delphi Pixel Detector, running experience and performance

Natale Demaria[a] on behave of the Delphi Pixel Group

CERN, Geneva, Switzerland;
CPPM, Universitè Aix de Marseille II, Marseille, France;
IEK- Universität Karlsruhe, Karlsruhe, Germany;
Università di Milano and INFN, Milano, Italy;
LPNHE, IN2P3-CNRS, Universités Paris VI et VII, France;
Charles University, Praha, Czech Republic;
Collège de France, LPC, IN2P3-CNRS, Paris, France;
Wuppertal Universität, Wuppertal, Germany;
ISN, Grenoble, France.

[a] CERN, CH-1211, Geneva23, Switzerland

The DELPHI Silicon Tracker has been optimised to satisfy the requirements of the LEP2 programme. It is made of a barrel part made by microstrip silicon detectors, upgraded from the old Vertex Detector, and the Very Forward Tracker (VFT) in the endcaps, composed on each side by two layers of pixel detectors and two layers of ministrip detectors. The use of pixels is crucial to allow stand alone pattern recognition thanks to the unambiguous three-dimensional determination of the track hit and the high efficiency. This dramatically improves the forward tracking in terms of efficiency and quality in the angular region between 25° and 10° w.r.t. the beam axis.

The Pixel Detector comprises 1.2 million pixels of 330 × 330 μm^2 size with 152 multi chip modules. It was partially installed in 1996, was completed in 1997 and it has collected data for two years. Module efficiency above 96 % and noise level below one part per million have been achieved.

A description of the detector is given and the running experience is reported. Results obtained are presented and the contributions to the forward tracking are shown.

1. Introduction and Motivations

The Delphi Silicon Tracker[1] is designed in order to satisfy the requirements posed by the physics programme at LEP2. The design takes into account the need for good hermeticity, giving emphasis to a good coverage of the tracking in the forward region[2], particularly important at LEP2 because of the following features of the processes studied or searched for:

- four fermion processes, important for both standard and non standard physics are relatively frequent, hence a larger angular coverage in polar angle is required compared to Z^0 physics.
- processes with the largest cross section, such as $e^+e^- \to q\bar{q}\gamma$ or $e^+e^- \to \gamma\gamma$ produce particles predominantly in the forward direction

The tracking below 25° for the Z^0 programme is provided by the forward wire chambers FCA and FCB[3] located far away from the interaction point, at Z = 155 cm and Z = 275 cm respectively and after more than one radiation length of material. The presence of γs confuses the tracking of forward wire chambers because of the high probability to shower before or between them, therefore creating a region with high density of hits belonging to the shower. In hadronic jets, where all π^0 particles decays into two γs, this causes both a low tracking efficiency and several unassociated neutral clusters in the electromagnetic calorimeters. To improve this situation for LEP2 it has been necessary to build a tracking detector close to the interaction point and able to provide stand alone pattern recognition.

The Silicon Tracker is the upgrade of the Delphi Vertex Detector[4]. The acceptance of the barrel part is extended from 40° to 25° in polar angle and it is made of microstrip silicon detectors, two layers out of three measuring both coordinates. In the barrel region the pattern recognition relies mainly on the tracking detectors, the most important of which is the TPC. In the forward region strip detectors alone are not capable of providing stand alone pattern recognition, due to the enormous amount of spurious combinations of hits and ghosts tracks that would arise.

For this reason pixel[5] detectors are adopted, in order to provide unambiguous three dimensional points with which to build tracks elements with high purity and efficiency. Naively, it could seem an ideal solution to use several layers of pixels detectors, but studies show that a combination of two internal layers of pixel detectors and two external layers of ministrip detectors is an adequate choice, and furthermore reduces substantially the cost of the project. The choice of the cells dimensions is determined by the fact that momentum resolution is limited anyway by Coulomb scattering such that a hit resolution of 100 μm is sufficient.

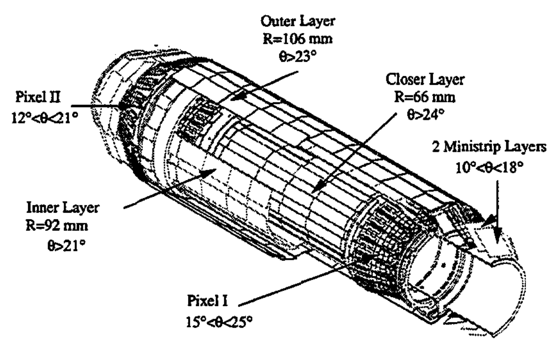

Figure 1. *Layout of the DELPHI Silicon Tracker*

The endcaps of the Silicon Tracker are therefore composed of two layers of pixel detectors, with cells of 330×330 μm^2, and two layers of back-to-back ministrips detectors with readout pitch of 200 μm and one intermediate strip. The endcaps cover the angular region $10° - 26°$ and $154° - 170°$ and they are called Very Forward Tracker (VFT in the following). The Silicon Tracker is illustrated in figure 1.

The design of the VFT has to satisfy the mechanical requirements on the Silicon Tracker. The space constraints are provided by the inner radius of the Inner Detector and the radius of the beam pipe and the total length of the detector must be limited to 1050 mm, in order to be able to install the structure inside DELPHI. The mechanical design must also be sufficiently rigid to support all components and suffer as little stress as possible from the varying deformations of the different components with changes of temperature, humidity, etc. At the same time, the extra support material must be kept to a minimum, so as to maintain the previous performance for the Rϕ impact parameter resolution in the barrel section. Figure 2 shows diagrammatically a cross section

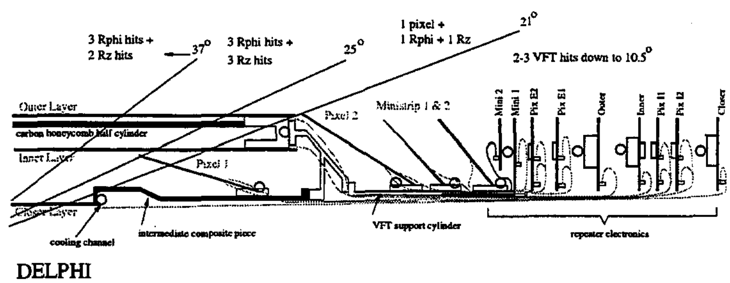

Figure 2. *Cross section of one quadrant of the Silicon Tracker for z>10cm*

of the modules and supports for one quadrant of the detector. It is evident how little is the space available for the internal pixel layer that is accommodated inside the Barrel part and this determines an angle of inclination of only 12° w.r.t. the beam axis.

The mechanical support consists of light aluminium endrings joined by carbon-honeycomb half cylinders. The internal pixel layer is accommodated on a composite piece that connect the endring of the Barrel closer layer with the Barrel endrings. The thermal expansion coefficients between the components are matched to reduce mechanical stress.

An adaptor piece connects the barrel to the forward cylinders. The forward cylinders support the external pixel layer and the two ministrips layers, and also serve to route the kapton cables towards the repeater electronic boards.

The resulting structure maintains the amount of material in the barrel at a similar level to the 1994-95 Vertex Detector, and moves forward material to significantly lower polar angles than previously. A photograph of part of the detector can be seen in figure 3.

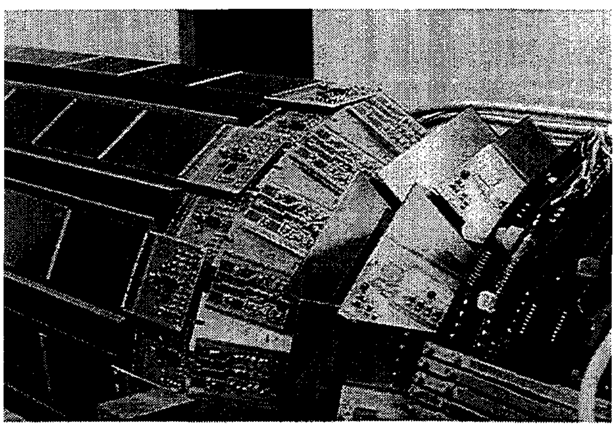

Figure 3. Photograph of part of the detector showing from left to right Rz detectors of the Outer layer with their hybrids, the second pixel layer, two ministrip layers and part of the repeater electronics.

2. Experimental conditions

Before going to describe the Pixel Detector, it is important to define the experimental conditions in which it is working. They are mild compared to those of a hadronic machine.

The time between two crossovers (BCO) at LEP, when running with 4 bunches is 22 μsec, giving the detector no problem to have the data ready to be read out every BCO. The Pixel Detector does not contribute to the trigger and it is read out every second level trigger. The trigger rates are 600 Hz for level one and less than 5 Hz for the second level: readout times are not very stringent.

The radiation level in the detectors is also very mild. It is constituted by off momentum electrons, often showering just in the material before the detector and by syncrotron radiation. The irradiation of the Pixels is estimated to be at the level of < 1 kRad per year.

3. Detector description

3.1. Sensor

A sensor module consist of a pixel silicon detector with p^+ diodes on a n substrate 300 μm thick, with high resistivity of 5-10 kΩcm determining a depletion voltage of 40-60 Volts. It consists of 10 areas each with 24×24 pixel cells and 6 with 18×24 pixel cells, each area corresponding to a readout chip. The pixel cell has a dimension of $330\times330\ \mu m^2$ but cells in the boundaries between different areas have dimensions doubled in order to avoid dead regions due to readout chips being few hundred μm apart one another. A picture of a sensor is in figure 4 where from the shape it is clear why they are called raquettes. Overall dimensions are length of about 7 cm and width of 2 cm. The Delphi pixels adopt a hybrid solution therefore each sensor is bump bonded to 16 electronic chips. The area available for the bonding on the pixel cell has a diameter of 140 μm.

The digital signal for the electronic chips are routed on the sensor,where a bus is integrated using double metal techniques. A guard ring surround the sensitive area. Supply lines to the chips do not go directly through the integrated bus be-

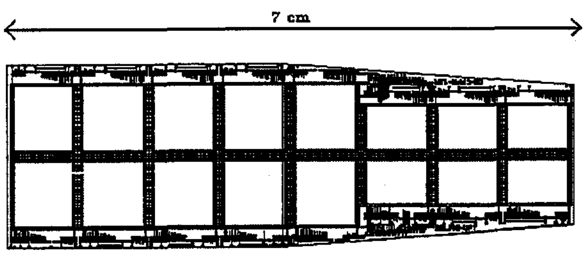

Figure 4. *Pixel sensor*

cause of voltage drop on the resistive lines. A kapton foil is glued instead on top of the chips and distributes the supply lines close to the single chips; then via bonding wire they are connected to the integrated bus and reach the chips.

One raquette has in total 8064 pixel cells. The supplier of the sensor is CSEM[1], the design was done at CPPM[2].

3.2. Readout chip

The readout chip is called SP8[3][6]. It is a VLSI chip in 3 μm technology and provides preamplification, shaping, discrimination and binary readout of cells with signal, using a 2D sparse data scan[7] and each signalled cell is readout in 200 ns. On two cells per chip, a p-well underneath the input pad defines a 30 fF calibration capacitance. The power consumption of the chip is of 40 μW per cell.

The threshold is adjustable between 5 to 20 ke$^-$, with 1.2 ke$^-$ RMS. From test beam data it has been proven that in the configuration of Delphi Pixel detectors, for a threshold up to 10 ke$^-$, an efficiency of 99 % is obtained.

The interconnection via the integrated bus is highly demanding in terms of failure rate of the interconnection technique. The connection between the bus lines and the corresponding pad on the chip is achieved by the same bump-bonding technique used for the pixel interconnection. The IBM C4 (Controlled Collapse Chip Connection) bump bonding process[4] was used with 100μm bond diameter on a 140μm diameter bonding area. A $(2.4 \pm 0.2) \times 10^{-4}$ failure rate was achieved, that determines 80% raquette efficiency due to bump bonding.

The SP8 is designed for a milder environment than LHC so it works stably for occupancy $< 20\%$ and it has a radiation tolerance of 10 kRad.

3.3. Assembly of a Raquette

The assembly of the raquette module is done in several steps:

- 16 SP8 chips are bump bonded to the detector;
- the ceramic providing the mechanical support of the raquette is aligned and glued;
- the 4 layer flat kapton[5] is glued on top of the SP8 chips;
- long kapton[6], providing the connection to the repeater electronics, is glued;
- wire bonding is done to connect: long kapton to flat kapton lines and then to the bus integrated on the detector; flat kapton to the supply lines on the detector.

The assembly of a pixel raquette is illustrated in figure 5. The complete raquette module determine less than $1\% X_0$ of material budget.

The yield of production at the several steps of the assembly is: 77% after dicing and bump-bonding; 68% for a full functioning of the readout of all 16 SP8 after the connection to the raquette and 85 % for the remaining phase of the assembly, including mounting on crowns and finally on the Silicon Tracker mechanical support. Taking into account also the 82% rate for accepting the sensor before considering the assembly, the total yield rate become of 36%.

[1]CSEM, Rue de la Maladiére 41, CH 2007, Neuchatel, Switzerland

[2]CPPM , Centre de Physique de Particules de Marseille

[3]Designed by College de France, Paris and CPPM; Made by FASELEC 3 μm technology, Phyllips (Taiwan).

[4]Metallisation done by IBM, Corbeil (France); flip-chip by IBM Montpellier (France)

[5]Design of CPPM; Made by TELEPH

[6]same reference of the flat kapton

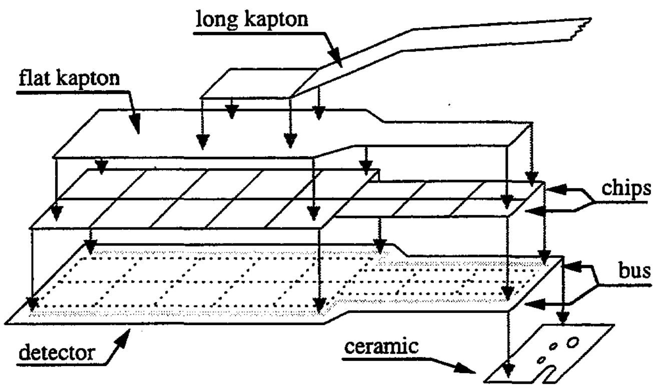

Figure 5. *Assembly of a pixel raquette*

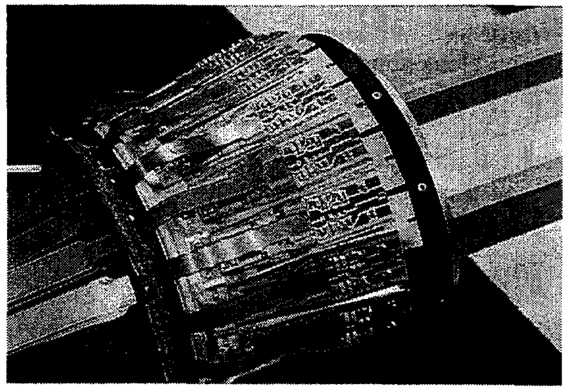

Figure 6. *Photograph of a assembled inner layer pixel crown.*

3.4. Crown

The pixels raquettes are mounted onto semicircular aluminium supports, with inclinations with respect to the z axis of 12° and 32° for the pixel and are arranged in groups of 19 forming a pixel crown. The raquettes are connected to the repeater boards with the long kapton cables, with two repeater boards per crown. A photograph of a pixel crown is shown in figure 6. There are 8 crowns, for a total of 152 raquettes and 1.2 millions pixels for a sensitive area of $0.2\ \mathrm{m}^2$.

Overlap between adjacent raquettes is provided in order to allow internal alignment: for the inner and outer pixel layers the overlap corresponds to 37% and 12%.

3.5. Readout system

The readout system[7] consists of a crate processor housed in a fastbus crate controlling 4 fastbus modules (PIxel Read-Out Modules PIROM) and reading them sequentially. Each PIROM contains 4 PIxel Read-Out Unit (PIROU) based on a micro-controller Motorola 68332, connected each one to one repeater board, and all PIROU are read in parallel. Each PIROU controls a group of 10 or 9 raquettes connected to the repeater, addressing and reading sequentially each chip of each raquettes. The readout scheme allows the skipping of malfunctioning/not responding chips. A mask of noisy pixels can be loaded on the PIROU in order to suppress them: this is particularly important in order to keep the size of the pixel data low avoiding unnecessary information.

3.6. Slow Control system

Stable and safe operation is a critical issue for running the Pixel Detector. There is an automated response to changes in the data taking conditions or possible misbehaviours of the detector, running within the framework of the general DELPHI slow controls system.

The slow control frontend-computer for the Pixel[9] is based on a 68340 processor running OS9 and the main components are a commercially available SY527 CAEN and a home made DAC-system.

The CAEN[7] controller supervises power supplies and depletion voltages for a total of 88 channels, distributed at the level of repeater or crown. The threshold settings is done at the level of single raquettes in order to optimise the working point of each one in terms of efficiency and noise per-

[7]Costruzioni Apparecchiature Elettroniche Nucleari S.p.A., Via Vetraia, 11, I-55049 Viareggi, Italy

formance. It is controlled by the DAC system

A procedure was developed to detect and react to an anomalous number of hit pixels, associated to either a high background or to a misbehaving chip. It is necessary to protect the detector against accidental very high occupancies because the power consumption of a cell connected to a hit pixel increases by a factor of about 10. If the required power exceeds the supply characteristics the detector may then trip off, leading to a jump in temperature of around 12°C, affecting badly the detector stability. A typical situation where this can arise is during the LEP injection, when the occupancy can be up to more than 2 orders of magnitude greater than nominal. When the occupancies are abnormally high the crate processor supervising the data acquisition notifies the slow control system, which raises the thresholds [9]. In addition, for the special period of LEP injection when the backgrounds are expected to be high, the discriminator thresholds are always automatically raised.

4. Performance

4.1. Noise level

The level of systematically noisy pixels is around 0.3%. Most of the noisy pixels are removed by masking in the crate processor, and the remaining ones, defined as those which respond to more than 1% of triggers, are flagged and removed off-line.

After the removal of noisy pixels, the hits which remain originate from particles traversing the detector and from random noise. The number of pixel hits is shown in figure 7 for three classes of events. Hadronic events, where some tracks pass through the forward region, have a mean number of pixel hits of about 4.5. Background events, which are triggered events with no tracks pointing to the primary vertex, include beam gas interactions at low angle and off-momentum electrons than might have showered before the Pixel, and result in a tail extending to very large numbers of hits. Such events become more prevalent at higher energies.

A class of events was also selected with just two charged tracks reconstructed in the barrel. These events should produce no physics background in the forward region, and the mean number of pixel hits places an upper estimate on the random noise of 0.5 ppm.

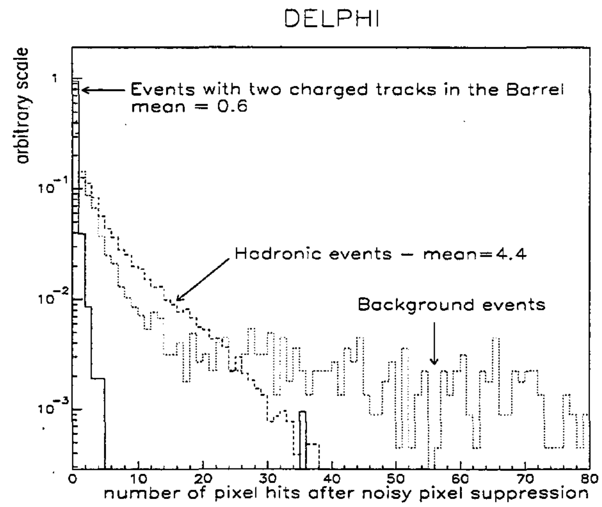

Figure 7. *Mean number of pixels per event for hadronic events, background events, and events with two charged tracks only in the barrel. The data are taken from the 1997 Z^0 running period. The normalisation is arbitrary.*

4.2. Alignment

The alignment of the full Silicon Tracker consists of a survey stage and an alignment using tracks.

The pixel detectors are surveyed in two steps. After the chips are bump-bonded and the ceramic support is glued to the detector, the two-dimensional position of the external detector corners and the ceramic are determined with a microscope with respect to pads close to the detector corners.

These pads have a well known position on the detector mask and define the position of the pixel array. They are chosen as a reference as they remain visible during the assembly. The kapton cables are then attached and the tested module mounted on the support. Its position, given by the location of the two corners plus the measurement of the module's plane, is related to that of three spheres mounted on the support. After all modules are mounted, the VFT crowns are joined to the barrel support and the positions of the spheres with respect to the barrel are measured.

Being the survey made before the installation inside DELPHI, the survey gives no information on the relative position of the two half-shells. Also the geometry of either half-shell after installation might slightly differ from the results of the survey, due to possible deformations of the mechanical structure. The survey is therefore the starting point for the alignment done using tracks.

The VFT alignment procedure uses track elements already reconstructed with the use of the other tracking detectors. The procedure optimises the VFT module positions by minimising the χ^2 of tracks refitted over all track elements. The weight of a track in the fit depends on the polar angle and the combination of tracking detectors contributing to the track. In addition, the intrinsic VFT resolution and the constraints from overlapping modules are exploited. The global parameters at the level of each quadrant are determined first, then the individual plaquette parameters are fitted, allowing 6 degrees of freedom per plaquette. The overlap between the first pixel layer and the Barrel Inner layer at $20° < \theta < 25°$ provides a good link between the Barrel and the VFT global alignment.

4.3. Efficiency

The efficiency of the pixels was studied using tracks which pass through a region where neighbouring plaquettes overlap and have at least one hit in a silicon layer other than the one being studied. If a track registers a hit in one plaquette, a second hit is searched for around a 3σ window in the neighbouring plaquette. Figure 8a shows the average efficiency measured in each pixel crown using this technique. The average efficiency excluding bad plaquettes was 96.6%.

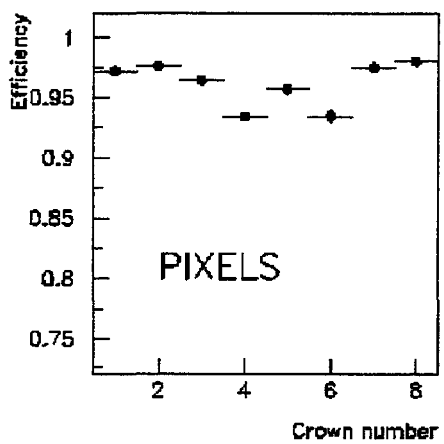

Figure 8. *Efficiency for the pixel crowns as measured inthe 1997 data using tracks (see text). The average quoted efficiencies do not take into account dead modules.*

4.4. Resolution

For the pixels, the expected resolution depends on the cluster size, which is a function of the track incidence angle. Tracks from the primary vertex traverse the first and second pixel layer at incidence angles ψ in the polar direction of 57.5° and 40.5° respectively. The incidence angle in the $R\phi$ direction is close to 90°. The majority of produced clusters are either single hits or double pixel hits split in the polar direction. Neglecting charge diffusion effects, the angular dependence of the single pixel hit rate is given to first order by the following equation:

$$N = (1-\frac{d}{\Delta}); \qquad d = w \times \tan\psi - \frac{t}{c} \times w \times \sin\psi \quad (1)$$

where w is the thickness of the depletion layer, Δ is the pixel pitch, c is the charge deposited by a minimum ionising particle and the parameter t is given by the detector threshold (about 10ke$^-$ is used). Knowing this rate, a simple geometrical consideration of ionisation charge sharing in the pixel sensitive volume leads to the following

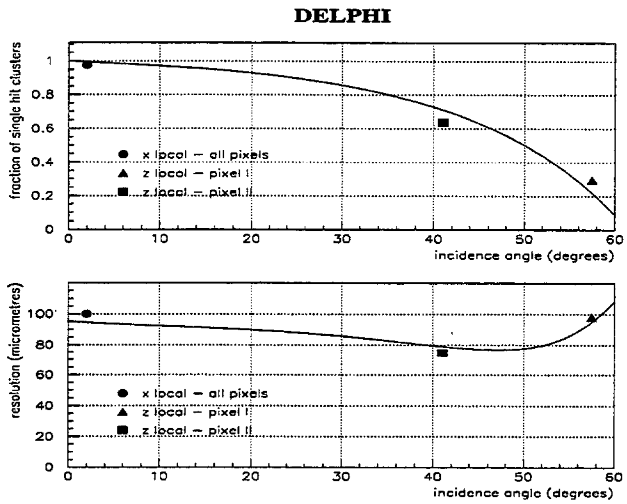

Figure 9. *Resolution expected in the pixels as a function of track incidence angle (solid line) shown together with the values measured in the data.*

expression for the expected detector resolution:

$$\sigma^2(\psi) = \frac{1}{12}\frac{(d^3 + (\Delta - d)^3)}{\Delta} + (\frac{\kappa}{c} \times w \times \sin\psi)^2 \quad (2)$$

Here κ is a parameter describing the effect of charge fluctuations (about 5ke$^-$ is used), and the other symbols are the same as in equation 1.

The expected distributions are displayed in figure 9 as a function of ψ. The resolutions in the data are measured in the detector plane for the z_local (polar) direction and the x_local ($R\phi$) direction. The values extracted are overlaid on the prediction. For the x_local points the incidence angle is the same for the pixel I and pixel II layers, and these points are shown together. The measured points are seen to be very close to those predicted by the simple model.

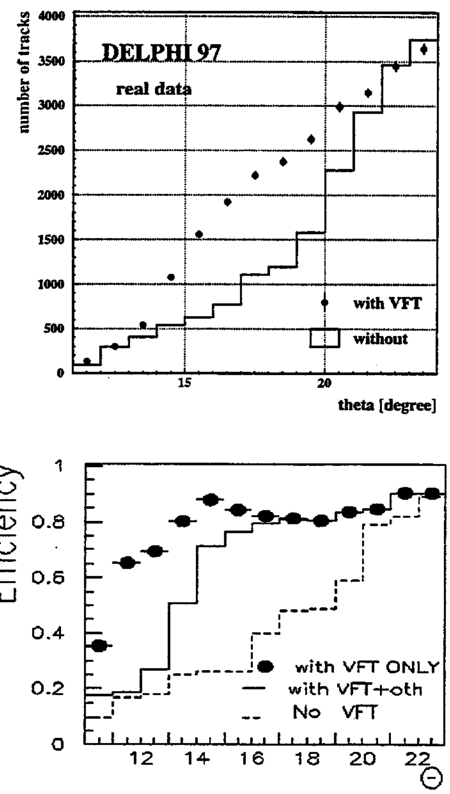

Figure 10. *Improvement on the forward tracking thanks to the Pixel Detector in the VFT*

5. Improvement in Forward Tracking and Hermeticity

Improvements of the forward tracking using the VFT data have been studied both at Montecarlo level, using the full reconstruction software of Delphi, and on real data. The performance of the tracking both excluding and including the VFT data has been been compared.

In the upper part of figure 10 is the number of tracks versus polar angle for real data collected in 1997, when including or not the VFT in the tracking. To measure an absolute tracking efficiency on real data is difficult since there is no redundancy in the forward tracking to do so. Therefore in the lower part of figure 10 is the tracking efficiency as measured on MC, with and without VFT.

Comparisons on data/MC of the ratio of number of tracks obtained with and without VFT give a good agreement giving confidence on values found by the MC studies.

When quoting *with VFT* is meant that the VFT is contributing to form a track together with another tracking detector (mainly FCA and FCB).

It was mentioned in the beginning of the paper that VFT provides standalone pattern recognition, and in certain cases a good VFT track might not find a clear association to the other tracking detectors. These tracks, called VFT only tracks, reach a high purity, greater than 95% when including hits from 3 layers and therefore they improve substancially the tracking hermeticity down to about 10°. In figure 10 is shown the tracking efficiency obtained when this category is added. The VFT only tracks have a poor momentum resolution but the direction of the track at the VFT is measured with 1-2 mrad precision. The use of the VFT only tracks is exemplified in picture 11 where a real event having two high energy deposit in the electromagnetic calorimeters but no tracks associated to them is shown. Including VFT only tracks, two tracks are visible, allowing to determine that the event is a Bhabha in the forward direction.

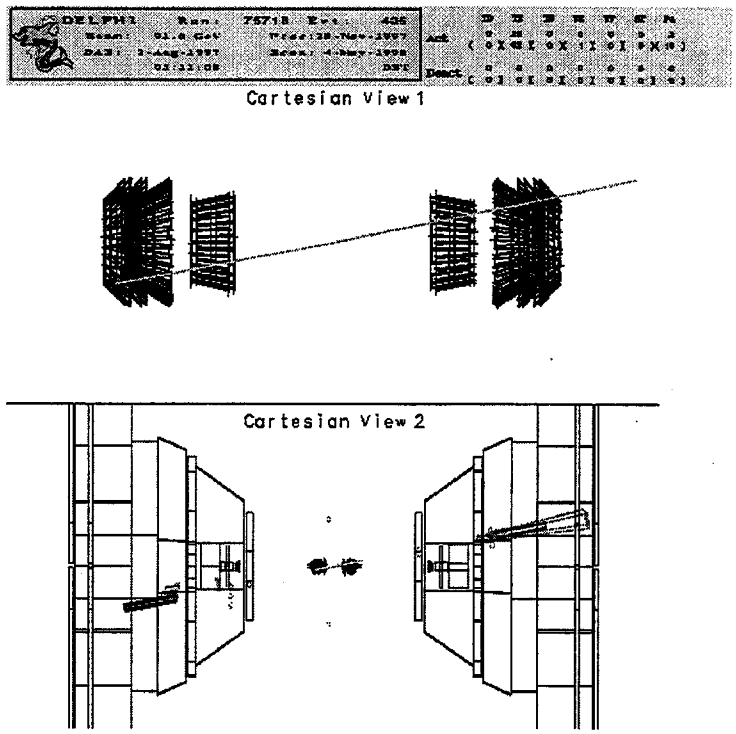

Figure 11. *Bhabha event with tracking provided by the VFT*

6. Conclusions

The Delphi Pixel Detector was commissioned on 1996 and then completed on 1997. Stable running performance have been obtained and the design performance has been achieved: random noise level of 0.5 ppm and single plane efficiency of 96% with a hit resolution of 80-100 μm.

This allows Delphi Silicon Tracker to satisfy the request imposed by the LEP2 programme. The VFT has been fully integrated in the tracking of Delphi and this has dramatically improved the tracking efficiency in the forward region.

Acknowledgements

This paper is presenting the results achieved thanks to the common effort of the entire Delphi Pixel group. I want to thank all my colleagues for the brilliant work done and for having supported me for this presentation.

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The ATLAS Pixel Detector

Guido Gagliardi, University and INFN Genova

on behalf

ATLAS Pixel Collaboration [1]

Albany, Berkeley, Bonn, Dortmund, Irvine, Genova, Marseille, Milano, Nikhef, New Mexico, Oklahoma, Prague, Santa Cruz, Siegen, Toronto, Udine, Wisconsin, Wuppertal

Abstract

The ATLAS Pixel Detector is presented in the context of ATLAS detector at LHC: the role of Pixel Detector in the tracking system is shown. The layout of the Pixel Detector is described. The pixel detector has a modular design, made by three barrels and 10 disks which are in turn made by modules: the detector uses the same modules for the barrel and disk region.The Read-Out architecture of a module is presented in particular detail. The electronic in a module consists of 16 Front-End (FE) chip which build the hits and a Module Control Chip (MCC) which builds the event and re-routes the fast and slow commands from the control room to the FE's. The expected performance of the Pixel Detector in the tracking system is reported. Results on the required bandwidth and buffer size are also reported.

1. Introduction.

The ATLAS collaboration is developing a Pixel Detector as a vertex detector for the Inner Detector tracking system[2][3]. The role of tracking in the experiments which will be positioned in the Large Hadron Collider (LHC) has increased with the time, subsequently to the effort done in the understanding the behaviour of the tracking system in the LHC high luminosity environment.

One of the features one requires from the tracking system in the LHC experiments is the ability to identify hadronic jets containing a *b* quark (*b-tagging*). Many of the interesting physics channels at LHC benefit from a good b-tagging: among them there is the $H \rightarrow b\bar{b}$ channel, which could increase the signal of a low mass Higgs (m_H < 130 GeV); the $H \rightarrow hh \rightarrow b\bar{b}b\bar{b}$ channel (if the heavy MSSM Higgs can couple to two light Higgs); and virtually every channel that involves the *t* quark, as, for example, the *t* quark decaying into a charged Higgs and a *b* quark. To obtain a good b-tagging is mandatory to have a vertex detector as close as possible to the interaction point.

The tracking detectors near the interaction point in LHC must cope with high instantaneous and integrated particles rates. The LHC high luminosity (the project luminosity is 10^{34} cm^{-2} s^{-1}) is obtained by circulating 2835 proton bunches with small interaction cross section and up to 10^{11} protons per bunch. The time between two Bunch Crossing Over (BCO) is 25 ns. The number of collision for bunch crossing depends on the pp cross section: the expected value is ~25 pp interaction per BCO.

The high instantaneous rate implies fast detectors and fast Front-End (FE) and read-out electronics, with some pipeline memory close to the detector to store data while the trigger decision is pending. A good granularity is also required since the expected number of charged particles per interaction is ~7 per pseudorapidity[4] unit: in the $-2.5 < \eta < 2.5$ region there are about 10^3 charged particles per BCO. The high integrated rate implies that all devices and material should keep operating after a very high radiation dose (up to 30 MRad).

It is natural in this context to adopt a pixel detector as a solution for the vertex detector in ATLAS. Pixel detectors are fast; hybrid pixel detectors which are composed of a sensor bump-bonded to a front-end chip can use the front-end chip area to perform complicate task and act like a local memory; pixel detectors provide both granularity and high signal-to-noise ratio to cope with the high luminosity LHC environment.

2. ATLAS Pixel Detector Layout

The ATLAS Pixel Detector is shown in Figure 1. The layout covers the eta region $|\eta| < 2.5$ and provide at least three space points.

The Pixel Detector is made of three barrel in the

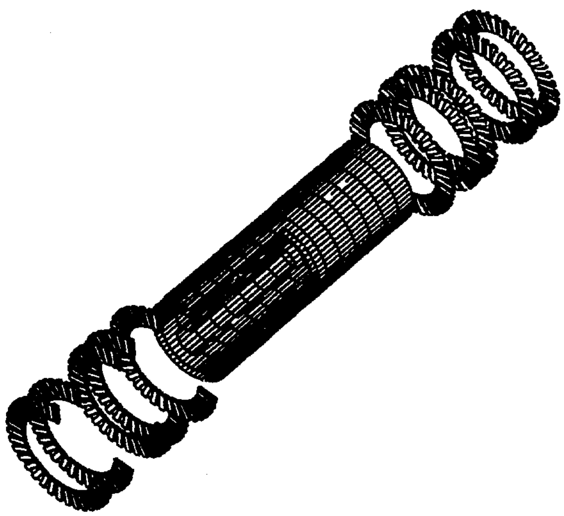

Figure 1: ATLAS Pixel Detector Layout

central region and 5 wheel in each of the forward regions. This geometry guarantees always a high incidence angle between the particles and the silicon sensors.

The barrel pixel tracker is made of pixel modules arranged in three cylindrical layers - the parameters are given in Table 2-1. The inner layer is called "B-Layer" since is the nearest to the interaction region and allows the precise measurement of impact parameter of the particles and of the secondary vertexes.

The barrel modules are arranged end-to-end on long 'ladders' which lie parallel to the z-axis - 13 modules per ladder. Overlap of the active area in the z-direction is achieved by having alternate modules shifted 0.03 cm above and 0.03 cm below the mean radial position, with the central module being located at the larger radius.

Each end-cap pixel tracker is made of the same modules as those in the barrel, with 250 μm pixel sensors used throughout, arranged in rings of 36, which are mounted on either side of disks which provide support and cooling.

Modules which are adjacent in ϕ are mounted on alternate sides of the support disk. The two rings are spaced in z by 0.7 cm and are identical except for a 5° rotation in ϕ in order to insure hermeticity. The parameters of the 5 disks are given in Table 2-2.

Table 2-1 Parameters of barrel pixel layers.

Layer	R[a] (cm)	Active half-length (cm)	Number of modules in z	Number of ladders in R-ϕ	Tilt angle (degrees)
B-layer	4.3	38.9	13	18	- 15.0
Layer 1	10.1	38.9	13	42	- 11.4
Layer 2	13.2	38.9	13	56	- 11.4

a. The radius is defined as the position of the centre of the sensitive silicon for the central module.

Table 2-2 Parameters of pixel end-cap disks.

Wheel number	z positions (cm)	Active R_{min} (cm)	Active R_{max} (cm)
1	49.52	12.63	18.67
2	61.18	12.63	18.67
3	66.95	12.63	18.67
4	84.12	12.63	18.67
5	92.61	12.63	18.67

The grand total of modules in the ATLAS Pixel Detector is 2228. In Figure 2 is shown the material in

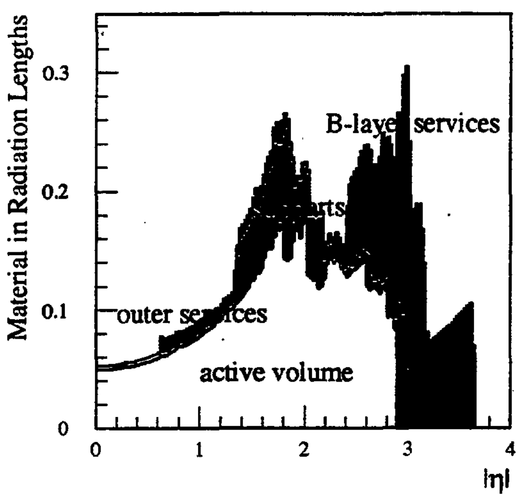

Figure 2: Material in radiation lengths in the Pixel system as a function of eta. The *active volume* includes sensor, hybrids, read-out electronics and optical links; the *supports* include mechanical supports.

radiation length of the ATLAS Pixel Detector as a function of the pseudorapidity of incident particles. The barrel supports are at $\eta = 2$. It must be pointed out that the B-Layer supports, also shown in the Figure 2, contribute with a big amount of material to the total material budget at large η, since they are routed along the beam pipe. This choice allows periodical replacement of the B-Layer, which is supposed to survive a few years at the nominal LHC luminosity.

3. Pixel Detector Modules

Modules are the basic building blocks of the ATLAS Pixel Detector. A module consists of the silicon sensor tile, the read-out electronics, the local signal interconnections and power distribution busses, and passive components such as temperature sensors, resistors and capacitors.

The sensor tile is made of 61440 pixels. The pixel shape is rectangular, $50(r\phi)$ x $300(z,r)$ mm. The asymmetric shape is chosen to achieve best performance in the transverse plane[1]. The ATLAS Pixel Detector choice is to do not have any information on the energy released in the pixels (binary read-out): the small pitch in the $r\phi$ direction together with the tilt angle, oriented to minimize the charge spreading due to the Lorentz force[2], is thus providing the optimal spatial resolution.

3.1. The read-out electronics

The read-out electronics has the task to build the hits (stream of data representing the passage of the particle through the sensor), to sparsify them and to reduce the amount of data[5].

The ATLAS Trigger System is structured in three levels: the first level (LV1 trigger) has a input bandwidth of 40 MHz and a decision time (latency) of 2.5 μs. Because of the high input rate, data are supposed to stay inside the detectors during the LV1 latency time: only data belonging to a LV1 accepted event are transferred to the next trigger levels. Another task for the read-out electronics is to store data during the LV1 latency time and to retrieve and send out data with a time resolution of 25 ns.

The read-out electronics of a module is structured in a two-level architecture. The first level is made of

[1] In the ATLAS coordinates the z axis go along the beam pipe and the transverse plane is perpendicular to the z axis.
[2] The ATLAS Pixel Detector is posed in a 2 T solenoidal magnetic field.

16 FE's, bump-bonded to the sensor tile. The FE's build, sparsify and store the hits during the LV1 latency time. The second level is made of a Module Control Chip (MCC). The MCC builds the event collecting together data from the 16 FE's and redirects the control signals and the clock to the FE's.

The module read-out architecture is shown in

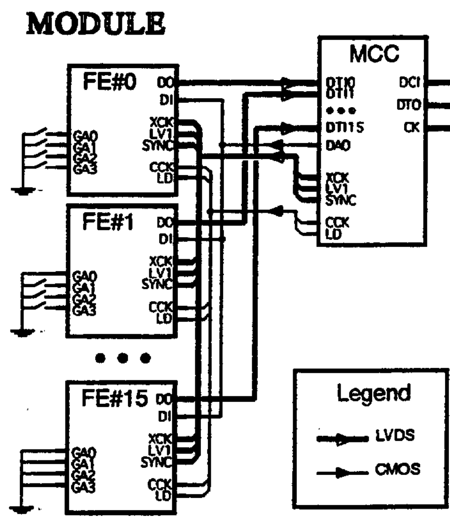

Figure 3: Module read-out architecture

Figure 3. It is a data push architecture: the FE hits are transmitted as soon as they are ready. All data link between the FE's and the MCC, and between the MCC and the Read-Out Buffer (ROB, the external buffer electronics) are serial. The interconnections have been kept very simple, and all connections which are active during data-taking use low-voltage differential signalling (LVDS) standards to reduce EMI and balance current flows. Other signals use full-swing single-ended CMOS to reduce the pin count. The LVDS data links allow a bandwidth of 40 Mb/s.

The FE's and the MCC are connected with a point-to-point topology that ensures fault tolerance and parallel data read-out from the FE's: this allows a better bandwidth usage and smaller buffers in the FE chip. Each FE chip is identify by geographical addressing.

Each FE has a LVDS data line (DO) connected to the MCC; all FE's shares a LVDS line for the clock (CK), the LV1 accepted signal (LV1) and the fast reset (SYNC). The MCC has 16 LVDS data input lines, one for each FE, and three LVDS connection to the external: the input command line (DCI), the output data line (DTO) and the clock.

3.2. The FE's

There are at the moment two architecture for the FE chips: FE-A, which is developed by Bonn and Marseille groups, and FE-B, which is developed by LBNL[5][6].

Both FE chip are organized in 24 column (mirrored in pairs), each column in turn is made of 160 read-out pixel cells, one for sensor pixel (Figure 4).

The pixel cells are composed by a preamplifier that amplifies the charge released by the particles in the sensor, and a discriminator that identifies the over-threshold signals. Each pixel cell sends as soon as possible the information of which cell is hit and when (timestamp)[3] to the End of Column (EoC) logic. this information is called "hit".

The EoC logic stores the hits into buffers (EoC buffers) during the LV1 latency time. At the LV1 accepted signal the EoC logic retrieves in the buffers only the hits with the correct timestamp and serializes them out to the MCC.

As optional information the FE's provide, for each hit, a Time Over Threshold value which can be used as a coarse measure of the released energy in the pixel.

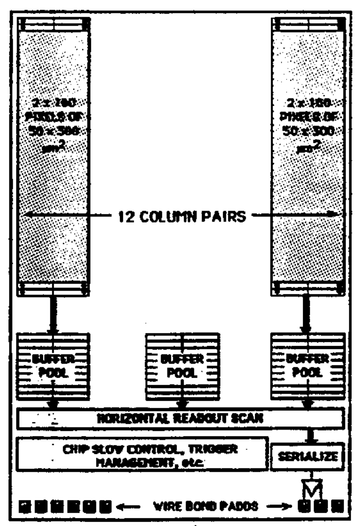

Figure 4: FE chip schematic.

[3] The timestamp is added to the cell number information only in the FE-B scheme, while in the FE-A it is built by the EoC logic.

3.3. The MCC

A floorplan of the MCC[5][7] is shown in Figure 5.

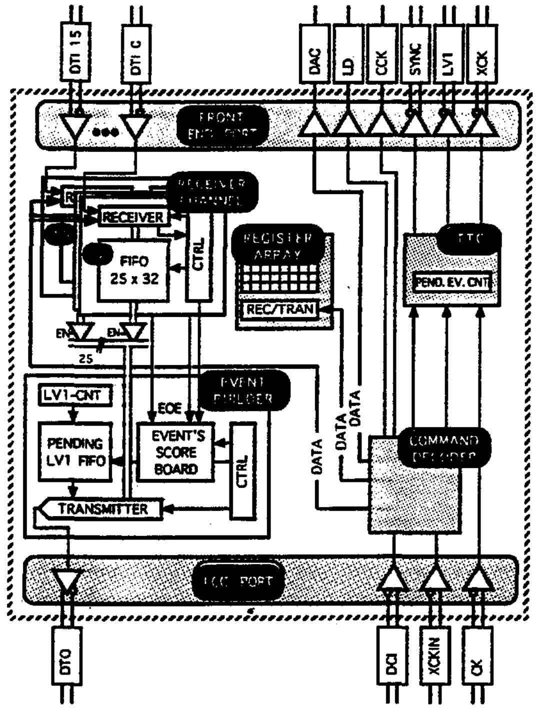

Figure 5: MCC schematic.

The MCC basic blocks are 16 Receivers and an Event Builder. The 16 Receivers collect hits from the FE's and store them until all the FE's have sent the hits belonging to a LV1 accepted event. When all hits are collected, the Event Builder scans the Receivers and serializes out the event.

There are in the read-out electronics two buffer levels: in the FE's the buffers store the hits until the LV1 accepted signal; in the MCC the buffers store the hit until all the FE's have sent the hits belonging to a LV1 accepted event. Local fluctuation of occupancy in one FE thus has a minor impact on the buffer occupancy in the other FE's.

Other tasks of the MCC are the FE's control, the handling of the LV1 accepted signal and the redistribution of the clock.

4. Pixel Detector simulated performance

A complete GEANT simulation of the ATLAS Pixel Detector including all services and mechanical supports has been done. LHC events has been simulated as well.

The results of the simulation has been used to adequately dimensioning the buffer sizes in both the FE's and the MCC, and the maximum available bandwidth between the FE's and the MCC and between the MCC and the ROB's.

In Figure 6 is reported the average double column occupancy per event in both the B-Layer and the Layer 1. The occupancy in the B-Layer is a factor 5

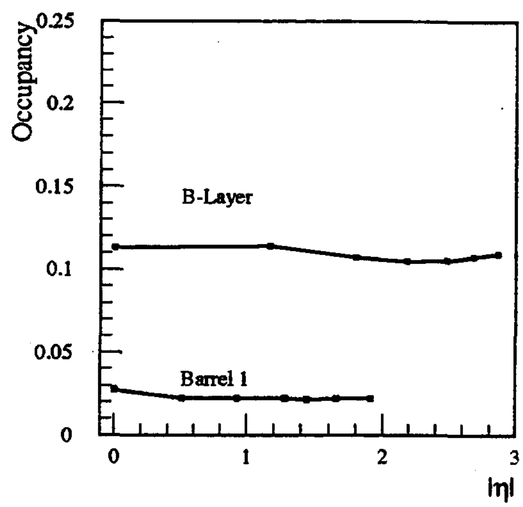

Figure 6: B-Layer and Layer 1 double column occupancy as function of eta

greater than the Layer 1. It is clear that the B-Layer is more demanding for the read-out electronics than the other components of the Pixel Detector. The single pixel occupancy per event is very small as expected for the high granularity pixel detector.

In Figure 7 is shown the data rate from the FE's to the MCC as function of the pseudorapidity of the module. The dotted curves correspond to the presence of the ToT information; continuous curves are for the binary read-out. The average data rate is of the order of few Mb/s, which fit nicely in the 40 Mb/s maximum available bandwidth. The value are similar for the B-Layer and the Layer 1 because for each LV1 accepted each FE's send the hits and a end-of-event word, which is present even in empty event. This end-of-event constitutes the main component of data traffic between the FE's and the MCC.

In Figure 8 is reported the average data rate from MCC to ROB as function of eta. For the Layer 1 the average value is of the order of 10 Mb/s, which is still acceptable for the 40 Mb/s of maximum available

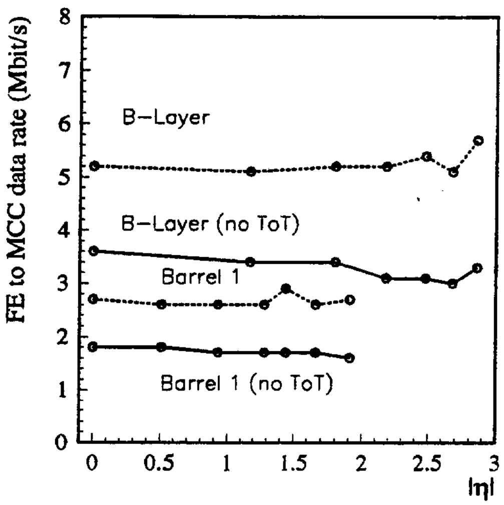

Figure 7: FE to MCC data rate as function of eta.

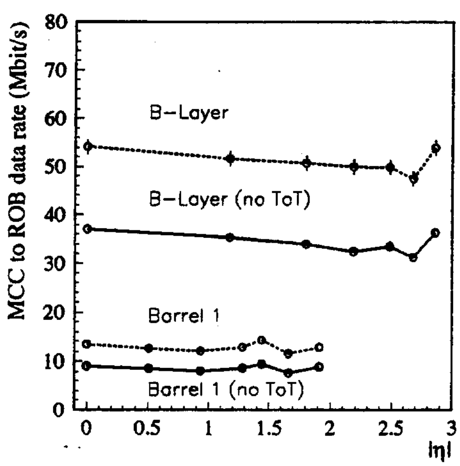

Figure 8: MCC to ROB data rate as function of eta

bandwidth; for the B-Layer it is clear that the maximum available bandwidth should be doubled to cope the 40-60 Mb/s average data rate[4].

A detailed study[3] has been performed to understand the MCC and FE buffer occupancy and the inefficiency induced by the read-out architecture in the Pixel Detector. The results show that the B-Layer is very demanding in the buffer size: the inefficiency induced by the MCC buffer size is less than 1% with 32 buffer per Receiver, but the inefficiency induced by the FE buffers is of the order of 3-5% only with a sizeable amount of buffer, 25-30. This is because the FE's chip store for 2.5 μs (the LV1 latency time) all the hits that occurs in a column pair, while the MCC Receivers store only LV1 accepted events for the time needed to complete the extraction of data to the ROB's. The Layer 1 is less demanding and, with the same buffer size than the B-Layer, virtually dead-timeless.

In Figure 9 is reported the resolution in the transverse plane for the B-Layer.

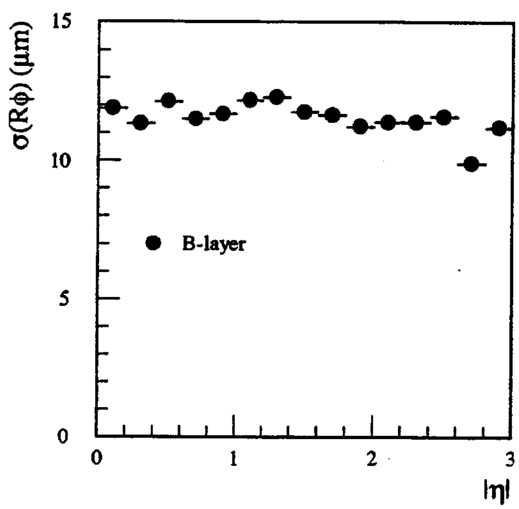

Figure 9: rϕ resolution in the B-Layer as function of the pseudorapidity.

The presence of the B-Layer also at high luminosity is crucial for the b-tagging. In Figure 10 it is shown the transverse impact parameter as a function of the p_T of the particles for two different configuration of the ATLAS Inner Detector, one with the B-Layer and the other one without. The effect of the B-Layer is to increase the asymptotic resolution as well to increase the resolution at low p_T. With the B-Layer the light quark rejection at 50% of b-tagging efficiency is ~120[3].

[4] This is foreseen in the Pixel Detector by doubling the number of optical link in the B-Layer, or by doubling the available bandwidth.

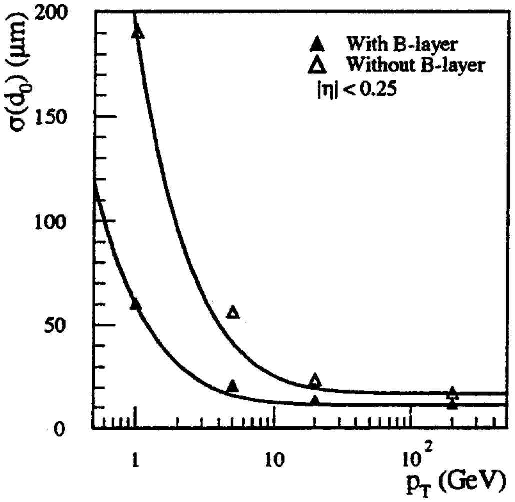

Figure 10: Impact parameter resolution as function of the pT of the particles. The two curves correspond to a Pixel Detector with or without the B-Layer.

5. The Demonstrator programme

In order to demonstrate the feasibility of the ATLAS Pixel Detector a demonstrator programme has started. Pixel Detectors are currently used in several particle physics experiments (SLD, WA97, DELPHI, NA57), but in a much less demanding environment than the one foreseen at LHC.

The main steps of the demonstrator programme are: a single chip bump-bonded to a ~0.6 cm² sensor (single chip module); a set of 16 FE's bonded to a sensor tile and connected to a MCC, with the MCC not integrated on the module (16-chip module); and finally the ATLAS module with the MCC integrated on the module.

The main differences between the demonstrator and the final design are: all the electronics are designed in rad-soft technology; the number of FE EoC buffers is limited (i.e. sufficient for the outer layers, but not for the B-Layer at nominal luminosity); the pixel cell size is 50 μm x 400 μm; the data transmission from the MCC to the ROB uses copper lines, instead of optical links.

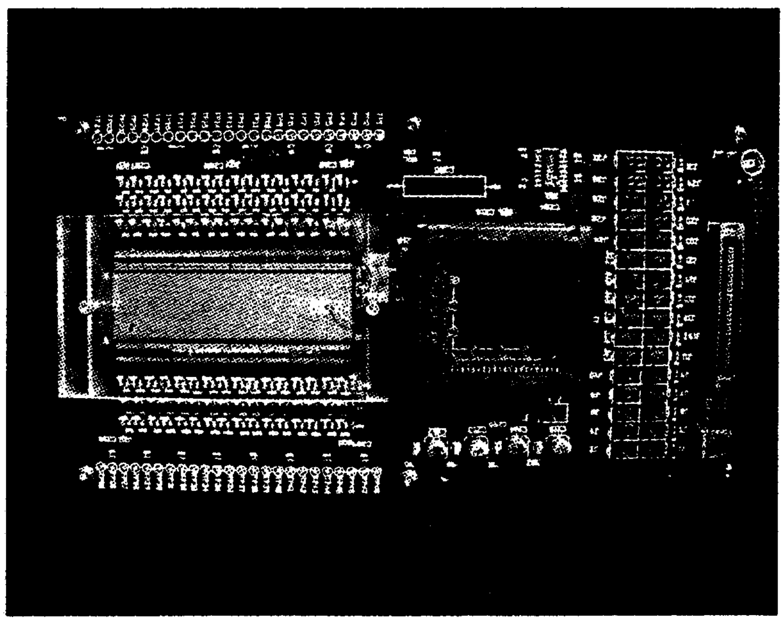

Figure 11: 16-chip module prototype.

The demonstrator programme has so far produced two different FE chips (FE-A and FE-B), both of them functional to LHC environment; a MCC, that has to be tested on the test beam on August 1998; and a module prototype (16 FE-A and 16 FE-B bump-bonded to the sensor). In Figure 11 a prototype of a 16-chip module is shown.

6. Conclusion

The ATLAS Pixel Detector is the nearest detector to the interaction point in the ATLAS spectrometer. The main reason to adopt pixel detectors as vertex detector in ATLAS is that only pixel detectors can survive at the radiation damage so close to the beam in the LHC environment; furthermore, pixel detector high granularity guarantees a very low occupancy even at few centimetre from the interaction point, of the order of 10^{-4} hits per pixel per event.

The Pixel Detector is made of modules, that are read-out individually. The module read-out architecture is structured in two levels: the first level (FE chips) builds the hits, the second level (MCC) builds the events and transmits them.

A detailed simulation showed that the data rates are compatible with the maximum available bandwidth. The derandomizing buffer size required to have a less than 1% inefficiency in the MCC is easily obtained, while an effort has to be done to reduce the inefficiency in the FE chips.

However, it is clear that dimensioning the system for reasonable performances in the B-Layer leads to over-dimensioning it for the outer layer of the ATLAS Pixel Detector.

Prototypes of the read-out electronics and sensor tiles have been built and operated in test-beam. These prototypes contains a full LHC logic.

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[2] ATLAS Inner Detector Technical Design Report, CERN/LHCC/97-17.

[3] ATLAS Pixel Detector Technical Design Report, CERN/LHCC/98-13

[4] The pseudorapidity is defined as $\log\tan\theta/2$, where θ is the angle between the particle and the z axis.

[5] G. Darbo et al., "ATLAS Pixel Demonstrator: Pixel Electronics Specification", ATLAS INDET Note in preparation.

[6] K.Einsweiler, T.Kuhl, these proceedings.

[7] G.Darbo, these proceedings

CMS PIXEL

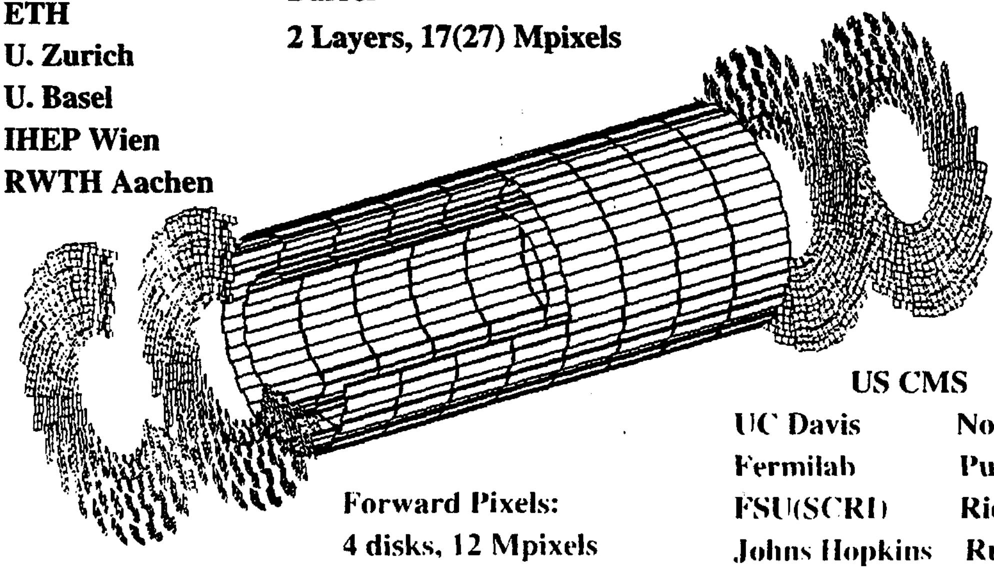
D. Bortoletto
Pixel98 FNAL May 7

- Physics requirements and layout
- Modules, Mechanics and cooling
- Design concerns: material, services, access
- Sensors R&D, specifications and prototyping
- Readout electronics
- Bump bonding
- Summary

Collaboration

PSI (Horisberger)
ETH
U. Zurich
U. Basel
IHEP Wien
RWTH Aachen

Barrel
2 Layers, 17(27) Mpixels

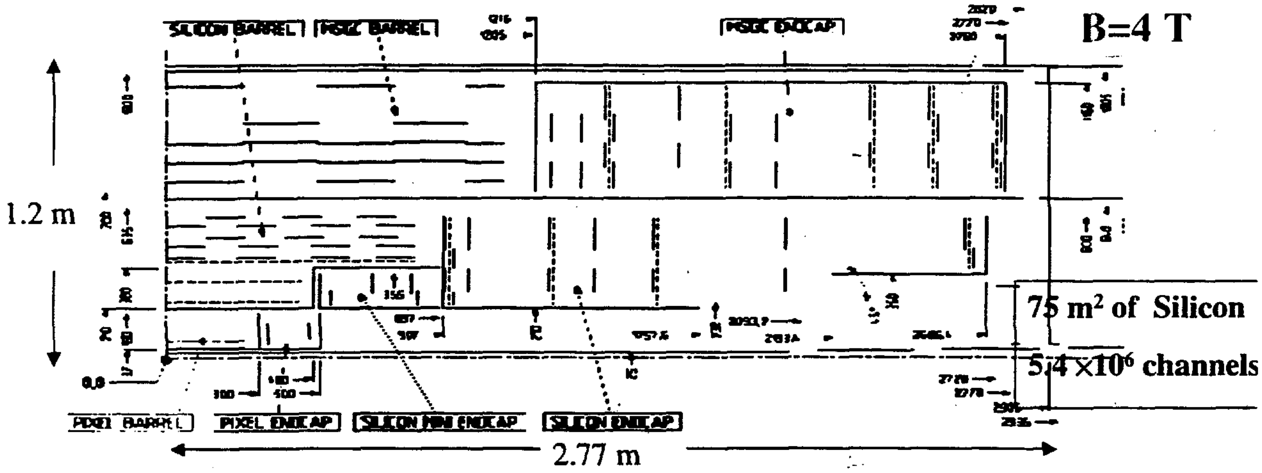


Forward Pixels:
4 disks, 12 Mpixels
$1.5<\eta<2.5$

US CMS

UC Davis	Northwestern
Fermilab	Purdue
FSU(SCRI)	Rice
Johns Hopkins	Rutgers
Los Alamos	Texas Tech
Mississippi	

CMS Tracking

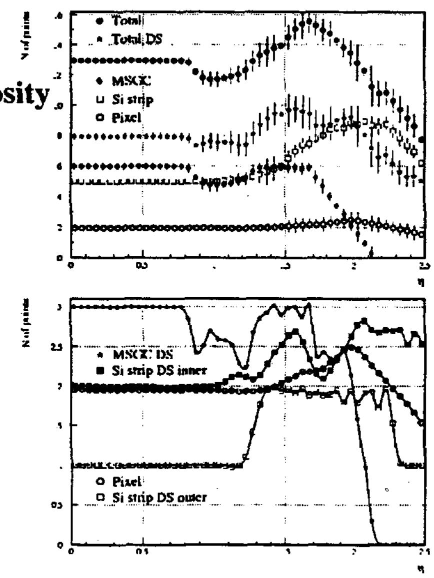


Phase I (Low Luminosity) : First Pixel layer at 4.cm; Silicon: Omit L4 and 2 end-cap disks; MSGC: Omit L4 and 2 end-cap disks

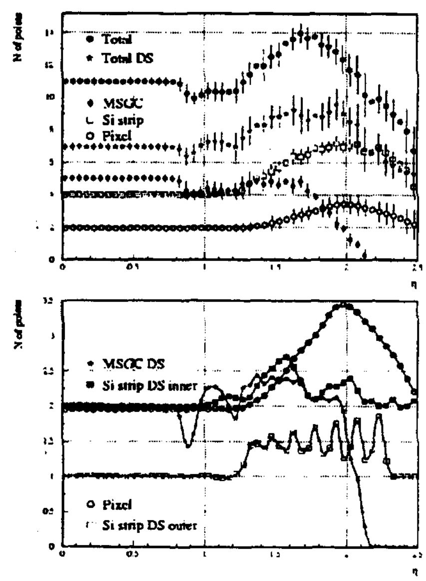
Phase II (High Luminosity): First Pixel layer at 7cm. Instrument missing silicon and MSGC layers.

Layout Optimization

High Luminosity



Low Luminosity



13 hits in central barrel $|\eta| \leq 0.8$

8 Space points

11 hits in central barrel

6 Space points

Requirements

- Reconstruction of high P_t isolated tracks ($H \rightarrow ZZ^*$, W', Z', χ, $°$,$\chi\pm$)
  - $\delta P_T/P_T \approx (15\ P_T \oplus 0.5)$ % for $|\eta| \leq 1.6$
  - $\delta\ P_T/P_T \approx (80\ P_T \oplus 0.5)$ % as $|\eta| \approx 2.5$

  P_T in TeV range
- Muon momentum resolution
  - $\delta P_T/P_T \approx (4.5\ P_T \oplus 0.5)$ % for $|\eta| \leq 1.6$
- Hadron reconstruction (also important to establish isolation)
  - $\varepsilon \sim 95$ % for $P_T \geq 2$GeV
  - $\varepsilon \geq 85$ % for $1 < P_T < 2$GeV
- Impact parameter resolution (b/τ tagging $\Rightarrow$ Higgs, SUSY, $\not{C}P$)
  - δ d (r- ϕ)<25 μm over the full η range for $P_T > 10$ GeV
  - δ d (z)<100 μm over most η
- Material
  - <53 % of $H \rightarrow \gamma\gamma$ with either γ converted in tracker

Pixel Requirements

- Provide two or more hits per track
  - Secondary vertices for b,c and τ tagging (Higgs, SUSY, B physics)
  - Reduce background of light quarks and gluons
- Help the pattern recognition at high luminosity
  - Confirm/reject track segments ($\approx$25MB events with each beam crossing)
  - High precision extrapolation to vertex
  - Small occupancy in high multiplicity environment of heavy ions
- Performance
  - Sensors must operate up to $\phi = 6 \times 10^{14}$ hadrons/cm^2 at R=7 cm and provide sufficient charge
  - Readout analog block must operate with increasing $I_{leakage}$ and less Q. It must provide good S/N and time walk <25 ns
  - Readout architecture must minimize data loss of triggered bunch crossings

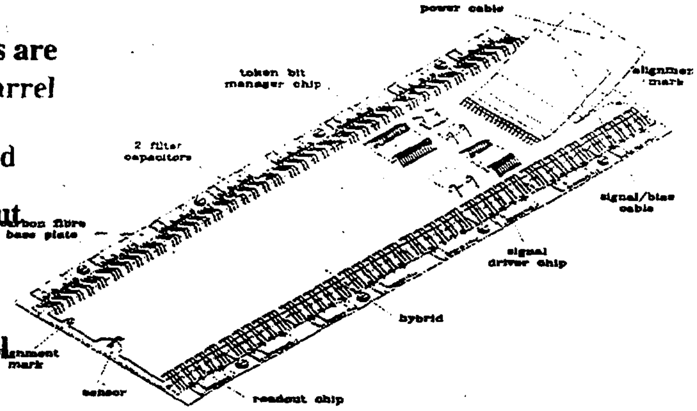
Modules

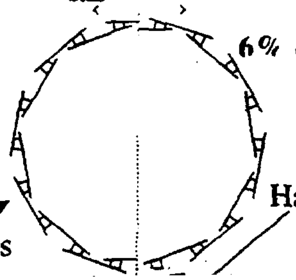
800 Modules in two configurations are the basic building blocks for the barrel

Sensors, 2× 8 readout chips, hybrid

carbon fiber plate glued to readout chip and attached to the cooling frame

Kapton cable supply clock, control signals, V_{bias} and send out hits





6% overlap in Φ

Full modules

Half module

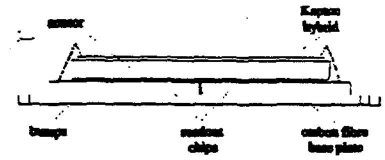
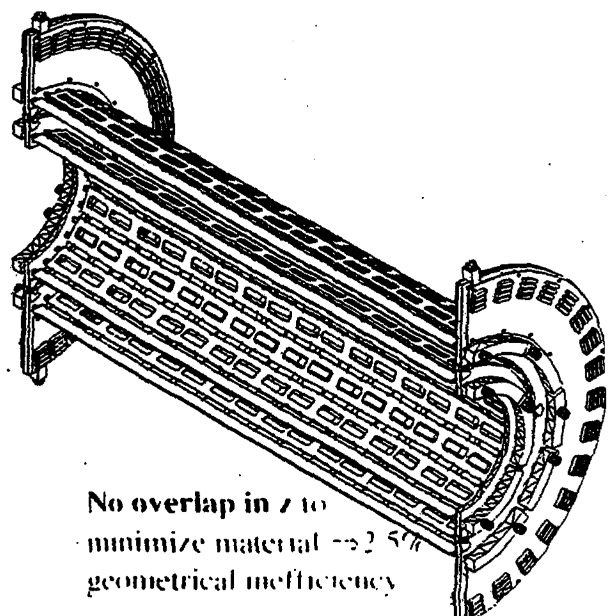


Plate 270 μm Chip 180 μn

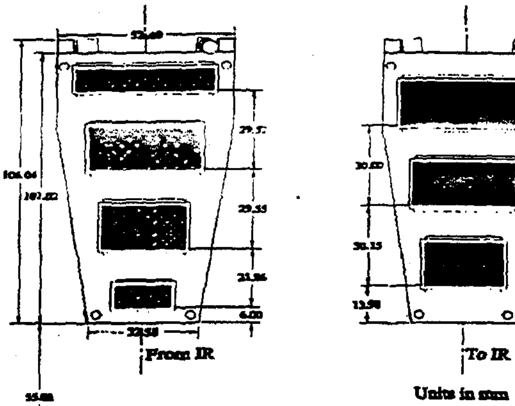
Sensor 250 μm Hybrid 50 μ

Barrel

- **Structural stiffness to provide stable pixel position O(10μm)**
- **Cooling must keep silicon T≤-10°C and remove 3kW**
- **Distortion due to ΔT must be <10 μm**
- **Material budget**
  - **Total Module 0.0101 X/X_0**
  - **Total cooling frame 0.0064 X/X_0**
  - **Total/layer 0.0165 X/X_0**
- **Must be built in two halves separated along a vertical line to accommodate pixel insertion scheme**



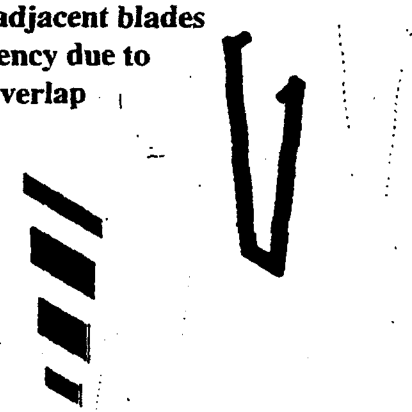
End Disk Blades



5 different size of sensors with 2,5,6,8 and 10 chips

Segmentation in r allows to bias sensors receiving different doses separately

Overlap: 5% front back of blade, 4% adjacent blades
2% inefficiency due to imperfect overlap



96 Blades are the building blocks of Forward Pixel

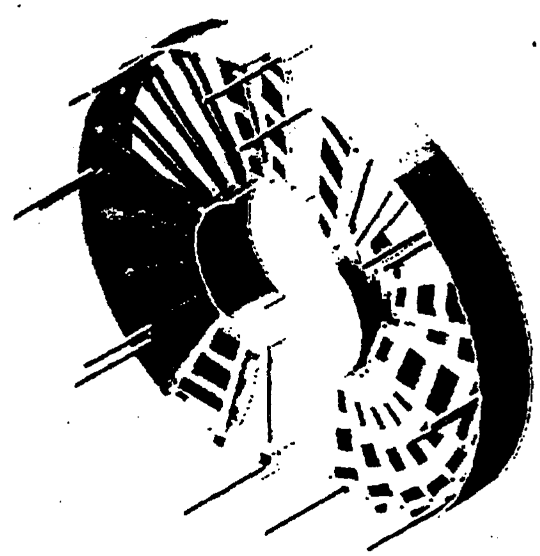
cooling tube: U shaped Al tube

A-frames high strength carbon fiber composite

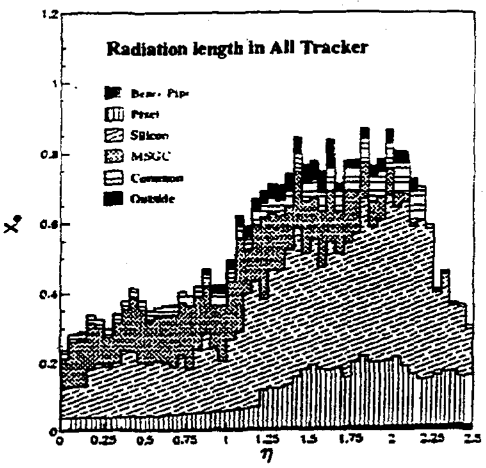
Tube and frames are gold plated and connected by dip brazing

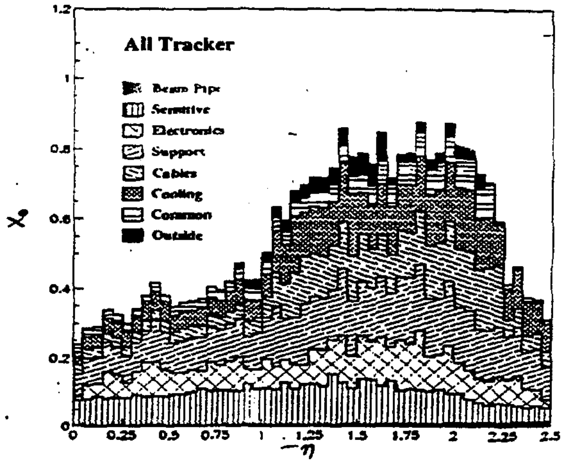
Turbine Geometry

- 12 Panel Support Structures are mounted between 2 half rings
- 20° rotation allows for charge sharing. Rotation is opposite for disks on different sides of IP
- Cooling supply and return lines are part of the space frame and service cylinder
- Material Budget
  - Panels 0.003 X/X_0
  - A frames 0.00316 X/X_0
  - Cooling pipes 0.00258 X/X_0
  - Total /wheel 0.023 X/X_0



Material





Constraints : Thermal screen between SST and MSGC.

Silicon tracker services require service to be axially at R=60 cm

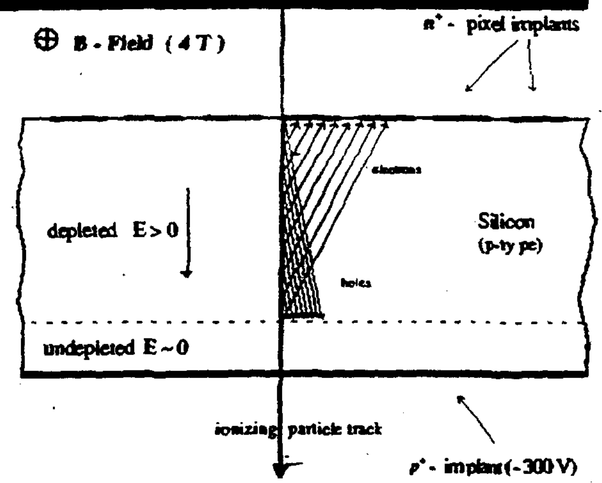
Installation of pixel sensor require services to be removed axially to the end flanges at R<20 cm

Cooling

- **Power consumption 60 μW/pixel$\Rightarrow$2.3 kW**
- **Total power 3kW**
- **Sensors must run at T=-10 °C**
- **Coolant should be**
  - **electrically isolating**
  - **inflammable**
  - **non-toxic**
- **HFE-7100 by 3M is a candidate but has radiation length=23cm**

Pixel size and shape

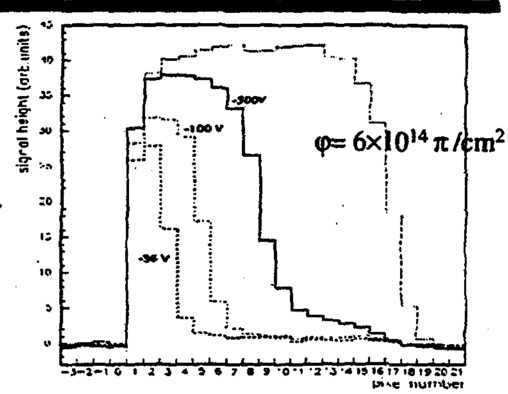
- Use n$^+$ on n-bulk silicon
  - ▶ Allows running with partially depleted sensors
  - ▶ large Lorentz angle in 4T field
- Impact parameter resolution depends on:
  - ▶ Hit resolution
  - ▶ Material budget
  - ▶ Distance from interaction region

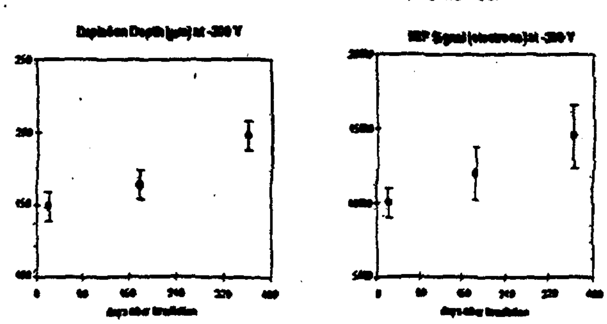


- **Pixel size depends on: readout chip, dissipated power, cooling. Minimum pixel area needed to host chip is 0.015 mm^2 $\Rightarrow$ 120μm side $\Rightarrow$ 35 μm. Improve resolution by seeking charge sharing and analog readout $\Rightarrow$ side 150 μm to accommodate partial depletion .**

Sensors R&D

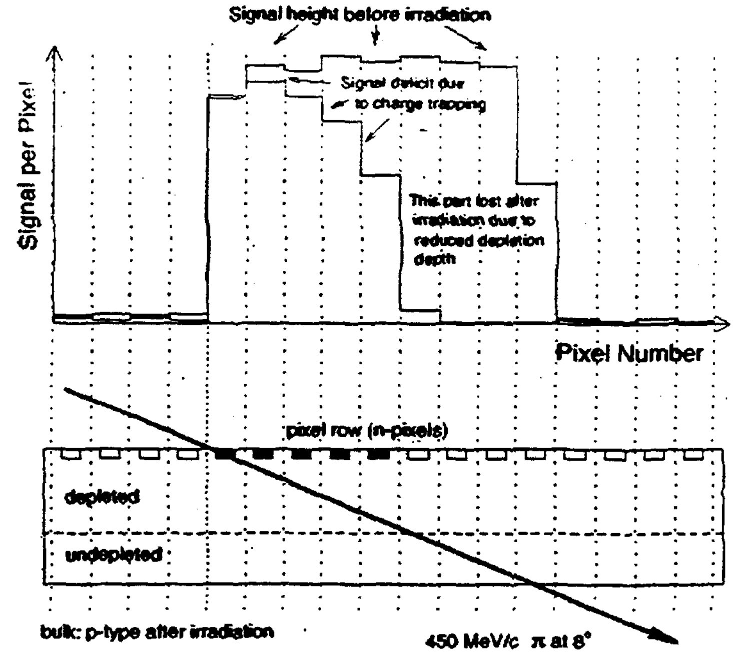
- A 8 $\times$32 squared Pixel array (125 ~ μm side) was irradiated up to φ= 3,6,9 $\times 10^{14}$ π/cm^2 ((p(π)=300 MeV/c) at T=3°C.
- Depletion depth measurement by the "grazing pions" method before and after irradiation.
- After irradiation sensors were kept at T=3°C. Annealing effects were observed after 6 and 12 months:
  - ▶ increase of the depletion depth
  - ▶ lower leakage current
- Expected signal 12000 e
  - ▶ Hit threshold 2000-3000 e
  - ▶ enc 400-600 e
  - ▶ $I_{leakage}$ =100 nA





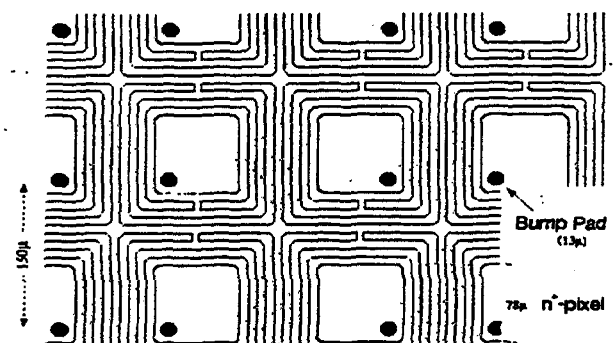
Grazing Method

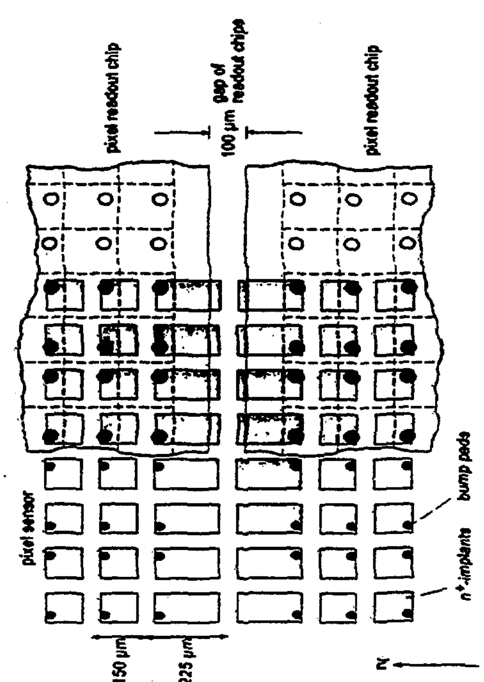
Signal from hit pixel measures the response at different depths



π graze pixel array at 8°

Sensors R&D





Pixels: 78 μm n-implants surrounded by two concentric p-stops rings with openings:

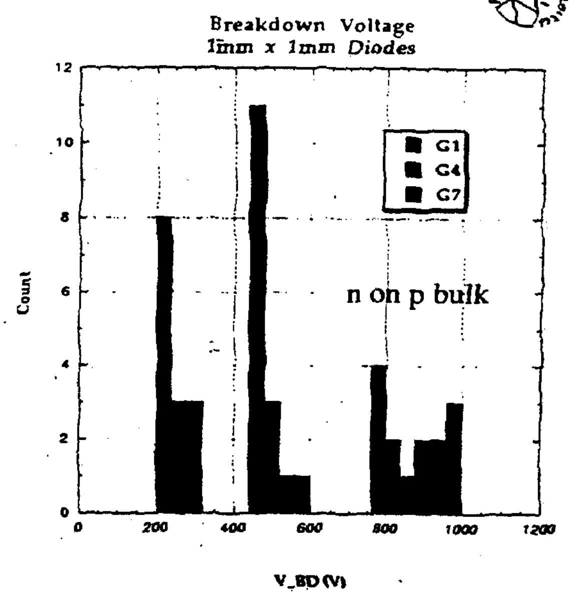
•high resistive path (O(100KΩ)) ⇒ Keep the n-implants biased if bump failed and allow $I_{leakage}$ testing before bump bonding.

•Reduce inter-pixel capacitance

Bump Pad =13 μm shifted by 25 μm to fit roc double column layout

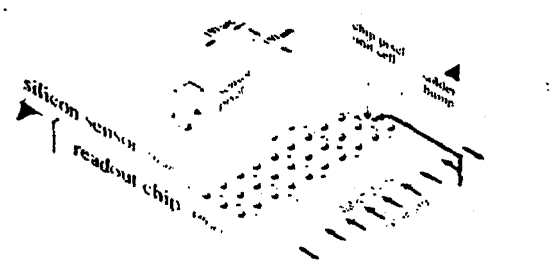
Sensors R&D

- Detectors must operate up to 300V. Breakdown voltage >500 V for $\varphi = 6\times10^{14}\ \pi/cm^2$
- **Design with 7 guard rings have given good breakdown results.**
- **Avoid large ΔV between sensor and chip (15-20 μm gap)**
- **Comprehensive study of guard ring design is still going on**



READOUT CHIP

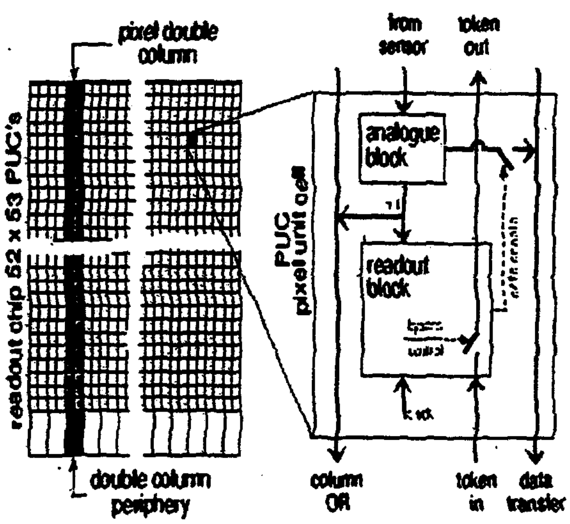
Analog ROC



•Each pixel connected by a bump bond to Pixel Unit Cell (PUC)

•Double column architecture controlled by double column periphery

•Local bus lines connect all PUCC to column periphery (column Or)

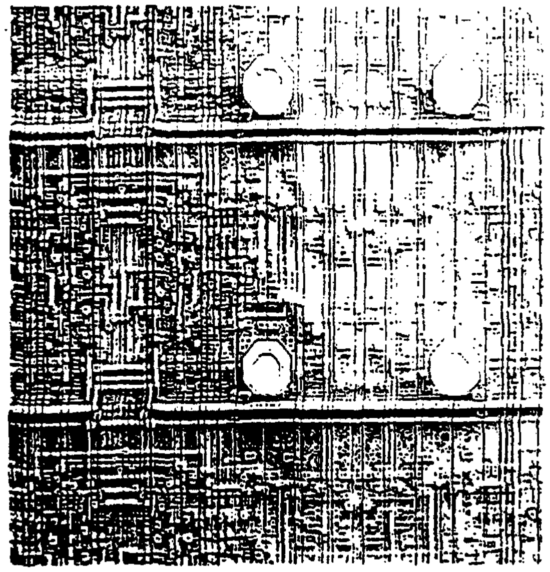


•PUC analog block signal amplification

•PUC digital block transmit a pixel hit ASAP to column periphery

READOUT CHIP

- **ROC and readout architecture design was guided by detailed *simulation* of sensors at the expected rates**
- **MC: PYTHIA top signal + 25MB. Low p_T tracks(>40 MeV/c) included. GEANT simulation included δ rays. ENC=300 e^- and 4 σ threshold.**
- ***Milestones:***
  - analog front end
  - choice of readout architecture
- **Radiation hard prototype has been constructed and operated**

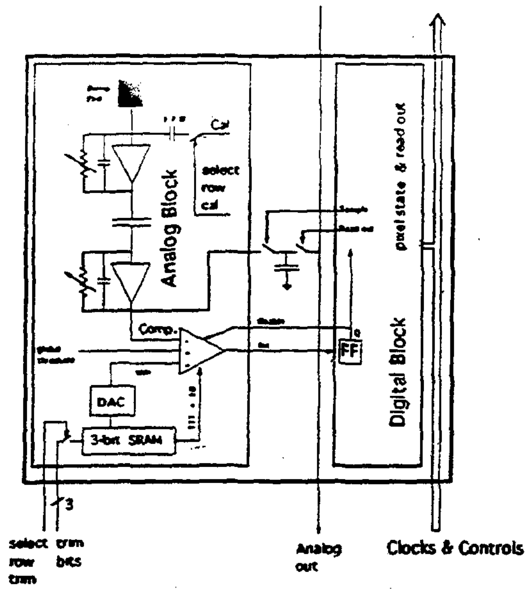


Pixel Unit Cell (PUC) Design considerations

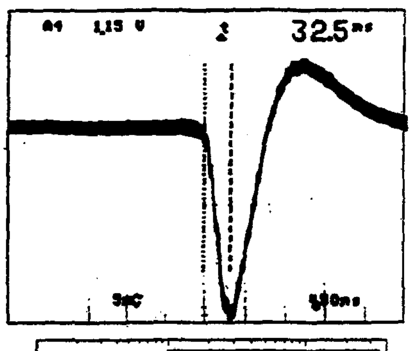
- **Charge $Q_{initial}$=3fC down to 2.3 fC after 4 years at 7cm**
- **Increasing $I_{leakage}$ leads to:**
  - **additional noise $\propto$ to shaping time (average 50 e^- for 10 nA)**
  - ***sink* leakage current up to 100 nA because of large tails**
- **Low noise operation requires ENC < 500 e^-**
  - **minimize pixel capacitance (expect 80 fF for 150μm squared pixels)**
  - **minimize bump pad capacitance (15 fF)**
- **Rate of noise hits is function of threshold**
  - **Pixel to pixel variations require trim mechanism**
- **Minimize time walk for correct association of hit to bunch crossing**
  - **amplifier peaking time <25 ns (limit CMOS technology)**
  - **zero-level threshold**
  - **off line pulse height dependent time-walk correction**
- **Minimize crosstalk**

Pixel Unit Cell (PUC) Analog block

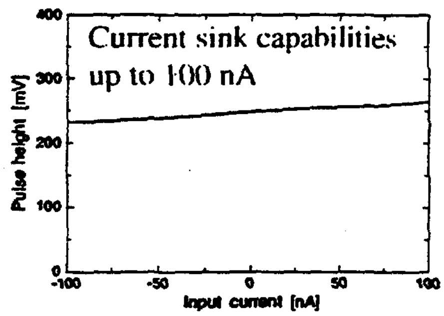
- Signal amplification: charge sensitive amplifier (feedback capacitor 30 fF) and capacitively coupled shaper⇒ gain=20-30 e/mV
- Hit detection: If signal > threshold PUC notifies periphery by column OR
- Global and trimmed threshold ⇒ Pixel masking and pulsing
- Temporary single hit storage



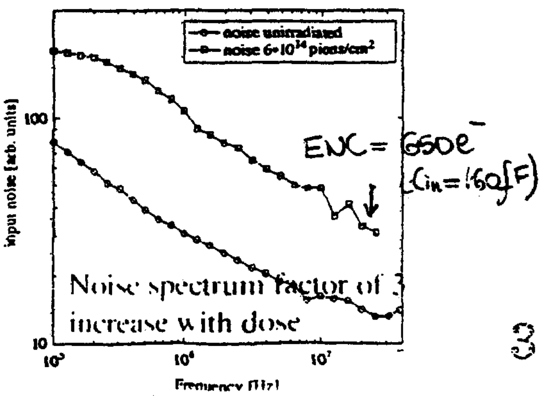
Pixel Unit Cell (PUC) Prototype results



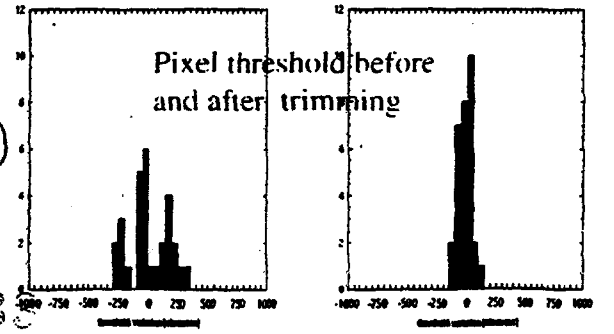
Signal pulse at the shaper output peak=32.5 ns with microprobe (100fF)



Current sink capabilities up to 100 nA

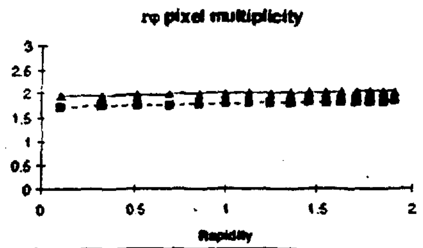


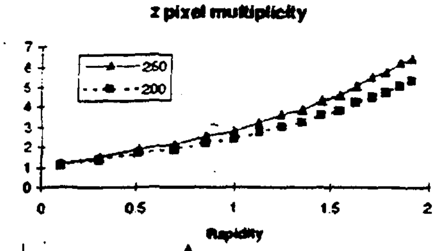
Noise spectrum factor of 3 increase with dose

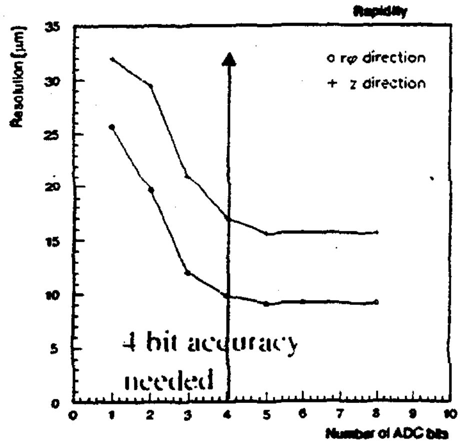


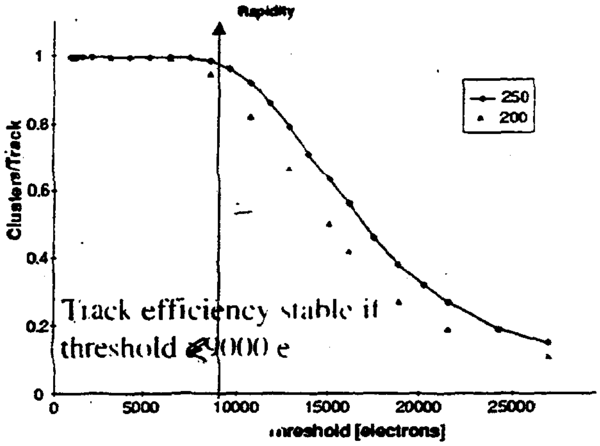
Pixel threshold before and after trimming

Pixel Unit Cell (PUC)
Simulation results

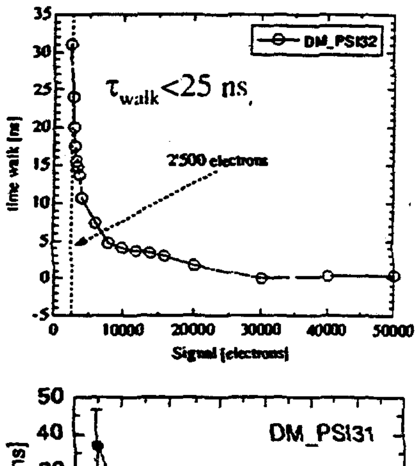


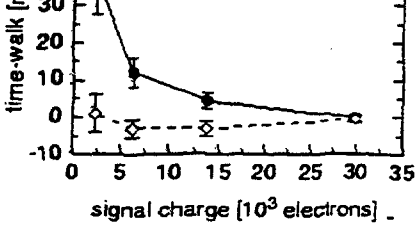




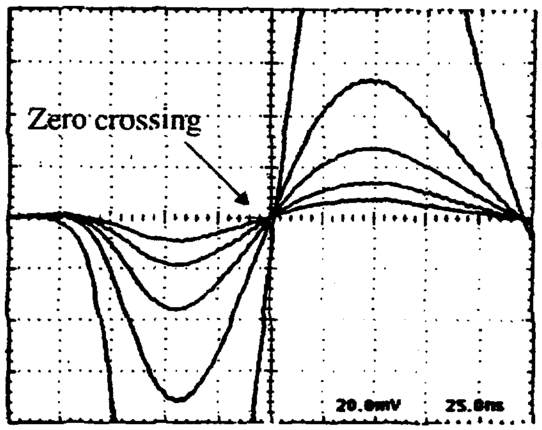


Pixel Unit Cell (PUC)
Prototype results



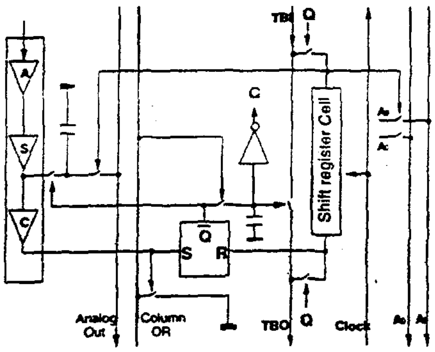


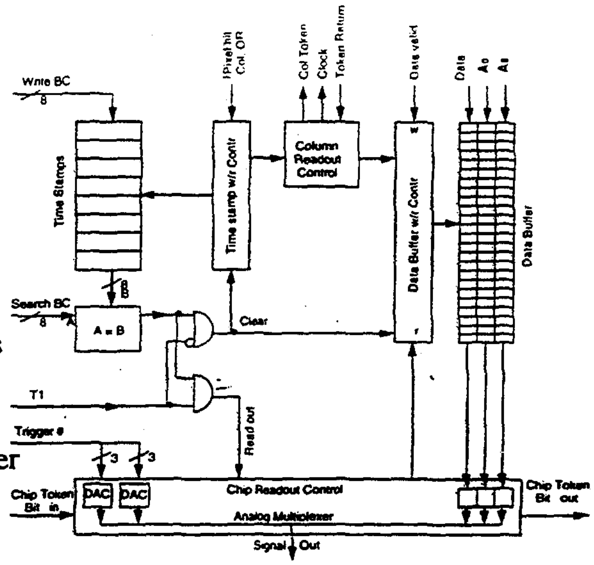
Amplifier pulses for different injected Q (1200-30000 e⁻) after irradiation with $10^{14}\pi/cm^2$



Implement pulse-height independent timing by using a second comparator

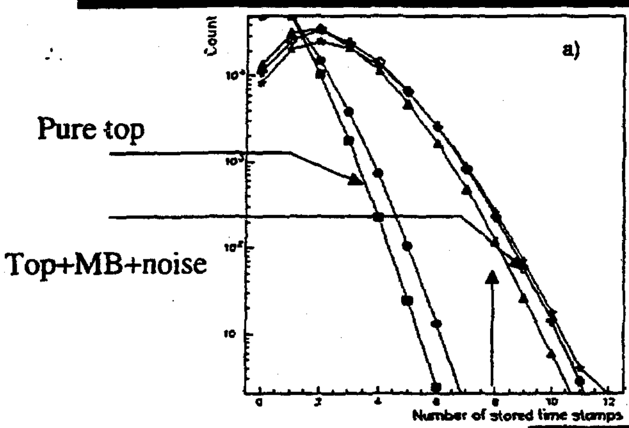
Column Drain Architecture

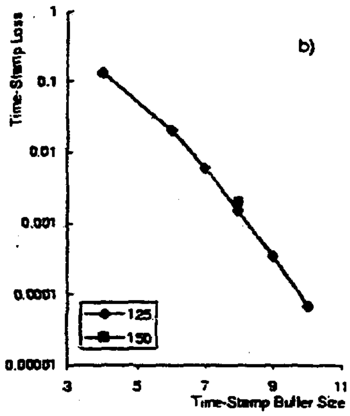




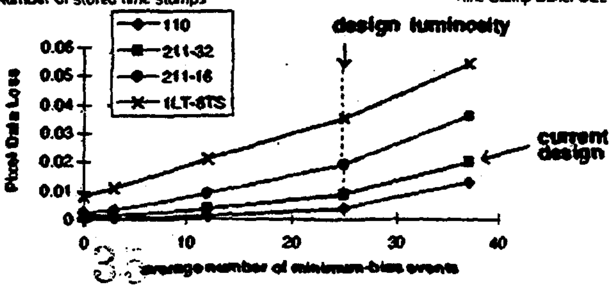
- The column periphery registers BC and sends token signal up and down the double column skipping empty pixels (at 1.6 GHz)
- In hit pixel the token signal initiate the transfer of pixel address and signal (Data Buffer) awaiting for L1T
- Time stamp, signal, addresses are transmitted from periphery to FED

Architecture Simulation



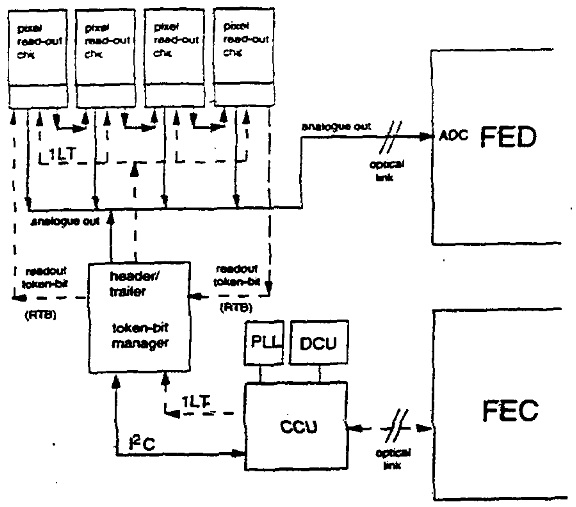


Architecture were pixel information stays on PUC until ITL is unacceptable



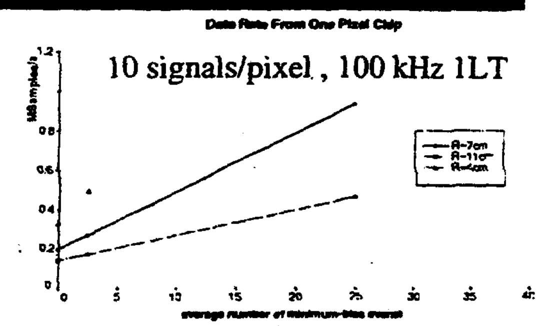
Data transmission

- Data accepted by 1LT is transmitted from column buffers to Front End Drivers located in the counting room.
- When and 1LT is present the Token bit manager chip (located on hybrid or portcard) puts a readout header signal on Analog-out bus and sends a readout token bit.
- RTB is passed through all the chips.



Data Rates

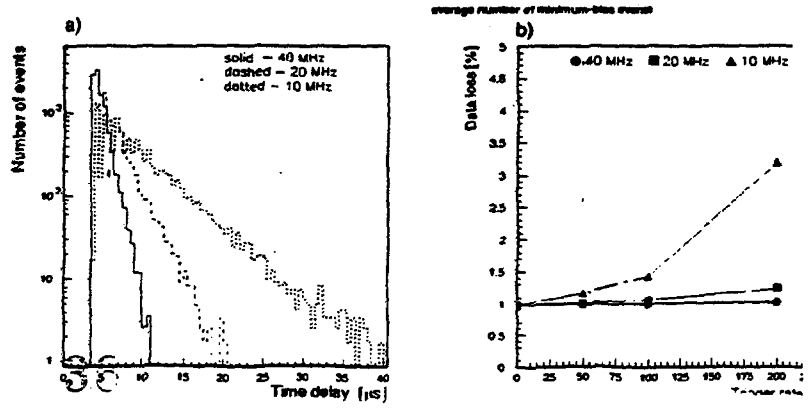
- High Luminosity a ROC will have one hit pixel/BC
- # of chips readout by a link must be chosen so that link does not saturate
- Assume analogue link will run ≥ 20 MHz



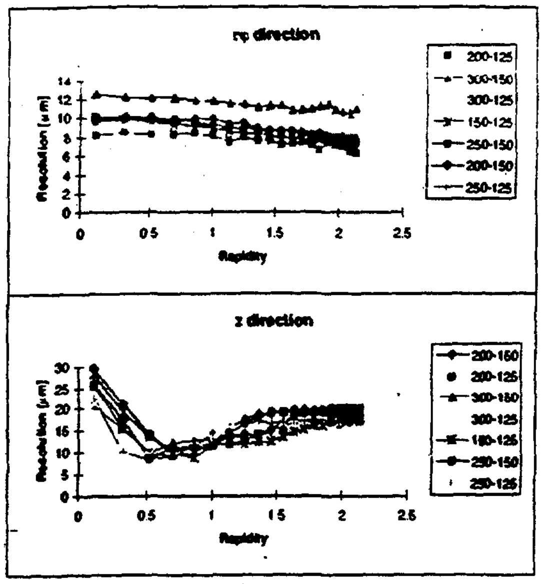
4 chip/link @7cm

8 chip/link @11cm

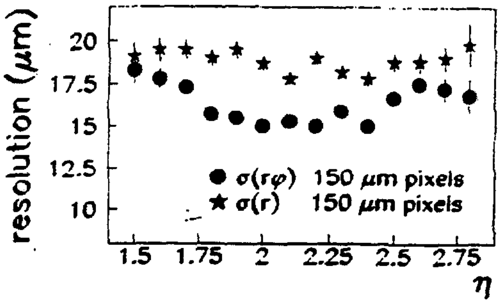
<7chips>/link for endcaps



Hit Resolution



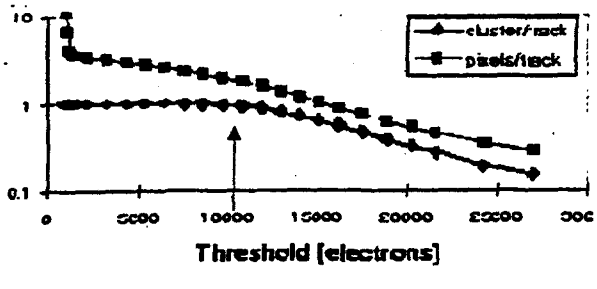
Hit Resolution for squared pixels as a function of the thickness and side length.

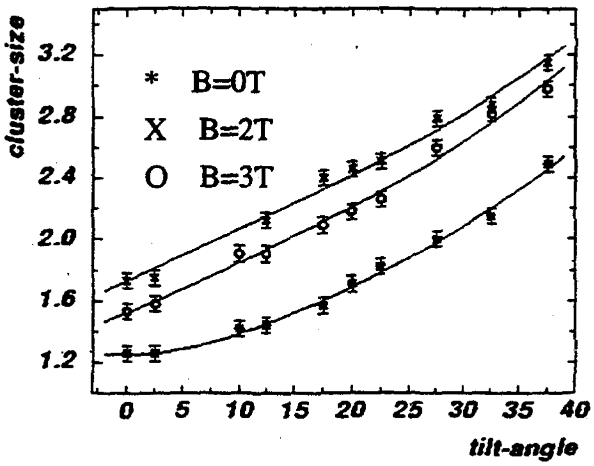


Endcap hit resolution

Hit Efficiency

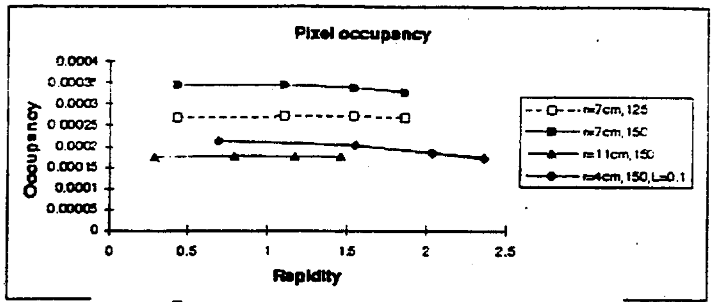
Cluster track efficiency ≈ 1 for threshold <10000e$^-$

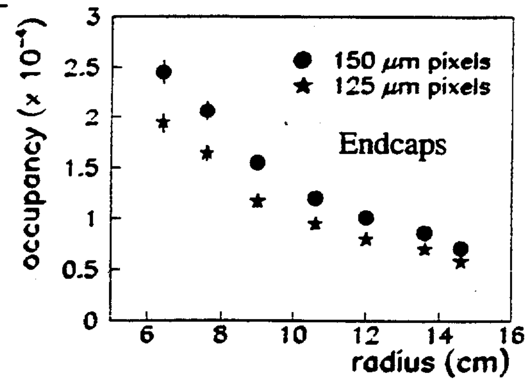




Measurements of 8×32 pixel array in B field (125 μm pixel side) agree with simulation

Occupancy





Barrel

Occupancy is defined as

$n_{pixel} > 4\sigma / N_{total}$

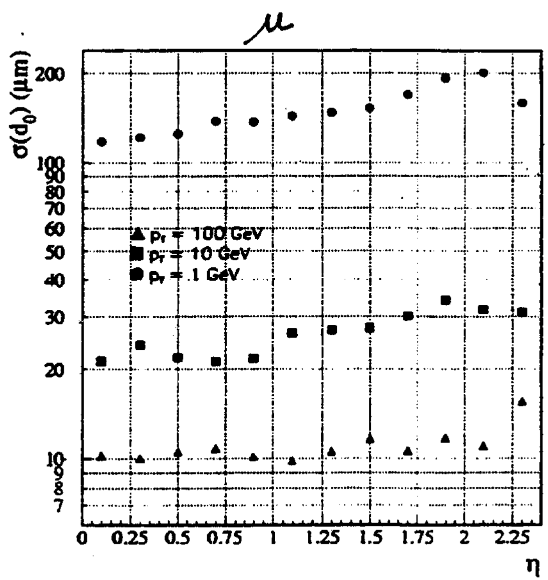
- **strong radial dependence influenced by B**
- **independent of η**

Performance

- **Impact Parameter resolution :**
  - **Dominated by the Pixel hit resolution and multiple scattering in the innermost pixel layer.**

    $\sigma(d0) \cong 9\ \mu m$ for high P_t
  - **In phase II the innermost layer is at 7 cm and**

    $\sigma(d0) \cong 12\ \mu m$ for high P_t

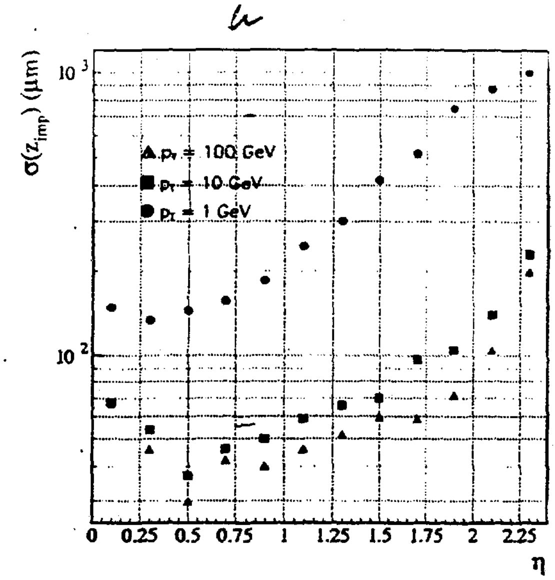


Performance

- Z_{imp} resolution:
  - At low P_T z_{imp} is degraded by multiple scattering and depends strongly on η

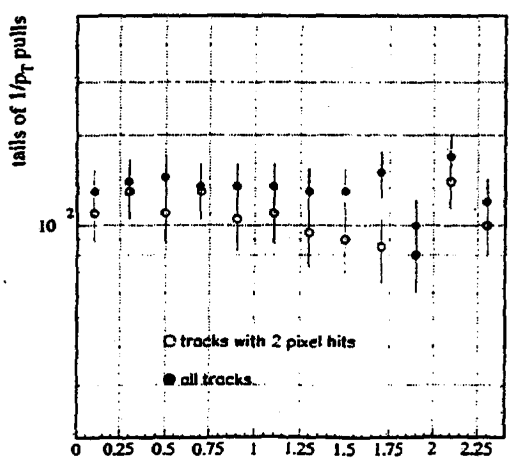
    $\sigma(z_{imp}) = 100\ \mu m$ central tracks

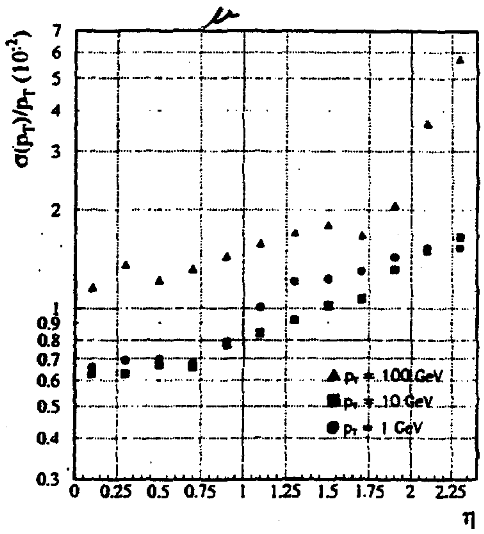
    $\sigma(z_{imp}) = 400\ \mu m$ at $\eta = 2$
  - Further degradation in phase II since in Phase I barrel extend to $|\eta|$=2.3 while in phase II measurement is provided by endcap only



Performance

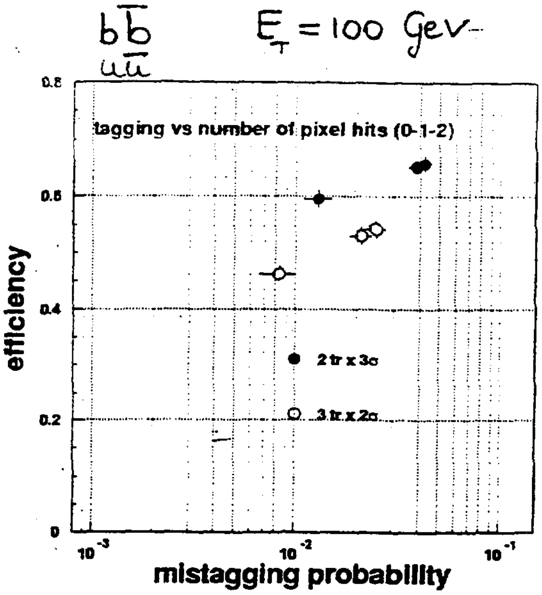
- P_T resolution:
  - 1-2 % for $|\eta| \leq 1.7$
  - Degradation at higher $|\eta|$ because of smaller tracker lever arm





B-tagging

- Impact parameter Tagging Efficiency as a function of mis-tagging rate for 100 GeV jets:
  - **Phase I has a higher b-jet efficiency since the pixel layer is closer to beam pipe**
  - **At least 2 measurements in the pixel detector are necessary to achieve high quality**



Summary

- **Pattern recognition and track reconstruction quality are achieved at high Luminosity**
- **Sensors R&D shows that operation at high voltage is feasible**
- **Novel p-stop design should minimize capacitance and allow to keep pixels at V if bump bond fails**
- **Radiation-hard Prototype chip achieves performance within the LHC requirements**

  Pixel threshold of 2500 e⁻ is above cross talk level

  A 5σ cut requires noise level of 500 e

- **Prototypes power dissipation is within the analog power budget of 40 μW/pixel**

Federico Antinori (INFN-Padova)
for the Alice Collaboration

Silicon Pixels in Alice

Alice Pixels Institutes:
Bari, Catania, CERN, Padova, Roma, Salerno

Contents:
- Introduction:
  Alice, why Si pixels, requirements
- Bird's eye view of basic concepts and status of R&D for:
  - Ladder assembly
  - Front-end chip
  - System r/o and control
  - Bussing
  - Mechanics & Cooling

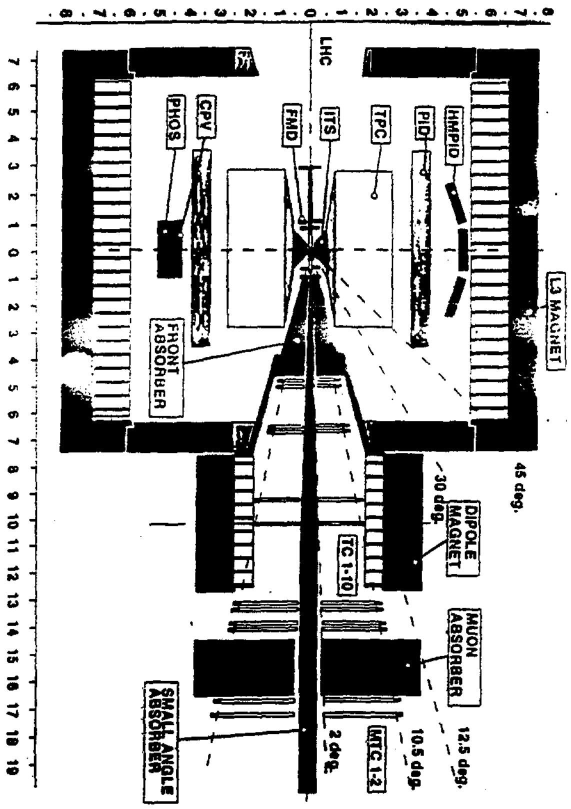
→ see also related talks:
- E. Cantatore on RD19/WA97/NA57
- W. Snoeys on front-end chip
- W. Klempt on Alice Inner Tracking System mechanics

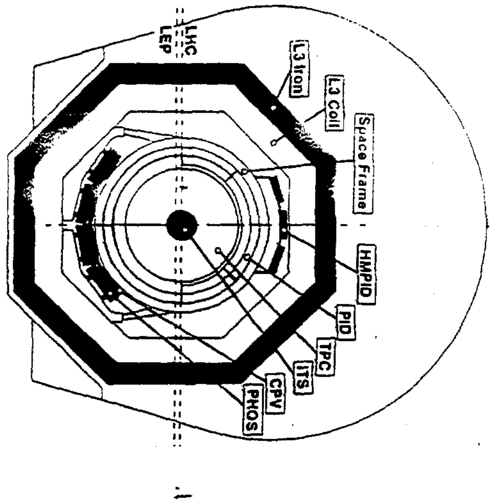
Alice environment

Nucleus-Nucleus collisions at $\sqrt{s}$ = 5.5 TeV/nucleon
☞ search for deconfinement phase transition
hadronic matter → Quark-Gluon Plasma (QGP)

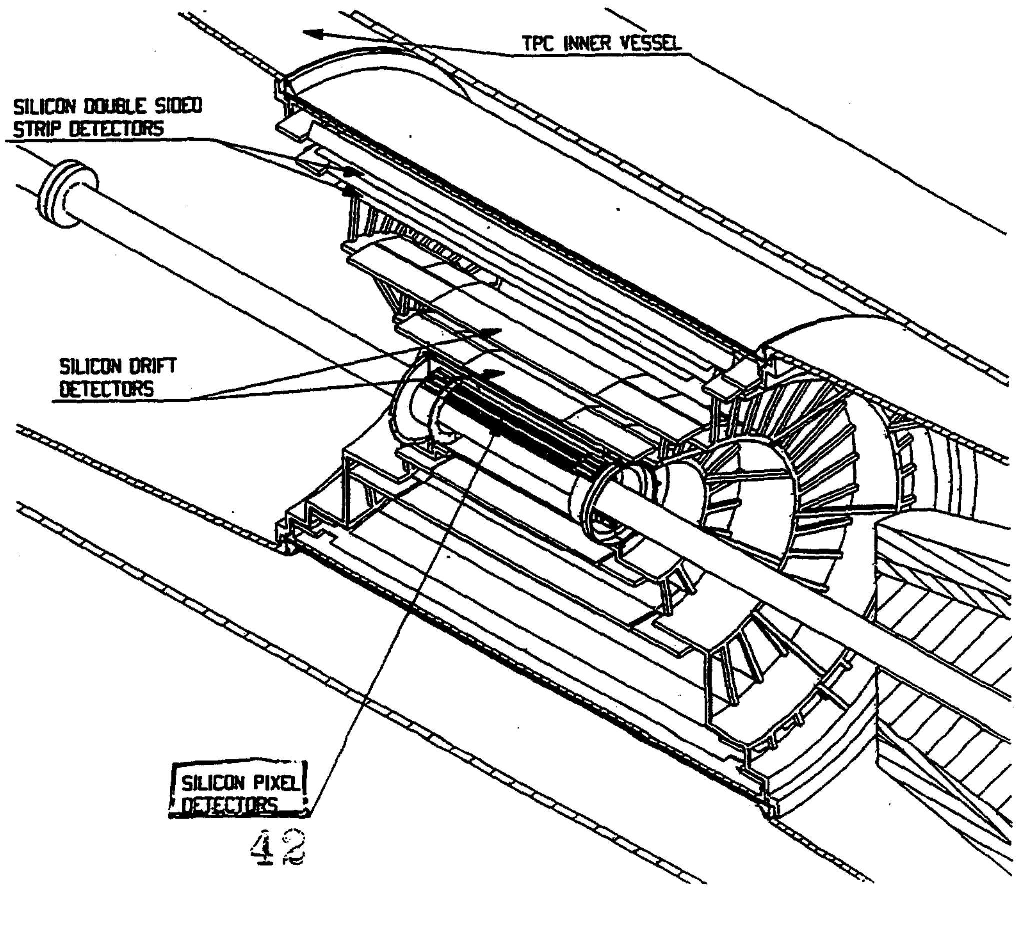
	Pb+Pb	p+p	Ca+Ca (low)	Ca+Ca (high)
L ($cm^{-2}s^{-1}$)	10^{27}	10^{30}	$2.7\ 10^{27}$	10^{29}
Rate (kHz)	8	100	8	300

Radiation:
at ~ 4 cm from beam in 10y standard running scenario:
200 krad, 10^{12} n/cm^2





ALICE Inner Tracking System



Si Pixels in Alice

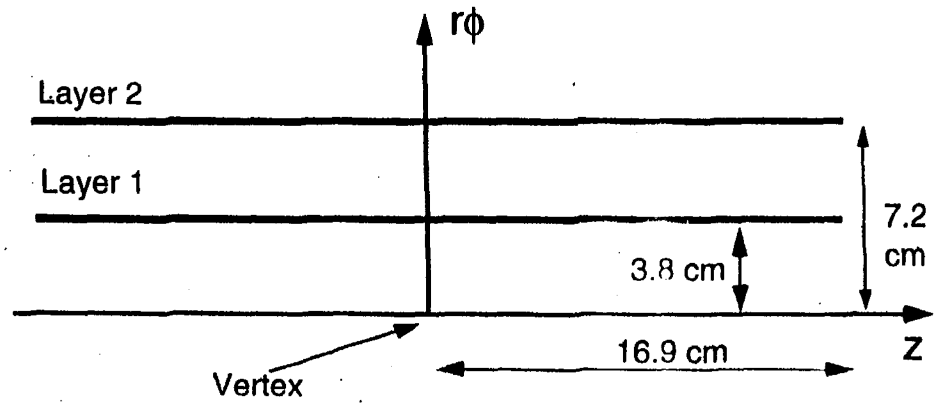
→ Two innermost layers:

- Mainly for secondary vertex detection (strangeness, charm)
- Less than 10 cm from the vertex
- Track density > 50/cm²

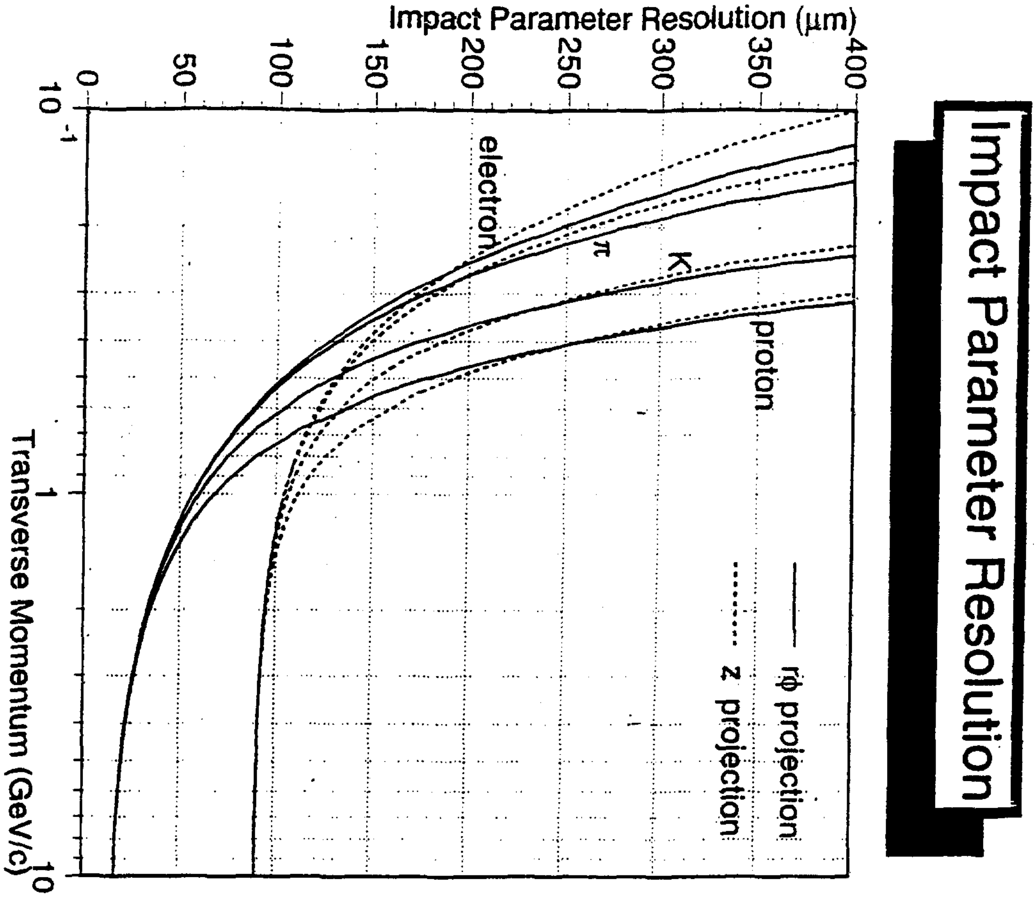
☞ Need high precision, high double track resolution → Si pixels!

→ High rate capability can be exploited in high luminosity running modes, e.g. standalone determination of primary vertex position for Debye screening runs (~ 500 kHz in Ca+Ca collisions at $L=10^{29}$ cm^{-2} s^{-1})

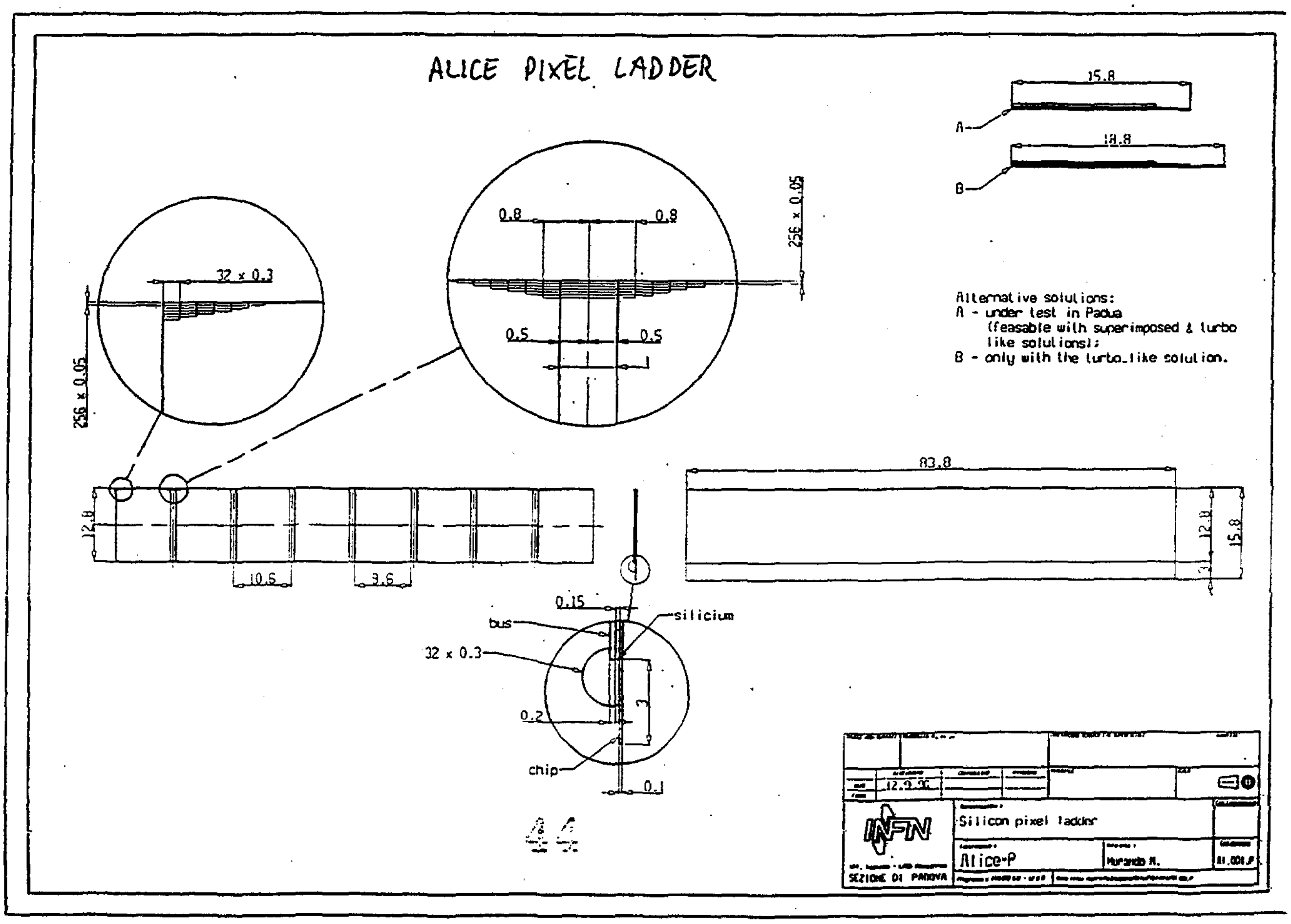
Requirements



- cell size: 50 µm (rφ) x 300 µm (z)
- strobe latency: up to 2.5 µs
- strobe duration: 200 ns
- r/o speed: < 200 µs / event
- material thickness: ~ 0.6 % X_0 / layer
- radiation tolerance: 200 krad, 10^{12} n/cm²



Impact Parameter Resolution
Impact Parameter Resolution (μm)
Transverse Momentum (GeV/c)
electron
π
K
proton
rφ projection
z projection



ALICE PIXEL LADDER
Alternative solutions:
A - under test in Padua
(feasable with superimposed & turbo like solutions);
B - only with the turbo_like solution.
32 x 0.3
256 x 0.05
bus
silicium
chip
Silicon pixel ladder
Alice-P
SEZIONE DI PADOVA

Bump-bonding

- Production of Omega3 assemblies for NA57 experiment ongoing with GEC-Marconi
- 1.2 M pixels installed in the NA57 telescope
- In the present production we have reached a ladder yield of ~ 70%

Thin assembly

- Thinned-down chip (100 μm) and thin detector (150 μm) Omega3 wafers at GEC-Marconi, ready for bump-bonding

Front-end chip specs

- Cell size: 50 μm (critical) x 300 μm (non critical)
- Binary read-out
- Strobe latency: 2.5 μs
- Strobe duration: 200 ns
- R/O time (system): 200 μs
- Rad tolerance: > 200 krad
- Threshold: 2000 e with 200 e spread (thin detector)
- Individual chip bias adjustments with on-chip DACs
- JTAG controls
- Individual cell mask at digital level + column mask
- 32 x 256 cells per chip

LHC2Test / Alice1Test chip
(CERN-MIC group)

2 x 65 cells in MIETEC 0.5 μm:

- Gate-all-around design for rad tolerance
- individual cell leakage current compensation

☞ rad tolerance at least several 100 krad
→ OK for Alice

but:

- density still insufficient for full Alice cell implementation in 50 μm x 300 μm
- relatively large threshold variation

→ <u>see presentation by Walter Snoeys</u>

Alice2Test chip
(CERN-MIC group)

2 x 65 cells in IBM 0.25 μm, ready for submission

improvements w.r.t. Alice1Test:

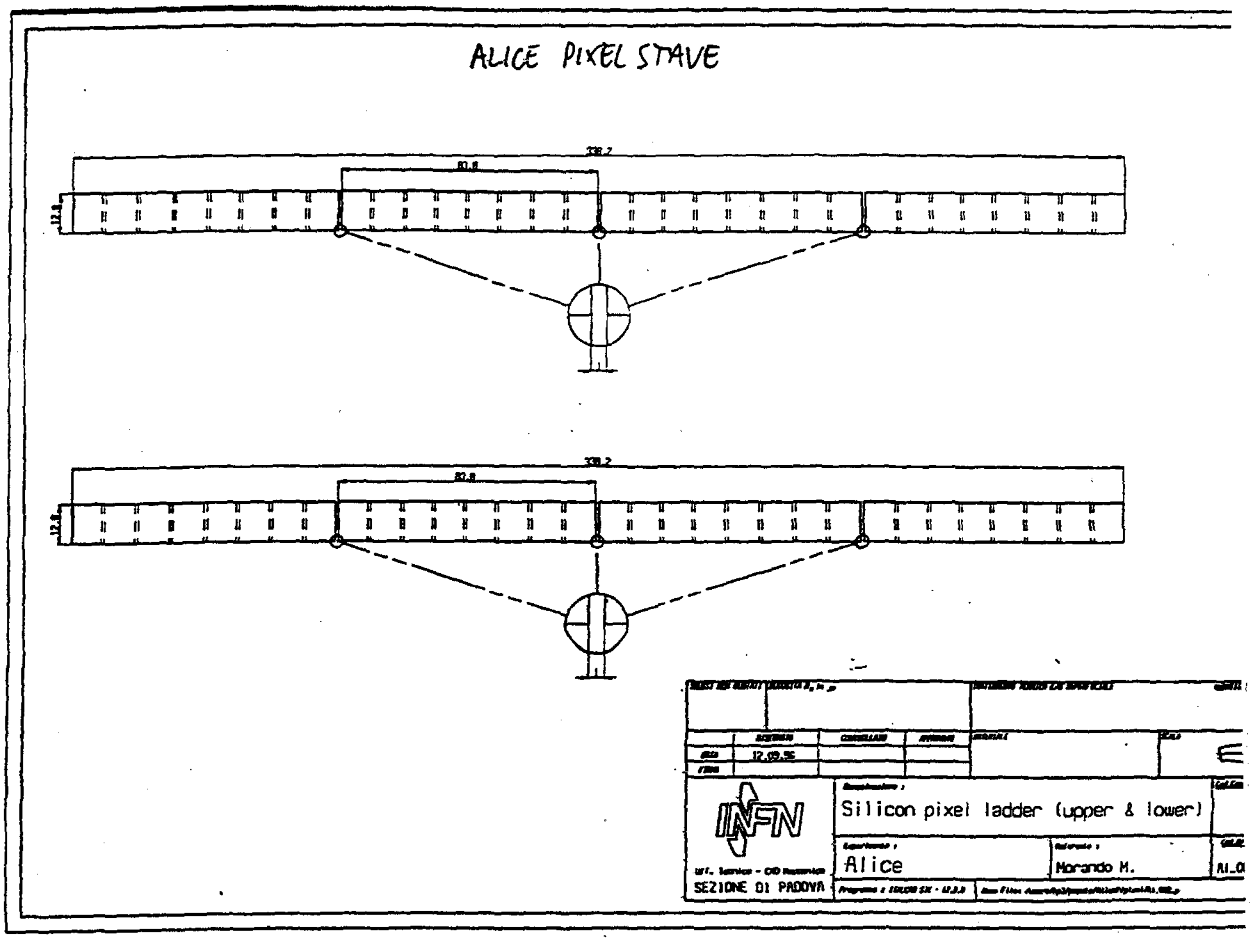
- higher density (→ still higher radiation tolerance?)
- no nMOS current mirrors (better use of real estate)
- counter replaces delay line

→ density sufficient for full Alice cell implementation in 50μm x 3

- <u>individual cell 3-bit threshold adjust</u>

→ see presentation by Walter Snoeys

☞ full-size Alice chip being designed, submission at end of 199



System r/o and control:
(CERN - ED group)

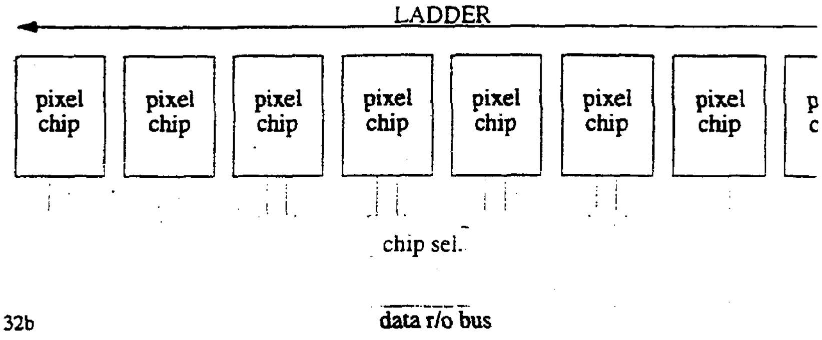
<u>Basic principles</u>:

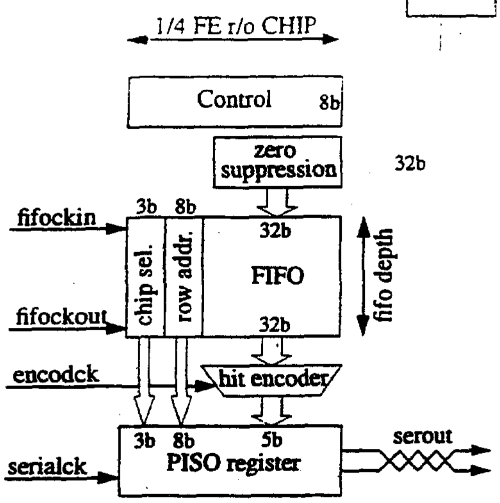
- Readout in 200 μs → 10 MHz clock row shift
- Minimize cabling → serial link (+ buffering)
- Minimize data on link → zero suppression, address encoding
- Simple control + testability (boundary scan) → JTag - IEEE 114
- High integration → custom control chip at end of the stave (rad. tolerant like front-end chip)

4 May 1998

Readout block diagram.

- *The basic modularity for the Readout is the Ladder.*





$$fifockin = \frac{256 \times 8}{200\mu} = 10.24 MHz$$

$$serialck = \frac{(8196 \times 1\%) \times 16 \times 8}{200\mu} = 52.5 MHz$$

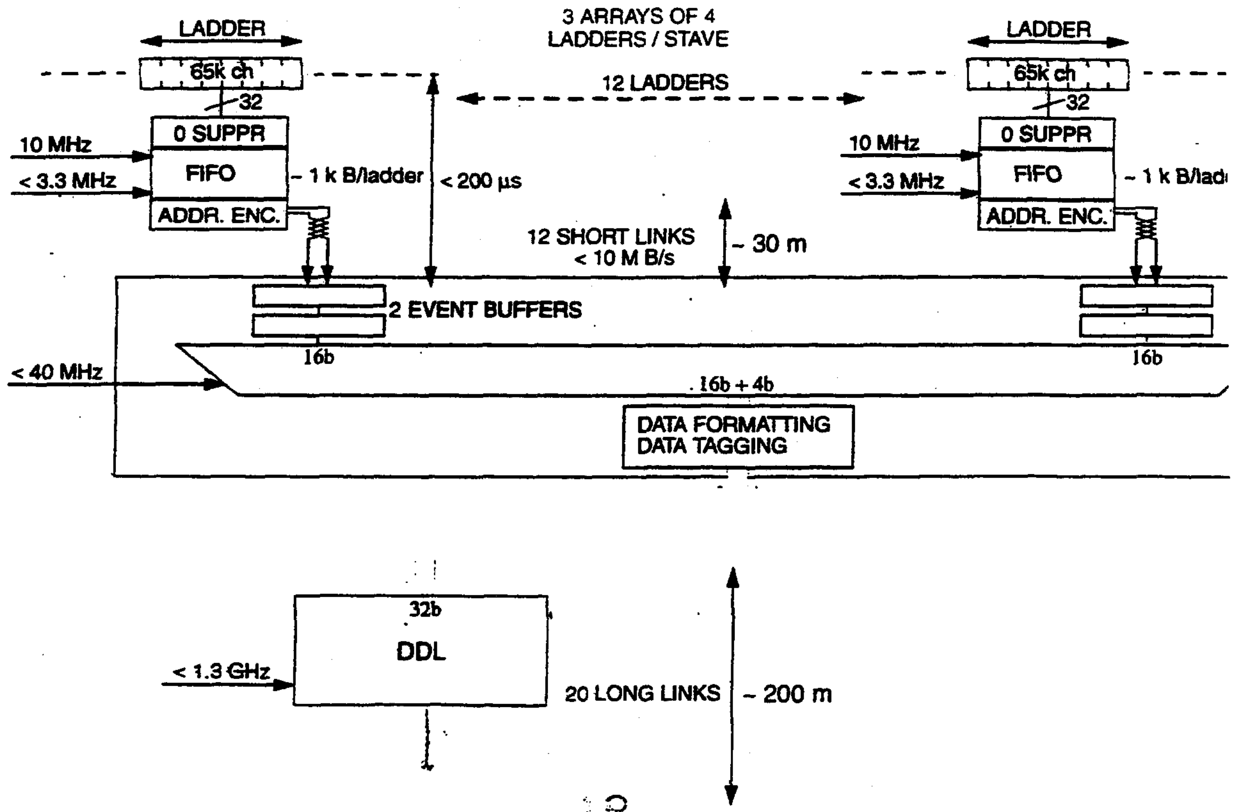
$$encodck = \frac{52.5 MHz}{16} = 3.3 MHz$$

$fifockout \leq 3.3 MHz$:(Worst case = 1 hit/row)

$$fifodepth = R(n \geq 1) \times 8 = 70 \times 8 = 560w$$

4 May 1998

Readout by DDL.



Bussing

Read-out and control bus:

- Multi-layer (~5)

- thin (~10 μm Al, ~ 20 m polyimide per layer)

- 100 to 150 μm line pitch.

- CERN workshop → down to ~ (<) 200 μm line pitch → OK for Omega3 ladders

We are:

- producing an Omega3 version to learn how to handle these circuits on the present ladders

- contacting vendors, preparing a market survey
  → from informal contacts:
  150 μm pitch feasible now,
  100 μm pitch in 1-2 years

Mechanics, cooling
(INFN - Padova)

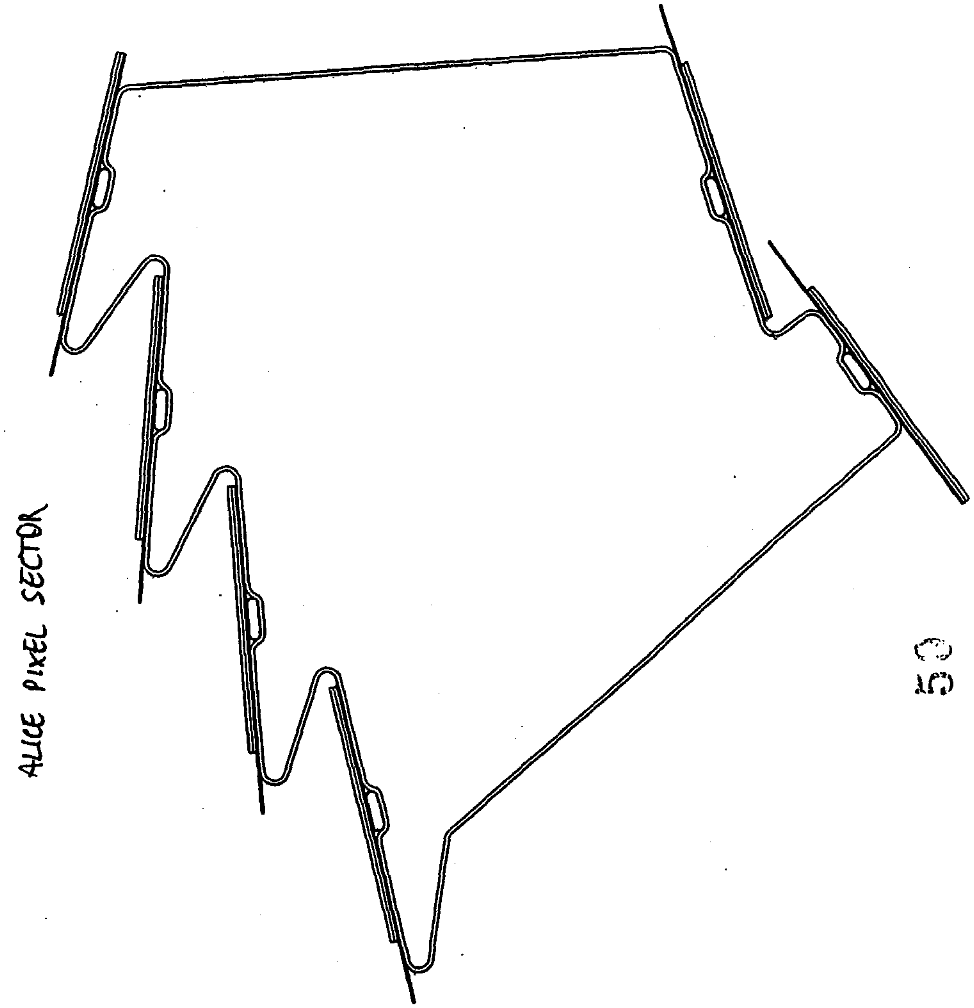
<u>Basic choices</u>:

- Material:
  - minimize radiation length
  - high modulus
    → unidirectional carbon fibre
  - optimize thermal and mech. properties
    → cyanate resin
  - maximise fibre/resin ratio
  - adapt material to geometry

- Geometry:
  - minimize material for required stiffness
  - reasonable modularity for maintenance
    → 10 independent support sectors
  - maximise ladder support surface
    → turbo solution

Basic choices, contd:

- Cooling:
  - No need to go below room temperature
  - W_{TOT} ~ 500 W
    → air cooling is out
  - Minimise fluid density
    → water cooling
  - Robustness w.r.t. plumbing faults
    → "leakless" (below 1 Atm)
  - Maximise exchange surface
    → squeezed cooling vessel
  - Integrate cooling vessel in carbon fibre structure



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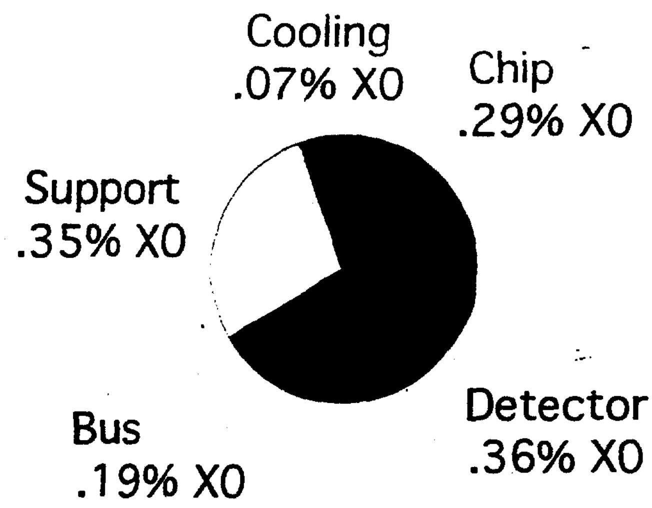
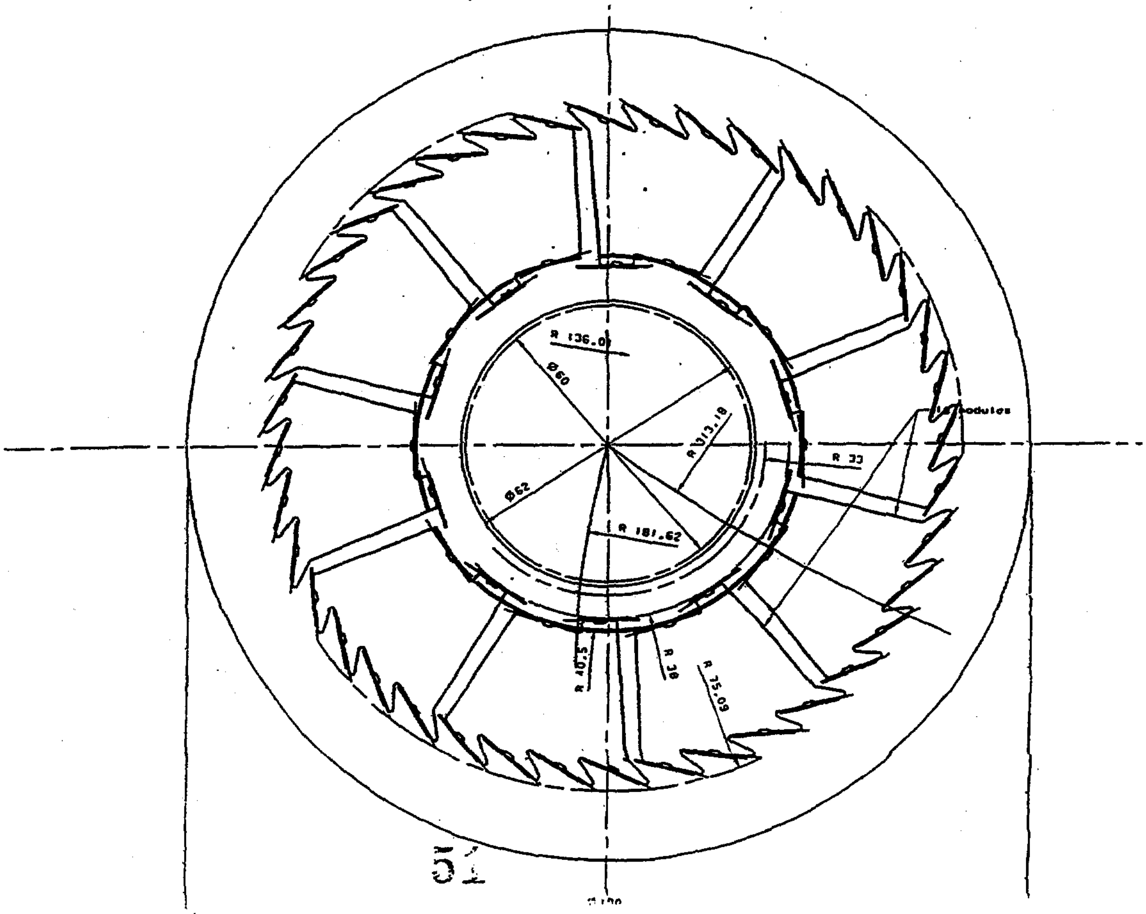
Material Distribution

Average material seen by a particle traversing both layers = 1.26% X0



ALICE PIXEL BARREL



Mechanics, cooling R&D
(INFN Padova)

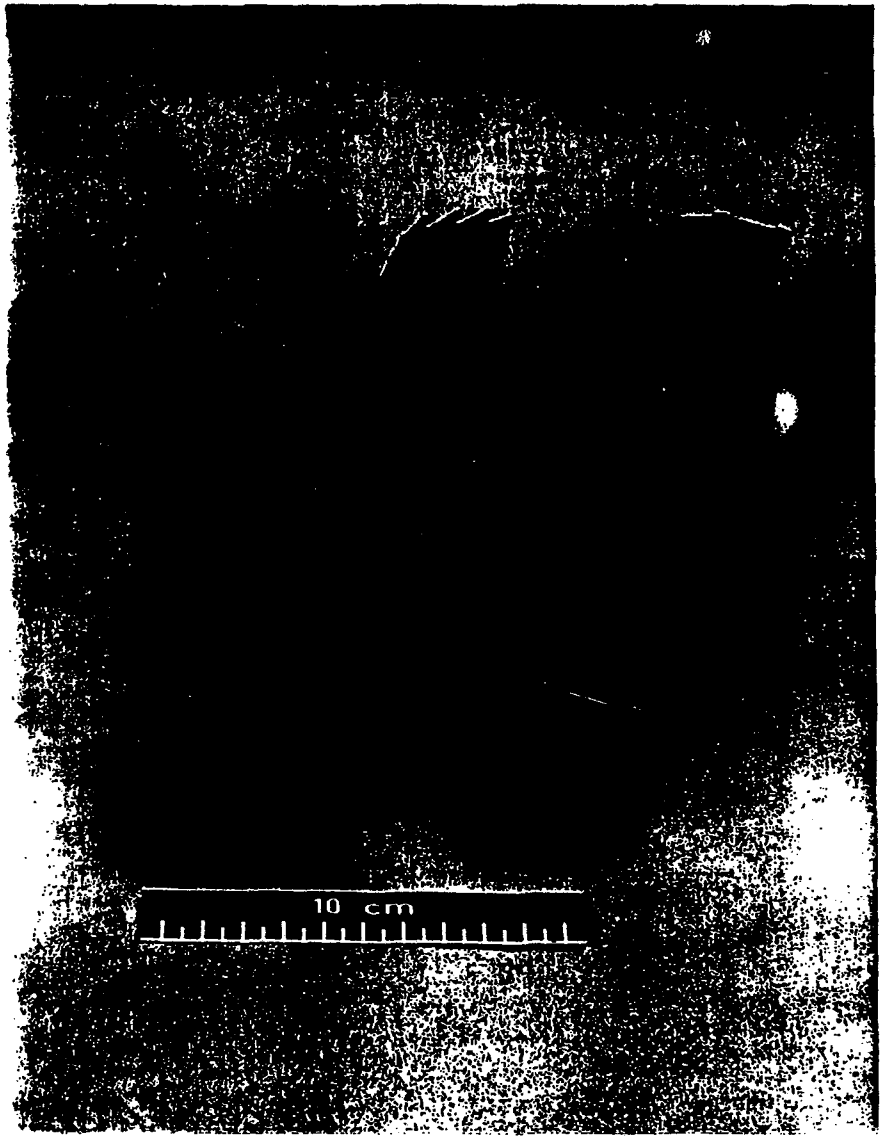
- Full-size prototypes of carbon-fibre support sectors produced in industry

→ feasibility demonstrated

- Composite material lab at LNL (Legnaro) now operational → next phase in-house

- Setting up "leakless" cooling system in LNL

- To do:
  - study/control stability of production tolerances
  - control local buckling
  - verify cooling simulations



Main Design Parameters

		Layer 1	Layer 2
r		3.8 cm	7.2 cm
Δz		33.8 cm	33.8 cm
cell size	50 µm x 300 µm		
# cells	15.7 M	5.2 M	10.5 M
occupancy		1 %	0.3 %
# ladders	240	80	160
surface	0.26 m^2	0.09 m^2	0.17 m^2
strobe latency	2.5 µs		
strobe duration	200 ns		
min. threshold	2000 e		
threshold rms	200 e		
r/o time	200 µs		
power	~ 500 W	~ 150 W	~ 350 W
total thickness	1.2%X_0	.6% X_0	.6%X_0
det. thickness	150 µm		
chip thickness	100 µm		
rad. tolerance	200 krad, 10^{12} n/cm^2		

International Pixel Detector Workshop
PIXEL98
May 7-9, 1998
Fermilab, Batavia, Illinois

Developments of Pixel Hybrid Photon Detectors for the RICH counters of LHCb

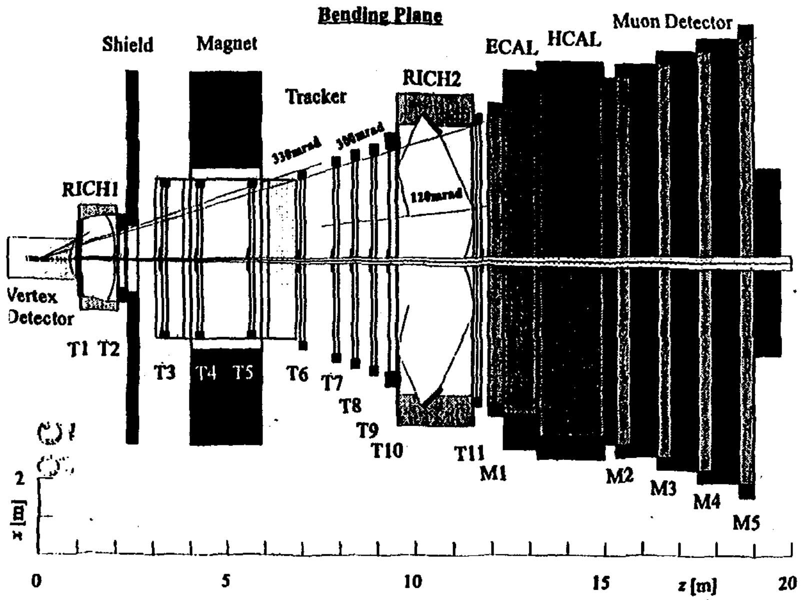
M. Alemi[1,2], M. Campbell[1] (speaker),
F. Formenti[1], T. Gys[1],
D. Piedigrossi[1], D. Puertolas[3],
E. Rosso[1], W. Snoeys[1], K. Wyllie[1]

1 CERN, Geneva, Switzerland
2 University of Milano, Italy
3 INFN Section of Rome, Italy

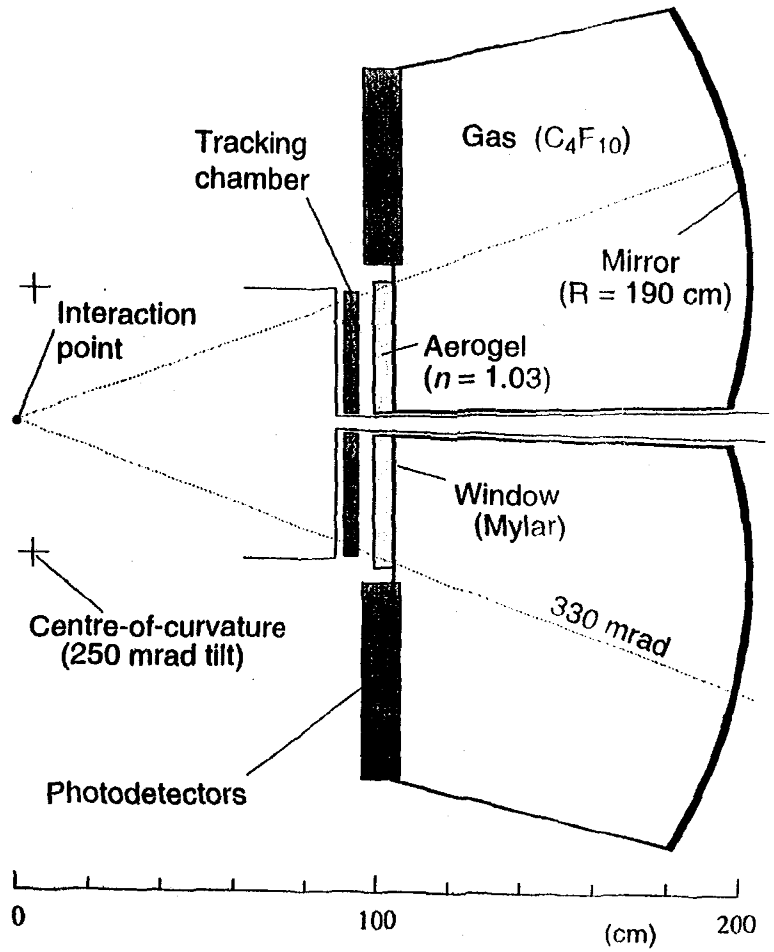
Outline of the talk

- Introduction
  - The LHCb RICH counters
  - Overall system requirements
  - Photo-detector requirements
- Half-scale prototype tube
  - Schematic design
  - Single-photoelectron efficiency
- Large tube developments
  - Schematic design
- Front-end and read-out electronics
  - Architecture
  - Implementation
- Conclusions

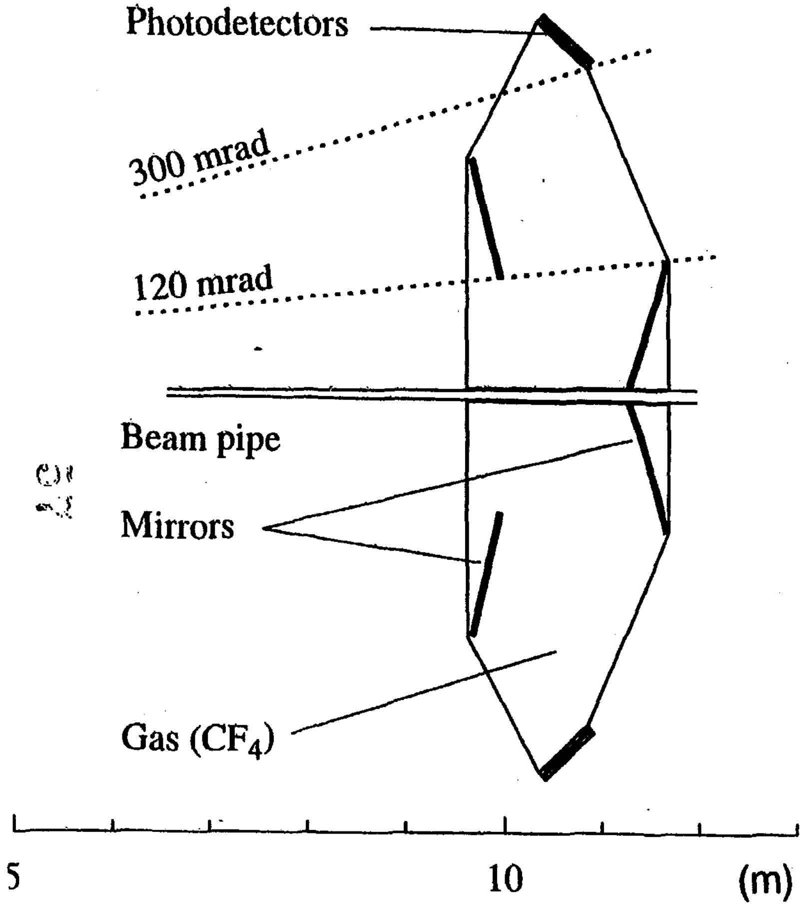
The LHCb detector



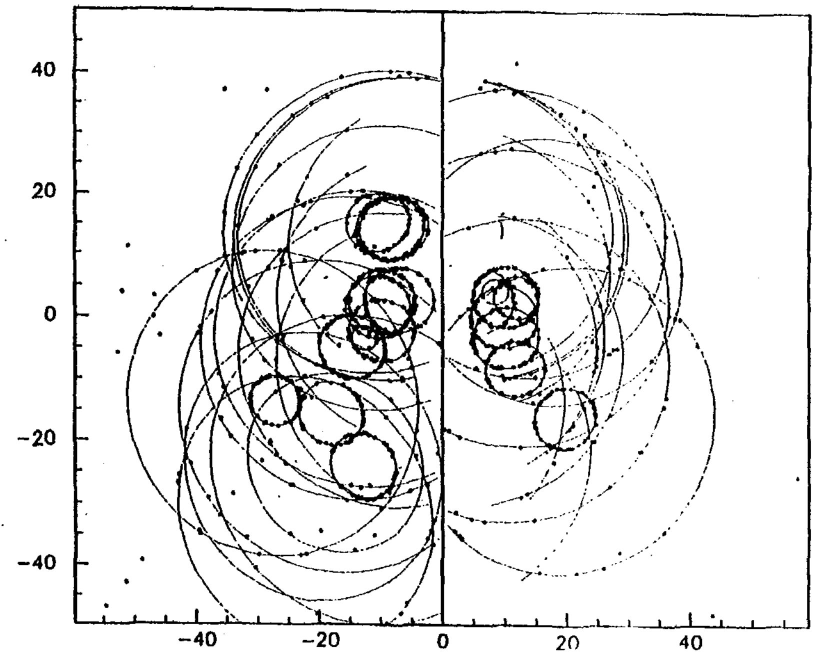
The RICH 1 counter



The RICH 2 counter



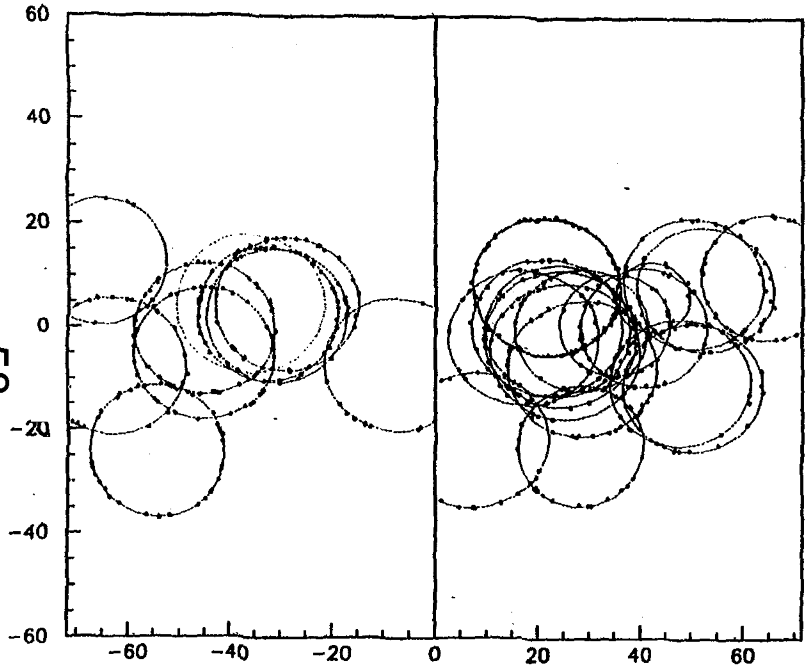
A simulated event in RICH 1



Contains $B_d^0 \rightarrow \pi^+\pi^-$

C_4F_{10} rings: 55 pe, ~10 cm Ø, $p_{th}(\pi)$ = 2.6 GeV/c
Aerogel rings: 15 pe, ~40 cm Ø, $p_{th}(\pi)$ = 0.6 GeV/c

The same event in RICH 2



CF_4 rings: 30 pe, ~20 cm Ø, $p_{th}(\pi)$ = 4.4 GeV/c

Overall system requirements

- **Photon detection**
  - **RICH 1: 2 × (60 cm × 100 cm)**
  - **RICH 2: 2 × (72 cm × 120 cm)**

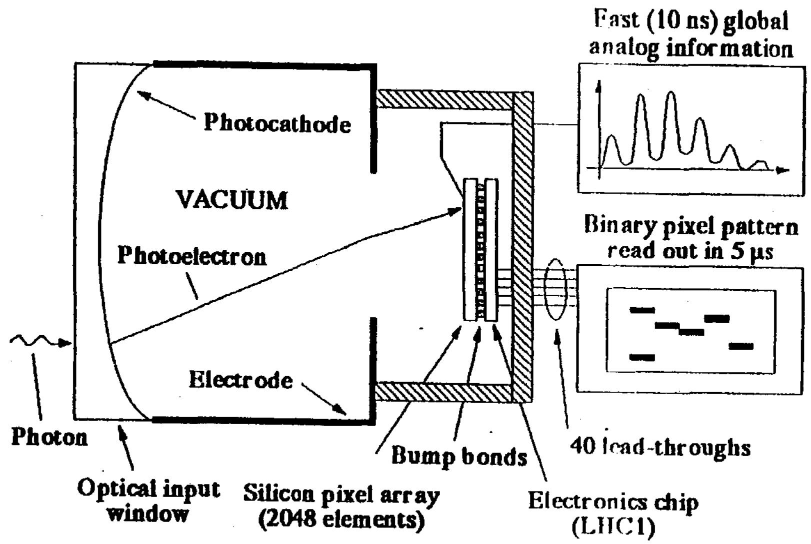
    => ~2.9 m^2 total surface
  - **Granularity: 2.5 × 2.5 mm^2**
  - **Active area coverage: 73 %**
    => *~340'000 channels*
  - **Single-photon sensitivity (λ = 200-600 nm)**
- **Environment**
  - **Radiation dose: 3 krad/year (RICH 1)**
    1 krad/year (RICH 2)
- **Read-out**
  - **Maximum occupancy: 8 % (RICH 1)**
    1 % (RICH 2)
  - ***LHCb-specific trigger scheme* (see *later*)**
- **Photo-detector options**
  - ***Pixel-HPD:* *cross-focussing geometry,* binary pixel readout (this talk)**
  - ***Pad-HPD:* "fountain" tube geometry, analogue pad readout**
  - **Multi-anode PMT: metal channel dynodes, analogue or binary readout**

Motivations for pixel-HPDs

- **Features**
  - Past experience
  - Cross-focussed optics with kovar electrodes
  - Pixels bump-bonded to readout electronics
  - Binary read-out
  - Pixels
  - Vacuum tube compatibility

- **Performance**
  - ISPA-tubes + RD19
  - Good spatial resolution, robust to external E and B
  - Small capacitance (low noise, high speed), compact anode structure
  - Low power consumption (i.e. low heat dissipation)
  - Pattern recognition
  - Low outgassing, survives bake-out cycles

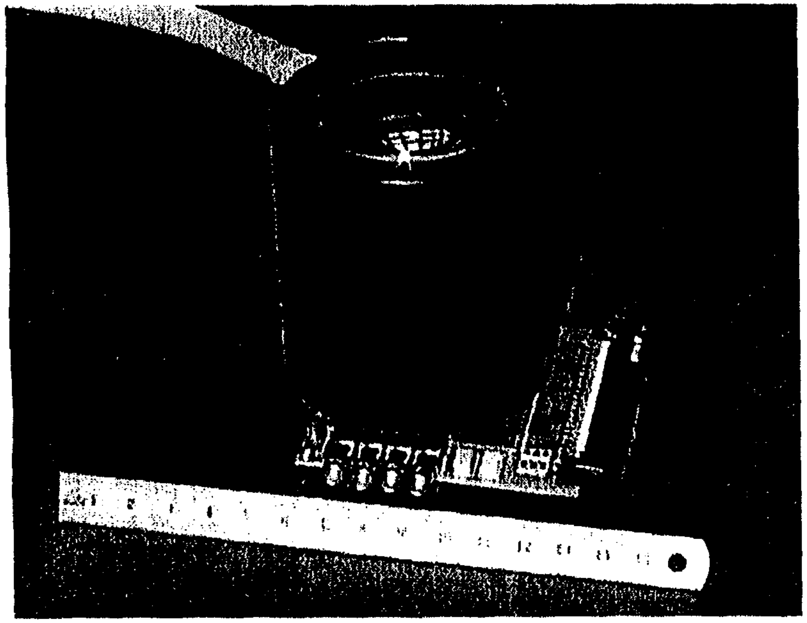
Half-scale prototype tube (schematic design)



40 mm active input diameter
11 mm active output diameter
4:1 demagnification factor
30 μm spatial resolution
20 kV accelerating potential (5000 e-h pairs)

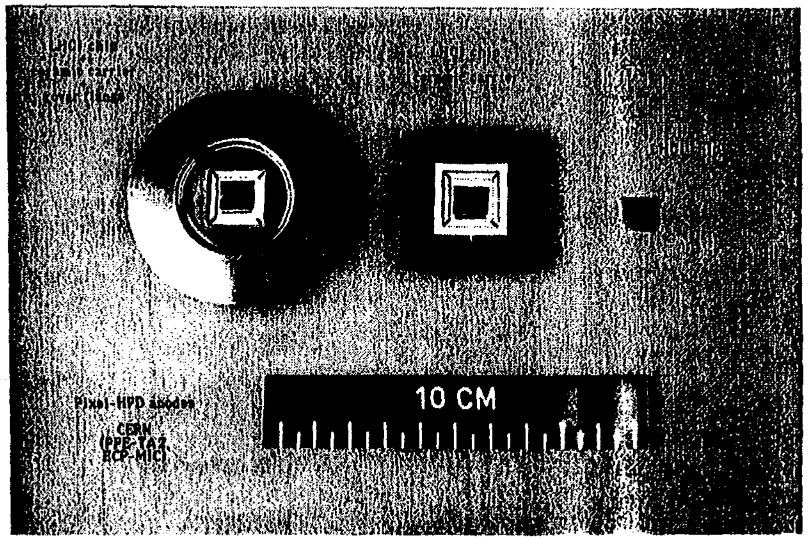
LHC1 electronics (see talk of E. Cantatore)

Half-scale prototype tube (photograph)

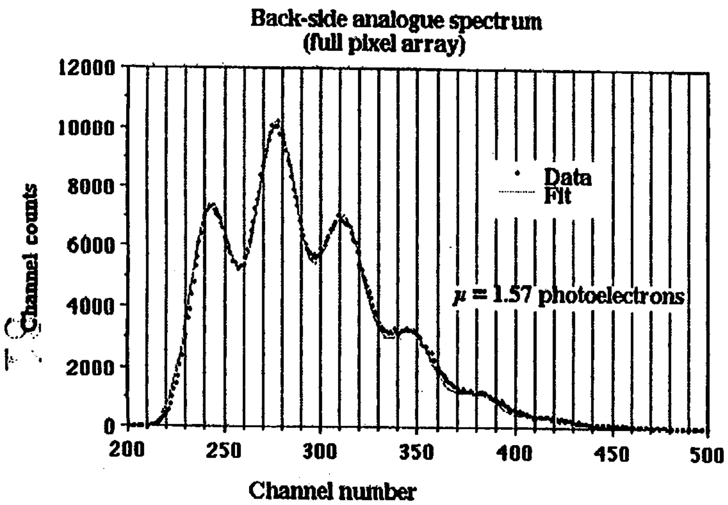


Manufactured by DEP B.V., Roden, The Netherlands

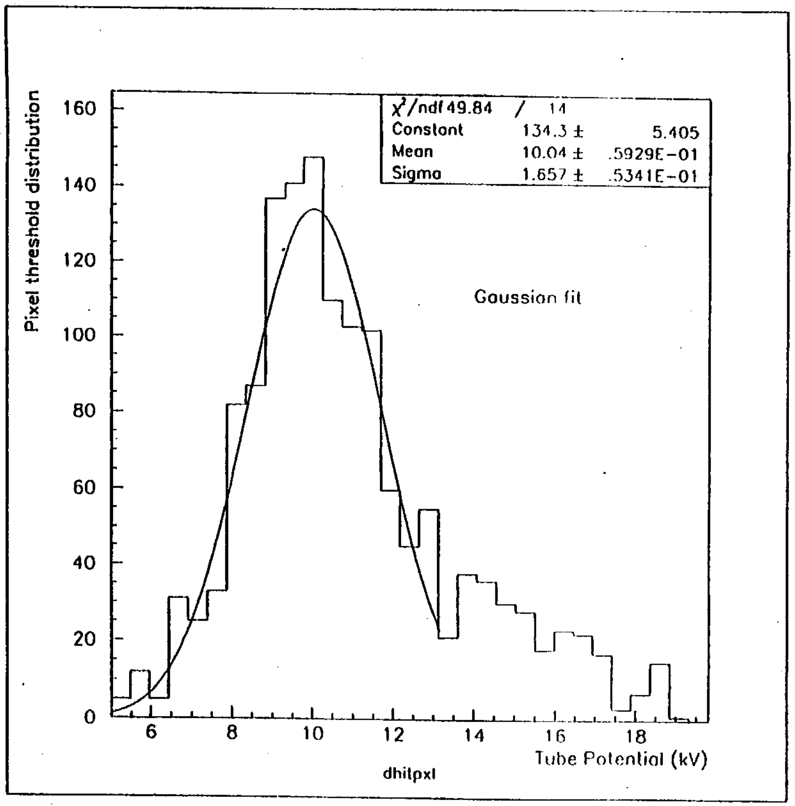
Half-scale prototype tube (anode assembly steps)



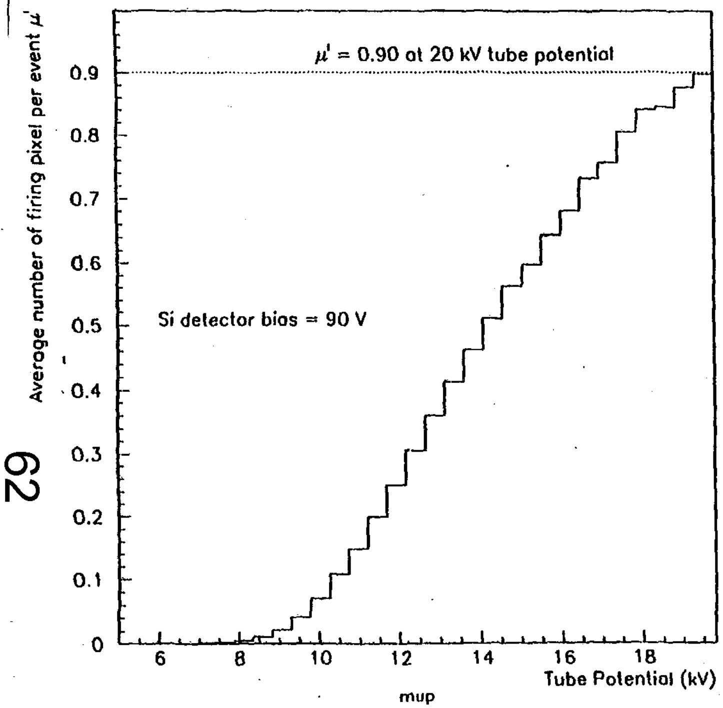
Back-side analogue spectrum



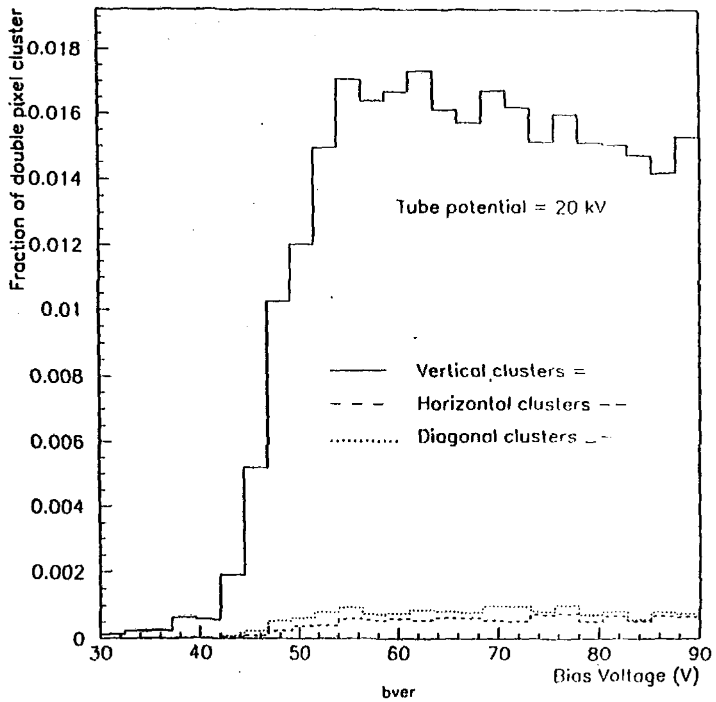
Threshold distribution



Firing pixels vs tube potential



2-pixel clusters vs det. bias



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Single photo-electron detection efficiency

- Average number of pe μ (back-side analogue spectrum)
  - $\mu = 1.57$ pe
- Masked and inactive pixel correction (low or high thresholds)
  - 1456/2048 = 0.71
- Average number of firing pixels μ' (LHC1 binary readout)
  - $\mu' = 0.90$
- Single photoelectron detection efficiency
  - 0.90/(1.57*0.71) = 0.81
- Inefficiency attributed to:
  - photoelectron back-scattering at the detector surface (charge signal decrease)
  - charge sharing effects at the pixel boundaries (charge signal division)

Full-scale prototype tube

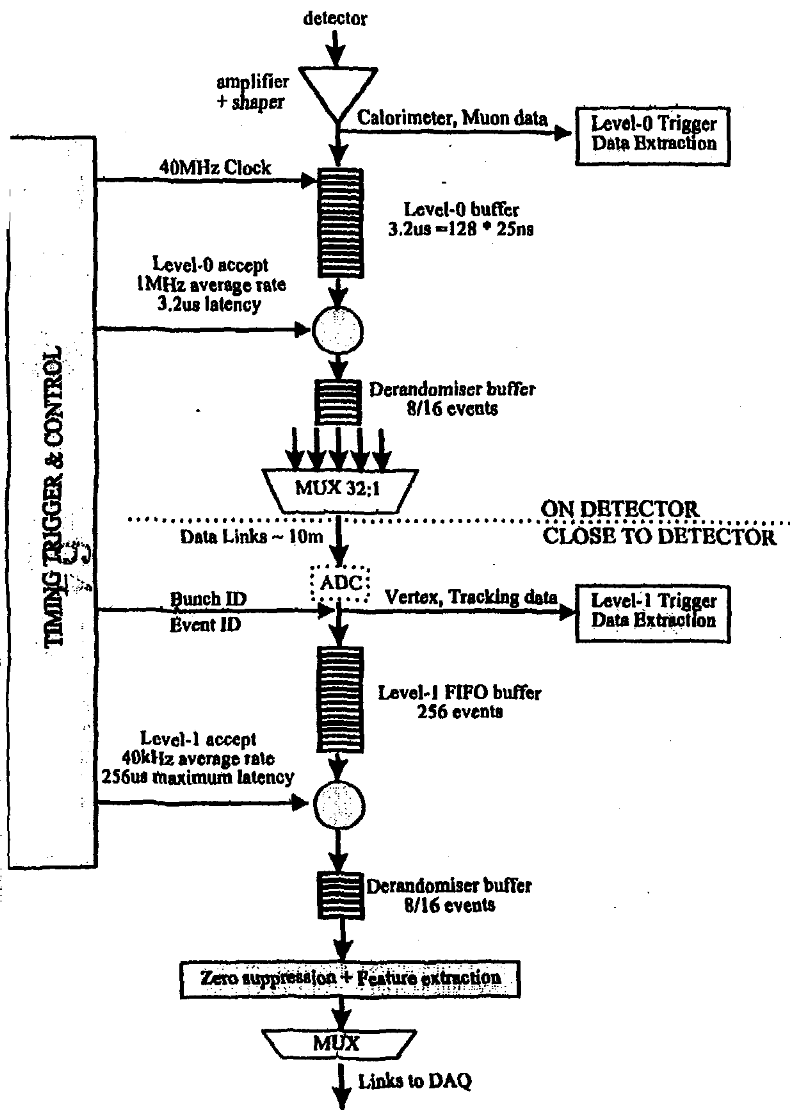
- Geometry
  - 72 mm active input diameter
  - 18 mm active output diameter
  - 4:1 demagnification factor
  - 100 μm spatial resolution

  => ~500 tubes for the entire RICH system
- First prototype
  - Phosphor screen anode
  - CCD readout

  => check of active area, electron-optics, magnetic field sensitivity.
- Second prototype
  - 61-pixels anode
  - UK RICH prototype readout

  => check of pe response to Cerenkov light

LHCb front-end architecture



Binary pixel front-end chip

REQUIREMENTS:

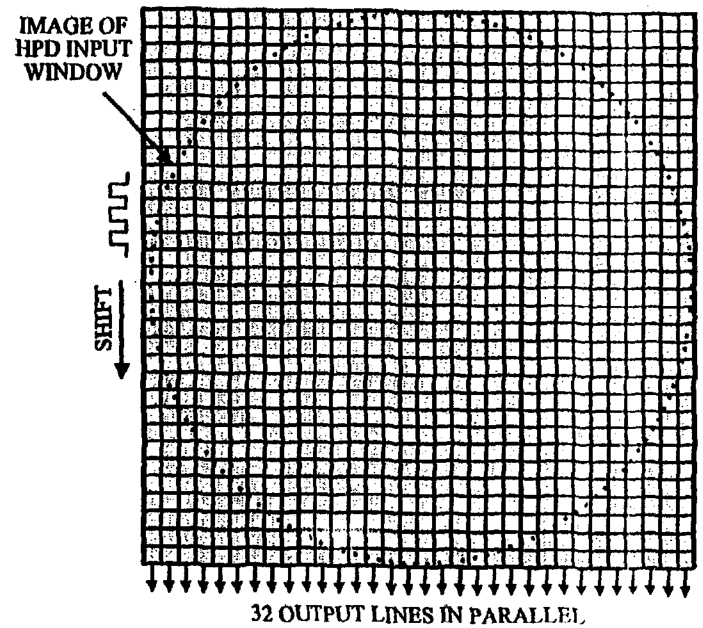
PIXEL DETECTOR & PIXEL ELECTRONICS CHIP PLACED INSIDE VACUUM OF HPD.
HIGH VOLTAGE OF 20kV => SIGNALS OF ~ 5000 e- PER PHOTOELECTRON

PIXEL SIZE DETERMINED BY GRANULARITY OF RICH DETECTOR AND DE-MAGNIFICATION OF TUBE

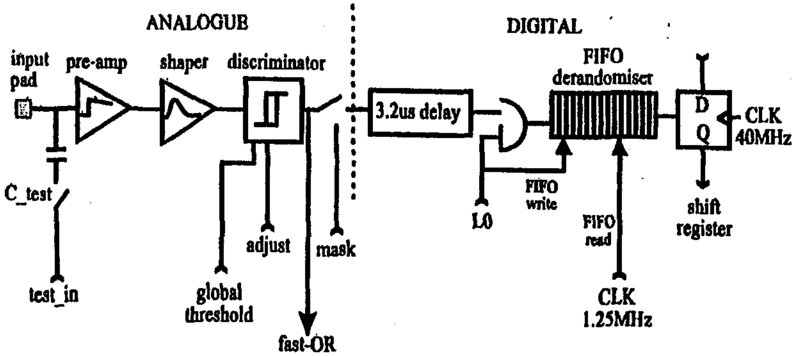
=> 32*32 MATRIX OF 500um*500um PIXELS

LARGE PIXELS: REDUCE CHARGE SHARING
RELAX CONSTRAINTS ON INTEGRATION OF ELECTRONICS
BUT INCREASE LOAD CAPACITANCE ON FRONT-END

EACH COLUMN CONFIGURED AS A SHIFT REGISTER FOR READOUT @ 40MHz (32*25ns ≈ 800ns => 1.25MHz).



Pixel cell



SPECS

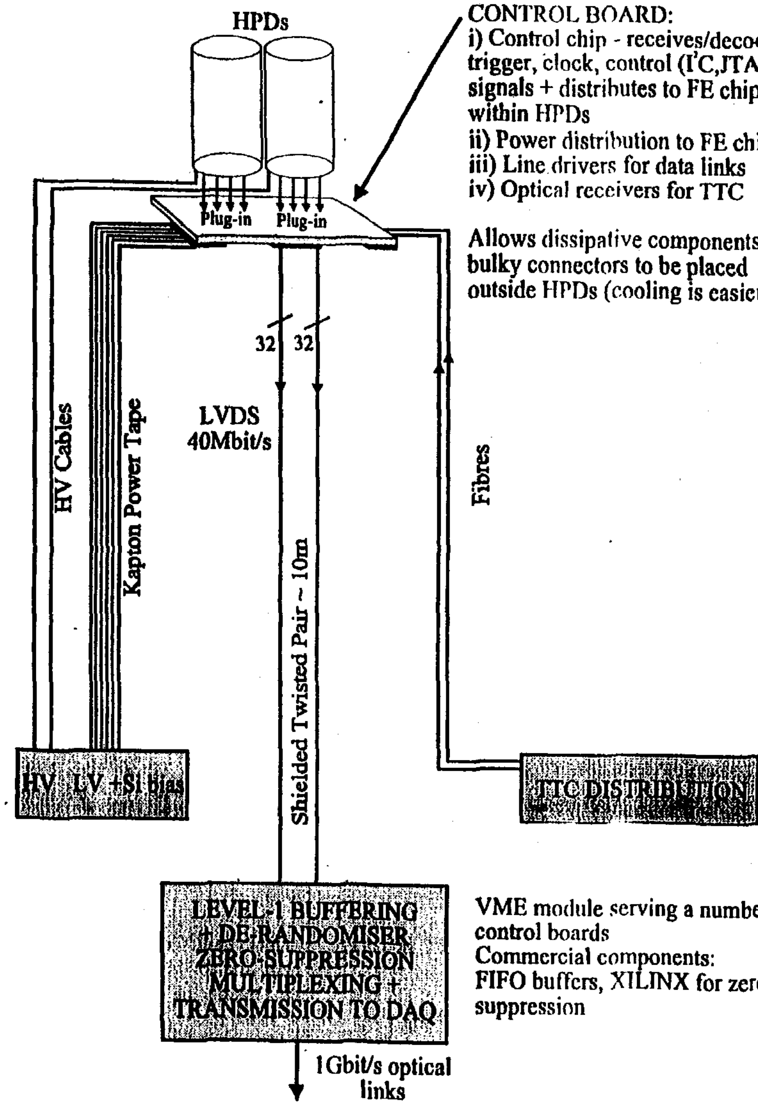
Analogue: Test input - test capacitors for system calibration
Pre-amp - DC-coupled to detector so must sink leakage current
Shaper - 25ns peaking time (tag hits with correct BX) with fast return to baseline
Discriminator - low threshold (2000e-), uniform (200e- RMS)
global setting + adjustment per pixel (current sources)
resets after 25ns
Fast-OR - OR of column/chip - advantage for chip testing
Mask - remove noisy/malfunctioning pixels

Digital: Delay - 3.2us, accurate to 25ns, store mutiple hits
analogue delay line of current-starved invertors is suitable if tuning circuitry is included
FIFO De-randomiser - depth for 16 triggers
input rate ~ 1MHz, output rate = 1.25MHz
16-bit RAM with sense amplifier
write & read pointers per column
Shift register - clocked @ 40MHz

Radiation Tolerant to 30kRad

Low power consumption < 100uW per channel

Interface, links and off-detector electronics



CONTROL BOARD:
i) Control chip - receives/decodes trigger, clock, control (I²C,JTAG) signals + distributes to FE chips within HPDs
ii) Power distribution to FE chips
iii) Line drivers for data links
iv) Optical receivers for TTC

Allows dissipative components and bulky connectors to be placed outside HPDs (cooling is easier)

VME module serving a number of control boards
Commercial components:
FIFO buffers, XILINX for zero suppression

Current status and future plans for electronics

l Prototype HPDs successfully read out with LHC-1 electronics (100ns peaking time, mean threshold = 3000e- with 1000e- sigma)

l Reliability tests of chips inside vacuum following encapsulation within HPD
- do chips survive? (high temperature bake-out)
- do chips/detectors outgas? (contamination of photocathode)
- do bonds (wire and bump) survive?
Prototype HPD results are encouraging

l Implementation of circuitry in IBM 0.25um technology:
i) high density
ii) radiation tolerance - low threshold shift
iii) multiple metal layers - extra shielding
iv) small V_{dd} - lower power dissipation

l Additional radiation tolerance by using 'gate-enclosed' layout & guardrings

l Analogue front-end: ALICE pre-amp + shaper (see talk by Walter Snoeys) peaking-time/timewalk suitable for LHCb

l Discriminator: 1400e- threshold, 80e- RMS achieved on MEDIPIX chip ALICE design (see W.S.) is for 2000e- with < 200e- RMS

l Digital: adjustable delay line & FIFO de-randomiser designs underway

l Test structures of digital components to be submitted for fabrication by end of 1998.

l Design of full chip for LHCb to begin in 1999.

Conclusions

- **Half-scale prototype tube**
  - Electron-optics: behave as expected
  - Single-photoelectron response:
    - 80 % efficiency for active pixels
    - Inactive pixels due to tails in threshold distribution
  - Beam tests in June '98
- **Full-scale prototype tube**
  - Electron-optics design completed
  - Phosphor screen version in summer '98
  - 61-pixels version in autumn '98
- **Pixel front-end and readout electronics**
  - LHCb-specific front-end design underway
  - Readout implementation under study
  - Strong collaboration with Alice
  - Test chip submission by the end of '98

The BTeV pixel detector

Marina Artuso
Syracuse University
for the BTeV collaboration
PIXEL 98 WORKSHOP
Fermilab May7th, 1998

Introduction

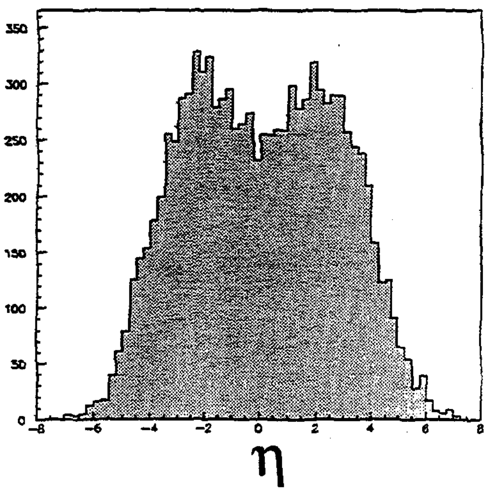
- BTeV's physics goals:
  - study b and c decays to
    - uncover phenomena beyond the Standard Model
    - measure CKM parameters
  - for example:
    - CP violating asymmetry in $B^0 \to \pi^+\pi^-$
    - CP violation and mixing in B_s decays

to achieve physics goals

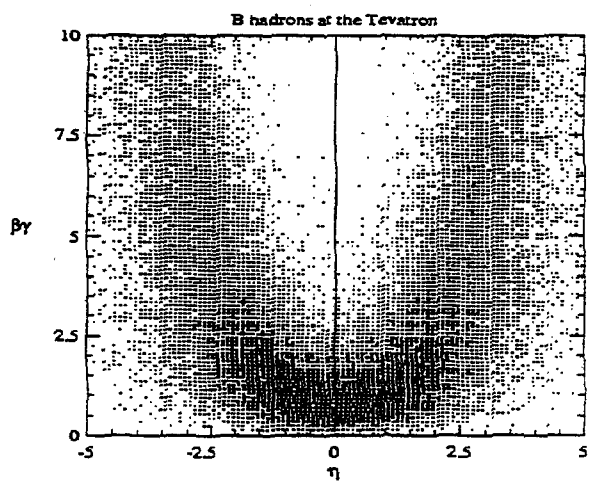
- pixel micro-vertex detector crucial for
  - tracking system - to achieve the vertex resolution and momentum resolution suitable for the physics goals (B_s studies and background rejection)
  - trigger system - detached vertex trigger in Level I, high efficiency for a variety of final states and flavor tagging options
- excellent particle id for π, K, p, μ ,e

Characteristics of hadronic b production

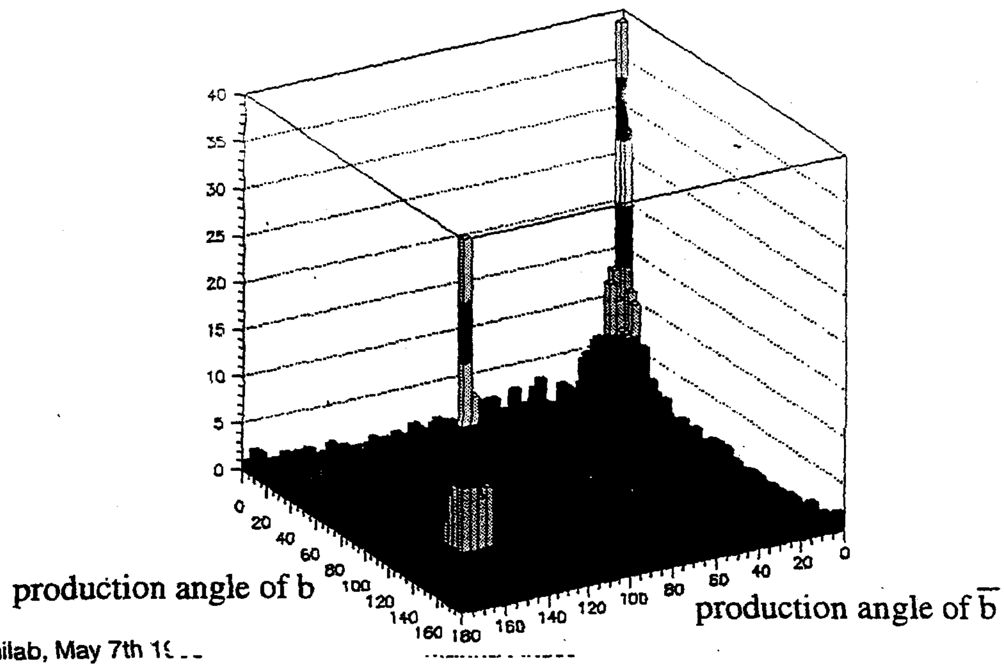
- b's produced "flat" in η, with $<p_t>\sim m_h$



- The higher momentum b's are at larger η's (fig)



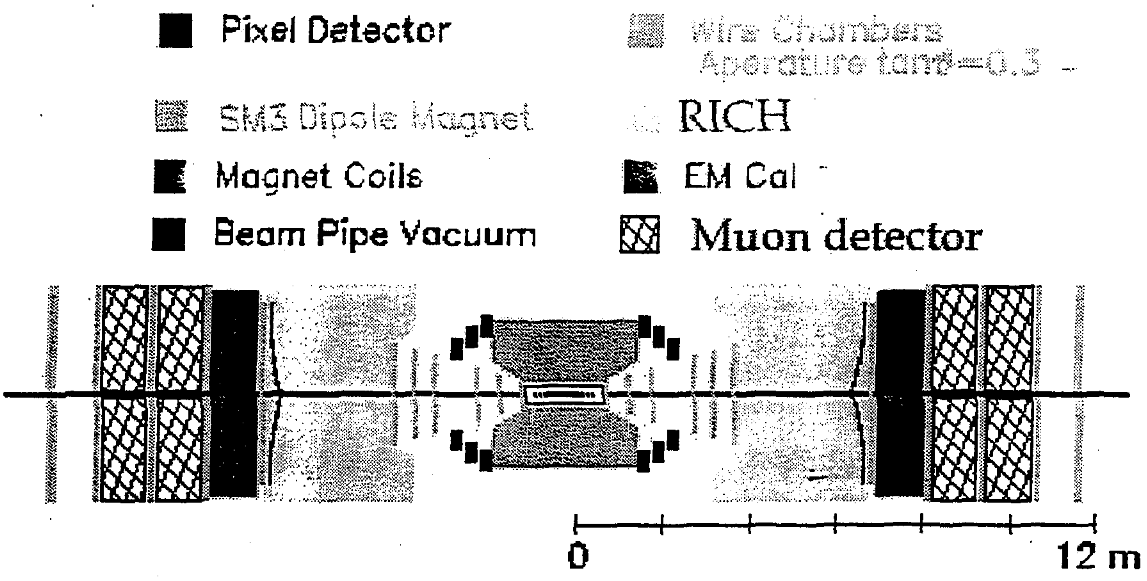
$b\bar{b}$ production angle correlation



The Tevatron as a b & c source

Luminosity (leveled)	2×10^{32} cm^{-2}s^{-1}
b cross-section	100 μb
# of b's per 10^7 sec	8×10^{11}
b fraction	2×10^{-3}
c cross-section	>500 μb
Bunch Spacing	132 ns
Luminous region length	$\sigma_z = 30$ cm
Luminous region width	$\sigma_x \sim \sigma_y \sim 50\ \mu$m
Interactions/crossing	<2>

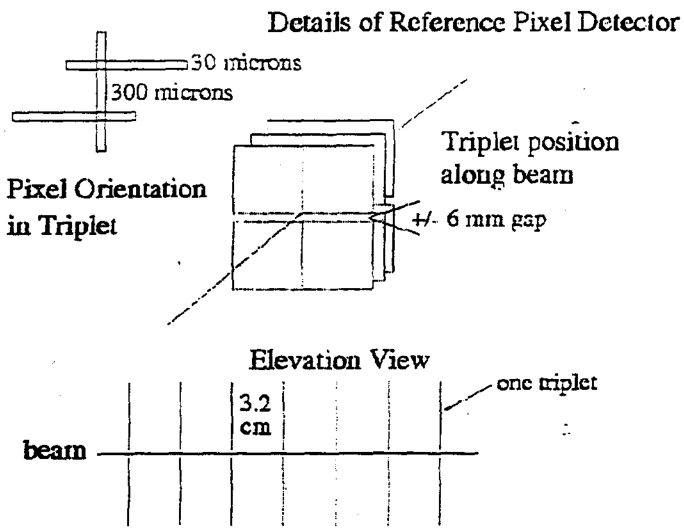
The BTeV detector



The Pixel Vertex detector

- Pixels necessary because we want to put detector as close as possible to beam. We have to fight radiation damage and detector occupancy problems. Expected dose ~8MRad/yr at 6 mm radius.
- System is inside vacuum pipe 6 mm from beam line. Distance is limited by radiation damage. (Done by P238 at CERN).
- Spatial resolution goal better than 9 μm

BTeV pixel detector geometry

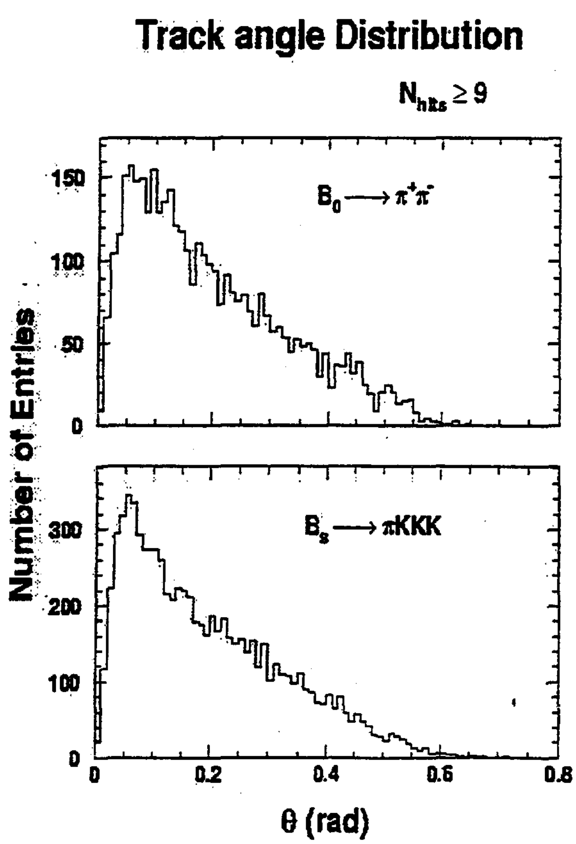


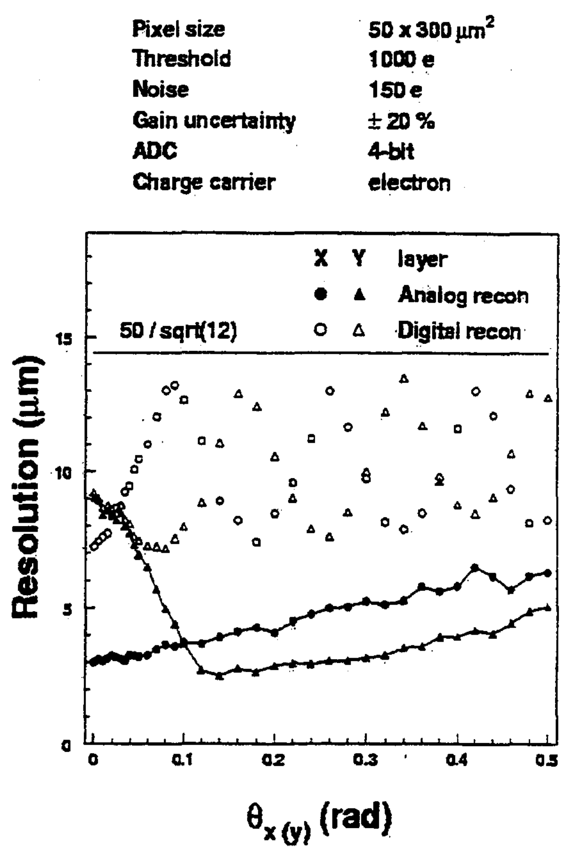
The pixel system

- Long detector system (93 planes along a 0.96 m distance along the beam line because of extended interaction region)
- Planes organized in triplet stations (three planes closely spaced) in order to provide a local slope, critical to our present trigger algorithm

Factors affecting the spatial resolution

- Parameters affecting pixel resolution
  - pixel size
  - digital or analog electronics
  - threshold, adc bits, gain variations
  - electrons or holes as charge carriers (v_d 3:1 for electrons:holes)
- Factors affecting charge sharing
  - v x B effect
  - track angle

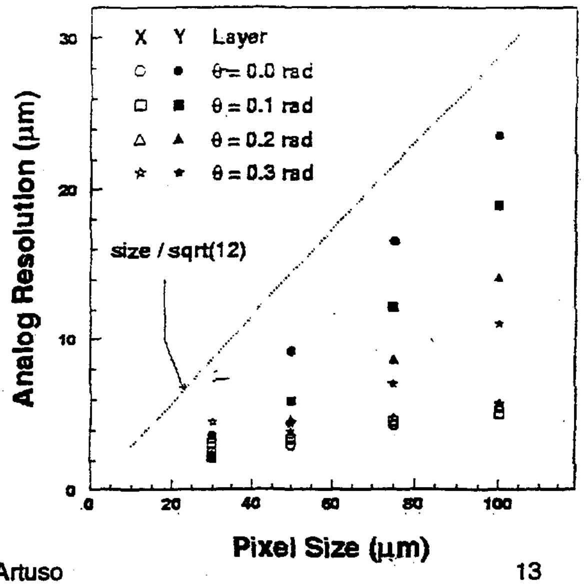




Results of pixel resolution studies

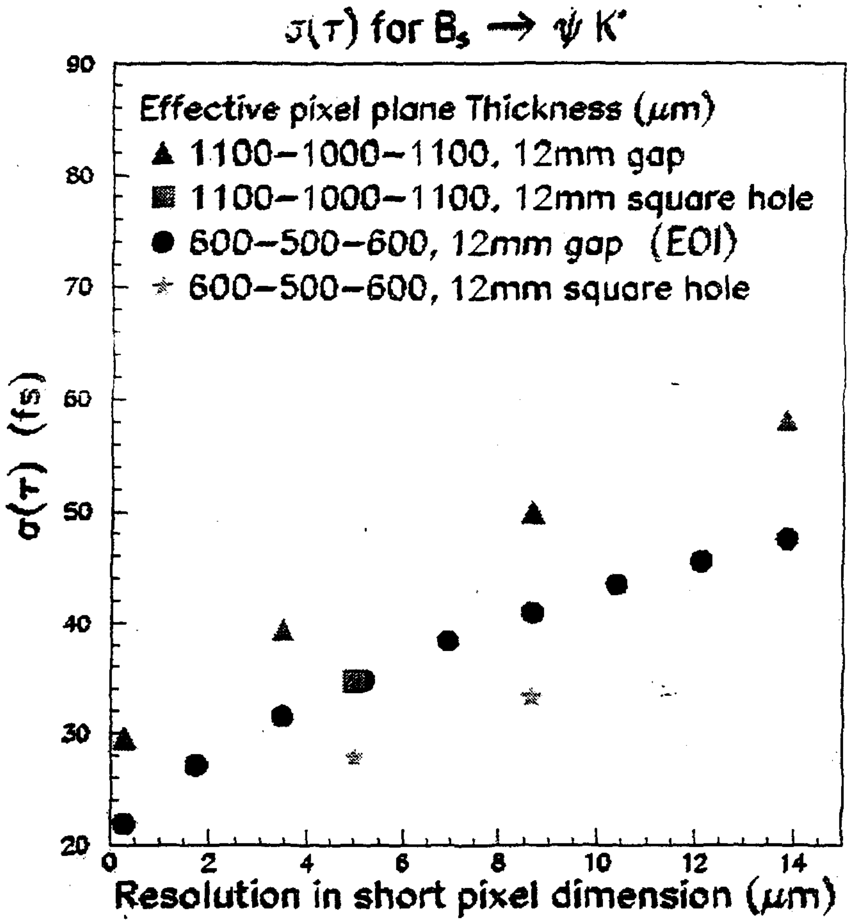
- Analog electronics gives average $\sigma <$ $5\mu m$ for $50\mu m$ pixel
- Alignment errors can be made not to dominate

Electron as Charge carrier



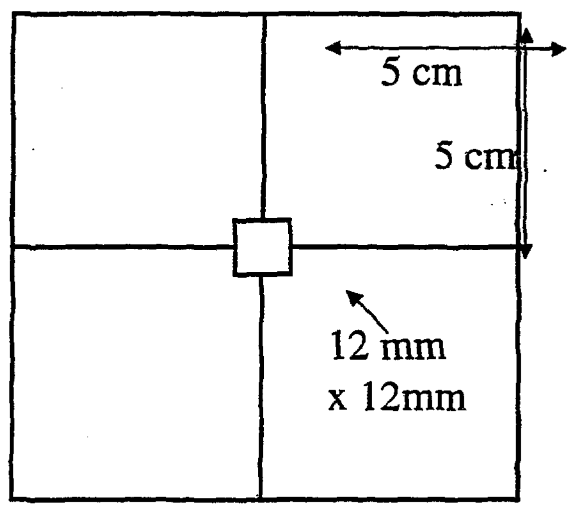
Factors affecting the time resolution

- There are two crucial techniques for reducing backgrounds: particle id & vertex resolution $\equiv$ decay time resolution $[\sigma(\tau)]$
- How does $\sigma(\tau)$ depend on σ_x, detector material thickness and detector geometry?
- We have assumed 6 mm as minimum distance of detector to beam line, though 4 mm is what we calculate is safe (figs)



"Square Hole" pixel option

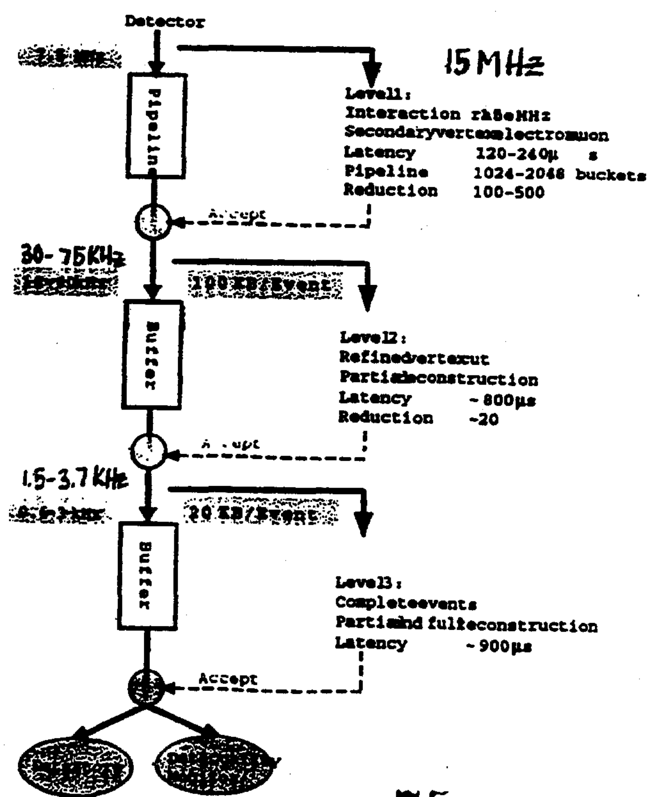
- Big Improvements possible by arranging detector to limit the gap:
- x_s reach



Readout system

- The baseline detector design dictates a system comprised of about 650,000 channels per plane (assuming a pixel size of 30μm x 500μm)⇔60 million in total
- average occupancy expected in the hottest chip (64 mm^2) is about 6 MHz at the maximum luminosity

BTeV data flow diagram

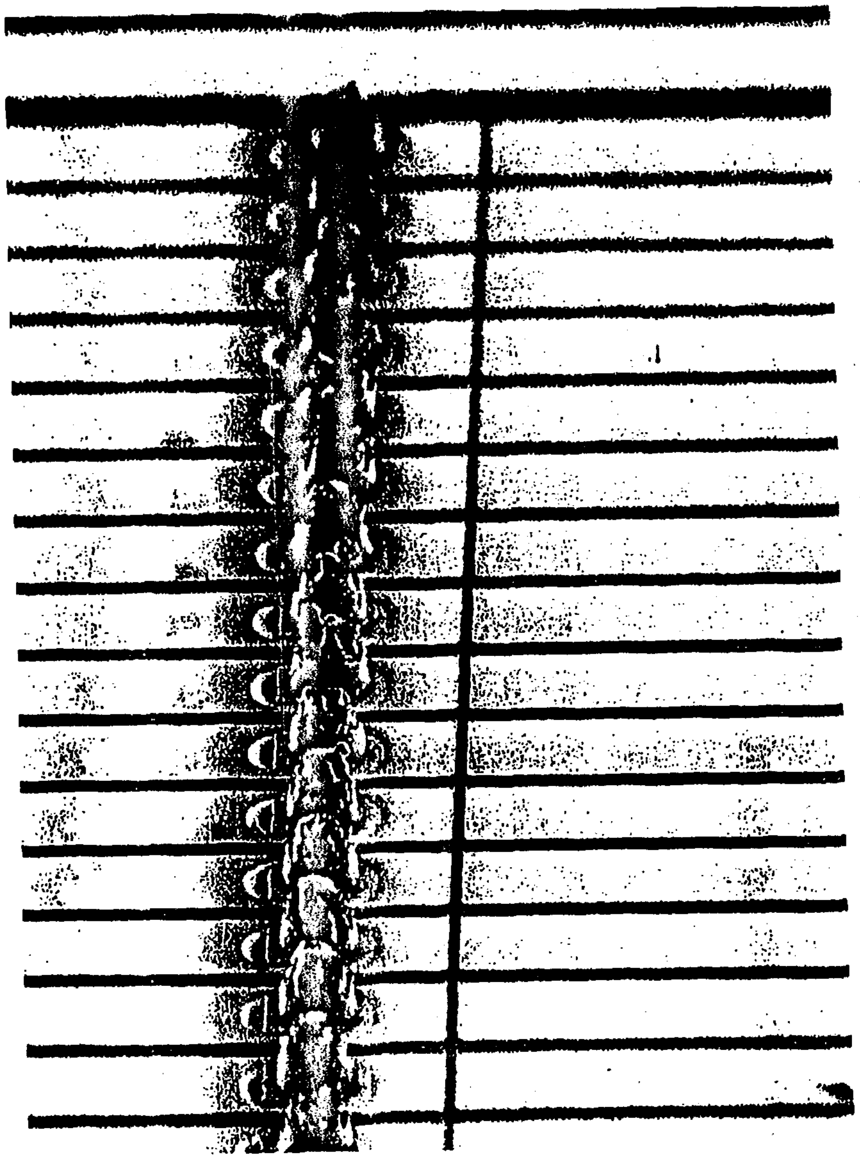


R & D plan: our challenges

- fine pitch bump bonding on a large scale system
- radiation hard components
- excellent readout electronics preserving the intrinsic low noise and low threshold performance in a complex system and with a data processing speed adequate for our needs ***(no information lost, trigger algorithm)***
- alignment accuracy consistent with the spatial resolution needed and with a retractable system
- low mass cooling and support structure

R & D stage I (1997- Spring 1998)

- Test of small prototypes of analog front end design stand alone and bump bonded to detector at the fine pitch considered for the final system (30-50 μm)
  - ✓**Indium bump bond of small readout chips to small detectors with pitches as small as 30 μm**
  - ✓**Evaluate performance of 2 different analog front end design**: FPIX0 (FNAL) and AIC501 (E. Atlas and S. Shapiro, tested at FNAL).



(PRB 2-2 Hong Kong Chip)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1				H								H	H			H
2				H O												
3		H														
4																H
5					H		H O									
6						N										H
7						H		N			H					
8															O	
9	H			D							H	H				
10													O*			
11																
12														H		N
13			H		H		H						O			
14															N	
15				H												
16																

N: not responding to test input
H: hot pixel
D: dead
O*: poor contact

5-not connected
20-hot
1- dead
4-not responding to input
28-bad one way or the other

R&D - stage II (1998-1999)

- Test of small detectors (~2cm x 2cm) bump bonded to full scale readout electronics (~1cm x 1cm).
  - →Prototype chip meeting BTeV specs
  - →Radiation hardness studies
  - →System issues associated with signal and power distribution
  - →large scale bump bond studies

R&D - stage III (1999-2000)

- Full scale module (1 sensor plane) to be used in BTeV system assembled
  - →Sensors bump bonded to readout electronics will be attached to the substrate providing mechanical support and thermal coupling to the cooling structure.
  - →Radiation hard technology
  - →Optimization in system design

R&D - stage IV (2000-2001)

- Full station assembly (triplet of planes closely spaced)
  - →Cooling system design
  - →Optimization of material budget
  - →Alignment procedure
  - →Full integration with trigger electronics

R&D - stage V (end of 2000-mid 2002)

- Full BTeV system prototype.
  - →Vacuum support
  - →Movable detector/readout relative to support
  - →Power supplies, regulation and voltage distribution
- This phase is the early part of the production!

Conclusions

- The pixel detector system is a crucial element in the BTeV tracking and triggering system
- Several challenges in the design of:
  - sensor
  - readout electronics
  - mechanical support and cooling system
- We have a detailed R&D plan, already under way

Status of Front End Chip Development for the ALICE Pixel Detector

Presented by W. Snoeys[1] for the ALICE collaboration

[1]EP Division, MIC Group, CERN 1211 Geneva 23, Switzerland

ABSTRACT

The ALICE pixel development strongly builds on the experience gained at CERN in the WA-97 [1] and NA-57 [2] experiments from operating a full pixel system developed in close collaboration with the RD-19 collaboration [3]. Two chips have been designed as prototypes for the ALICE pixel detector. Both contain front end and digital readout circuitry for 130 pixels. The first one, implemented in a commercial 0.5 μm technology, contains a newly designed front end capable of handling large detector leakage currents and large leakage current variations (~ 100 nA) with minimal threshold variation (~1 %). Special layout techniques studied in more detail in the RD-49 collaboration [4] were used to increase the radiation tolerance of the circuits. At an X-ray dose rate of 4 krad/min the chips started to degrade significantly only after 600 krad. In an ionizing particle beam significant degradation set in after 1.7 Mrads administered in approximately two days.

Density considerations pushed to go to even deeper submicron for the next prototype. It was designed in 0.25 μm standard CMOS, the front end and discriminator have been modified to avoid using large enclosed NMOS devices for current mirroring. As a result of this and the smaller feature size the front-end now measures only 120 μm on a 50 μm pitch compared with about 270 μm on the same pitch in the old design. Moreover, a 3-bit threshold adjust has been added. 2 different counter designs have been implemented which should replace the delay line used in the Omega3 chip. The static counter measures 40 μm by 60 μm whilst the dynamic counter measures only 40 μm by 35 μm. It is now clear that the functionality required of the Alice pixel cell can be implemented within 300 μm using this technology.

[1] F. Antinori et al. : "First Results from the 1994 Lead Beam run of WA97", Nucl. Phys. A590 (1995) 139c-146c.

[2] F. Antinori et al.: "Study of strange and multi-strange particles in ultrarelativistic nucleus-nucleus collisions" CERN/SPSLC/96-40 SPSLC/P300.

[3] F. Anghinolfi et al. : "A 1006 element hybrid silicon pixel detector with strobed binary output", IEEE Trans. Nucl. Sci. NS-39 (1992) 650, and E. H. M. Heijne et al. : "LHC1 : A semiconductor pixel detector readout chip with internal, tunable delay providing a binary pattern of selected events", Nucl. Instr. Meth. A383 (1996) 55-63, and RD-19 Progress reports 1992-1997.

[4] P. Jarron et al., RD49 Proposal CERN/LHCC 97-2, January 1997, and first status report CERN/LHCC 97-63, December 1997, and G. Anelli et al. : "Total Dose behavior of submicron and deep submicron technologies", Proc. of the Third Workshop on Electronics for LHC Experiments, London, September 22-26, 1997 (CERN/LHCC/97-60)

Status of Front end development for the ALICE Pixel Detector

Presented by :

Walter Snoeys

EP Division - MIC - CERN

Fermilab Pixel Workshop, May 7-9, 1998

Other Contributors

- Pierre-Marie SIGNE
- Katelijn VLEUGELS
- Willy SANSEN
- Eugenio CANTATORE
- Domenico MINERVINI
- Roberto DINAPOLI
- Cristoforo MARZOCCA
- Francesco CORSI
- Elena PERNIGOTTI
- Michael CAMPBELL
- Erik HEIJNE
- Michael LETHEREN
- Michael BURNS
- Michel WACHNIK
- Fabio FORMENTI
- Stefania SALADINO
- Bettina MIKULEC
- Paolo MARTINENGO
- Peter SONDEREGGER
- Federico FACCIO
- Pierre JARRON
- Alessandro MARCHIORO
- Federico ANTINORI
- Emmanuele QUERCIGH
- Wolfgang KLEMPT
- Franco MEDDI
- Iztok ROPOTAR
- Luca CASAGRANDE

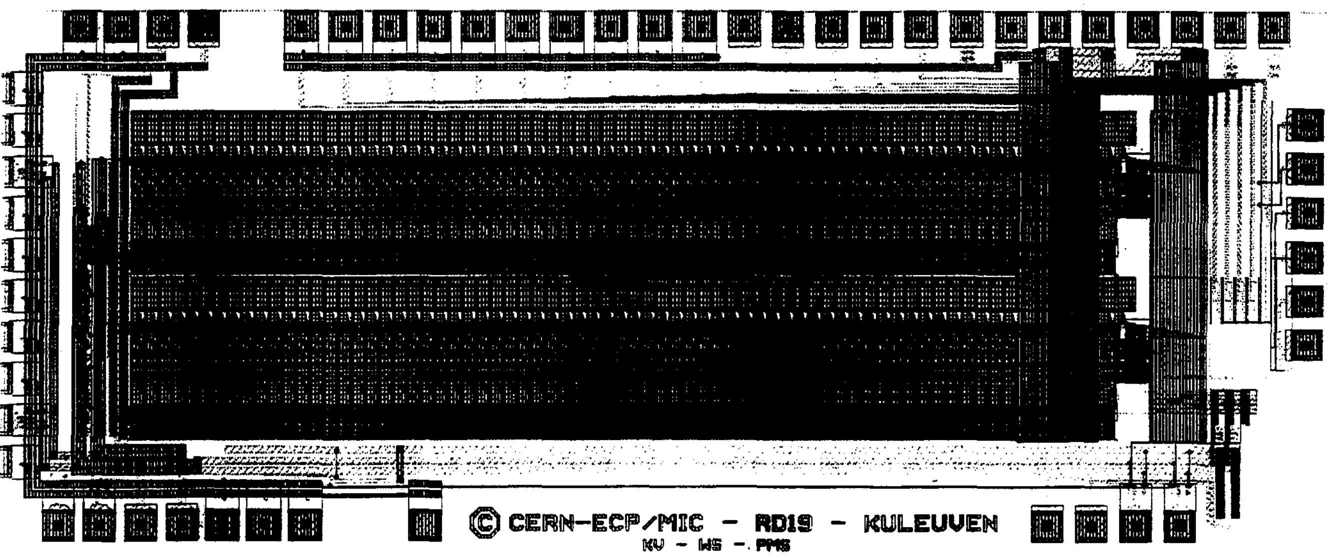
OVERVIEW

- **LHC2TEST in 0.5 micron CMOS**
  electrical and irradiation results
- **Photon Counting Chip (PCC) threshold adjust**
- **New submission ALICE2TEST**
- **Conclusions**

LHC2TEST in 0.5 micron

- Contains 2 columns of 64 pixels + 1 test pixel with analog outputs)
- Each pixel element contains :
  - test and mask
  - front end with capability to collect holes or electrons, and detector leakage current compensation
  - readout logic (strobe but no delay line)
- laid out in radiation tolerant layout

W. Snoeys - CERN - EP - MIC

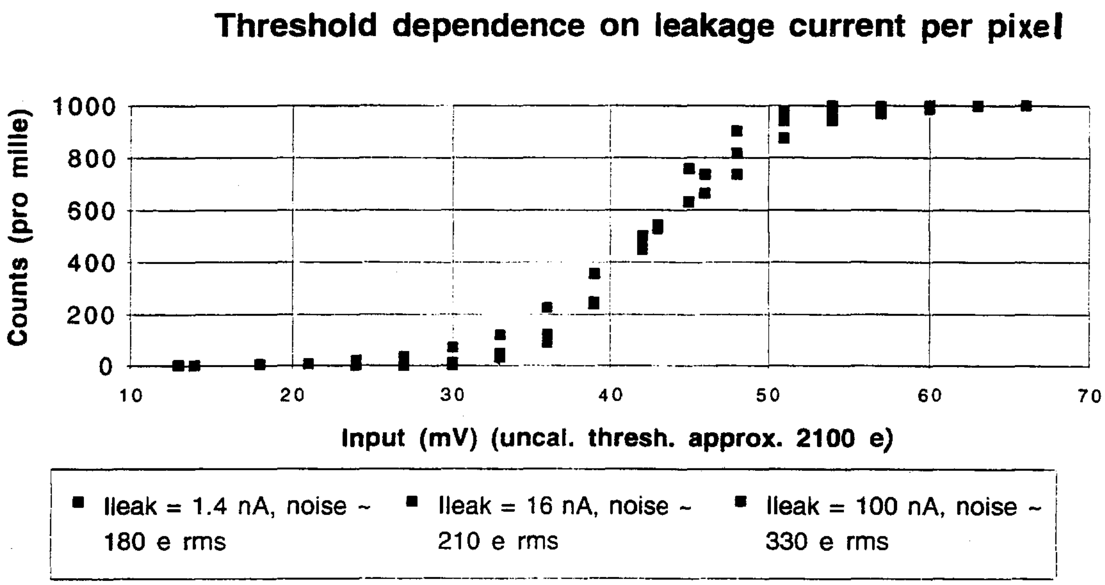


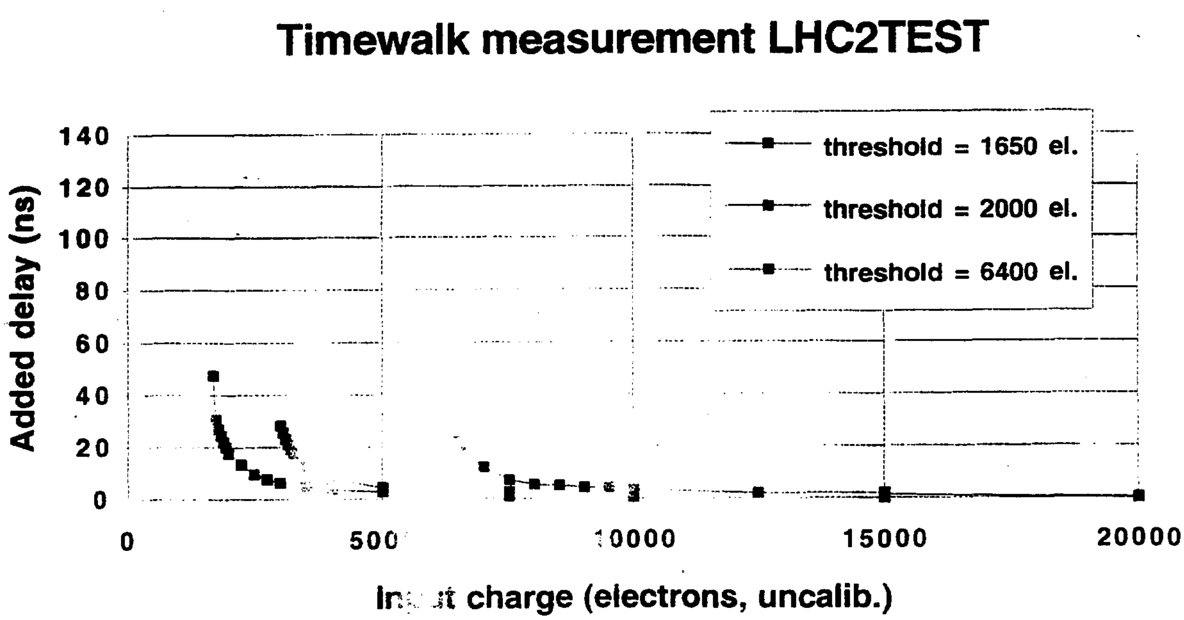
LHC2TEST

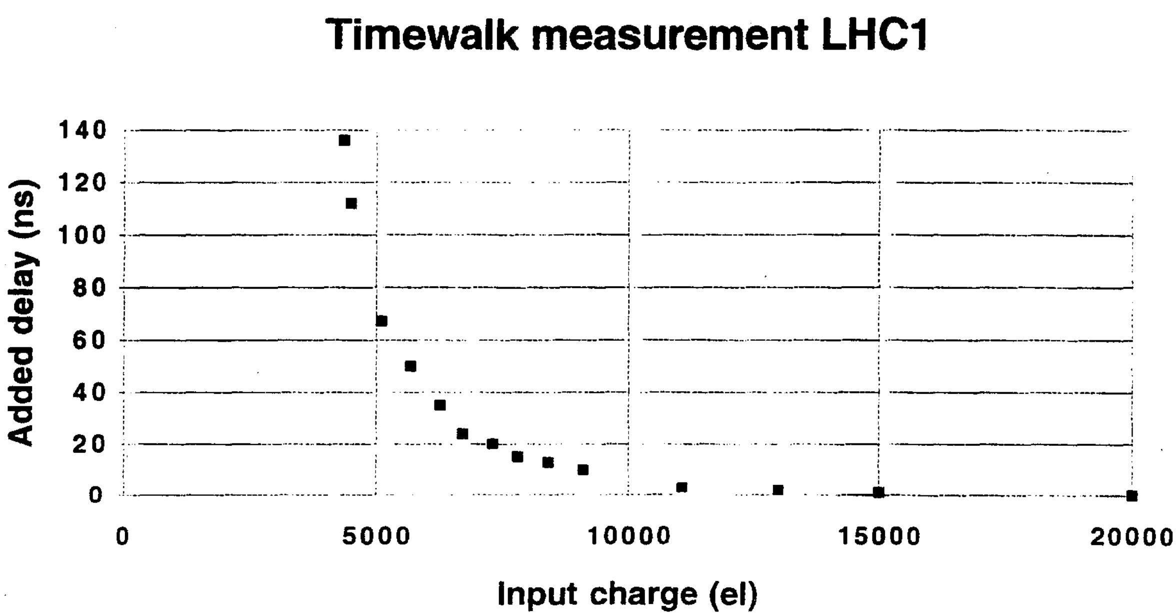
Pixel Readout Prototype in Radiation Tolerant Layout in commercial submicron technology. CERN ECP-MIC RD19 - RD49 ALICE

(Mieke 0.5µm)

2x65 pixelcells (50x420µm²)


Threshold dependence on leakage current per pixel
Counts (pro mille)
1000
800
600
400
200
0
10
20
30
40
50
60
70
Input (mV) (uncal. thresh. approx. 2100 e)
Ileak = 1.4 nA, noise ~ 180 e rms
Ileak = 16 nA, noise ~ 210 e rms
Ileak = 100 nA, noise ~ 330 e rms


Timewalk measurement LHC2TEST
Added delay (ns)
140
120
100
80
60
40
20
0
threshold = 1650 el.
threshold = 2000 el.
threshold = 6400 el.
0
15000
20000
charge (electrons, uncalib.)



LHC2TEST electrical results

- for a detector leakage current increase of 1 to 200nA :
  - threshold variation ~ 1%
  - noise increase from about 200e RMS to 400e RMS for holes, and to 350e RMS for electrons.
- threshold variable between 2000 to 15000 holes or electrons
- threshold spread too large (400 - 500 e RMS)
- timewalk within 25 ns for only a few 100 electrons above threshold

LHC2TEST Radiation Tolerance

- Irradiation tests done with 10 keV X-rays, Gamma ^{60}Co, 6.5 MeV protons, and electrons in NA50
- No large increase in supply currents with dose => rad tolerant layout techniques prevent leakage
- Serious degradation (= severe pixel threshold increase) sets in only after ~600 krads with Xrays and ~1 Mrad or higher for the other sources (e.g. 1.7 Mrad for NA 50 beam)

W. Snoeys - CERN - EP - MIC

(10)

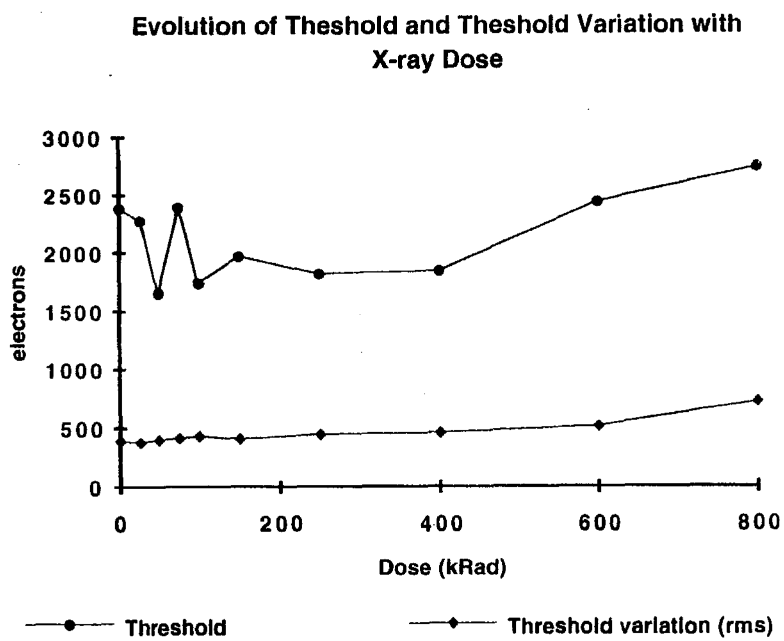
LHC2TEST Radiation Tolerance

- Main reason for threshold increase is shaper response decreases sharply in amplitude (verified on analog outputs)
- Significant recovery (annealing) after a relatively short time

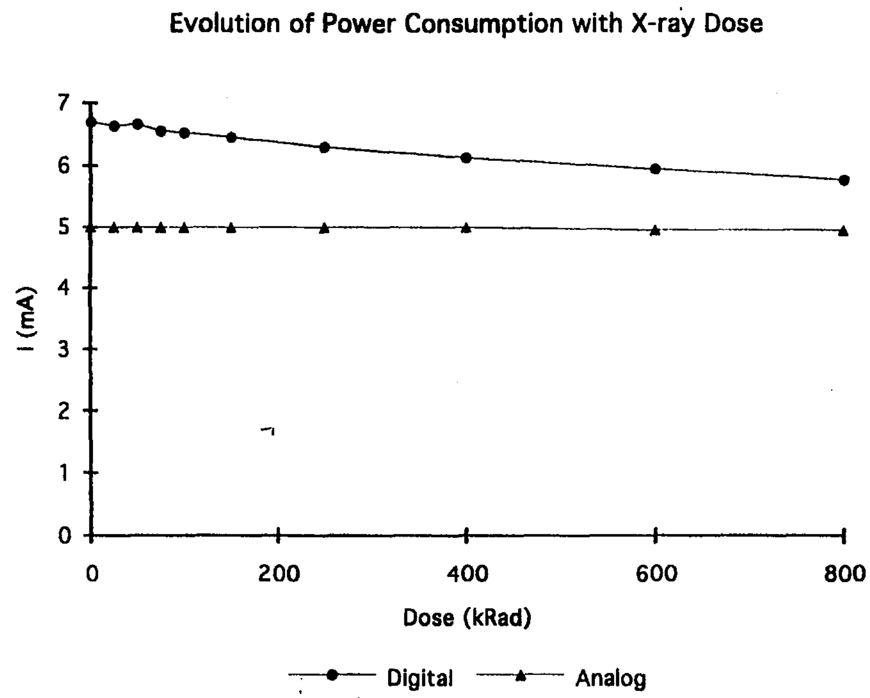
W. Snoeys - CERN - EP - MIC

(11)

(12)


Evolution of Theshold and Theshold Variation with X-ray Dose
3000
2500
2000
1500
1000
500
0
electrons
0
200
400
600
800
Dose (kRad)
Threshold
Threshold variation (rms)

(13)


Evolution of Power Consumption with X-ray Dose
7
6
5
4
3
2
1
0
I (mA)
0
200
400
600
800
Dose (kRad)
Digital
Analog

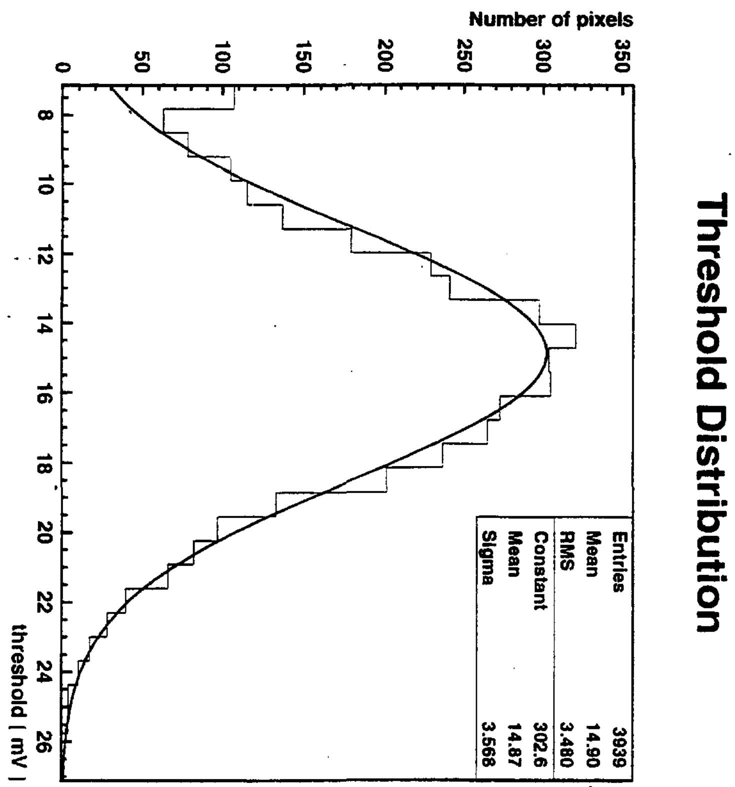
87

10 keV Xray irradation of LHC2TEST					
	Average Threshold	Threshold variation RMS	Average Noise	Noise variation RMS	Valid Pixels
400 krad					
before	2262	431	216	31	127
immediately after	2091	445	237	26	125
after 1 day at RT	2173	439	237	27	126
after 1 week at 100 C	1546	373	239	21	90
600 krad					
before	2243	431	218	26	130
immediately after	2554	560	263	20	130
after 1 day at RT	2357	483	237	21	129
after 1 week at 100 C	2234	447	226	16	128
800 krad					
before	2276	413	224	18	124
immediately after	4342	1657	372	69	130
after 1 day at RT	2534	629	265	25	126
after 1 week at 100 C	1689	475	261	28	90

(14)

PHOTON COUNTING CHIP

3 BIT THRESHOLD ADJUST



≈ 139e

≈ 326e

BEFORE ADJUST

RD-19

M. CAMPBELL

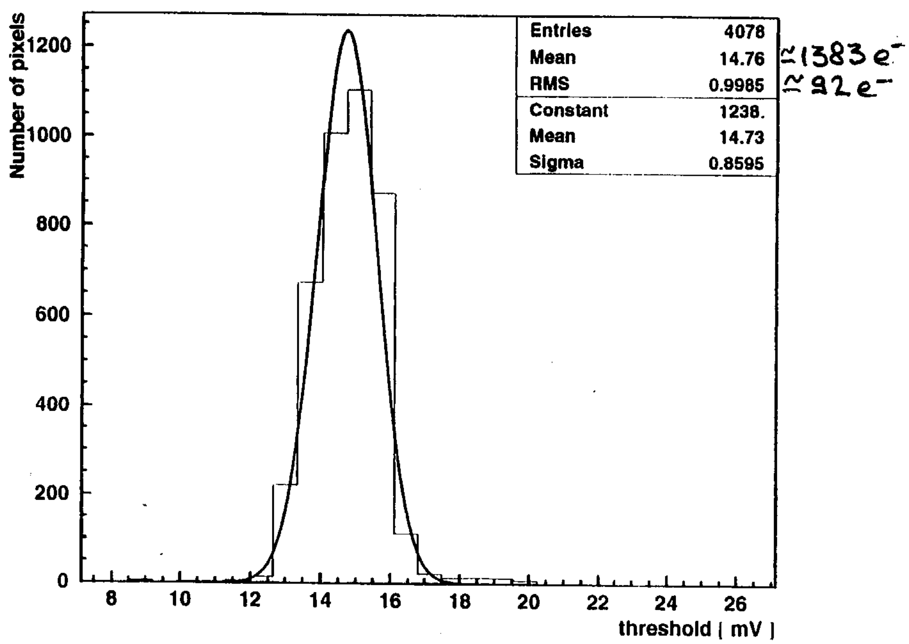
(15)

F. PERNIGOTTI

(16)

PHOTON COUNTING CHIP

Threshold Distribution

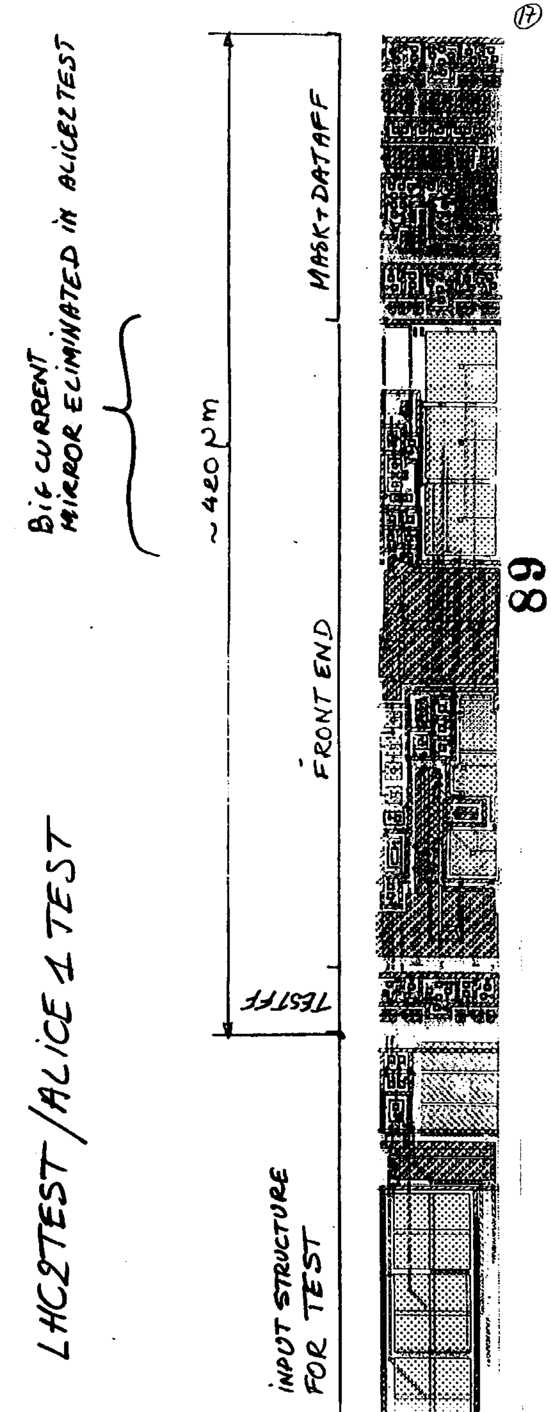


AFTER ADJUST

RD-19

H. CAMPBELL
F. PERNIGOTTI

(17)



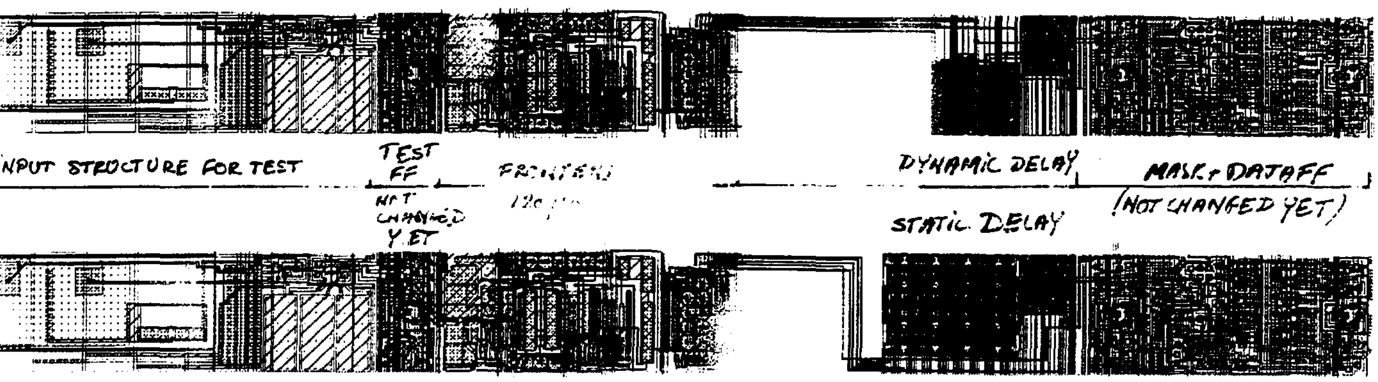
ALICE2TEST in 0.25 micron CMOS

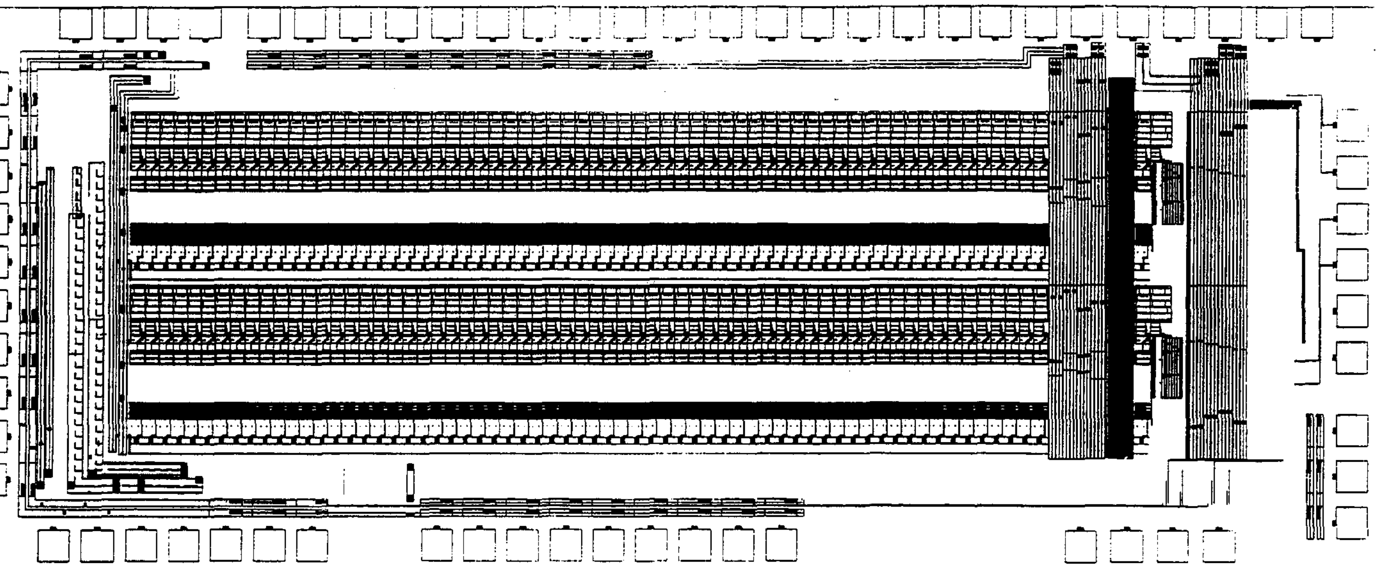
- Contains 2 columns of 64 pixels + 1 test pixel with analog outputs)
- Each pixel element contains :
  - test and mask
  - front end with capability to collect holes or electrons, and detector leakage current compensation, and threshold adjust (local digital storage not yet included)
  - digital counter - based delay line two versions : static and dynamic
  - readout logic
- laid out in radiation tolerant layout

ALICE2TEST

- static & dynamic delay based on counter
  counter itself (without control)
  static: $40 \times 60\,\mu m^2$
  dynamic: $40 \times 35\,\mu m^2$

- clear we will be able to fit full ALICE pixel in 300µm long pixel (50µm pitch)





ALICE 2 TEST
submitted in
0.25 µm
technology

(20)

CONCLUSIONS

- **LHC2TEST (0.5 um) excellent results regarding timewalk, detector leakage current compensation and radiation tolerance BUT insufficient density and relatively large threshold variation.**
- **Therefore ALICE2TEST (0.25 um), expected back early July, density sufficient to implement ALICE pixel in 50 x 300 um, threshold adjust added to improved front end (principle of adjust demonstrated on PCC)**
- **Full ALICE chip to be submitted by the end of the year.**

(21)

Readout chip development for the ATLAS pixel detector

Thorsten Kuhl
Physikalisches Institut Bonn

Contents:

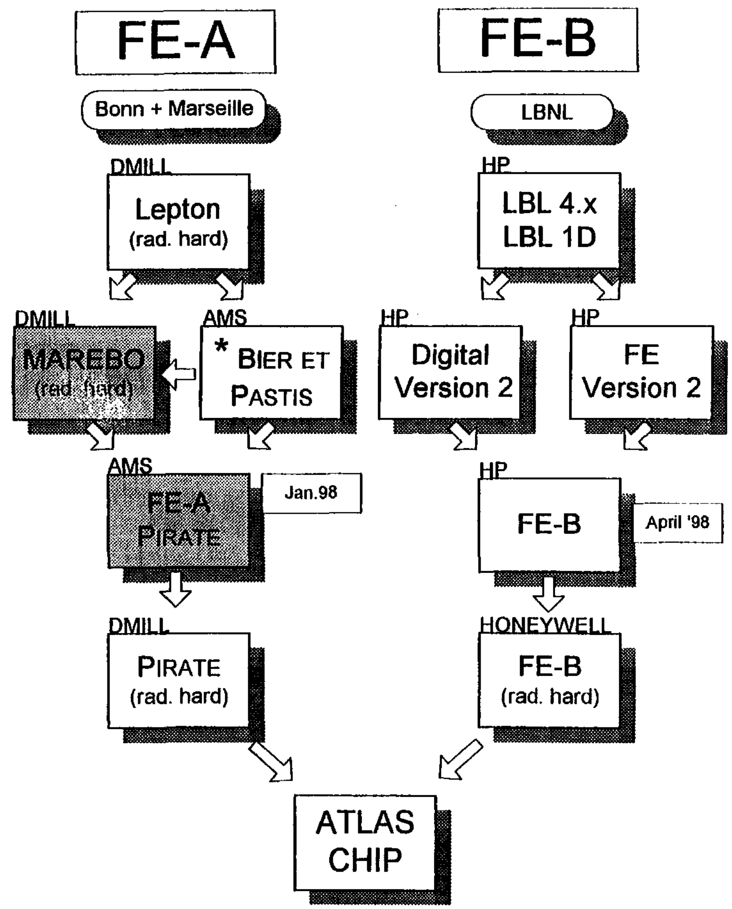
- Requirements for pixel frontend electronics at LHC
- **Pi**xel **R**eadout Chip for the **AT**LAS **E**xperiment (PIRATE)
- Radiation hard development (MAREBO)
- Summary

Requirements for ATLAS pixel electronics

1. Pixel size of 50 x 300 μm^2
   achieve required spatial resolution
2. Amplifier noise of < 200 e^- e.n.c.
   get low noise hit rate at low threshold, needed to detect small charges after radiation damage of sensor
3. Threshold uniformity of typ. 200 e^- rms
   required to set low global threshold
4. Power consumption of <50 μW per pixel
   reduce cooling effort (-> radiation length!)
5. Timing precision of 25 ns
   uniquely associate hits to bunchcrossings
6. Leakage current tolerance of up to 100nA
   operate with DC-coupled detectors
7. Zero supression
   read only hit pixels
8. Trigger selection
   buffer events for 80-100 crossings until T1 trigger occurs
9. Radiation hardness
   survive 20-30 Mrad in 10 years of operation
10. Testability
    test every pixel before module assembly

Note: pixel occupancy is < 10^{-4} hits / crossing

Readout chip development history



*) B&P was the first chips which fulfils the ATLAS analog requirements

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Pixel Readoutchip for **ATLAS** **PIRATE**

Universität Bonn / CPP Marseille
(received & tested jan. 1998)

direct successor of the BEER & PASTIS chip

- 18 x 160 pixels (50 µm x 400 µm)
- preamplifier for n/n detectors
- threshold adjust for every pixel (3 bit DAC)
- time over threshold information
- 8-bit DAC's for internal currents
- serial command protocol
- complete 40 MHz digital logic for ATLAS
- serial data readout
- works under full luminosity conditions

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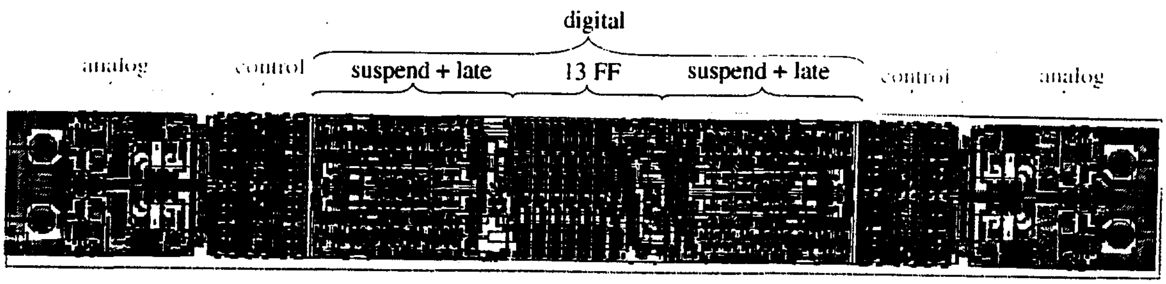
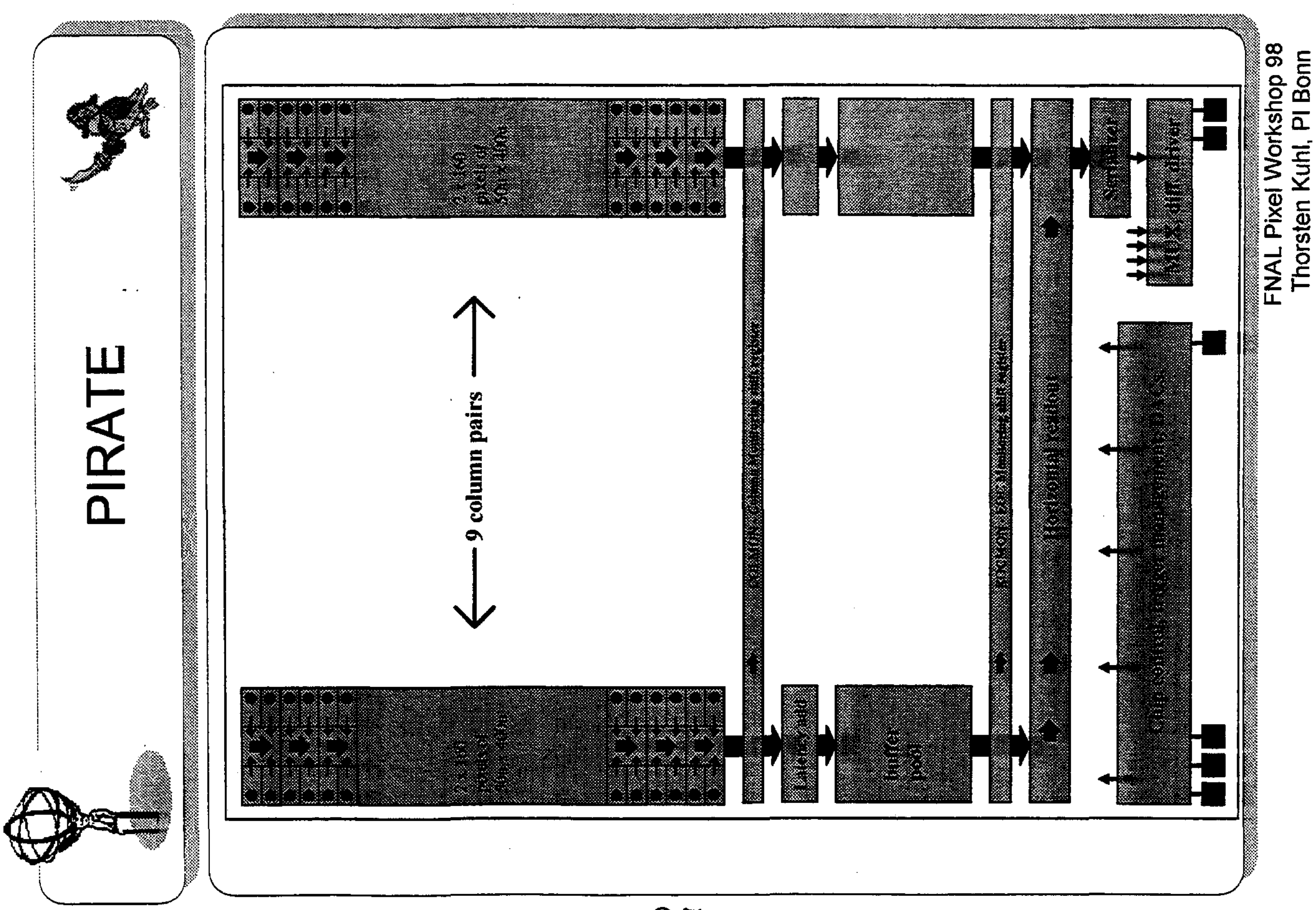
- ACTIVE PART

- ***Analog part (140u)***
  include 3 bits DAC for tuning
- ***Control part (80u)***
  mask, inject .....
- ***Digital part (180u)***
  1 RO part for 4 contiguous pixels
  7 bits of address
  2 bits late
  1 bit rise (for ToT information)
  1 bit Up/Down (for group)
  1 bit Left/Right (for group)



- pixel size : 400μm * 50μm



96

Digital performance

Full simulation of the FE-architecture

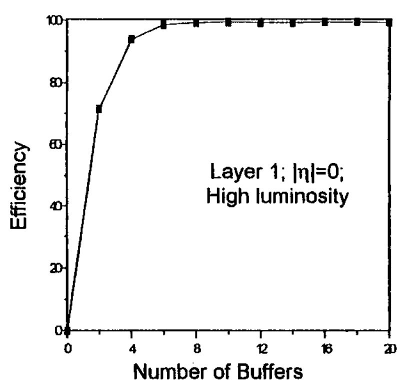
- simulation of digital part
- cluster taken from full detector monte carlo
- random tracks

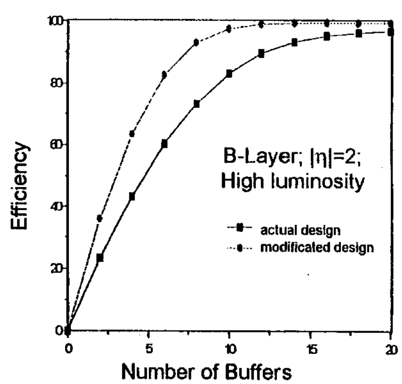
Inefficiencies can occur by:

- occupancy of single pixel
- collisions in the shift register
- buffer overflow

Results ($\mathcal{L}=10^{34}\,cm^{-2}s^{-1}$):

- at $|\eta|=0$, Layer 1: $\varepsilon \gg 99$ % with 8 buffers
- at $|\eta|=2$, B-Layer: $\varepsilon > 95$ % with 16 buffers;
  with small modifications: $\varepsilon > 99$ % with 12 buffers
- general: architecture can cope well with highest LHC luminosity





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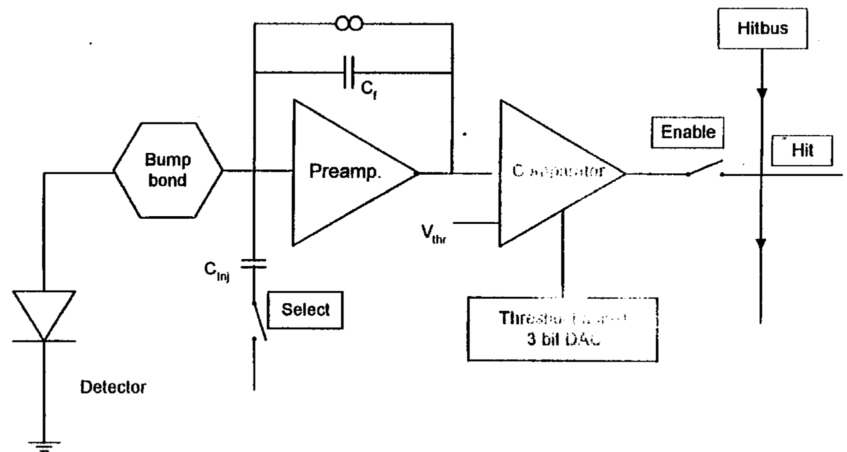
Analog part of the PIRATE

schema of analog part



- fast amplifier with novel DC feedback
- threshold adjust with 3 bit DAC in every pixel
- Enable: masking pixel
- hitbus for monitoring
- linear time over threshold (TOT) behaviour
- chopper for test injection on chip
- internal 8 bit DACs for bias currents

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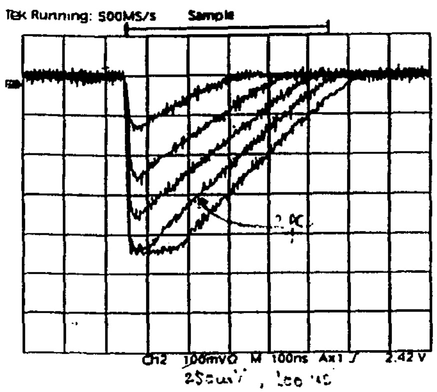
Analog signals from preamplifier

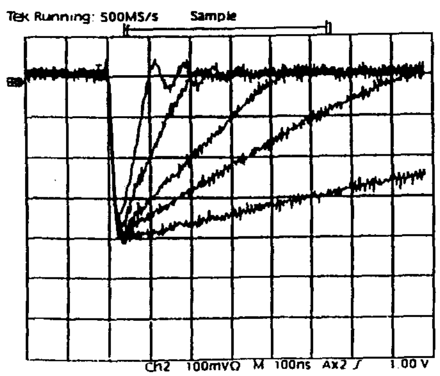
- Preamplifier operated at 30 uW
- Feedback in amplifier is a constant current source



Q_{in} = 0.5, 1, 1.5,... fC

$C_{feedback}$ = 1.7 fF

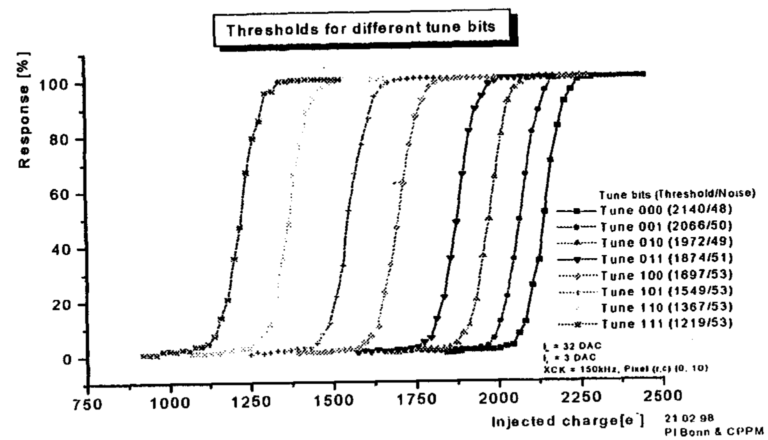
~ m.i.p. ≙ 2V signal at output

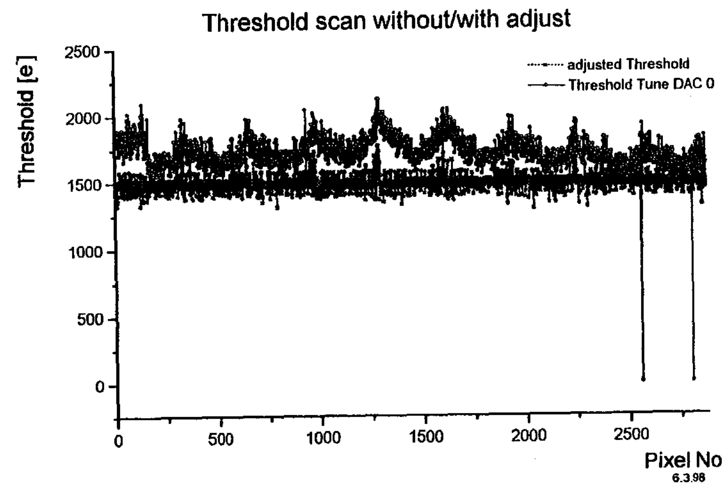


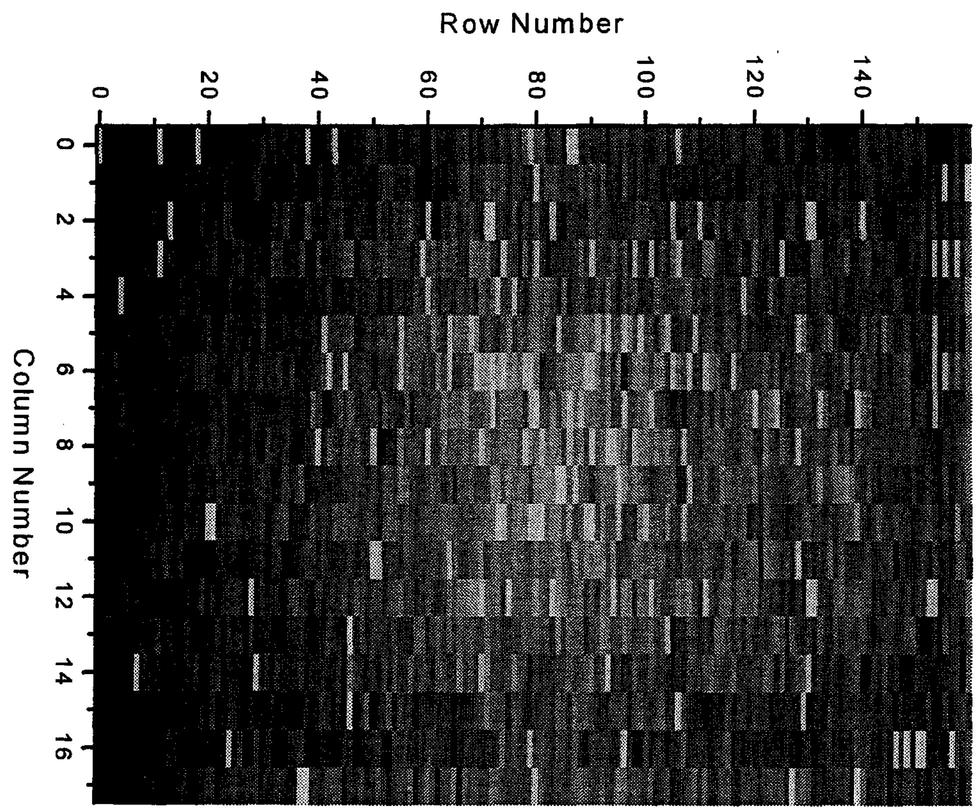
Variation of feedback current:

- very good stability
- small shaping loss
- high leakage tolerance

Threshold adjust







Hit map from Am^{241} source

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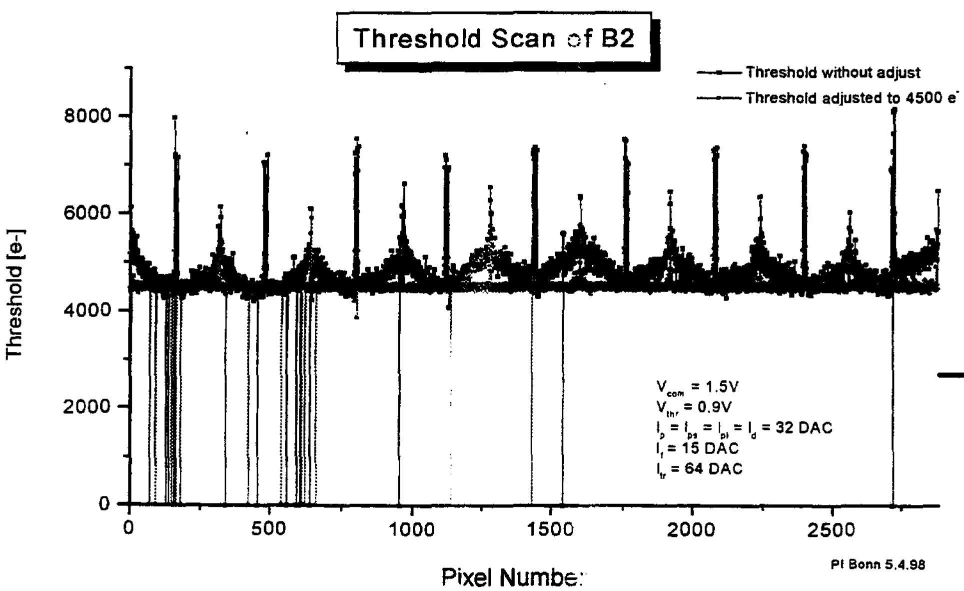
Threshold scan with detector



lowest threshold value set in beam ($3000\ e^-$)

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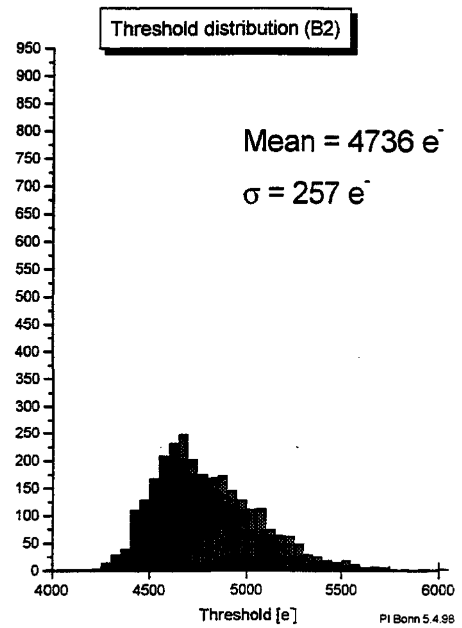
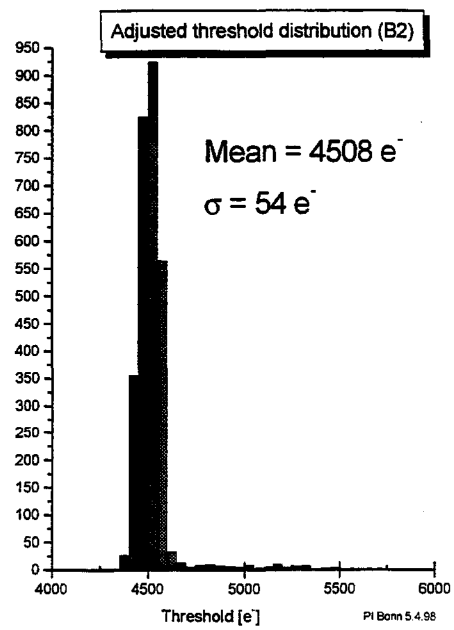
Threshold distributions





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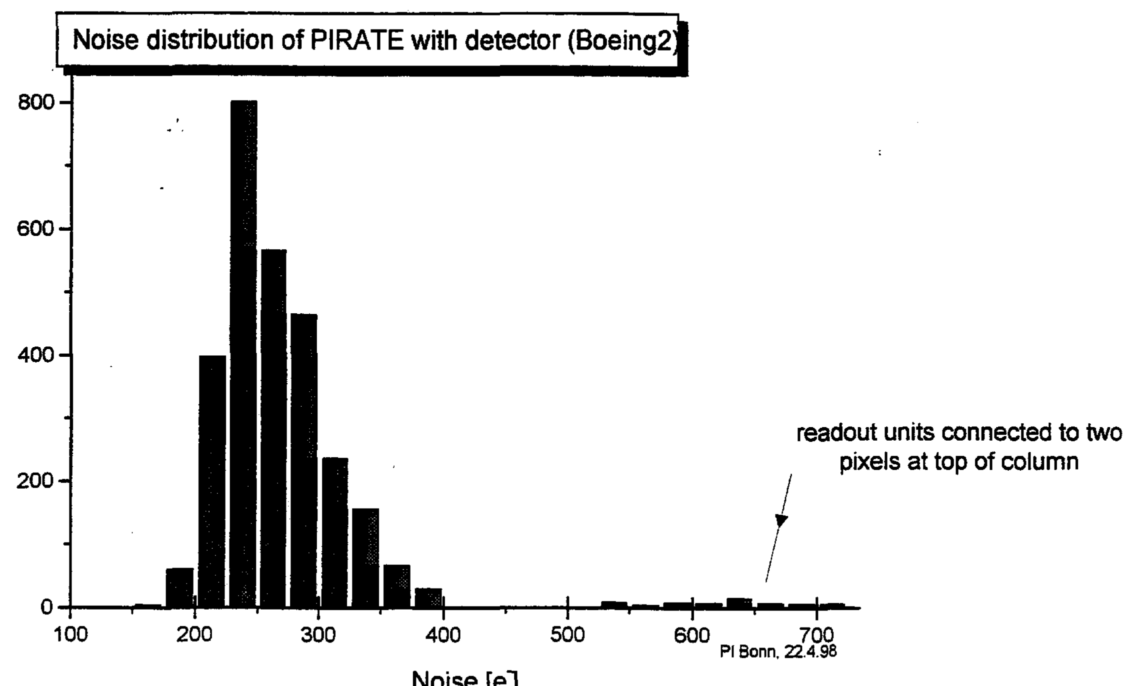
Noise



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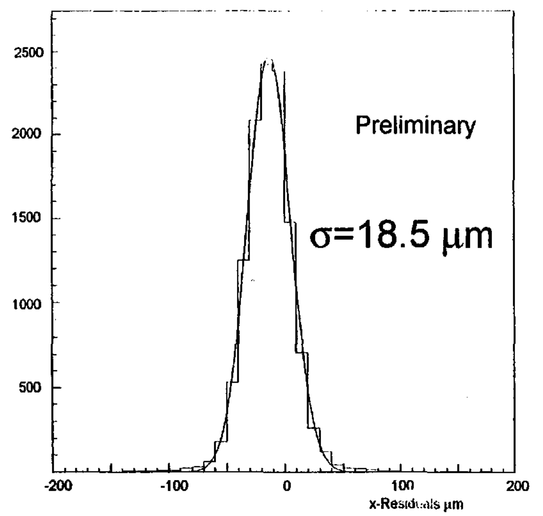
Test beam

First test beam 01.04.98-21.04.98
(CERN, 50 GeV Myons)

- test of several chips
- different detector configurations
- test system works well
- sucessfull data taking

PIRATE (IZM4) in test beam (April '98)

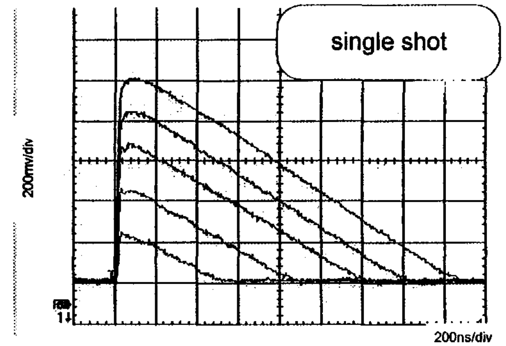


Analysis: LBNL Berkley

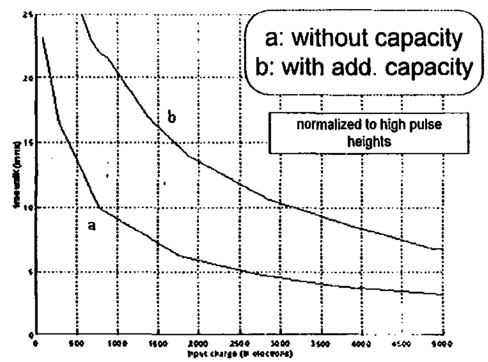
MAREBO

Radiation hard readout chip with reduced digital part.

Preamplifier signals single channel



Timewalk behaviour



Summary and outlook

PIRATE works well and has been successfully operated in beam

1) operation @ 3000 e^- setting in beam
2) at full ATLAS speed (40 MHz)
3) low noise (250 e^- with detector)
4) low treshold variation (< 50 e^- after adjust)
5) successfully bumped to sensors
6) radiationhard FE has timewalk <1000 e^- @ 200fF
7) serial ATLAS protocol for control and readout works @ 40 MHz
8) poor chip yield

Applications of the ISPA-tube in nuclear medicine and biology

C. D'Ambrosio[1], F. de Notaristefani[2], T. Gys[1], E. Heijne[1], H. Leutz[1], D. Piedigrossi[1], D. Puertolas[1,2], E. Rosso[1]
1 CERN, 2 INFN Section of Rome

abstract:

The Imaging Silicon Pixel Array (ISPA)-tube [1] is a position-sensitive photon detector based on the hybrid technology [2]. It consists of a vacuum-sealed cylinder with an optical entrance window on which is evaporated a photocathode. A potential difference (20 to 25 kV) is applied between the photocathode and a silicon chip anode. The chip anode is based on the Omega 2 and LHC1 chips, developed by the RD-19 collaboration [3,4]. It consists either of one detector plane divided into 1024 pixel diodes (500 çm x 75 çm in size) and one electronics plane also divided into 1024 equally-sized electronic pixels (Omega 2 chip) or of one detector plane divided into 2048 pixel diodes (500 çm x 50 çm in size) connected to 2048 equally-sized electronic pixels (LHC1). Each detector pixel is directly bump-bonded to its front end-electronics pixel. The binary response of individual pixels thus provides a space information and allows 2D-imaging. An important feature of the tube is the possibility to trigger it internally: the analog signal from the bias contact of the detector chip, arising from the photoelectron pool generated by each event in the scintillator, can be appropriately amplified and shaped. It provides a fast (10 ns), global information allowing an easy energy calibration and an energy window selection. All events falling inside this energy window start the gating and readout of the tube.
For nuclear medicine, we built an ISPA-camera for g-rays by coupling a YAP(YalO3(Ce)) planar crystal or a YAP-crystal array (consisting of 0.6 x 0.6 mm2 optically-separated YAP-elements) to an ISPA-tube [5]. Presently, using a YAP-crystal array containing 0.3 x 0.3 mm2 elements we achieve an improved spatial resolution (FWHM) of 100 çm at 122 keV g-energy, the overall spatial resolution of the system being dictated by the crystal element size. The energy resolution of the system can be made as high as 21% at FWHM for 122 keV photons, allowing rejection of Compton scatters, while still providing a good spatial resolution (~500 çm).
For biology and in particular autoradiography, we built a beta camera made of a thin scintillator placed onto the ISPA-tube window. Resolutions down to 100 çm have been achieved and beta detection sensitivities measured with calibrated Tritium and Carbon-14 Amersham calibrated sources. Microslices of mouse brain labelled with Sulfur-35 have been imaged and analyzed.
Last development, which consists in a new electrostatic focussing tube (demagnification ~4) containing an LHC1 chip, as well as future developments, both for the tube and for a specific chip, will be finally presented.

References
[1] T. Gys et al., "A new position sensitive photon detector based on an imaging silicon pixel array (ISPA- tube)", Nucl. Instr. and Meth. in Physics Res., vol. A355, 1995, p. 386.
[2] C. D'Ambrosio et al., "The ISPA-tube and the HPMT, two examples of a new class of photodetectors: the Hybrid Photo Detectors", Nuclear Physics B (Proc. Suppl.) 61B (1998) 638.
[3] E. H. M. Heijne et al., "Development of silicon micropattern pixel detectors", Nucl. Instr. and Meth in Physics Res., A348, 1994, p. 399 .
[4] E.H.M. Heijne et al., "LHC1: A semiconductor pixel detector readout chip with internal tunable delay providing a binary pattern of selected events", Nucl. Inst. and Meth. in Phys. Res., A383 (1996) 55.
[5] D. Puertolas et al., "An ISPA-camera for g-rays in nuclear medicine", Nuclear Physics B (Proc. Suppl.) 61B (1998) 644.

Fermilab 7 May 1998

C. D'Ambrosio

The ISPA – Tube in Medicine and Biology

Working Principle

Applications of the ISPA (Imaging Silicon Pixel Array) tube

- γ-camera for SPET
- β-camera for β-radiography

Conclusions and Future Outlook

People involved in our R&D :

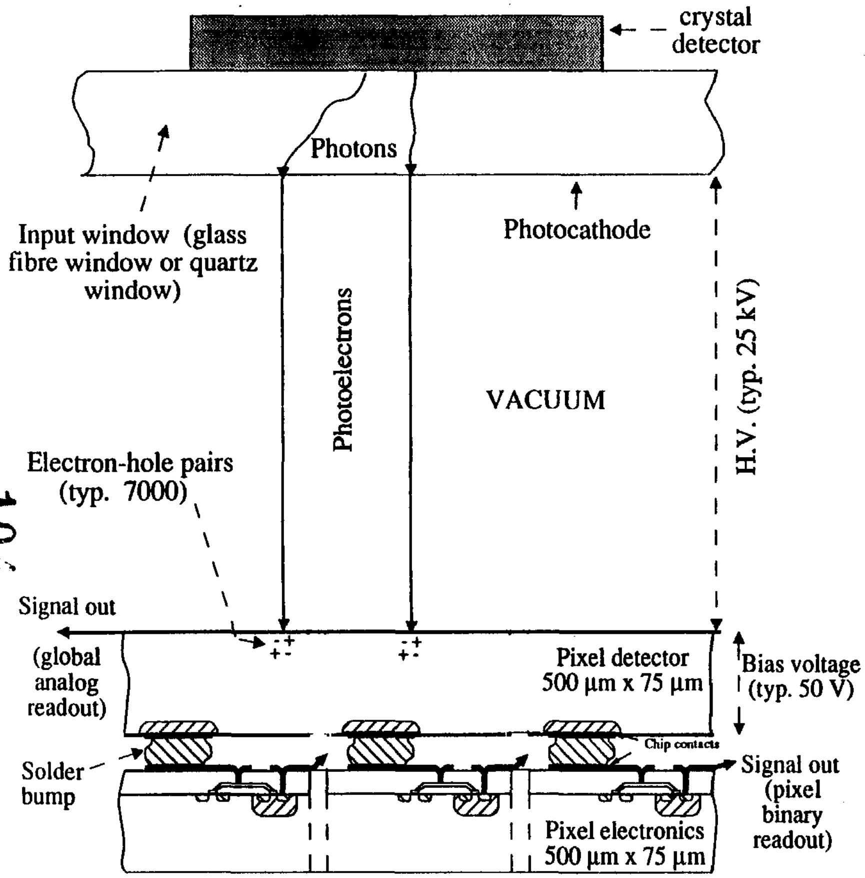
Different groups at CERN and INFN Rome

Industrial partners like:

DEP, Edgetek, GEC - Marconi, Preciosa - Crytur

Carmelo D'Ambrosio, CERN/EP-TA2

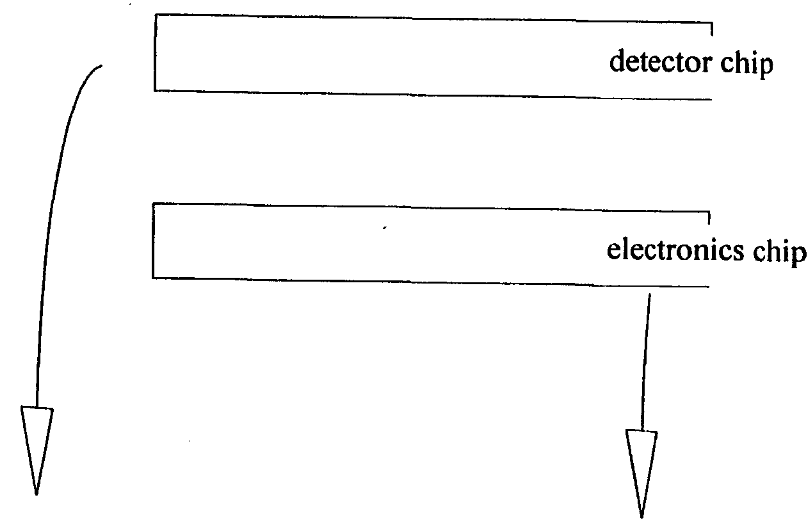
Position-sensitive photon detection with an ISPA-tube



pixels chip is Ω1, Ω2, Ω3
developed by RD-19 and
CERN-MIC group

CERN-PPE/OF
LAA-RD7
CERN-ECP/MIC
RD19

The Self – Triggering Principle



Fast, analogic and global information	Pixel signals out (with present chip, pixel response is binary)
Trigger for strobe	Precise space information
Immediate calibration in photoel. or energy	2-D imaging
Selection of a window in energy possible	

The ISPA Tube is a photon- and position- sensitive optoelectronic device.

It is fast : its "shutter" is as fast as nanoseconds;
It can stand high readout rates (at present 1 Mhz)
It features high spatial resolution: as low as 50 μm;
Its photocathode has a high Q. E. : ~25% in the near UV
It is photon sensitive with a Single El. Resolution ~ 20 %

Our goal is to have a "video camera" sensitive to photons from near-infrared to γ-rays, but also to charged particles, β-rays or neutrons.

The idea is to just use a "suitable lens" (or active medium) for our camera to convert a certain process into a photoelectronic image.

For Scintigraphy applied to human organs, requirements are:

- High counting efficiency (decrease the quantity of radio-tracer),
- Spatial resolution around 1 mm FWHM (better image definition),
- Energy resolution around 20% FWHM (background rejection),
- Event rate ~1 MHz/cm^2
- Readout rates ~10 kHz/cm^2
- Large active surface (50 cm^2 to 500 cm^2)

For β – autoradiography, main requirements are:

- Linearity,
- High counting efficiency for a wide range of beta energies,
- High spatial resolution (less than 100 μm FWHM)

γ - detection

for medical applications ^{99}Tc ~ 140 keV gamma energy

The active medium consists in either :

a YAP – crystal thin plate (1 to 2 mm) or

a YAP – array

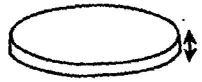
(from 300 μm to 600 μm square sizes and 10 mm length)

Results

- Spatial resolution: from 250 μm to 700 μm (FWHM)
- Energy resolution (at 122 keV): from 20% to 50% (FWHM)
- Detection efficiency (without coll.) from 20% to 90% (at 122 keV)

YAP crystal detectors *

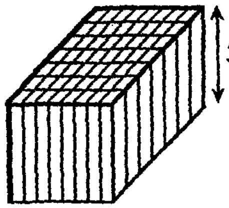
(emits light around 380 nm)



1 mm

YAP-plate

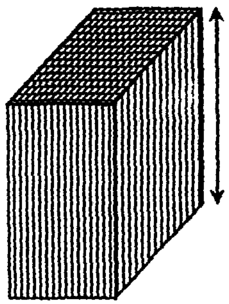
18 % eff. @ 122 keV



5 mm

YAP-array1
600 x 600 μm^2 crystal elements

62 % eff. @ 122 keV



10 mm

YAP-array2
300 x 300 μm^2 crystal elements

86 % eff. @ 122 keV

YAP emission peaks at ~365 nm

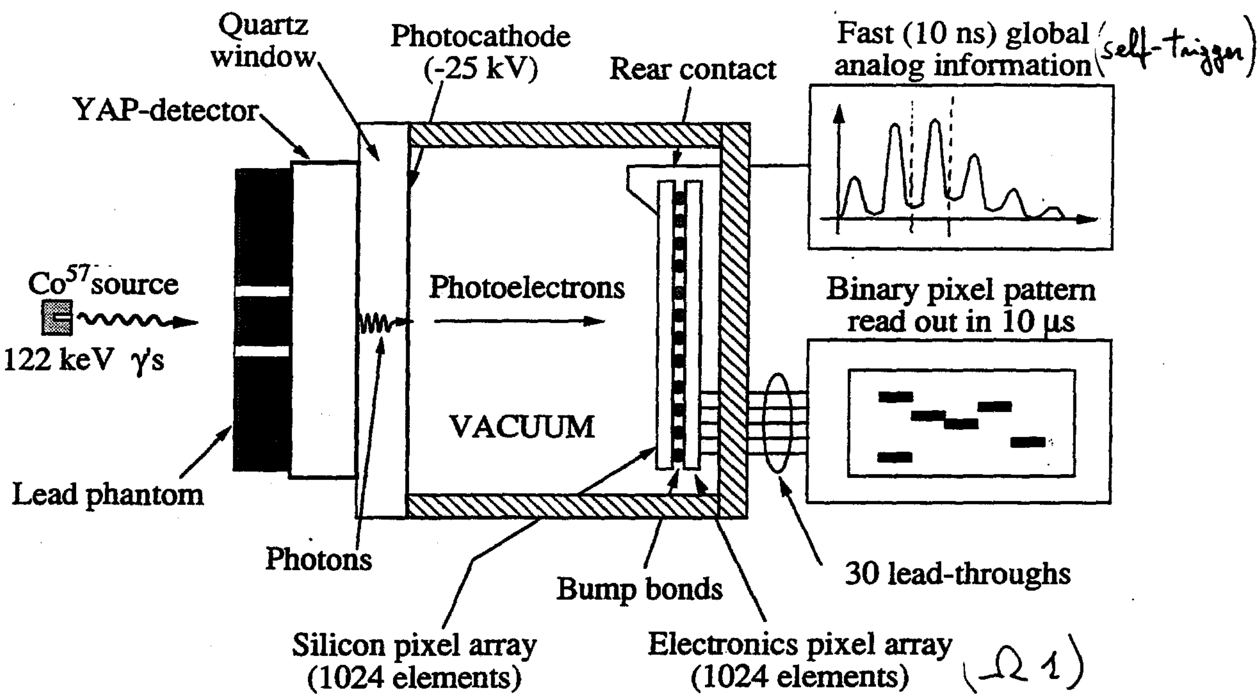
@ 122 keV ⟶ photoeffect = 63 %
Compton = 37 %

Our YAP crystal detectors are produced by Preciosa Krytur, Tournov, Czech Republic.

We have tried two basic configurations

- ISPA 1 : the photocathode is evaporated on a fibre optic window (glass)
  - adv.: high spatial resolution
  - drawback: poor spectral matching between YAP-emission spectrum and ISPA-window → low effective Q.E. → low energy resolution
- ISPA 3 : the photocathode is evaporated on Quartz
  - adv.: QE $\gtrsim 25\%$ → high energy res.
  - drawback: large cluster sizes

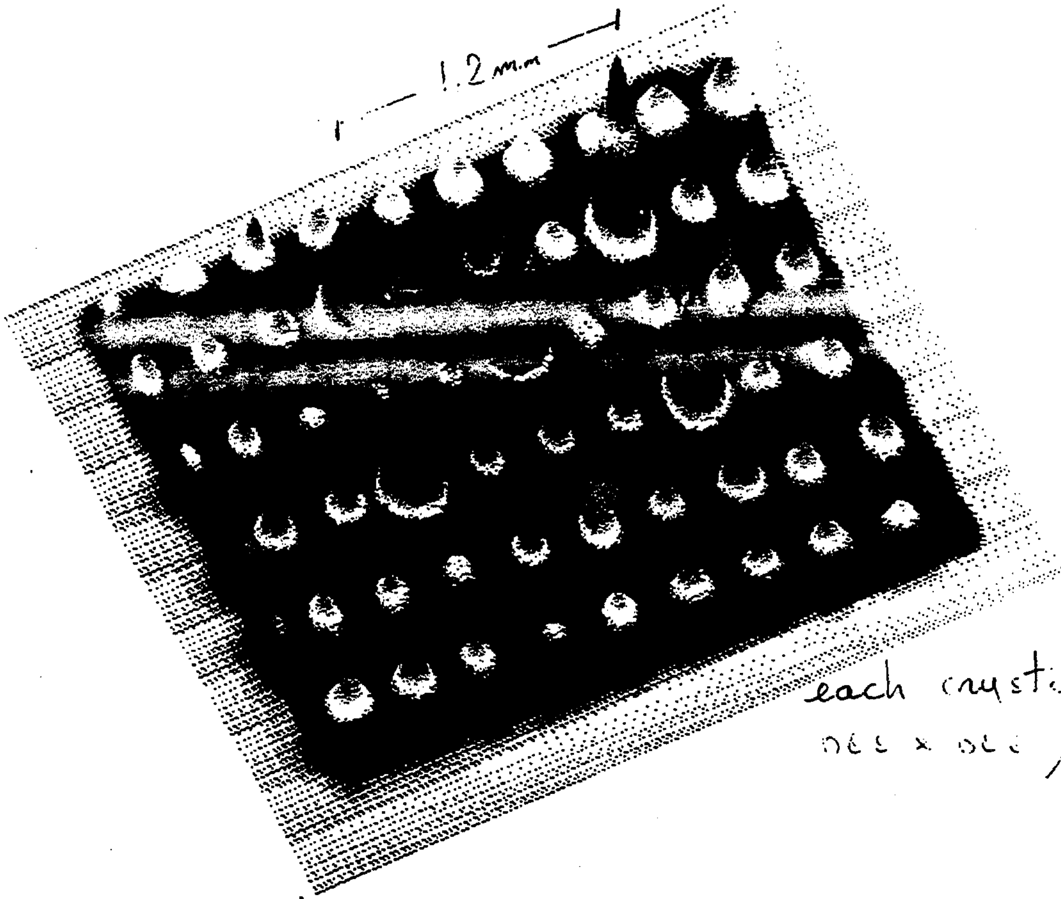
Space res $\propto \frac{\sigma}{\sqrt{N_{hit}}}$



(Ω1)

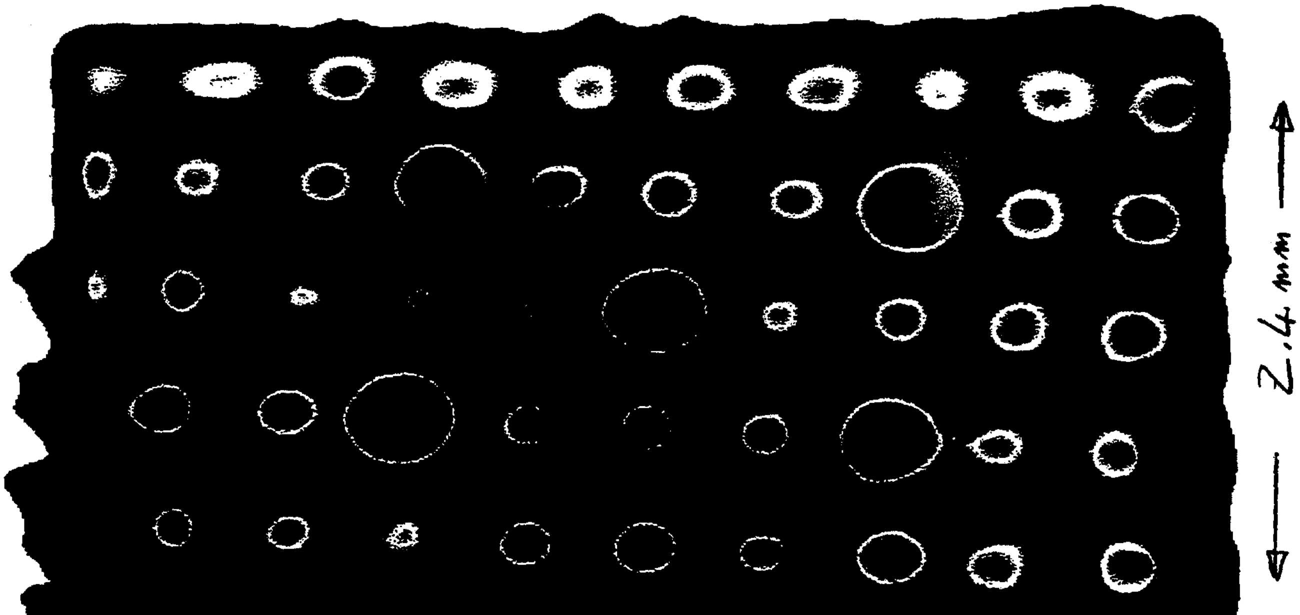
not to scale

3-D Plot



each crystal is

Gamma image of the collimator



Analog signal height distribution of 122 keV gammas detected by
a YAP crystal array or plate readout by an ISPA-tube with a glass fibre window

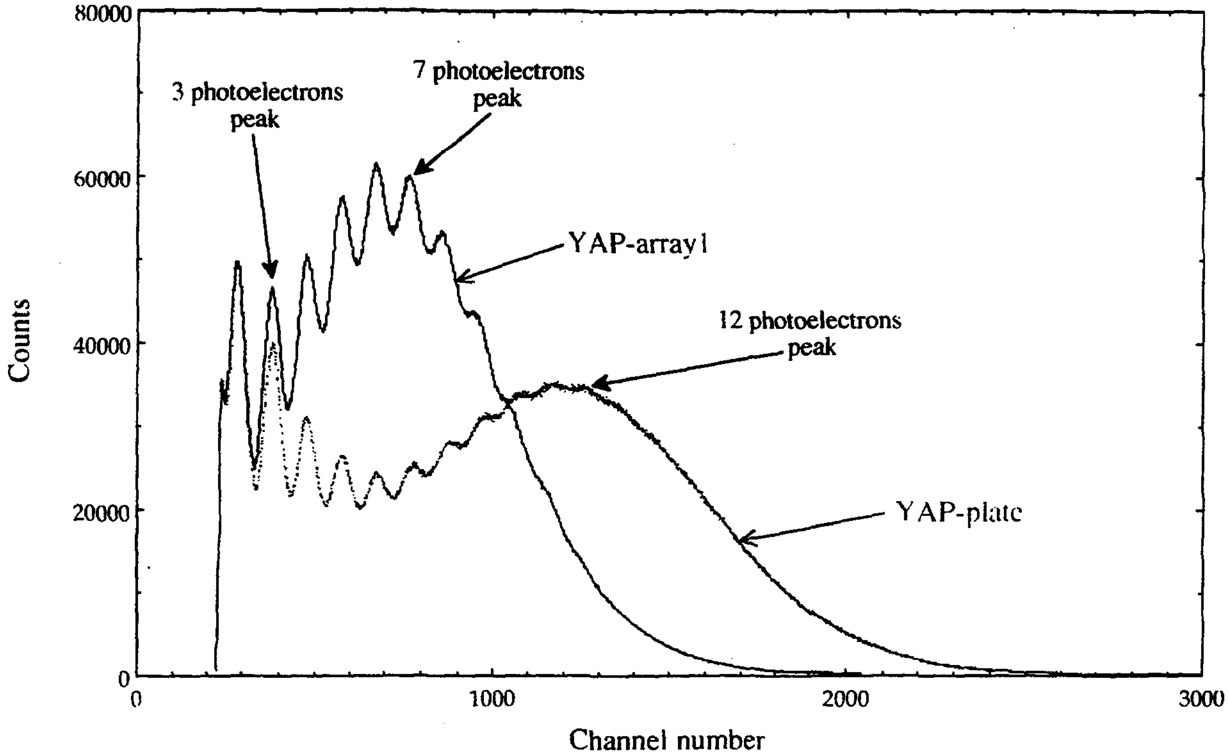
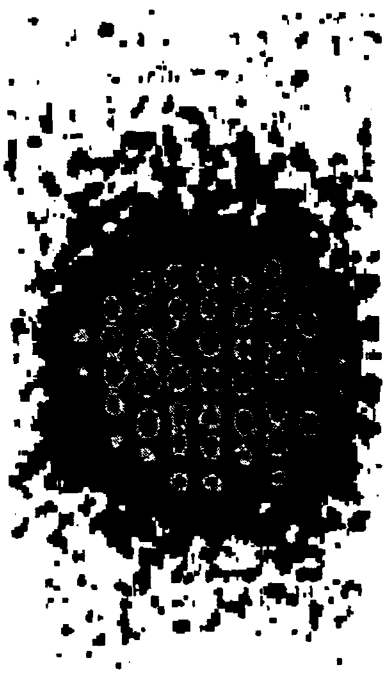


Image of a 122 keV gamma source (^{57}Co) through a 1-hole (2mm) lead collimator



YAP-array (300µmx300µm) + glass fibre window ISPA-tube

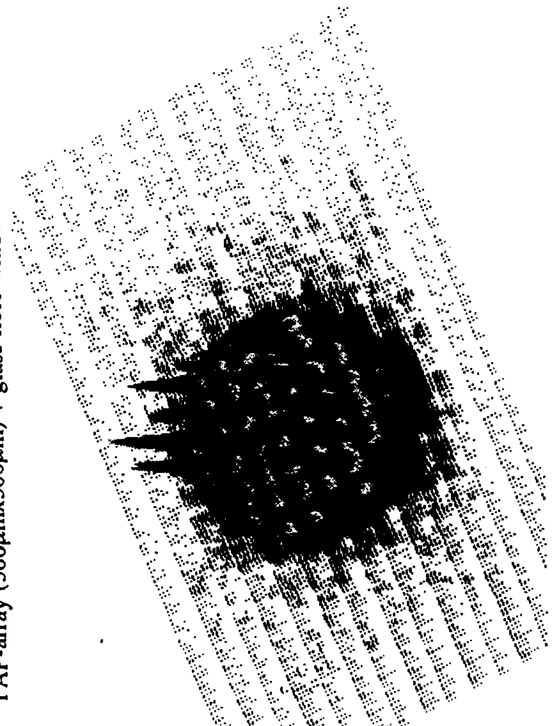
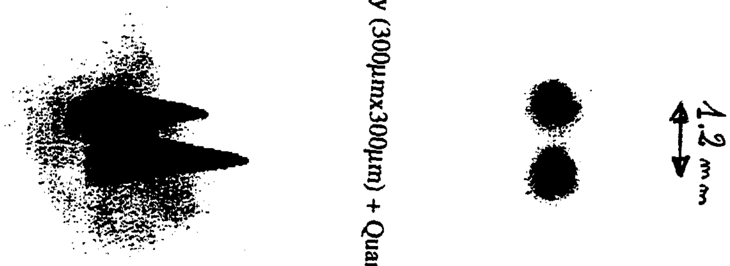
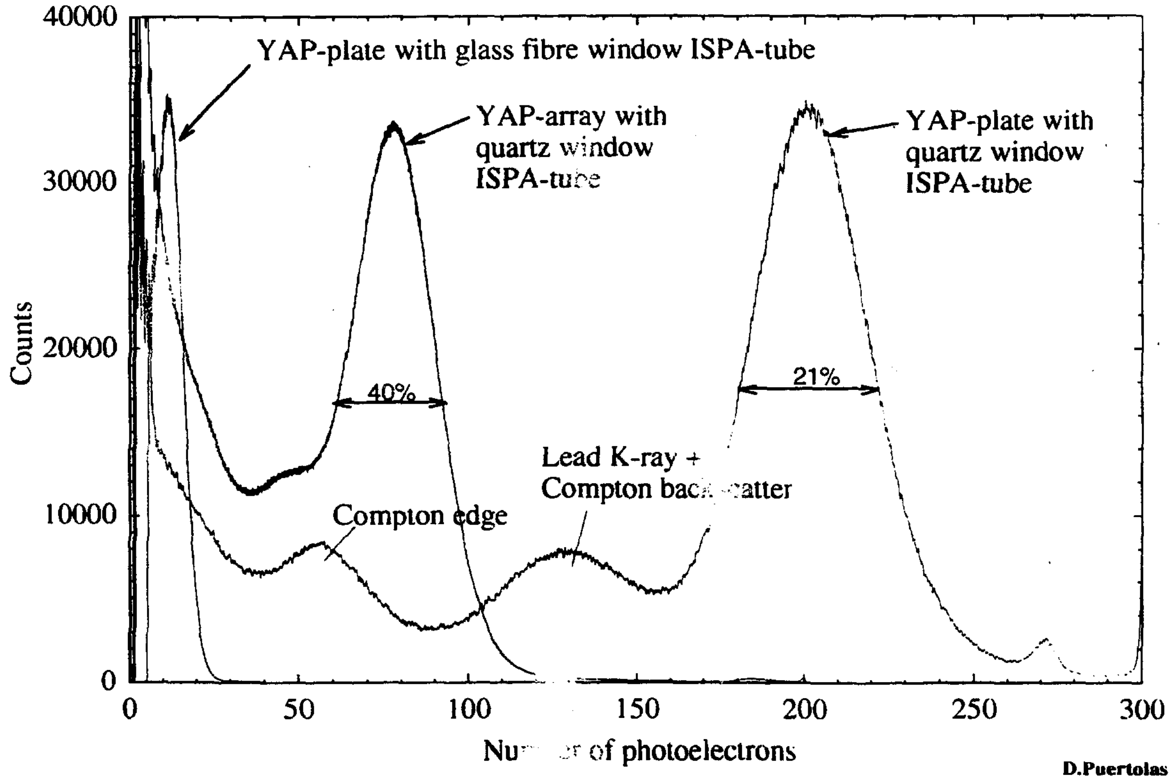


Image of a 122 keV gamma source (^{57}Co) through a 2-holes (300μm) lead collimator



YAP-array (300μmx300μm) + Quartz window ISPA-tube

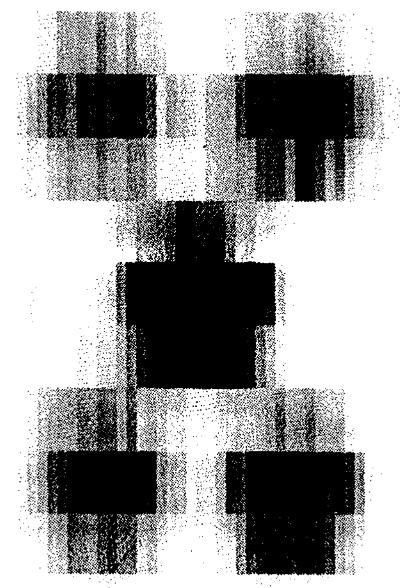


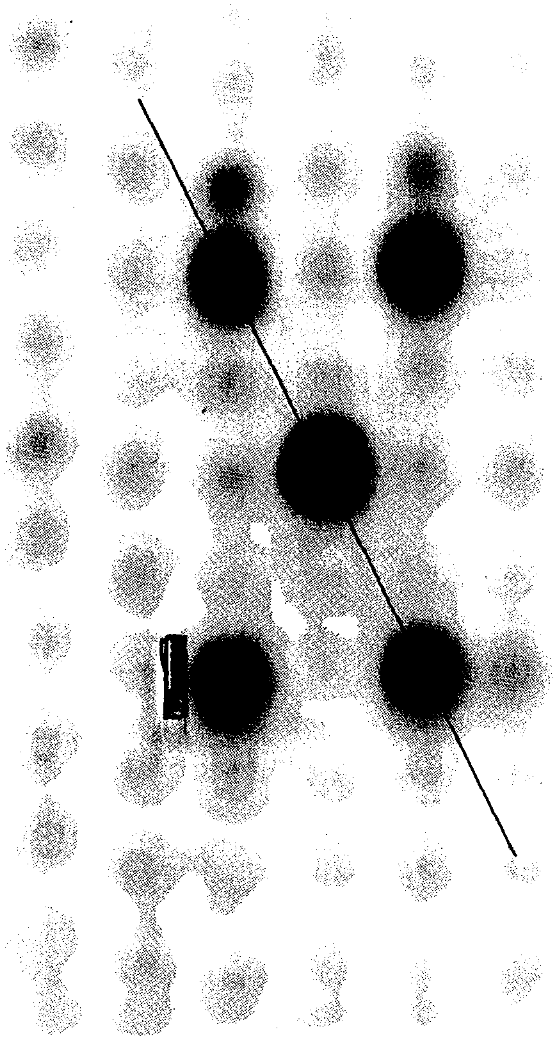
D.Puertolas et al.
CERN-INFN
Villa Olmo 96

With the ISPA - tube,
two modes of acquisition are available:

- raw accumulation of events

- for each triggered event, a centre of gravity is calculated and then accumulated
  - higher resolutions $\left(\frac{\sigma}{\sqrt{N}}\right)$, but not applicable on line for very high trigger rates (do the analysis off line)





β - detection

for β – radiography of "in situ hybridization"

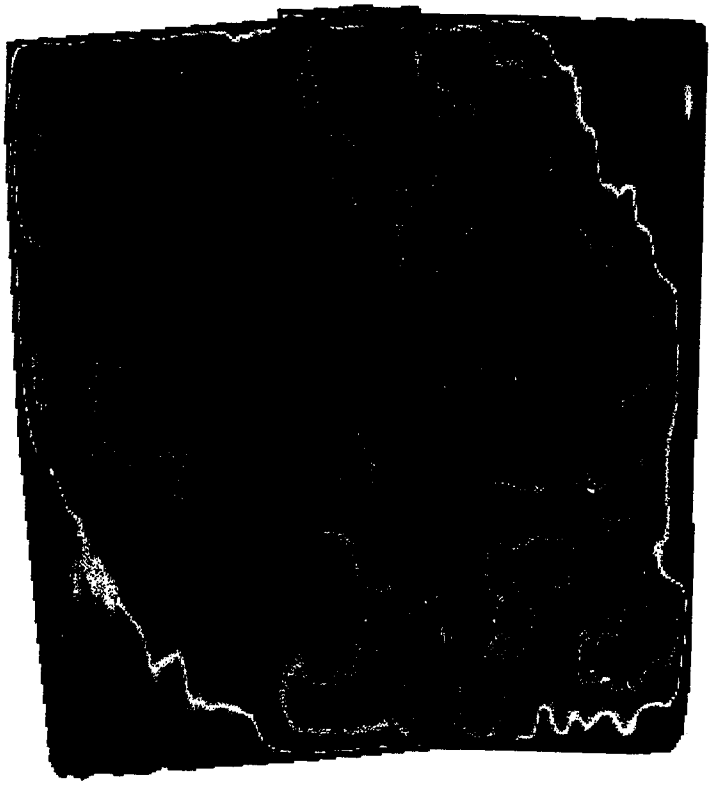
The active medium consists in either :
thin plastic scintillator sheets **(30 μm to 1 mm) or**
thin inorganic scintillators **(Si Y_2O_5)**

Application in Biology*: In Situ Hybridisation

- ^{35}S radioactive tracer in mouse cerebral trunk slices
- neurone calcium sensor protein

* In collaboration with M. Dubois Dauphin (CMU, Geneve)

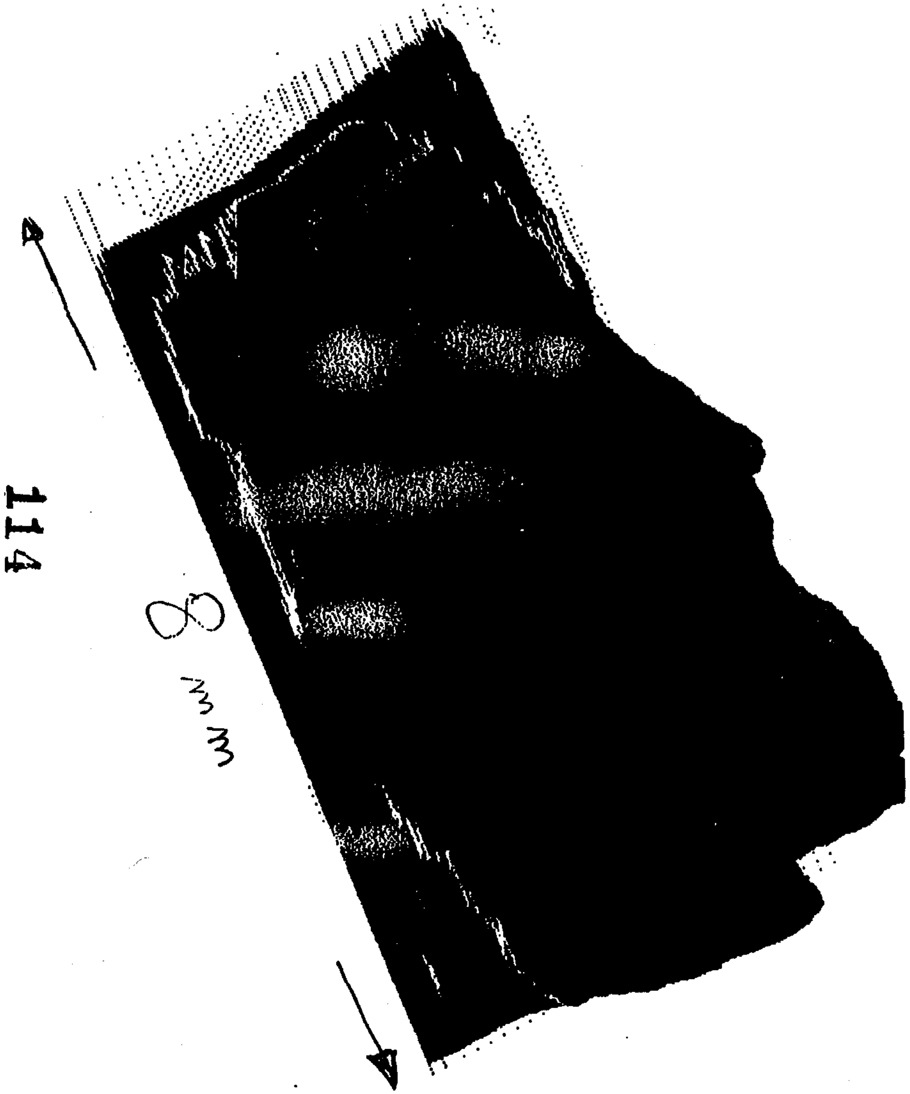
Carmelo D'Ambrosio, CERN/EP-TA2



In situ Hybridisation*
^{35}S

microslice of mouse brain

*Work performed in coll. with Dr. M. Dubois-Dauphin at CMU - Geneve



FUTURE PLANS (Two years ago)

- new RD19 chips (LHC1) implementation is going on (see M. Campbell talk)

- increase active surface
  - larger photocathode
  - demagnification
  - several chips in one tube

- test of other scintillators and geometries

- new chip design better adapted to these applications

- evaporation of the PK directly on the crystal

Up to now, chips specifically developed for ionizing particle detection were used in the ISPA-tube. The results obtained are impressive. However, in order to:

- avoid complexity where not needed,
- scale up active surface,
- improve detection efficiencies for low energy photoelectrons and uniformity responce,
- decrease operating voltages,
- and minimize costs,

a specific chip is needed.

Its main features would be:

- Square pixel size (200 to 400 μm),
- Low threshold (~2000 el)
- Thresholds spread ~300 el at FWHM (or individually adjustable thresholds)

see Medipix (W. Snoeys talk)

- El. Noise ~500 el at FWHM
- Digital readout and logic part as for LHC1 chip
- Delay line tunable to 2 ÷ 3 μs
- Thinned detector unit with "no" dead layer
- Large detectors to bump-bond four electronic chips on

see ALICE

New ISPA Tube

For Single Photon Emission Tomography

Active Surface ~80 mm diameter
Spatial Resolution ~ 1 mm (FWHM)
Energy Resolution (at 140 keV) ~ 15 – 20 % (FWHM)
Counting Rates > 1 MHz / cm^2

80 mm diameter photocathode on quartz
Silicon chip surface 16 x 13 mm^2 (four times the LHC1 chip)
Electrostatic focussing Tube (demagnification ~5)
1 x 1 x 10 mm^3 YAP or CsI array

A similar tube is being developed as a candidate for the Rich-detector readout in LHC-b (see M. Campbell contribution)

Conclusions

ISPA - tubes as optoelectronic readout offer a powerful tool for a wide range of applications:

- for high - energy physics:
  charged particle trackers, active targets, Rich counters;

- for spectroscopy and astronomy:
  time-resolved position-sensitive photon-counting;

- for nuclear medicine
  hadron beam diagnostic, 2-D imaging, β- or γ- cameras;

- for biology:
  in-situ physiological processes diagnostic, etc.;

- for material analysis...

Recent Performance of Prototype Readout-Sensor Assemblies for ATLAS

Eric Charles
Physics Department, University of Wisconsin-Madison,
1150 University Avenue, Madison, WI 53706, USA
For the ATLAS Collaboration

Abstract

The past two years have seen the first use of fast (40 MHZ) pixel readout arrays in testbeam situations. Among other achievements, several LBL designed M72b readout chips were bonded to various sensors and successfully operated during the 1997 testbeam season. Results are presented here covering both the bench characterization and beam testing of various M72b detector/readout assemblies. In particular: threshold uniformity, timewalk, efficiency, resolution and Lorentz effects have been studied. Furthermore, first results from the current generation FE-B chips are also presented here.

1 Introduction

There are good reasons why pixels are the detector of choice for the innermost region of the ATLAS detector at the LHC. The small element size implies both low leakage current and low noise, making them intrinsically more radiation hard than strip detectors. In addition, the true 3-D information avoids tracking ambiguities. This is especially important at the LHC where each bunch crossing is expected to yield about 25 minimum bias events.

The design luminosity of the LHC is $10^{34}\text{cm}^{-2}\text{s}^{-1}$ with a bunch crossing rate of 40 MHz. Noise occupancy and timing constraints are driven by the desired track finding efficiency at this high luminosity. These constraints dictate that each hit in the detector must be correctly associated with a single bunch crossing. In other words, the cumulative time of charge formation, drift, pre-amplification and discrimination must vary by less than 25 ns for all signals of interest. The noise occupancy should be less than 10^{-5} hits per channel per bunch crossing. Furthermore, the physics goals of ATLAS require a point resolution of 12 μm in the rϕ direction and 100 μm in the z direction. Finally, ATLAS requires a pixel dead time of less than .5 μs.

These timing and occupancy requirements must be met by a pixel layer at an 11 cm radius for the entire life of the detector. At this radius, the lifetime dose is expected to be 200 KGy and 5×10^{14} 1 MeV n cm^{-2}. At the end of the detector life, the maximum attainable depletion depth is estimated to be about 100 μm at 200 Volts bias. Thus an in time threshold of about 2000 e^- would be required to keep losses from pulse height variations at a tolerable (below 1%) level. With this threshold, the noise occupancy requirement dictates that noise and threshold dispersion each be kept below about 200 e^-. These requirements can be relaxed if the detectors can be operated at higher bias voltages after irradiation.

The ATLAS pixel baseline calls for $50\mu m \times 300\mu m$ elements with binary read out. The detectors will be n^+ on n doped Silicon aiming at a thickness of 200-250 μm. The requirements and baseline decisions are explained in detail in [1].

Parallel prototyping efforts for the pixel readout electronics of the ATLAS detector have been underway in both Europe and the United States. For more details of the role of pixel detectors in the ATLAS experiment see [1], [2].

In the past two years an LBL-Wisconsin group has designed and tested two prototype versions of ATLAS pixel readout chips, M72b and FE-B. During 1997 the M72b chip was extensively tested both on the bench and in the H8 beamline at the CERN SPS. FE-B chips were received in mid-April 1998 and some very encouraging first results have been obtained.

2 The M72b Chip

The M72b chip represented a development phase of the ATLAS pixel project. It was intended as a test chip to prove the soundness of the readout architecture and the feasibility of meeting the electronics requirements. The front-end performance was not intended to meet all of the ATLAS requirements.

The M72b chip was fabricated in a .8 μm CMOS technology and supports an array of 12 columns of 64 50 μm $\times$ 536 μm pixels. The readout is column based. End of column (EOC) logic for trigger coincidence has been implemented. The coincidence is made using an externally generated 8 bit 40 MHz timestamp which is bussed to the end of column logic. If any pixels in a column fire, the timestamp is latched in an 8 bit by 8 deep buffer and the buffer address is written to a 3 bit latch locally at each pixel which fired.

Triggers are bussed to the EOC logic and a coincidence flags buffer elements for subsequent readout. If a trigger for a particular buffer element does not arrive when expected, the corresponding pixels must be actively reset and the buffer element cleared. Analog information is provided by integrating the discriminator output onto a storage capacitor. During readout, the stored charge for each hit pixel is multiplexed off chip and digitized. Test circuitry allows checking the pixel front end and the readout components of the chip independently.

2.1 M72b Bench Results

During the first six months of 1997 M72b arrays were extensively characterized on the bench at LBL. In general the digital performance was quite good. The analog performance was adequate, although not up to ATLAS requirements.

On the bench the M72b array-sensor assemblies performed with high efficiency and essentially no spurious hits down to thresholds of 3000 e^-. At these settings 400 e^- dispersion and 700 e^- noise were measured. Furthermore, the analog information was reasonably good. For any given pixel it was possible to measure the input charge to within approximately 1000 e^- up to input charges well over the MIP charge of 25000 e^-.

Fig. 1 shows some timewalk parameters from a chip that was not bonded to a sensor. The upper plot shows a per channel histogram of the time between the arrival of earliest hits seen on any pixel in the array and the average hit on each particular pixel when given a large (60000 e) input charge. The excellent (sub nanosecond) skew in timing across the array is largely attributable to the readout architecture. The lower plot is a per channel histogram of the input charge required for the timewalk to be under 25 and 50 ns. One can see from the bottom figure that the M72b array does not meet the ATLAS timewalk requirement.

Systematic studies of performance parameters revealed significant differences between odd and even columns with the odd columns behaving somewhat better. Eventually this problem was diagnosed as a layout flaw which allowed the ground reference for the discriminators in the even columns to float relative to that of the preamplifiers, resulting in modified threshold, noise and TOT behavior in these channels.

2.2 M72b Testbeam Results

The M72b array was characterized in a 180 GeV pion beam at the CERN SPS. M72b chips were bump bonded to both n^+ on n and n^+ on p detectors. The detectors were 300 μm thick and had a bricked geometry, i.e. alternate pixel rows were offset by one half pixel length. Data were taken at various bias voltages, V_{bias}, with the detector normal to the beam as well as with the detector rotated about the long pixel axis (ϕ) or the short pixel axis (θ). Runs were taken both field free and with a 1.5 T longitudinal magnetic field to simulate operation parallel to the beam in the ATLAS solenoid. A high resolution Silicon strip tracking telescope was also read out. All results presented here were obtained from events where a single high quality track, $\chi^2 < 1.5$ was found in the strip telescope. Track errors projected into the pixel plane were on the order of 3 μm.

Fig. 2 shows the detector efficiency as a function of V_{bias}. The efficiency was determined from the number of events in which a pixel cluster was found within 50 μm of the track intercept in the short pixel dimension. The trigger was asynchronous with the 40 MHz clock of the pixel electronics, so a TDC was available to indicate at what point in the 25 ns time bucket the trigger arrived. The open circle values were determined requiring the hit to have arrived either in same time bucket as the trigger or the next time bucket. This imposed a timewalk cut of anywhere from 25 ns to 50 ns depending on when the trigger arrived. The solid circle values were determined including hits from the next two time buckets as well. Finally, the star values were determined by eliminating events in which the trigger arrived less than 10 ns into a 25 ns time bucket. This was to eliminate events where large charges may have caused the pixel to fire before the early end of the accepted region. It can be seen that except for the case of very low V_{bias} and a tight timing window, the efficiency is between .98 and .99. With the TDC cut imposed the efficiencies are uniform at .99. Though the cause of the residual 1% missing hits is not fully understood, this result obtained with a 40 MHz chip having full EOC logic is encouraging. It should also be noted that the level of spurious hits was below the ATLAS requirement of 10^{-5} hits per channel per bunch crossing.

Fig. 3 shows the mean charge measured in a n^+ on p sensor as a function of bias voltage. In the events considered, there was exactly one cluster found in the pixel detector and this cluster was required to be within 50 μm of the track intercept in the narrow pixel direction. The result of a fit to $\sqrt{V_{bias}}$ is shown on the figure. Unfortunately, most of the data from the n^+ on p sensors were taken at $V_{bias} = 40$ V, where the detector appears to be only about 75% depleted.

Fig. 4 shows the resolution measured along the short axis of the pixels with various levels of readout information as a function of ϕ. The cluster position was estimated by a simple charge centroid. As ϕ is increased, the number of clusters which span more than one row increases. We see that the best resolution comes at 10° when two pixels fire much, but not all, of the time.

Fig. 5 shows the effects of bricking. As with the short axis, the cluster position was estimated by a simple charge centroid. As ϕ is increased, the number of clusters which span more than one row increases. The added information this yields in a bricked detector, even with this simple position estimate, is exhibited in the strong ϕ dependence of the residual distribution. In confirmation of this, it was found that for a given cluster width the residual was nearly independent of ϕ.

Finally Fig. 6 shows the mean number of rows spanned by a cluster as a function of ϕ with and without the 1.5 T field. A Lorentz drift angle of approximately 9° can be estimated from the figure. A monte carlo study is underway to better understand the charge collection and should help interpret this behavior.

3 FE-B Chip

The FE-B effort, as with the M72b chip, uses a timestamp to make the trigger coincidence. Although the ATLAS baseline calls for binary readout, FE-B prototypes provide charge information via a time over threshold (TOT) measurement. In this generation the timestamps are bussed directly to the pixels, latched on the rising and falling edges of the discriminator and then written to end of column buffers. Buffering is provide for up to 20 hits from 16 different triggers. The M72b chip could handle events with an arbitrarily large number of hit pixels. Those pixels were then dead until read off of the chip. The FE-B chip can not store more than 20 hits per column pair at a time, however, the pixel deadtime is much shorter, being roughly equal to the return to baseline of the pre-amplifier. At 40 MHz, a 5 bit TOT measurement would give a pixel deadtime of roughly 800 ns. Another feature of FE-B is a dual level discriminator. The low discriminator determines the hit timing as well as the time over threshold, while the high discriminator validates the hit. The aim of this configuration is to satisfy the timewalk requirement within the power budget and without introducing excess crosstalk. Furthermore, each pixel contains a three bit tuning DAC which acts as a vernier adjustment for the threshold in that pixel. These tuning DACs can be individually set so as to minimize the threshold dispersion. For a detailed discussion of the FE-B pre-amplifier and discriminator configuration see [3].

3.1 FE-B Bench Results

Since the FE-B wafers' arrival at LBL on April 15 a wafer probe station has been commissioned and wafer probing is underway. Individual chips have also been probed on single chip support cards.

The results have been extremely positive. Aside from a bug in the priority scan that causes many hits from columns 11-18 to be lost, the chips have been nominal and the yield has been extraordinary. On the first wafer probed, 81 of 85 chips passed all tests.

So far, FE-B arrays without detectors have been operated at a 5000 e^- threshold setting with 450 e^- dispersion without use of the tuning DACs and less than 70 e^- noise. After tuning a 3000 e^- threshold with 100 e^- dispersion was achieved.

3.2 FE-B plans

Currently work is underway to produce module controller chips, MCCs, to be used in fabricating pixel modules. The modules will be composed of 16 front end chips with 18 columns of 160 pixels each mounted on a single detector substrate and read out through a MCC. The division of functionality between the two chips is close to that of the final system. The modules will first be fabricated in rad-soft technologies. After the successful completion and testing of the rad-soft versions, rad-hard submissions will follow.

4 Conclusions

Silicon pixel detectors offer an answer to many of the challenges of running at the LHC, but come with many challenges of their own. Though the first ATLAS prototypes were not intended to meet all of the requirements of this harsh environment, results obtained with them are encouraging. Despite a 2005 LHC turn on date, detector production, testing, installation and commissioning time scales make the immediate schedule tight. The second round of prototypes have yielded some very positive first results.

References

[1] The ATLAS Collaboration, ATLAS Pixel Detector Technical Design Report, CERN/LHCC/98-13, (1998).

[2] G. Gagliardi, these proceedings.

[3] F. Pengg, Proc. 1997 IEEE Nuclear Science Symposium, Albuquerque, Nov 9-15, 1997, to be published in TNS.

Timing Performace: M72b

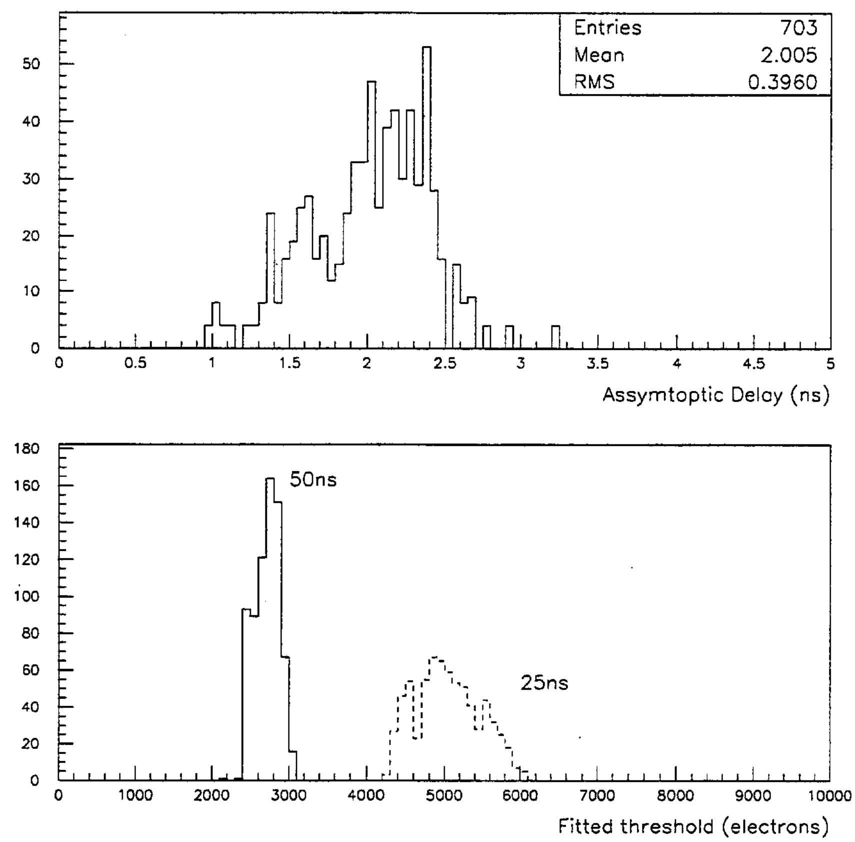


Figure 1: top) Timing skew across the M72b array. bottom) Threshold in electrons for hits to arrive within given delays.

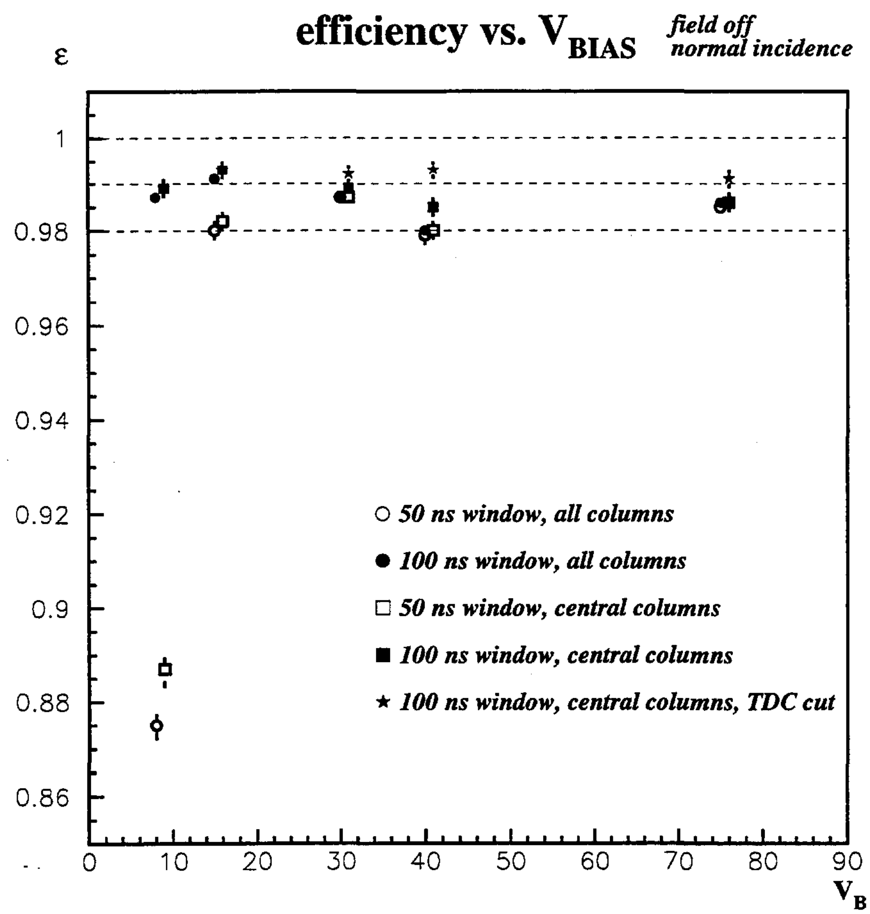


Figure 2: Efficiency as a function of bias voltage at normal incidence for an n^+ on p-bulk detector operated partially depleted. The various data sets are described in the text.

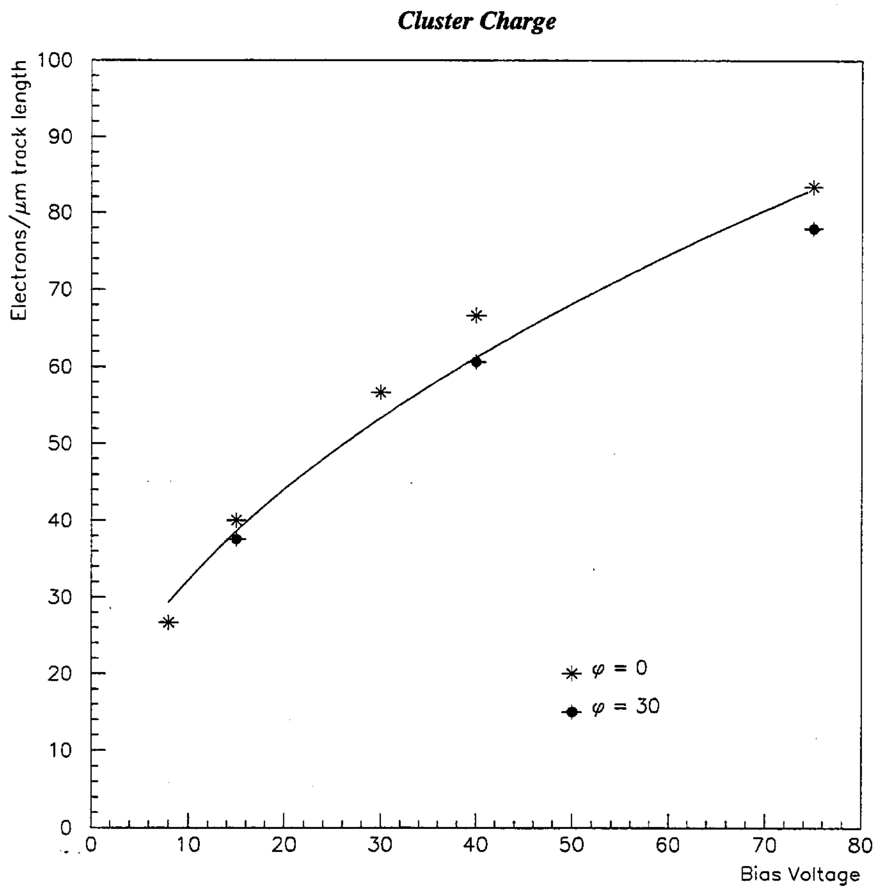


Figure 3: Mean charge deposited in the n^+ on p-bulk detector per track length as a function of the bias voltage.

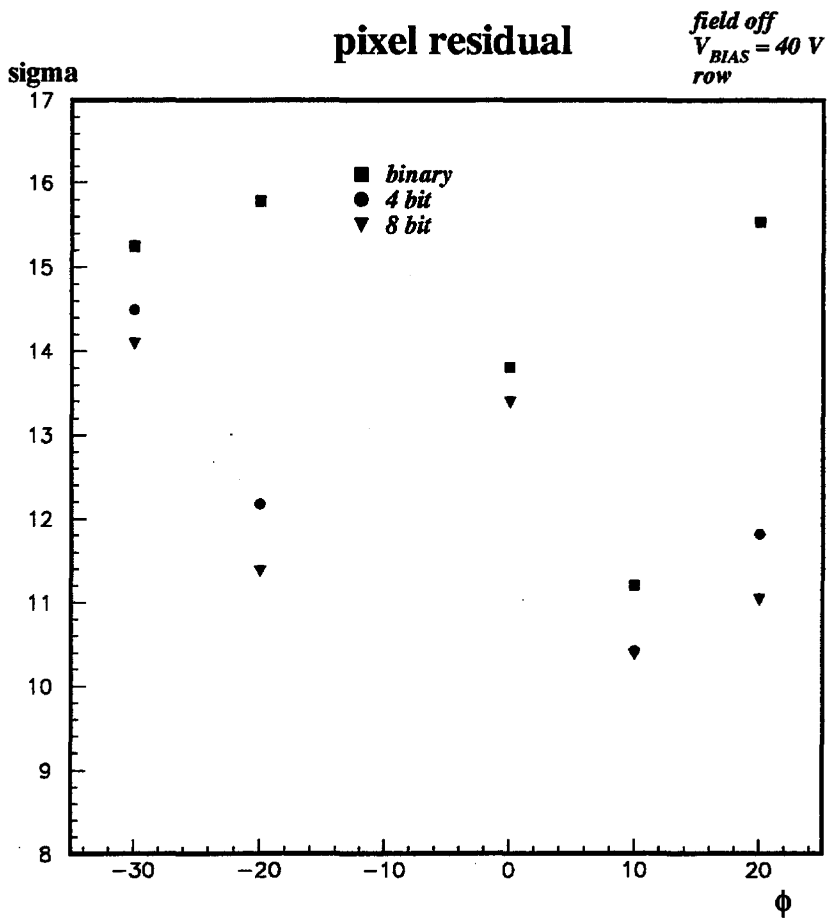


Figure 4: RMS of the residual distribution between the track projection and the pixel cluster location in the short pixel dimension as a function of ϕ.

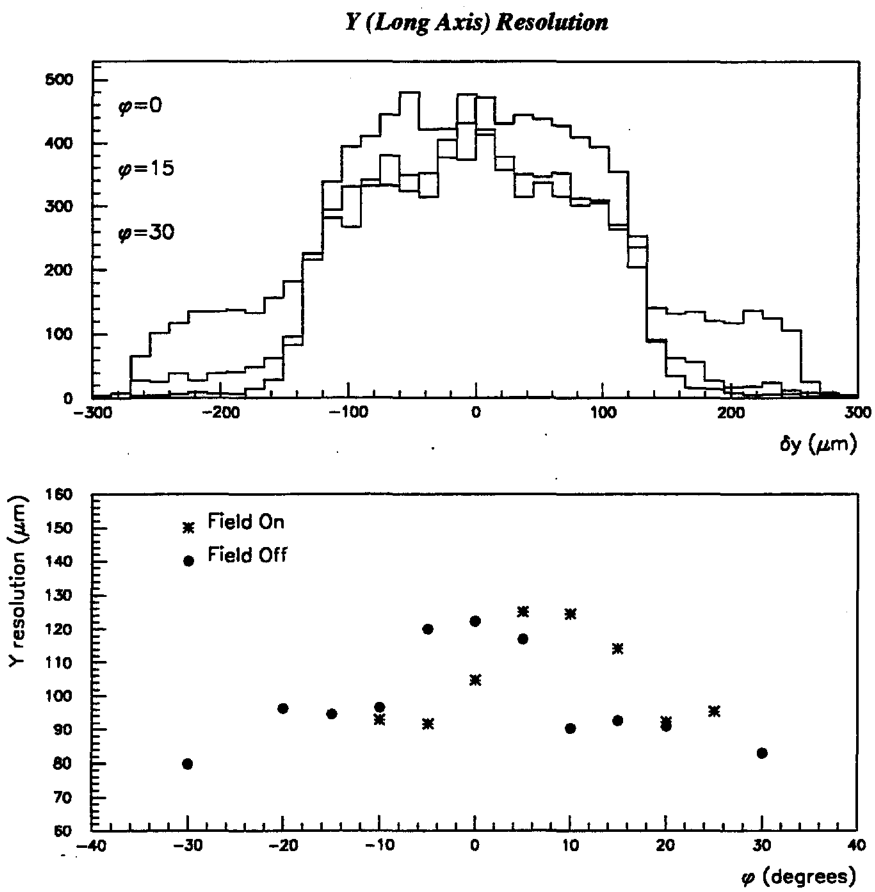


Figure 5: top) Histograms of residuals in the long pixel dimension for various ϕ. bottom) RMS of the residual distribution between the track projection and the pixel cluster in the long pixel dimension as a function of ϕ.

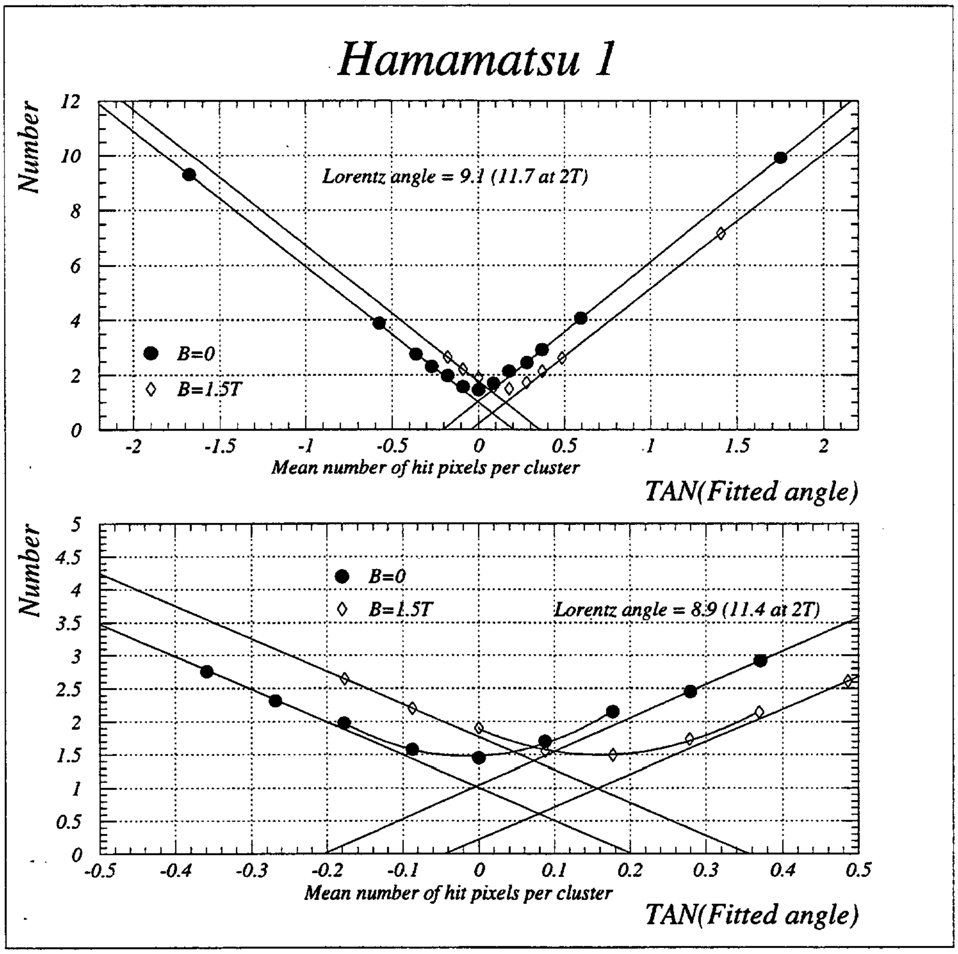


Figure 6: Mean number of rows spanned by a cluster as a function of ϕ with and without the magnetic field.

US ATLAS Pixel Electronics

K. Einsweiler, LBNL

LBL/Wisconsin electronics team: E. Charles, A. Ciocio, K. Dao, D. Fasching, A. Joshi, S. Kleinfelder, L. Luo, R. Marchesini, O. Milgrome, F. Pengg, J. Richardson, G. Zizka

ATLAS Pixel Electronics:

- Electronics requirements for ATLAS
- Electronics design effort:
  - → "Proof-of-Principle" phase (essentially complete)
  - → Realistic prototyping phase (now in testing phase)
  - → Production phase

Proof-of-Principle phase:

- Chips fabricated
- Lab and testbeam results

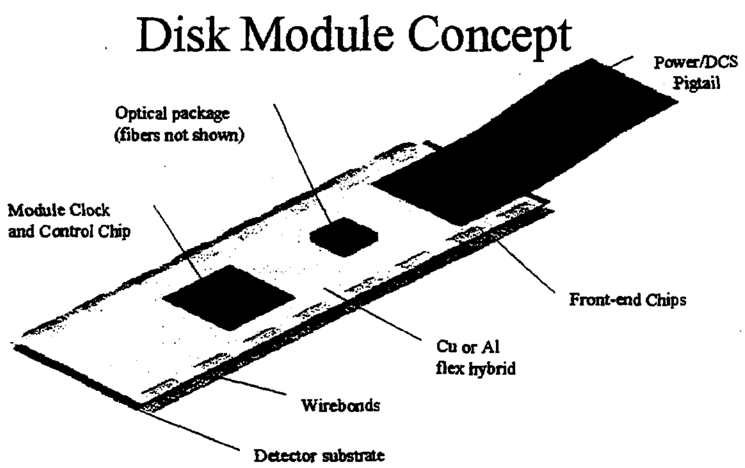
Realistic prototyping phase:

- ATLAS1 Chipset: design overview
- Design details and first results from FE-B chip

Overview of ATLAS Pixel Tracker

Basic Component:

- Modules which are placed on a mechanical support and cooling structure in "chips down" configuration, with detector substrate smaller than electronics:
  - → Silicon detectors (one per module), with active size roughly 16.4 x 60.4 mm
  - → Electronics chips bump-bonded to detectors (16 FE chips and 1 Controller chip per module)
  - → Hybrid interconnect that connects front-end chips to controller chip and services



Pixel Electronics Requirements for ATLAS

High overall efficiency is necessary:

- Pixel layers are complex, costly, and contain lots of material.
- Inefficiency sources include dead/inefficient regions, timewalk performance, electronics deadtime, masked or dead electronics channels, and high thresholds.
- Goal is for each of these to contribute less than 1% to the global hit inefficiency.

Maximum power budget is 0.6 W/cm^2, or 5.5 W/module:

- This corresponds to 250 mW/front-end chip and ≈40 μW/pixel front-end.
- It allows 300 mW for module control, and 300 mW for detector leakage.
- It allows up to ≈900 mW for power transmission and data transmission.

Radiation tolerance is at least 30 MRad, or 100 MRad for inner layer over full lifetime (silicon detectors would die).

Geometry of pixel and front-end chip:

- Pixel geometry determined by point resolution and feasibility ≈ 50μ x 300μ.
- Chip geometry determined by radhard yield, suggests die should be < 80 mm^2
- Goal: 24 column x 160 pixel matrix with ≈2.5 mm "deadspace" for peripheral logic.

Front-end requirements:

- Minimum silicon signal after 10^{15} fluence is ≈6 Ke. Efficient detection requires a threshold of about 2 Ke.
- Operating at this threshold requires a noise of less than ≈200 e, and a threshold dispersion of no more than ≈200 e.
- The timewalk should be small enough to allow 40 MHz beam-crossing association down to roughly the minimum threshold.
- The input capacitive load is expected to be about 200 fF.
- The DC-coupled preamplifier should handle leakage currents up to 50 nA/pixel.
- The noise occupancy should be below 10^{-6}/pixel/crossing.
- The crosstalk ratio (threshold/adjacent signal to fire neighbors) should be <5-10%

Readout architecture requirements:

- Unique beam-crossing association at 40 MHz.
- Store information for 2.5 μs L1 latency and handle 100 KHz accept/readout rate.
- Operation at pixel occupancies as high as 5×10^{-4}/pixel/crossing with deadtime <1%, implying no more than ≈500 ns deadtime per hit.
- Adequate buffering in perpheral logic to prevent significant hit loss, even for large local occupancy fluctuations (e.g. inside of jets where chip occupancy x 10-20).

The LBL Matrix (M72b)

The front-end design:

- The front-end design uses a fast high-gain preamplifier with an unusual "leakage subtraction" circuit, and provides linear TOT up to very large charges.
- A simple discriminator follows, giving reasonable threshold dispersion (250e), but only fair timewalk (50 ns required for pulses near threshold). The disriminator output is integrated on a capacitor to provide analog TOT information.

The readout architecture:

- Pixel address and charge information is stored in the array in a "content-addressable memory" structure which can retain 8 simultaneous events.
- Timing information is stored in the peripheral logic for each event on a per-column basis using an 8-bit Grey code timestamp and a 2-level buffering scheme to store 8 events prior to trigger coincidences and 4 events pending readout.
- A 2D sparse-scan readout system allows transfer of this information off-chip at up to 10 MHz. Only hits above threshold for triggered crossings are read out, and each hit contains the pixel address and timestamp, plus the analog charge information.

Pixel Electronics Development Program

ATLAS requirements go far beyond existing pixel systems

- "proof-of-principle" prototyping was carried out to explore different concepts and see if 40 MHz concurrent operation at low threshold was achievable.
- These first chips have achieved many of the ATLAS requirements.

Two major efforts were carried out inside ATLAS:

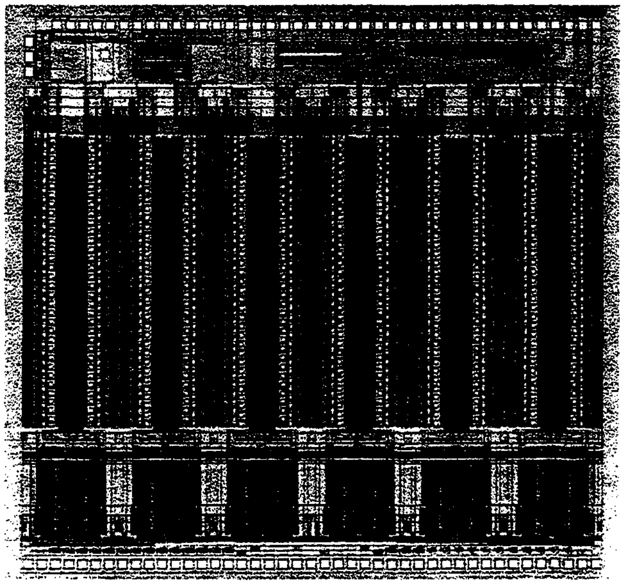
- Bonn/CPPM matrix: a 12x63 pixel array with 50μ x 436μ pixels and no peripheral logic, providing digital TOT information, fabricated using AMS 0.8μ BiCMOS process (see talk of T. Kuhl).
- LBL matrix: a 12x64 pixel array with 50μ x 536μ pixels and complete peripheral logic, providing analog readout of TOT information, fabricated using HP 0.8μ CMOS process (see talk of E. Charles).
- Extensive lab characterization and beam testing has been performed on both.

Now have moved to realistic ATLAS prototypes:

- Learned many lessons from prototypes and subsequent development work.
- Incorporate complete set of functional blocks required for module construction.
- ATLAS1 chipset includes 2 front-end chips and 1 module controller chip initially radsoft, but targeted for radhard.

Chip Layout:

- Pixel input pads use staggered geometry (100μ bump separation) and inputs are in center of pixel to support bumping to "bricked" detector geometry
- Peripheral logic includes 2 levels of FIFO buffering per column and sparse scan.
- Digital readout logic is on bottom, analog biassing and test points on top



Summary of Tests (see talk of E. Charles for more plots):

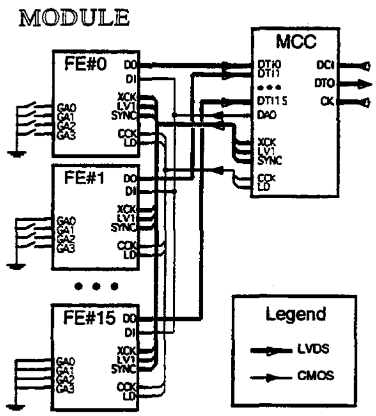
- Initial tests were performed with n^+ on p-bulk detectors fabricated at LBLn abd bump-bonded by Rockwell (now Boeing). They provide partially depleted operation, with only single-sided processing.
- Electronics was operated at a threshold of ≈ 4 Ke.
- Extensive testbeam data was aqcuired at CERN in Apr. 97, showing excellent bump-bonding and efficient operation down to depletion depths of ≈ 100μ.
- A second set of tests was performed with baseline n^+ on n-bulk detectors, fabricated by Hamamatsu.
- Four detectors were tested in the CERN testbeam in Sept. 97, and operated efficiently with V(depletion) ≈ 65 V and low bias currents.
- In collaboration with the RD-42 diamond R&D effort, we have fabricated an assembly using a piece of the 600μ D73 diamond detector. It has been bump-bonded by Boeing using their Indium bump-bonding technology. First results will be presented at this meeting by W. Trischuk.

The ATLAS1 Chipset: Definition and Development

Address ATLAS requirements with definition of new chipset

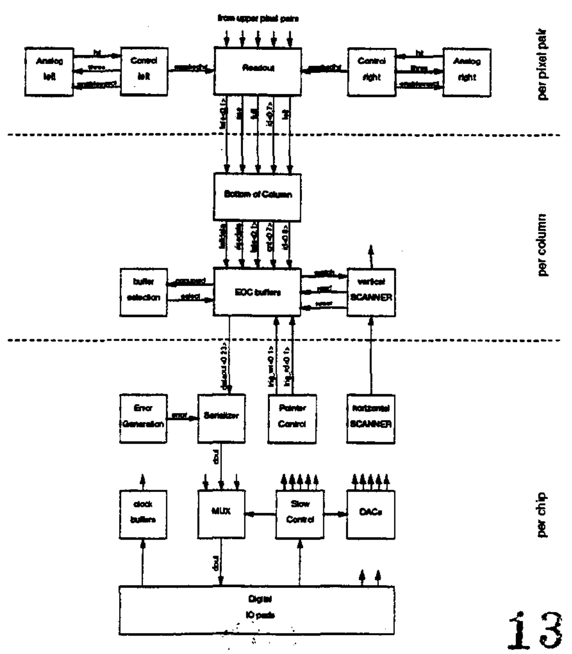
Based on system design concept with novel features:

- All control of the chips involved uses serial command interfaces
- Module interface is three wires: DataIn, DataOut, and Clock
- All fast digital activity uses LVDS drivers/receivers with ≈ ±300 mV swings
- Data (both event and configuration) is output over a 40 MHz serial link
- Module Controller Chip (MCC) drives signals to 16 Front-end chips, collects return data and build events using a star topology for bandwidth and redundancy.



Front-end chip design proceeded in two parallel directions:

- One effort is targeted for the DMILL radhard process, and follows closely the successes of the BP51 chip development (FE-A).
- The other effort is targeted for the Honeywell radhard process, and is based on new developments in the front-end and architecture areas (FE-B).



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Common features of two front-end chips:

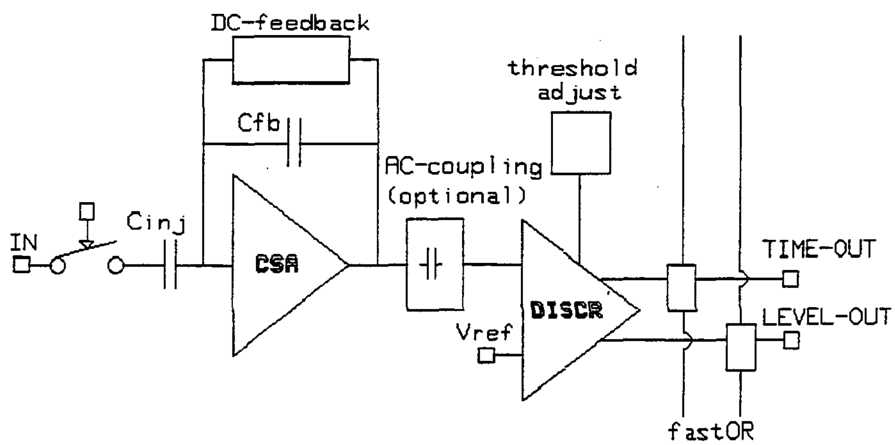
- Two FE designs are "pin-compatible", meaning pin assignments are identical, and they can be operated with the same MCC and test boards, although internal registers and their meanings are somewhat different.
- The geometry is 18 columns of 160 50μ x 400μ pixels with 50μ pitch bump pads. The die size is 7.2 x 10.8 mm, with 2.8 mm for all peripheral logic.
- Front-end biassing is controlled by an internal current reference and up to 8 current-mode 8-bit DACs, with bias points brought out for decoupling/reference.
- The readout architecture is column-pair based, meaning that two adjacent columns share a readout structure and enter a common EOC buffer block.
- The data is transferred from the pixels to the EOC buffers as soon as it is ready to minimize the total deadtime close to that required for the front-end alone.
- A 4-bit trigger number field is used to store up to 16 triggers pending readout.
- The protocol is "data push" where each FE chip receiving a L1 Trigger produces at least one data word. Data is sent out in the order triggers are received.
- The data format includes a 1-bit header and 25 data bits: 4-bit L1, 13-bit Row/Column, and 8-bit TOT, for each hit.
- A serial command processor with simple command format is used to read/write all internal registers. A MUX determines whether event data or register data is returned over the serial link.

Front-End B (HP/Honeywell version)

Front-end design:

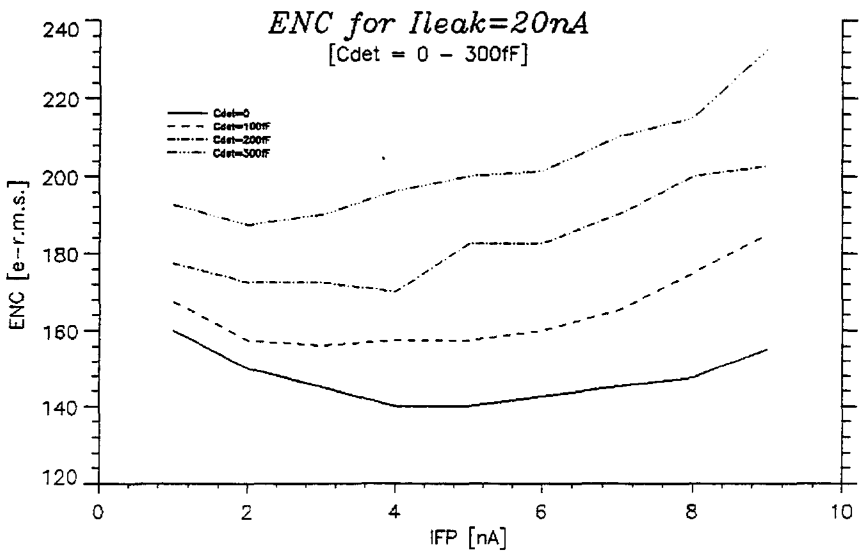
- Basic design uses a fast, high-gain DC-coupled preamplifier, followed by an AC-coupled slower differential amplifier, followed by a dual-threshold discriminator block:

BLOCK DIAGRAM OF THE ANALOG FRONTEND



Preamplifier design details:

- Preamp uses direct cascode for lower input impedance, and has a peaking time of about 30 ns.
- Feedback circuit is based on design of CPPM (L. Blanquart), and uses C(feedback) = 3.5 fF to avoid saturation. This feedback scheme has a very high tolerance for leakage current.



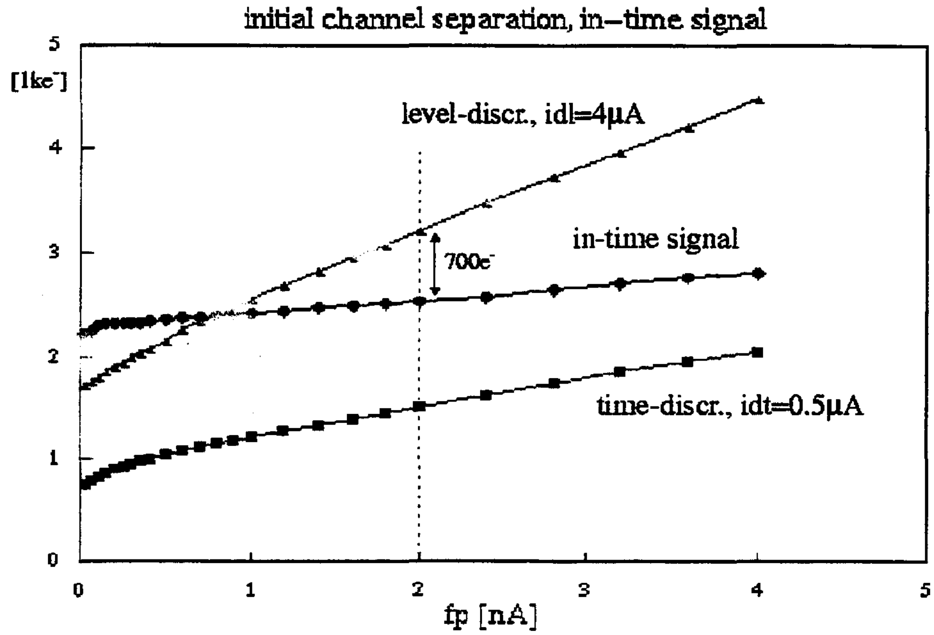
Differential Amplifier coupling stage design details:

- AC coupling uses novel technique to get best possible return to baseline.
- This is followed by a relatively slow (80 ns) but high gain differential amplifier to reduce crosstalk while retaining timewalk performance. The crosstalk suppression arises because the cross-coupled signal from the neighboring channels is faster than the primary signal from the detector. This approach offers reduced power consumption but suffers from greater sensitivity to the preamplifier shaping behavior.
- Threshold control is provided by adjustment of the differential amplifier baseline (coarse control) and by adjustment of the individual discriminator biases (fine control).
- A 3-bit in-pixel DAC is also provided for threshold tuning of individual pixels. The step size of the DAC is adjustable globally.

Dual Threshold Discriminator design details:

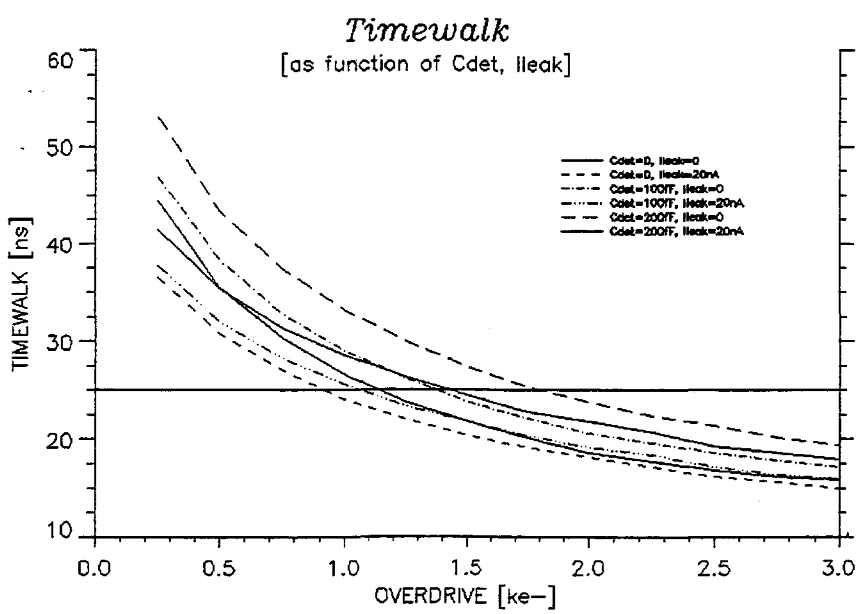
- A dual-threshold discriminator scheme is used to eliminate out-of-time hits, and provide flexibility by decoupling the low threshold required for optimal timewalk from the higher threshold needed for optimal crosstalk and low noise occupancy.

- The idea is that the high threshold is set to optimize noise occupancy and efficiency, and then the lower threshold is set so that its "in-time" threshold is lower than the high threshold, thereby eliminating out-of-time hits.:



Prototype results:

- A series of prototype test chips have been used to evaluate this design (and many variations). The present performance indicates a timewalk of 25 ns is achieved with an overdrive of about 1500e for a 35 µW power budget for the front-end:



- A threshold dispersion of about 300e RMS (before tuning) is achieved.

Command decoder and control features:

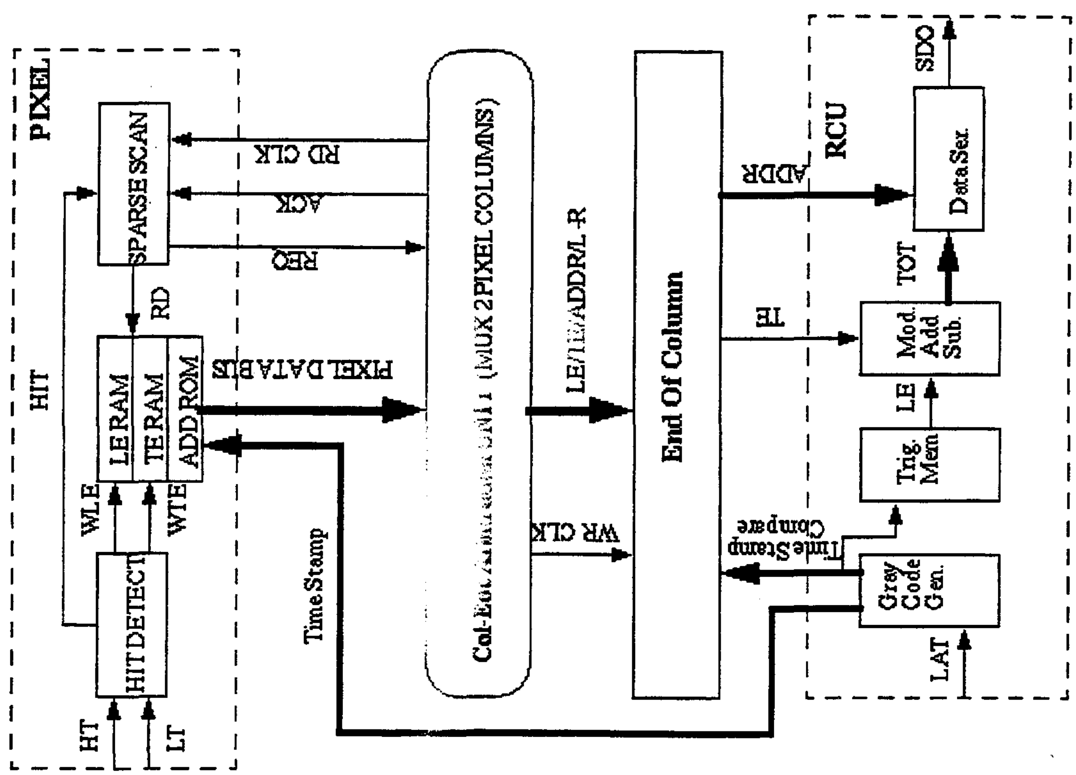
- The chip supports a simple serial protocol for writing and reading the internal registers. Presently, this runs at 1/8 of the full clock speed (5 MHz).
- Command Register includes:
  - → Single Discriminator Mode, FastOR Enable, Preamp Buffer Enable, Analog Injection Enable, Digital Injection Enable
- DAC Register for controlling 8 8-bit current-mode DACs which control biasing for:
  - → Preamp bias, Feedback, AC-coupling bias, Diffamp bias, Diffamp baseline, Dual-discriminator biasses, and step size of 3-bit TDAC. Value of 0 disconnects internal current source to allow external setting.
- Global Register includes:
  - → L1 latency control, DO MUX, Column Clock speed, TDAC values.
- Pixel Register includes:
  - → Select bit for charge injection control, Mask bit for readout control, 3-bit TDAC value.
- Hit Injection:
  - → Can occur digitally at input to readout logic, with pulse width given by external Strobe, analog via an internal VCal "chopper" in the chip periphery, or analog via an external chopper pulsing VCal.
- Monitoring:
  - → Provide two FastOR differential outputs from array, with participation controlled by Readout Mask
  - → Provide single buffered Preamplifier Output.
  - → Provide access to current reference used by internal DACs. Value can be set by external voltage.

Readout architecture:

- Individual pixels contain leading-edge and trailing-edge latches to record a 7-bit Grey code timestamp which associates the hit with a 40 MHz beam crossing.
- A hit is initiated by the leading edge of the low-threshold input. The TOT is determined by the trailing edge of the low-threshold input. The hit must be validated by the presence of a high-threshold input during the period in which the low-threshold discriminator is also turned on, otherwise the hit is reset.
- Pixels operate independently, and transfer their data to the EOC buffers immediately after the trailing edge occurs, over a shared (arbitrated) bus which services the two columns in a pair. The arbitration logic lives in the "bottom-of-column" region between the column and the end-of-column buffers.
- Hits are drained out of the column pair by two parallel ripple-through sparse scan circuits. These circuits use a look-ahead mechanism (10 groups of 16 pixels are scanned in parallel) to achieve a ripple-down time of about 25 ns in a 160 pixel column. This mechanism ensures that the "highest valid hit" in each column is presented for readout to the bottom-of-column arbitration circuitry. A column clock is used to synchronize this activity and eliminate metastable states.
- The EOC buffer block for a column pair contains 20 buffers to store hit information. The leading-edge timestamp, the trailing-edge timestamp, the 9-bit address, and the 4-bit trigger number are stored. Three status FF implement a simple state machine. The states are: Hit, Triggered, Readout Pending.

- The L1 latency is generated by two "offset" Grey counters, one of which supplies the pixel latches (distributed to 2880 pixels !) and one of which supplies the 7-bit comparators in each EOC buffer location. The latency is programmable from 1 to 128 crossings.
- The readout controller circuit keeps track of up to 16 triggers in a FIFO, storing the leading-edge timestamp, and the buffer overflow status bit.
- The overflow flag is a wire-OR of all EOC buffer full status lines, stretched by one L1 latency (the longest period over which an overflow can affect an event). It is transmitted in the End-of-Event word.
- A TOT subtractor unit combines the leading-edge and trailing-edge information, correcting for the latency, and provides the TOT as an 8-bit count.
- Hits are transmitted serially in individual 26-bit packets (1 header bit, 4 trigger bits, 8 row bits, 5 column bits, 8 TOT bits). Significant redundancy allows detection of errors, but no correction is possible. Illegal row numbers (224 and 240) are used to indicate End-of-Event words.
- The data serializer is pipelined to ensure gap-free transmission of the hit packets. A tenth "phantom" column supplies the End-of-Event word in all cases. The generation of an EOE word for every trigger accept is required to simplify event building in the MCC.

Simplified Block Diagram of Readout Architecture:



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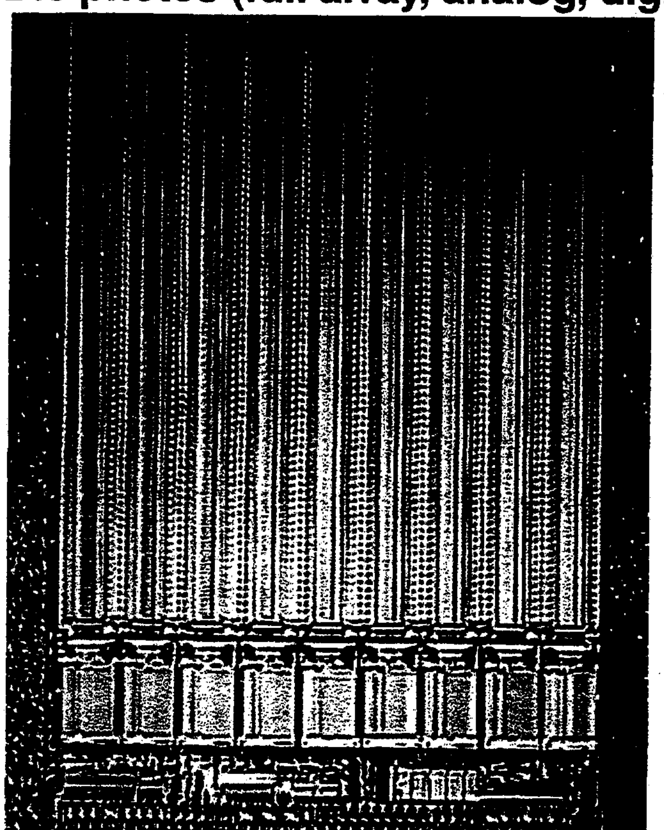
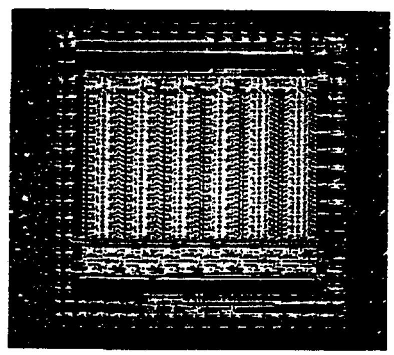
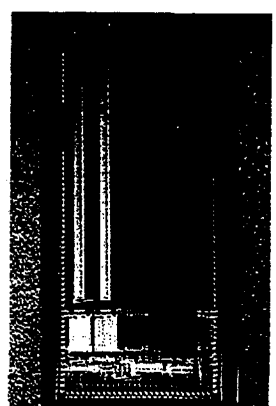
Status (see plots in talk of E. Charles):

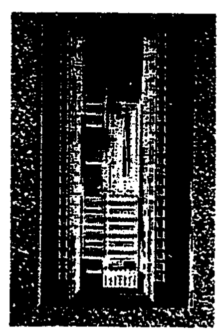
- The complete pixel array was submitted to MOSIS/HP on Feb. 23 for fabrication. The array contains 840K transistors, with about 250 per pixel in $50\mu \times 350\mu$.
- The reticle included:
  - → Two pixel arrays
  - → Analog test chip with 6 columns of front-ends, including biassing and DAC plus current reference circuitry. Many internal signals available, plus can apply capacitive loads and inject leakage currents.
  - → Digital test chip with 2 column pairs and 24 direct injection points to allow parallel load studies of the readout. The complete peripheral logic is included. Many internal nodes are brought out.
  - → A command decoder and I/O driver/receiver test chip.
- The wafers returned on Apr. 17, and die have been tested. Several minor errors were found, but chips perform largely as expected. Power is: DVdd = 50 mW, AVdd+AVcc = 170 mW of which 40 mW is FastOR buffers and 120 mW is pixels.
- Only serious error is a timing problem in the horizontal sparse scan of the EOC buffer blocks, which causes the readout of the last 8 of 18 columns to be unreliable. This means that only 1600 channels behave perfectly on each chip.
- A first wafer was probed earlier this week, with a yield of 81/85 good die (95%), and all 129,600 expected good channels operated correctly under digital injection. Operation at 40 MHz on the probe station, with analog charge injection has been quite successful, with noise levels of about 100e observed. Wafers are now out for bump deposition and flip-chipping, will go to testbeam in June.

Die photos (full array, analog, digital, and command chips):



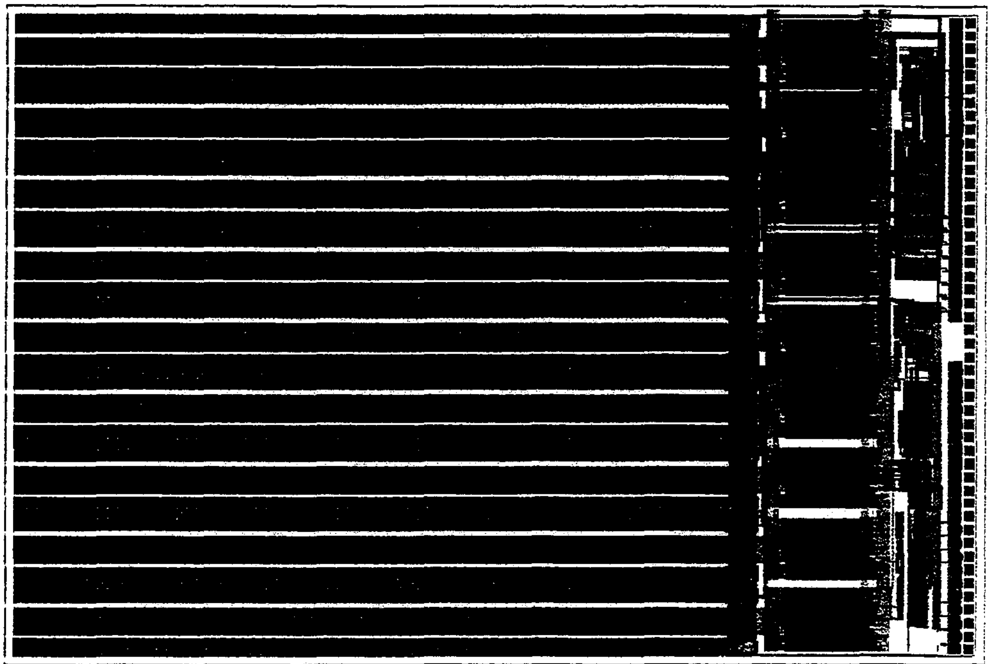






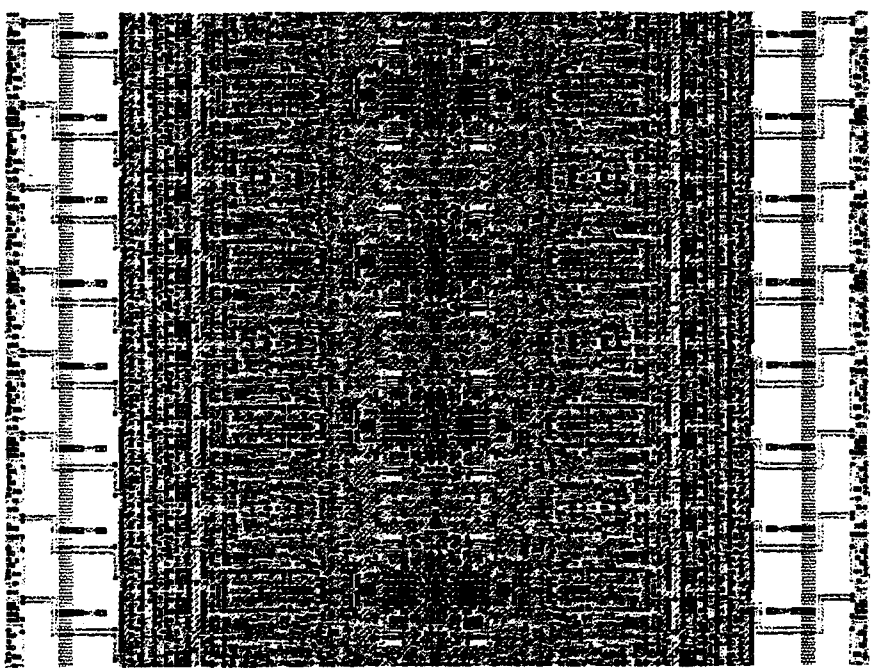
Complete Array

- Complete array includes roughly 837K transistors before merging:



Circuitry in Pixels:

- Analog front-ends, showing connection to digital back-end with empty zone between which contains substrate contact for digital logic:



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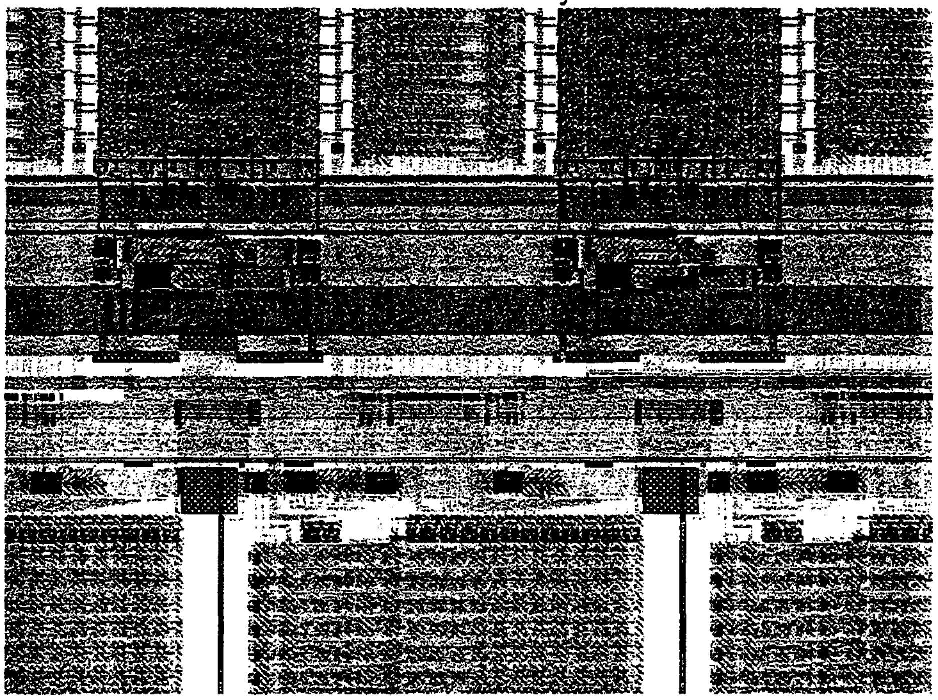
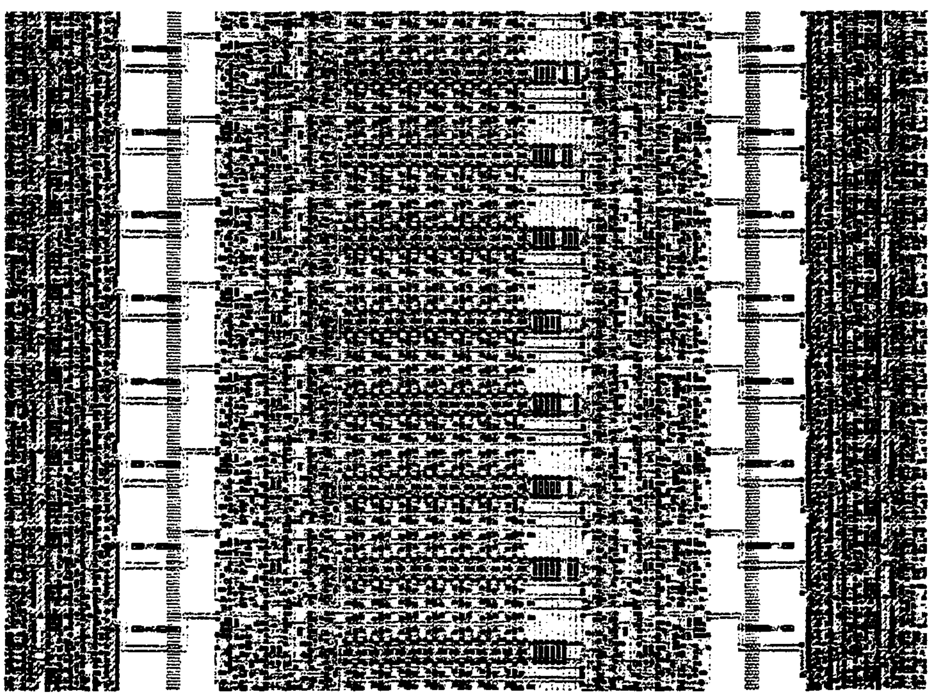
Bottom of Column Circuitry

- Contains active bias buffering and DAC circuitry (one DAC per column pair).
- Interleaving of circuitry: digital connections to pixel back-end are made in M2, horizontal distribution of biasses done in Poly with M1 AGnd shield in between:

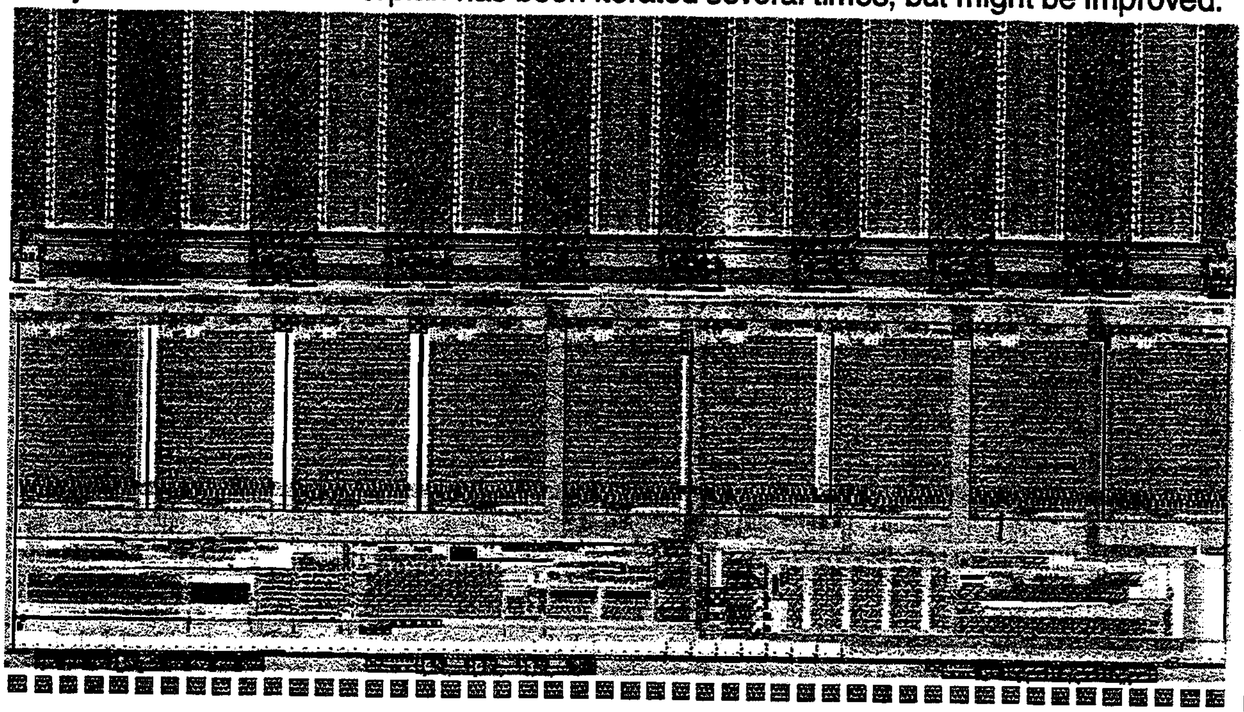


- Digital back-ends, showing extensive bussing to transfer data from pixels to EOC.
- This region is covered by an M3 shield which is brought out on Shield pin.



Bottom of Chip Circuitry

Bottom of the chip is quite full, with many routing details, making further compression very difficult. Present floorplan has been iterated several times, but might be improved:



■ FNAL Pixel Workshop, May 1998 ■

VME-based Test System

High performance chips and modules need a high performance test system:

- Have developed a VME-based readout system, which supports one chip or module per VME card, and is hosted by a PC running LabWindows software.
- High performance "list processor" design, with an "instruction set" which supports basic operations in the system, e.g. FE-CONFIG, INT_DATA, EXT_DATA, etc. A simple linear "program" can be built using these atomic operations, and executed at high speed by an FPGA controller.
- I/O is through large parallel FIFOS, separate for command and data. A large local SRAM is provided to support "hardware histogramming" of the returning data, with one 256-bin histogram per pixel in a FE chip, with ID given by 13-bit Row/ Column. A detailed threshold scan can be performed in well under a minute.
- Provides a simple uniform interface for all control registers and operations in the system (local Control Card, MCC, and FE chips) which use different protocols and speeds.
- Does all parallel-serial conversions, word alignment, and simple data formatting at 40 MHz serial stream speed.
- Supports operation over 25m cable using PECL I/O and local connections using LVDS I/O for wafer probing, lab characterization, and testbeam readout.

Summary

Prototype pixel arrays have been operated at close to ATLAS requirements:

- Two parallel efforts have produced lots of measurements and new concepts, and demonstrated that LHC performance goals do seem achievable.

Realistic ATLAS prototypes are now being tested:

- We should have first operating modules (≈ 46K pixels each) by June 98.
- We expect to learn a great deal from these, particularly concerning the many system integration issues involved in module construction.

Next step is to submit "identical" chips to radhard foundries (both DMILL/TEMIC and Honeywell):

- This will give us experience with complete irradiated assemblies.

A final iteration (ATLAS2 chipset) will be developed before production begins:

- This gives us the opportunity to feed ATLAS1 radsoft and radhard experience into "pre-production" chips.

Real production should begin in 2000-2001...

The Module Controller Chip (MCC) of the ATLAS Pixel Detector

Giovanni Darbo[1], INFN-Genova

on behalf

ATLAS Pixel Collaboration [1]

Albany, Berkeley, Bonn, Dortmund, Irvine, Genova, Marseille, Milano, Nikhef, New Mexico, Oklahoma, Prague, Santa Cruz, Siegen, Toronto, Udine, Wisconsin, Wuppertal

Abstract

The ATLAS pixel detector is organized in 3 barrels and 5 forward and backward discs. The basic building block for each of those detector components is the detector module. There are a total of 2,228 modules, each one having 16 analog Front-End (FE) chips and a Module Controller Chip (MCC). Each module has 61,440 channels and must deal with a complex signal structure: 40 MHz event interaction rate, 75 kHz trigger rate and 2.5 µs trigger latency. The MCC has the main task to coordinate the 16 FE's: it does event building, handles errors and overflows and deals with trigger and synchronization signals. The ATLAS Pixel Collaboration is designing a radiation soft version of the detector module, as "demonstrator" of feasibility, before developing the final version.

This paper describes the MCC architecture and the prototype chip designed for the demostrator.

1. Introduction

The ATLAS pixel detector [2][3] is constituted of 3 barrel layers and of 5 forward and backward disks. Each barrel is organized into staves and each disk into sectors, both of which are in turn composed of modules. A total of 2,228 modules are used in the whole detector.

The read-out of the several thousand pixels hit amongst the $1.4 \cdot 10^8$ channels is a difficult problem.[4] To solve it, ATLAS has adopted a column-based read-out system because of its simplicity, and the high bandwidth operation provided by independent columns. High parallelism is maintained at each step of the read-out architecture together with apprpriate data compression. This is necessary to extract the extremely sparse information in the most efficient way. This read-out system is implemented using a tree-like structure with distributed intelligence at each node.[5]

2. Module

A perspective view and a simplified block diagram of the module are shown in Figure 1 and Figure 2. The two different blocks in Figure 2 are the *Front-End* (FE) chip, which is replicated 16 times, and the *Module Controller Chip* (MCC). The interconnections have been kept very simple, and all connections which are active during data-taking use low-voltage differential signalling (LVDS) standards to reduce EMI and balance current flows. Other signals use full-swing single-ended CMOS to reduce the pin count.

The interconnect topology between the MCC and the 16 FE chips in a module is a star topology using unidirectional serial links. This topology has been chosen to improve the tolerance of the system to individual component failure, as well as to improve the bandwidth by operating the serial links in parallel.

The ATLAS Pixel Collaboration is currently designing a "detector module demonstrator" which implements the final functionality required for the experiment, but with two main exceptions: it has slightly larger pixel cells (400 x 50 µm^2 instead of 300 x 50 µm^2), to leave adequate room for diagnostic and control logics, and it has electrical instead of optical inputs and outputs. In addition, the chips on the current built module are designed in radiation-soft technology.

[1] e-mail: darbo@genova.infn.it

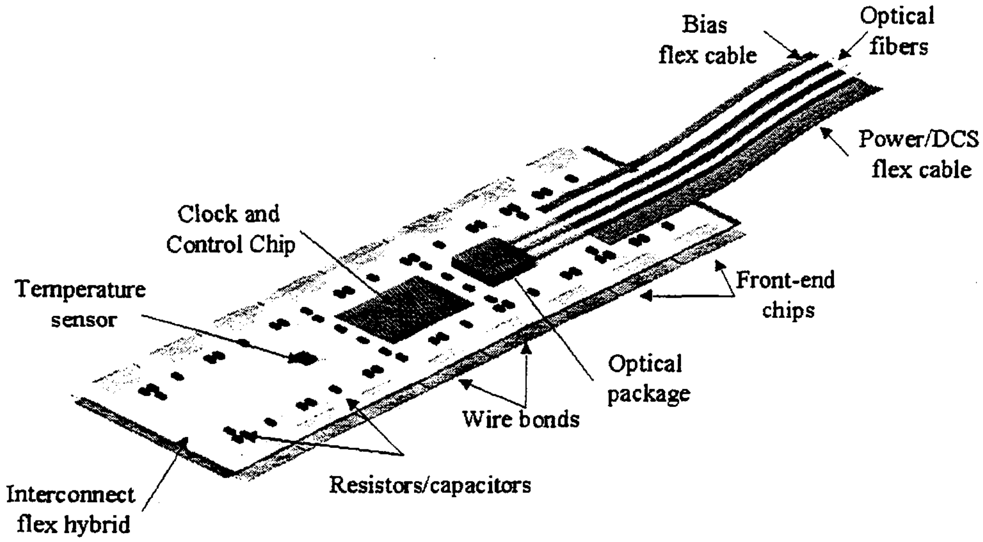


Figure 1: Perspective view of a detector module.

The prototyping effort for the demonstrator is being pursued with the aim of providing two front-end chip designs in rad-hard technologies using two different vendors, according to the official ATLAS policy for rad-hard electronics development. The two front-end designs (FE-A and FE-B) differ in many internal details, but are intended to be "functionally pin-to-pin compatible", so that modules can easily be built with either front-end chip and comparatively tested.

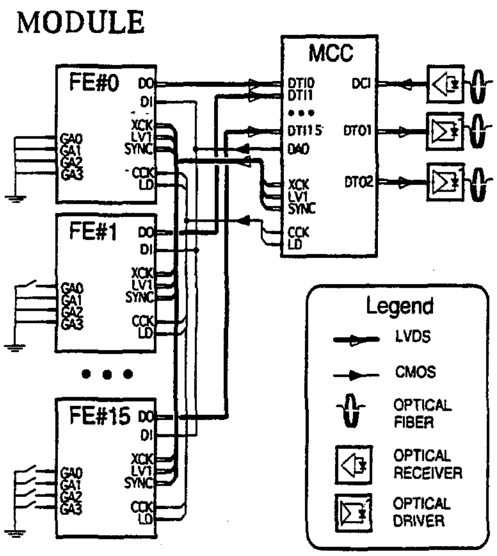


Figure 2: Module block diagram

Both FE chips have 18 columns (will be 24 with the pixels shrinking to 300 μm) and 160 rows of pixel cells. Every second column is mirrored and the architecture for the *End-of-Column* (EoC) logic is organized for a column pair. Both pixel front-ends will provide modest digital information using a time-over-threshold (TOT) front-end design, and digitizing the charge information in units of the 40 MHz beam crossing rate.

3. MCC System Architecture

The MCC has 3 main functions: event readout and building, FE chip configuration and trigger and timing distribution to the FE chips.

3.1. Event Readout and Event Building

The first significant event building occurs in the End-of-Column (EoC) logic on the Front End chip, where data are organized into events labelled by 4-bit trigger numbers. These events are then pushed from the FE chips to the MCC as soon as each FE chip has a complete event. The MCC collects the parallel data streams from all of the FE chips and performs real event building. It then transmits these events to the ROD (Read Out Driver). The final event building tasks is left to the ROD's, where power and space are not as constrained as they are on the detector.

The End-of-Column logic receives input from a pair of pixel columns. All pixel hits are stored in the EoC buffers until a level one trigger (LV1) coincidence is performed. After that, only hits associated with a triggered beam crossing are kept and are transferred off the FE chip into the MCC. These basic operations, namely hit storage, LV1 trigger coincidence, and event readout, must be simultaneously performed by the EoC logic in order to prevent generating significant inefficiencies. Each FE chip uses a 4-bit trigger number to uniquely label events which are awaiting readout into the MCC. The MCC has the ability to suppress additional LV1 trigger signals if the number of LV1 triggers sent to the FE chips exceeds *n* (where *n* can be programmed from 1 to 15). This number represents the maximum number of events that a single FE chip can store.

The high luminosity of LHC forces an "*as-quickly-as-possible*" *approach in getting data* transferred from hit pixels to the End-of-Column buffers. This process causes data entering the EoC buffers to become somewhat scrambled, and will therefore no longer be organized sequentially into events. Hence this buffer will not behave as a FIFO, and data from a given event will not be stored contiguously. It becomes therefore necessary to scan the EoC buffer pool in order to find the next free location prior to writing new data. The buffer pool has also to be scanned a second time to find all the hits corresponding to a given event in order to provide the MCC with data ordered by event.

Event building is performed by two concurrent processes running in the MCC. The first (*Receiver*) deals with the filling of the 16 input FIFO's with data received from the corresponding FE chips, while the second one (*Event Builder*) extracts data from the FIFO's and builds up the events. Each FE chip sends data as soon as they are available with two constraints: event hits must be ordered by event number and for each event an `End-of-Event` (*EoE*) word is always generated. *EoE* is also sent for the case of an empty event to keep event synchronization.

Each time an *EoE* is received by a *Receiver* in the MCC this information is stored in a "score board". Therefore the *Event Builder* knows exactly when to start the event building by checking the "score board" which keeps track of which events are completely

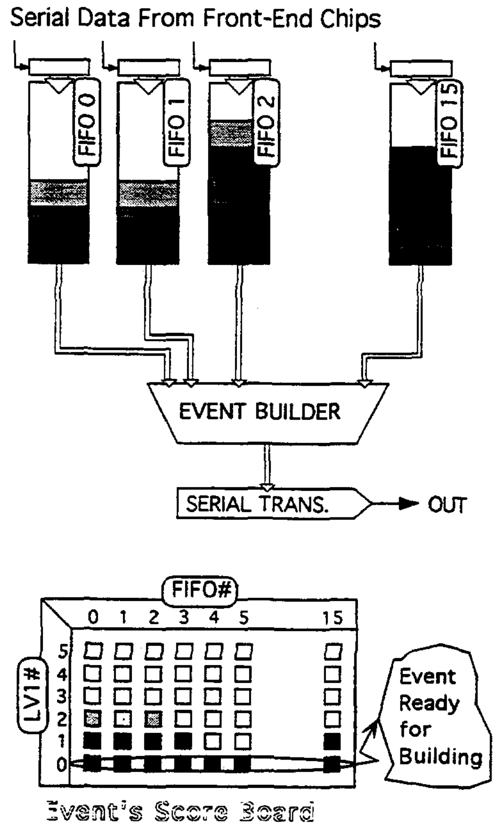


Figure 3: Event "Score Board" used in the MCC for event building.

stored in each of the 16 input FIFO's. When an event flagged with LV1 number *n* is ready in all the FIFO's the *Event Builder* process takes all the hits from FIFO#0, appends them to that of FIFO#1, and so on up to the last FIFO#15. At the end of this process the corresponding "score board" entry is erased. While the *Event Builder* fetches the hits out of the FIFO's, the MCC transmits them upstream to the *optical encoder*. The event number is removed from each hit and sent only once, together with the FE chip addresses, to the ROD. The event building score board is sketched in Figure 3.

The block diagram of Figure 4 is an expanded view of one of the sixteen FIFO's of Figure 3. During normal conditions, the RECEIVER fills data into the FIFO. When an *EoE* word arrives, CTRL copies the contents of W.PTR (Write Pointer) into L.PTR (Last Pointer). When the Event Builder finds that an event is completely received from all of the 16 FE chips

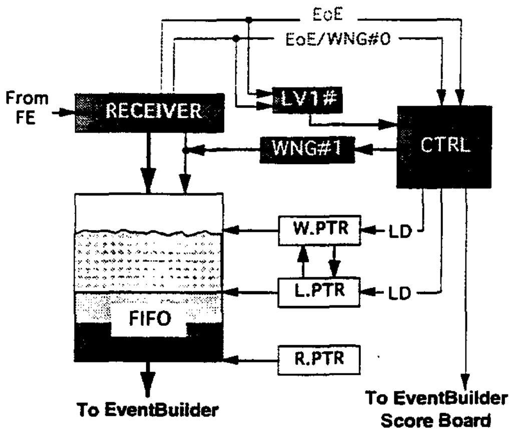


Figure 4: Event readout: Front End RECEIVER and input FIFO.

(*Event Builder* knows from the scoreboard about the existence of complete events) it starts fetching data. After every FIFO read operation its R.PTR is incremented. R.PTR will never overtake L.PTR and the *Event Builder* can start processing the next FIFO once it finds an *EoE* in the data.

The MCC is able to handle both warning and error conditions during event building. A `warning` occurs when there is a condition which causes a partial event loss. An `error` is a destructive condition that cause the loss of one or more events until the MCC recovers. Both `warning` and `error` conditions are flagged in the output data stream. Due to the data push architecture, the overflow of an input FIFO could always occur: the mechanism the MCC uses to resolve such a condition is to issue a `warning` or an `error` condition.

3.2. System Initialization and Configuration

Front end chips and MCCs must be configured after power up or before starting a data taking run. This is done by a system initialization procedure. To write or read configuration data to/from the FE chips, two levels of addressing are necessary:

1. The data path to the given module must be selected.This is done by selecting the I/O port on the ROD corresponding to the module on which the target FE chip resides. The ROD uses point-to-point links to the MCC's for both input and output connections.
2. The FE chip must be addressed. This is done by the FE chip itself, which recognizes its geographical address in the Command plus Address field of the message. Once the address is recognized, the remaining data stream will be used by the FE chip either to execute the command or to upload/download internal registers. Since all of the information going to the FE chips must pass through a MCC chip, the MCC must recognize whether the data is for its own use or must be transferred to the *MCC-DAO* (Data Address Out) pin of the FE port, which is connected to the FE chip inputs (see Figure 2). This is done by looking at the secondary address field present in the header field of the message.

Data streams sent to (or returned from) the FE chips have variable length. When writing, this length must fit the size of the relevant internal FE registers. To ease the FE chip design for the demonstrator chips, configuration data are transmitted at a reduced 5 MHz bit rate, using the *MCC-CCK* clock, instead of the 40 MHz used for event readout. Experience will tell us whether this can be eliminated in the next generation of chips.

To simplify the control decoder the *MCC-LD* signal is used to distinguish, in the bit stream from the *MCC-DAO* pin, the address plus control words from the subsequent data words.

The MCC architecture foresees up to 16 general registers which can be written and read back during system configuration. Two of them are used to define the length, respectively of the `data` and of the `control` part, in the bit stream which will be sent to the FE chip. The MCC registers support both system control functions and access status information that is particularly useful at debugging time.

3.3. Trigger, Timing and Control

During normal operation, the on-detector electronics of the pixel system needs a precise timing signal (XCK - Bunch Crossing Clock) and a trigger signal (LV1 - Level 1 Trigger). In addition to those two signals several control commands are understood by the system. The main signals are:

- XCK (Bunch crossing clock)

  This is the clock seen by the FE chip on its *FE-XCK* input line. XCK is generated from the 40 MHz clock signal received by the MCC through the *DCCI* input pin. The 40 MHz clock signal and *FE-XCK* both have the same frequency as the LHC machine clock. Each detector module uses the same 40 MHz clock, but a small phase

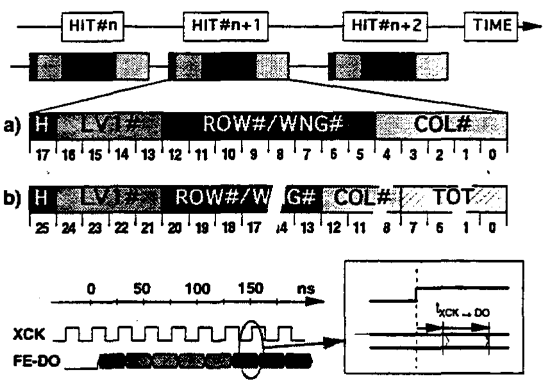


Figure 5: Hit Data format at the input of the MCC. Case b) illustrates the Time over Threshold encoding.

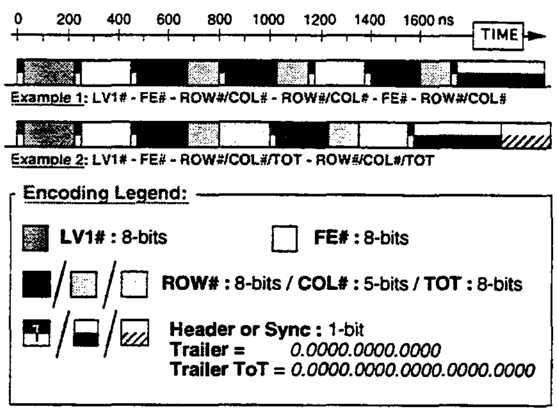


Figure 6: Event Data format at the MCC output. Example 2 illustrates the case of Time over Threshold encoding.

difference can be programmed in the ROD to take into account timing differences. The XCK signal is used by pixel Front End to latch and associate track hits to a particular bunch crossing number.

- LV1 (Level 1 Trigger)

  This signal validates the rising clock edge of the bunch crossing clock (*FE-XCK*) for those crossings that have been accepted by the level 1 trigger system. The serial control protocol is used to transmit the LV1 command from the counting room down to the MCC, where it is received serially encoded on the *MCC-DCCI* pin. Once received by the MCC this signal is decoded by the *Command Decoder* inside the MCC and distributed to all the FE chips. One of the features of the MCC is the ability to generate a pattern of contiguous LV1 Accept signals to allow possible multi-crossing read-out, both for diagnostic and timing initialization, and to allow for the possibility that all of the interesting hits may not be available in a single beam crossing. Hits belonging to triggered bunch crossings cause data to be stored by the End-of-Column logic in the FE chips and subsequently pushed to the MCC. The MCC puts together hits from the same event and pushes them to the ROD's.

- SYNC (Event Synchronization)

  This signal is used to automatically re-synchronize all FE chips in a module in case of error conditions. The MCC can generate this signal autonomously whenever the particular module is empty, or when it detects an error condition. It can also receive a SYNC command from the ROD. In the first case all the FE chips on the module controlled by the MCC which issued the SYNC reset their internal LV1 counter and delete any pending triggered event. The FE chips will then resume data taking and pushing as soon as they see the next LV1 signal. In a similar way, all MCC's respond to a SYNC sent by the ROD by resetting all FE chips connected to them and resetting the LV1 counter and data inside the FIFO's once as many pending events as possible have been reconstructed. The MCC then sets a warning condition in this events data streams.

- Slow Commands

  These commands are used to program the MCC or the FE chips in a particular module. When one of these commands is issued, the pixel system is taken out of data acquisition mode, and command operations like system configuration or read/write operations can be executed at any level of the hierarchy. There is a Data-Take command in order to resume data taking.

4. Data Formats

Data will be transmitted from the FE chip to the MCC using a simple protocol in which each hit is transmitted in a stream of 18 bits (26 if the optional Time-over-Threshold (ToT) information is produced): 1 header bit, 4 LV1 bits, 8 row number or end-of-event/warning bits, 5 column number bits and 8 optional ToT bits. Individual hits can be separated by any number of zeroes in the data stream. The average occupancy of the link is expected to be fairly low. This, together with the encoding scheme described here, permits automatic recovery after data transmission errors, so long as a gap longer than 18 (or 26 in case the ToT option is selected) bits appears in the data stream. The data encoding and transmission is represented in Figure 5.

The format of the event generated by the MCC is made of ordered fields separated by synchronization bits ("1"), starting with a header ("1") and ending with a trailer ("100 0000 0000 0000"). The header is to "wake up" the receiver from the idle condition when no data are transmitted, while the synchronization bits together with the trailer are used to define the end of event. The trailer has been chosen to be a pattern that can never occur in the data stream, due to the insertion of synchronization bits. The format always requires a LV1 number at the beginning followed by a sequence of FE chip numbers, followed by any number of hits (row plus column or row plus column plus ToT when this option is selected) interrupted by a new FE chip number plus the sequence of hits. Warning and error flags can be introduced in the event format. An example of such a format is given in Figure 6.

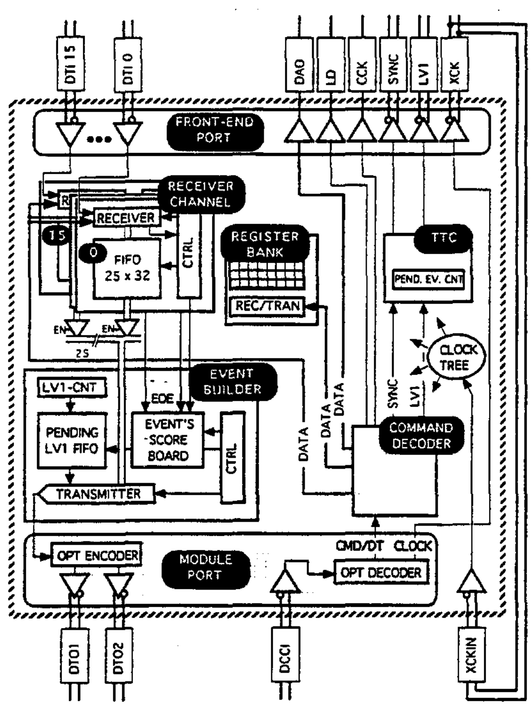


Figure 7: MCC Block Diagram.

5. MCC Architecture Implementation

The MCC architecture is shown in the block diagram of Figure 7. The blocks represented are:

FRONT END PORT: (I/O to the FE chips)
This module performs all of the interface functions between the FE chips and the MCC.

RECEIVER CHANNEL: (Front End receiver)
This block includes the 16 derandomizing FIFO's (one for each FE chip output), made with a full custom memory of 32 25-bit long words with arbitration logic and read/write pointers, and the FE receivers and the state machine running the interface to the FE link. FIFO overflows are handled by this block.

EVENT BUILDER:
A scoreboard keeps track of complete events read by each FE chip. Once all 16 FE chips have sent a complete (even empty) event, the *Event Builder* sorts, formats and prepares the event stream to be transmitted to the RODs once encoded by the *Module Port*. Errors at the level of event building are dealt with by this block. Both `error` and `warning` conditions are added in the output data stream if necessary.

REGISTER BANK:
The MCC architecture provides up to 16 general purpose registers, only 11 of which have been implemented in the demonstrator MCC. As an example, a register is used to mask one or more input lines coming from FE chips in case of failure. Two special registers contain the bit length of commands and data to be written to the Front End chips as these quantities may vary each time a FE chip is accessed.

COMMAND DECODER:
This block decodes all commands sent to the MCC. The LV1 trigger command (fast command), as well as read/write operations to internal MCC registers or to FE chips (slow commands) are amongst the commands interpreted by this block.

TTC: (Trigger, Timing and Control)
This block generates the LV1 trigger to the FE chips. It has the ability to block LV1 accepts to all of the FE chips on a module if there are too many LV1 events still to be transmitted to the MCC. This block therefore keeps track of all LV1 signals sent to the FE chips and all the Event-Done signals received by the Event Builder. One of the functions of this block is to deal with the automatic Sync signal programmable into the MCC or received by the RODs via a dedicated command.

MODULE PORT: (Interface to the ROD's)
This module performs all of the interface functions between the MCC and the RODs. Clock and serial commands are decoded and sent respectively to the *Clock Tree* and the *Command Decoder* block. Outgoing signals are encoded with the clock and are sent out on *MCC-DTO1* and *MCC-DTO2* pins according to bandwidth requirements. Bandwidth requirements predicate the use of three optical fibres.

CLOCK TREE:
Once the clock has been decoded by the *Module Port*, it must be distributed to the whole module. In order to minimize clock skew between the MCC and the FE chips, the MCC generates the clock and latches all input/output data with this clock signal. This signal is then sent to all the components of the module via the *MCC-XCK* output pin. The MCC itself will use this distributed clock for all its internal operations.

The MCC chip will be fabricated in rad-hard technology using the DMILL 0.8 μm double metal CMOS process. To minimize the risk of errors in the rather complex MCC design, a top-down design methodology has been used, using standard cells with logic synthesis from a high level Verilog description. The only full custom parts of the design will be the 16 FIFO's, the LVDS I/O drivers/receivers and the Bi-phase Mark Encoding and Decoding blocks, which do not exist in the DMILL standard cell library.

6. MCC for the ATLAS "Demonstrator"

Since the demonstrator module does not have optical links, the main differences between it and the final version are the absence of the Bi-phase Mark Encoding and Decoding blocks which will be added to the Module Port (see Figure 8). Another difference is that this version of the chip has been produced in rad-soft technology using the AMS 0.8 μm double metal CMOS process.

Due to the complexity of the circuit a top-down design methodology has been chosen. The whole design was first coded in Verilog at a behavioural level, and then mapped to the 3.3 V, 0.8 μm CMOS AMS standard cell library using a logic synthesis tool (Synergy), with the exception of the full-custom blocks. After hand-positioning the custom blocks, the layout was made with an automated place and route tool. The final steps of this process were the layout versus schematic comparison and the design rule check. The whole design was made using the Cadence Design Framework. Figure 11 presents the final

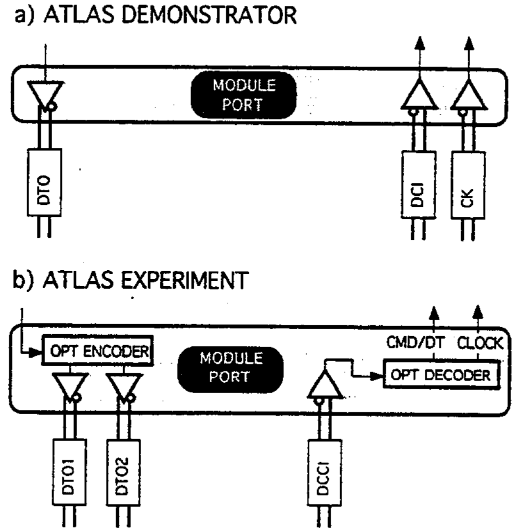


Figure 8: Difference between the "Demonstrator" MCC (a) and the MCC which will be designed for the experiment (b), The final chip will receive clock and data encoded on a single fiber (DCCI), while two output fibers will be used to increase the bandwidth (DTO1 & DTO2).

layout with the main building blocks highlighted. Approximately half of each receiver channel foot print is occupied by a FIFO.

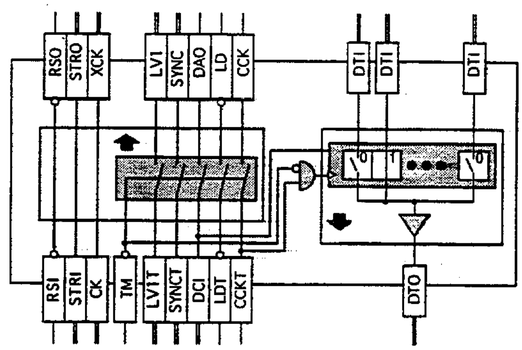


Figure 9: Block diagram to illustrate the "Transparent Mode" operation of the MCC.

Since the 16 FE chips in a module will be accessed through the MCC by a rather complex protocol, we have added a "Transparent Mode" of operation to the MCC. This mode requires the addition of several pins and a small amount of logic, but allows transparent access to all input and output pins of the 16 FE chips. This operational mode bypasses all of the MCC

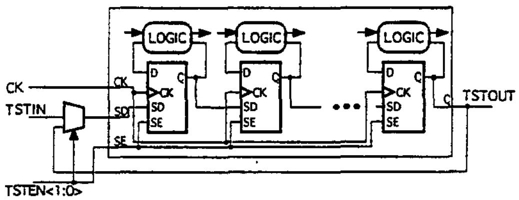


Figure 10: Scan chain to access in read and write mode MCC internal flip-flops.

functionality and directly connects all data, control and timing signals going to (or returning from) the FE chips with corresponding externally accessible pins on the MCC.The Figure 9 shows the implementation of the "transparent Mode" in the MCC.

The MCC has additional pins which can be used to put the circuit into test mode and increase the accessibility and observablity of internal nodes. In this test mode all the internal flip-flops are configured as a shift register, see Figure 10, which allows both reading and writing the MCC internal state. This mode will be used to test the chip on a probe station before mounting it in the system.

The MCC has 60 signal pins, and with the inclusion of power and test signals, there will be a total of 81 pins on the chip die. The chip area is 67 mm^2 and has approximately 430,000 transistors. The design will not be optimal in its area and power consumption, but this approach provides the safest route to produce the MCC prototype on this short time scale.

The MCC is in fabrication in an engineering run, and we will receive functionally-tested chips, in order to facilitate the assembly steps of the whole module. A first test of the whole module should take place in August 1998 in the CERN H8 test beam.

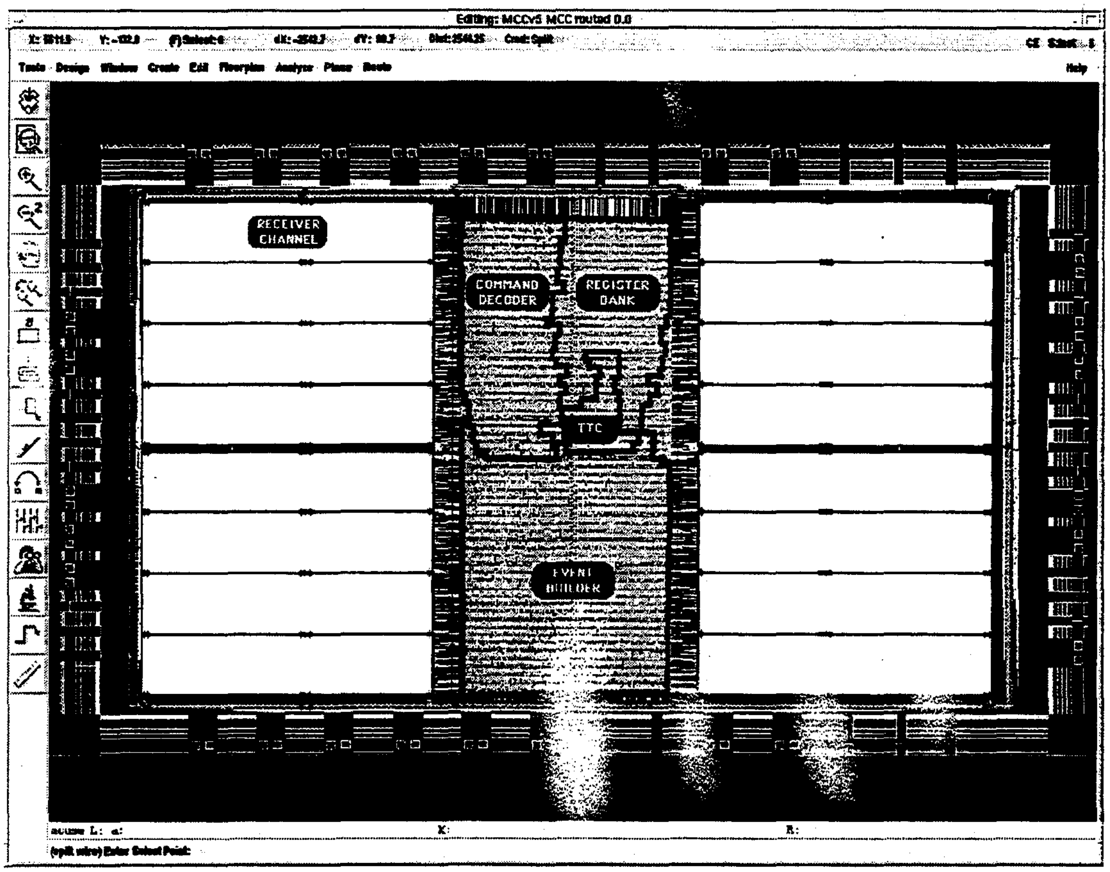


Figure 11: MCC layout. The different functional blocks have been highlighted.

Aknowledgments

I wish to thank the co-authors of the MCC demonstrator chip design: R. Beccherle, G. Comes, G.Gagliardi, G. Meddeler and P. Musico.

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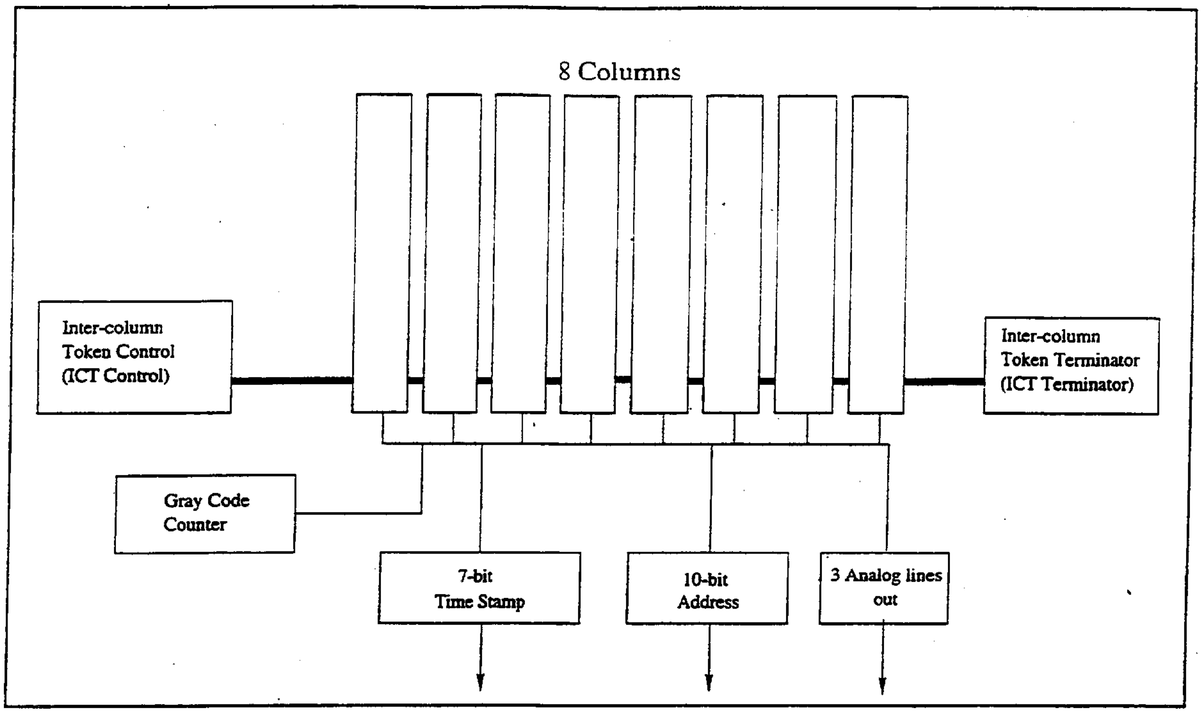
BFE 168
Chip Level Diagram

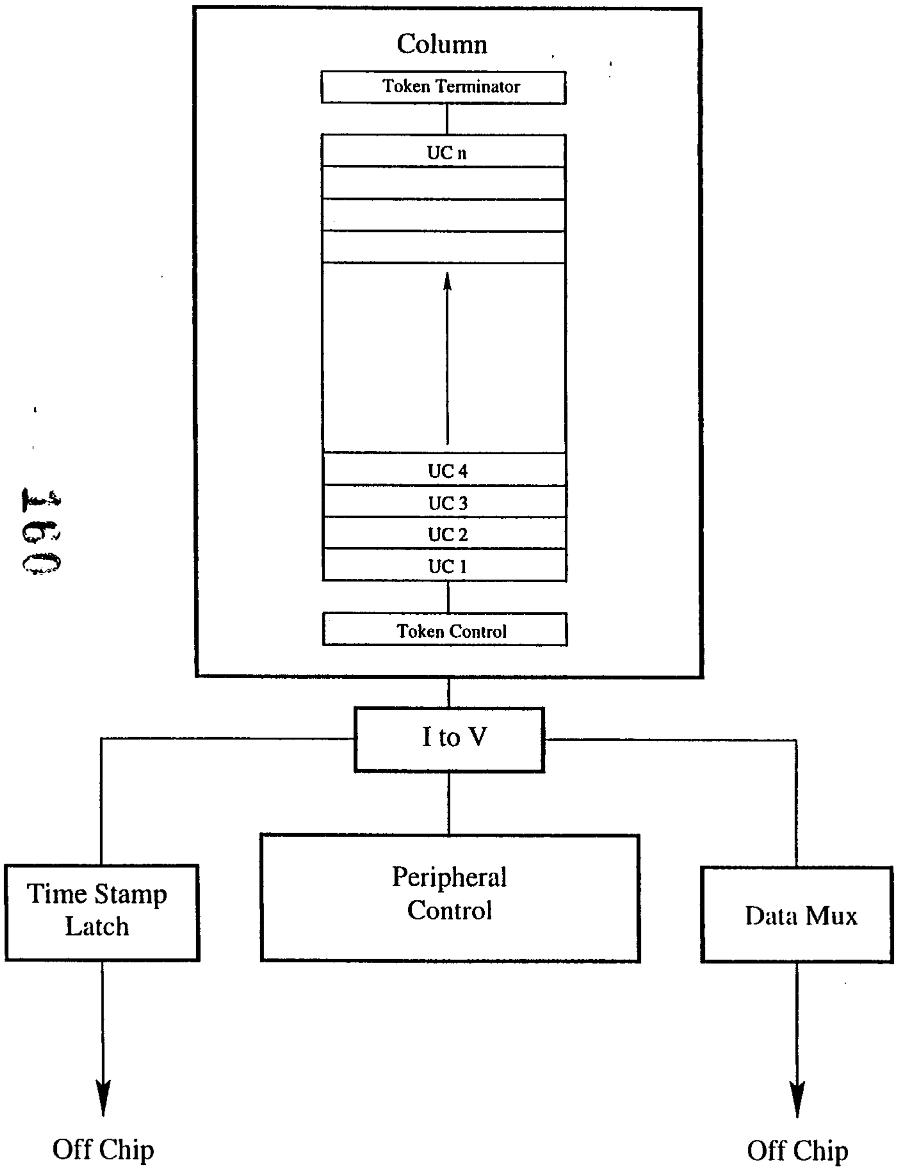


Results from a Pixel Readout Chip for CMS

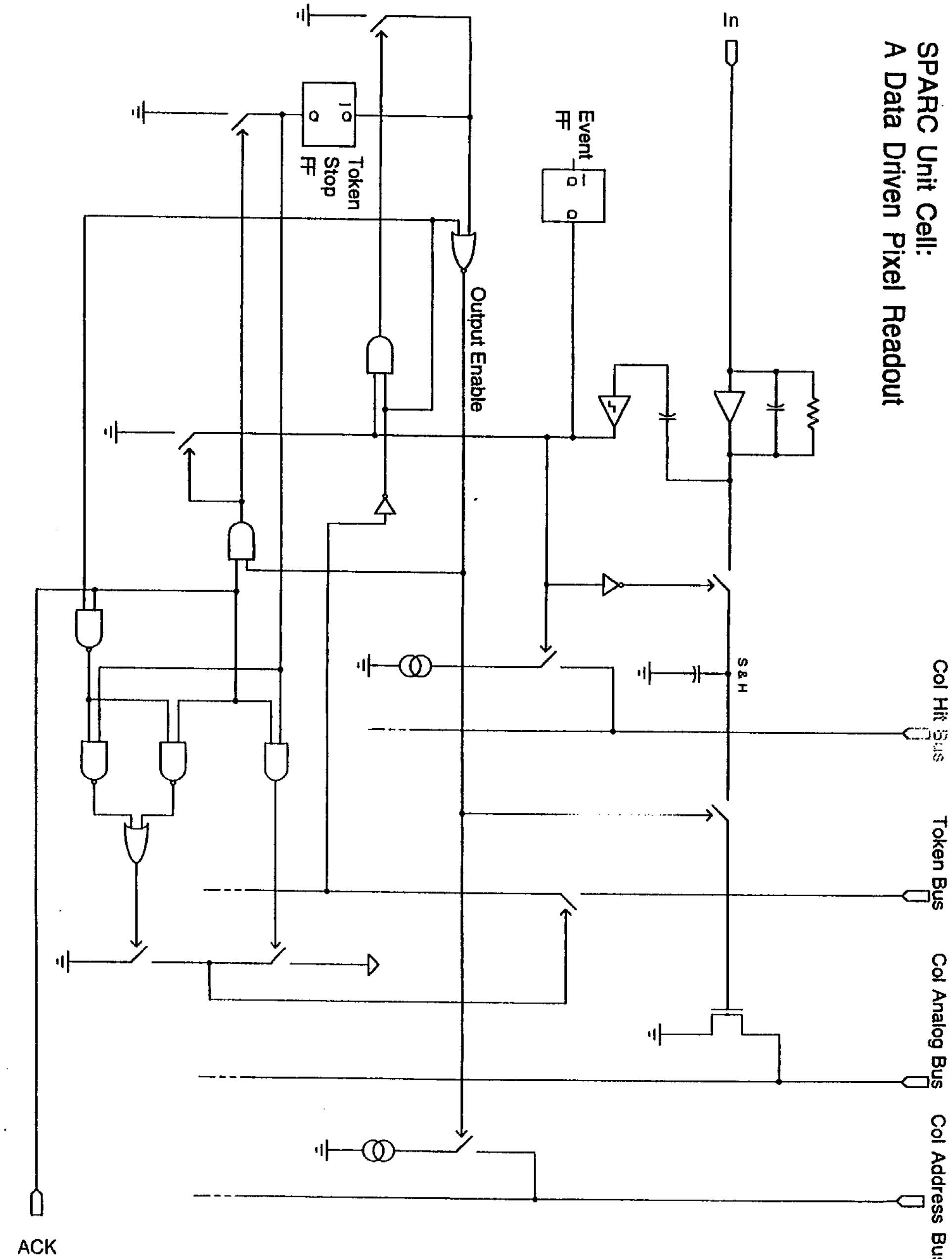
Gary Grim

UC Davis

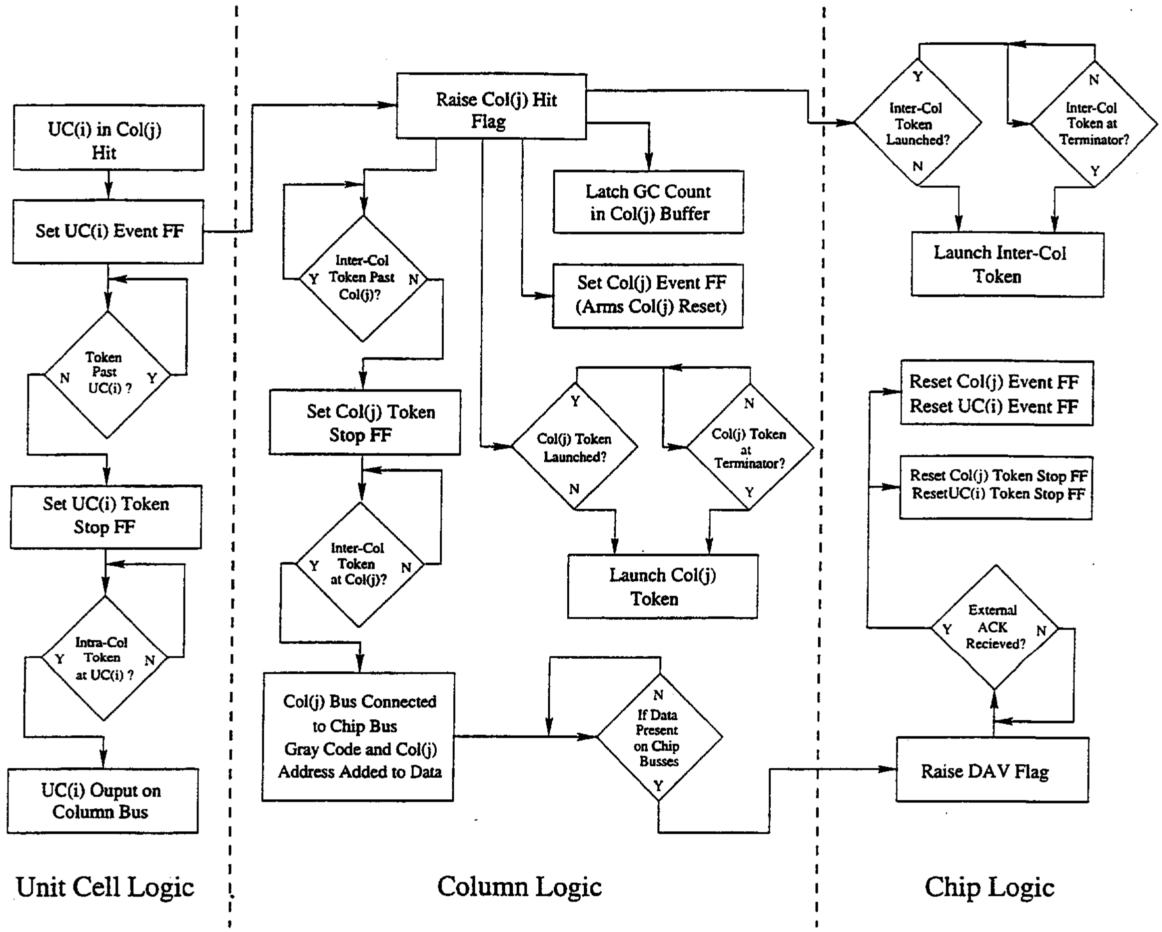
Column Block Diagram



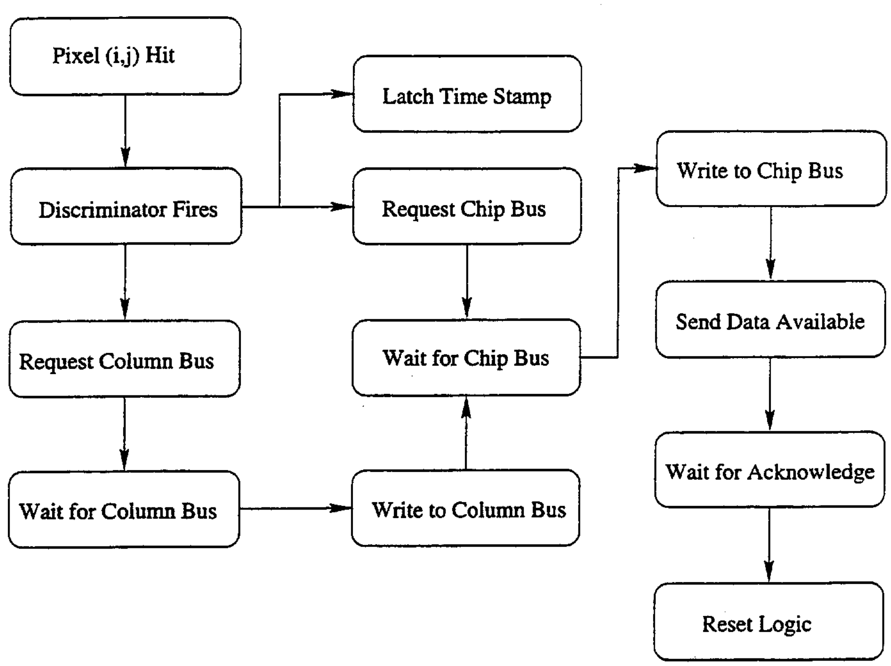
SPARC Unit Cell:
A Data Driven Pixel Readout



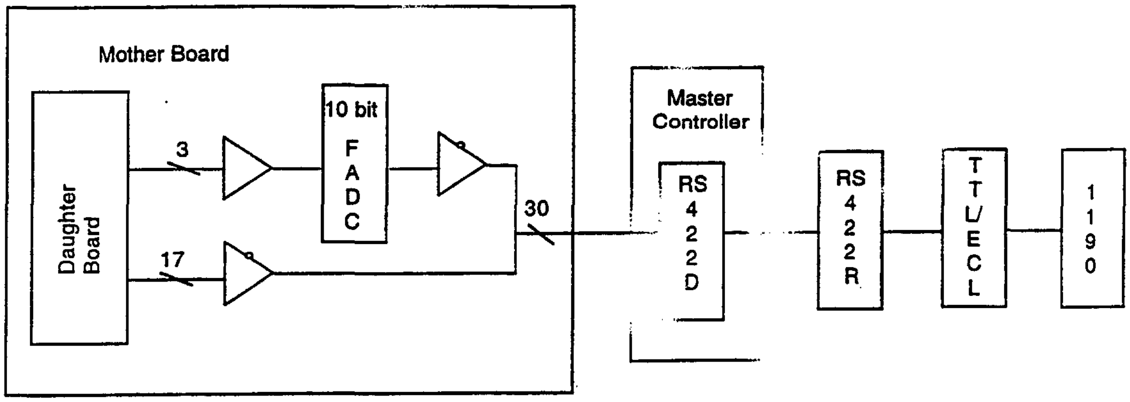
BFE-168 Readout Logic

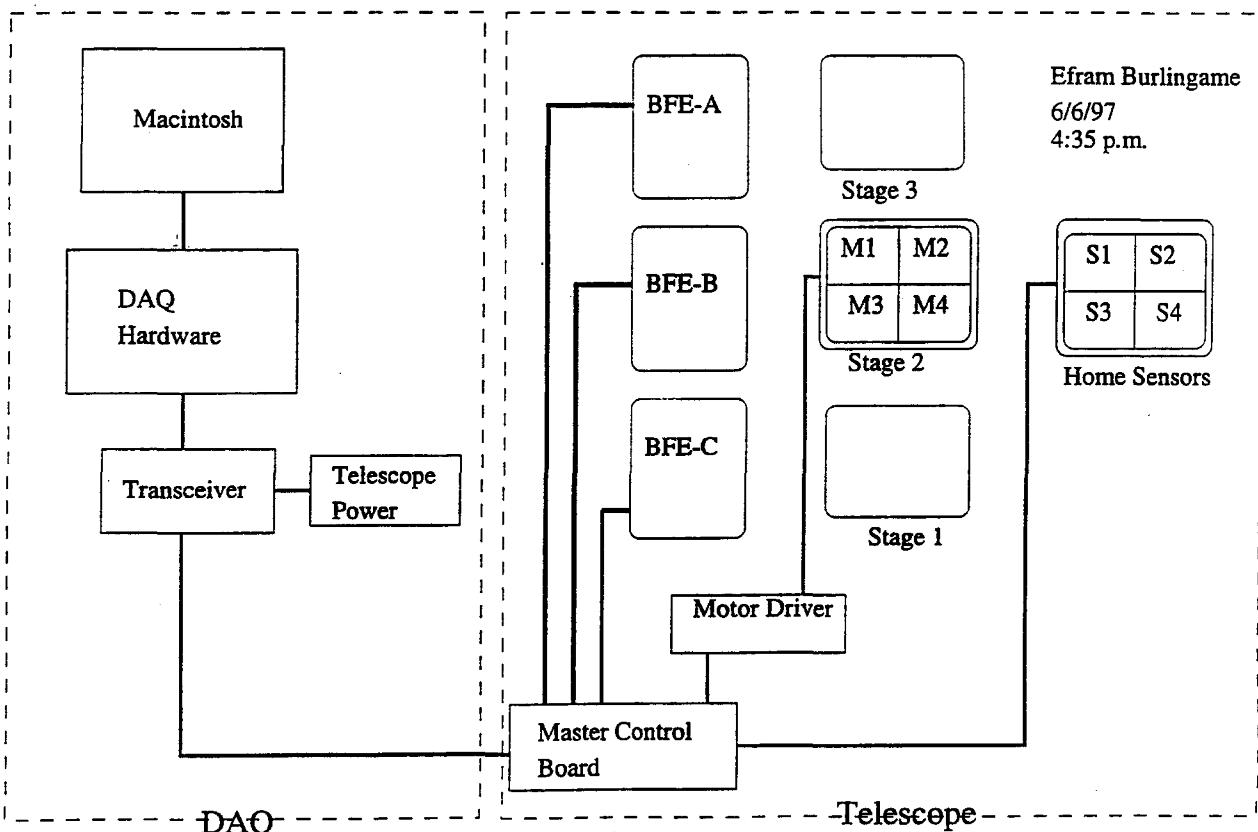


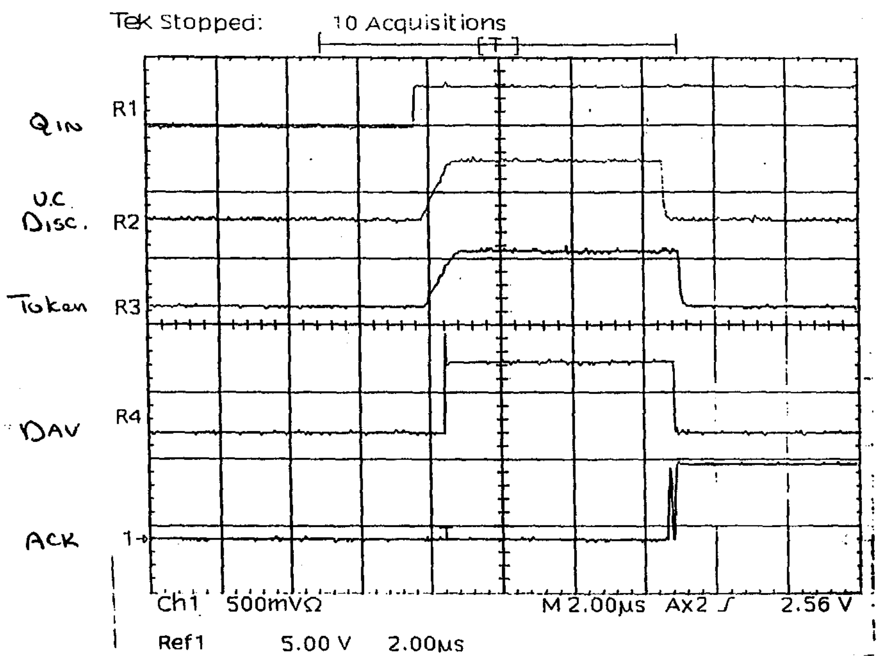
BFE-168 Data Flow



Data Path


Mother Board
Daughter Board
3
17
10 bit
FADC
30
Master Controller
RS 422D
RS 422R
TTL/ECL
1190

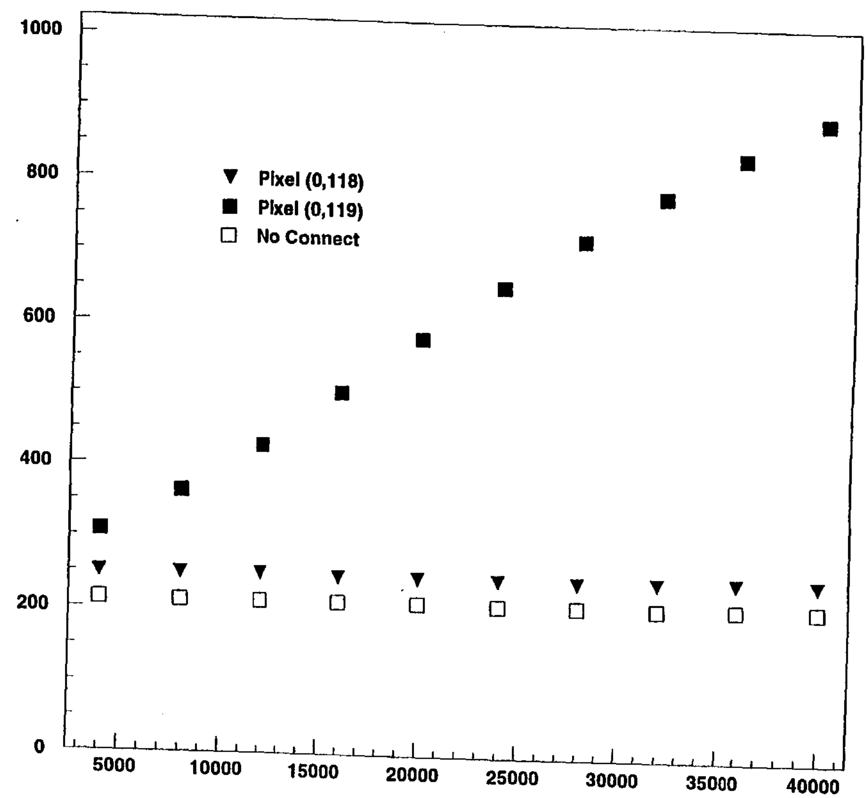

Macintosh
DAQ Hardware
Transceiver
Telescope Power
BFE-A
BFE-B
BFE-C
Stage 3
M1
M2
M3
M4
Stage 2
Stage 1
Efram Burlingame
6/6/97
4:35 p.m.
S1
S2
S3
S4
Home Sensors
Motor Driver
Master Control Board
DAQ
Telescope

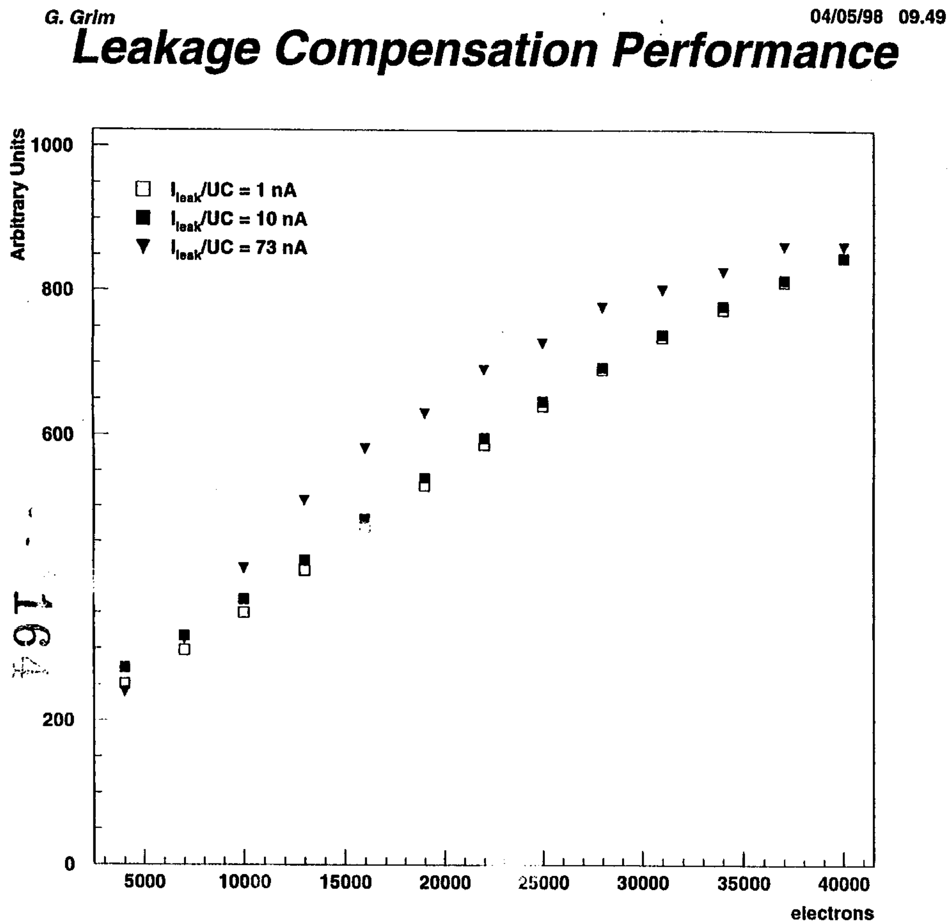


G. Grim

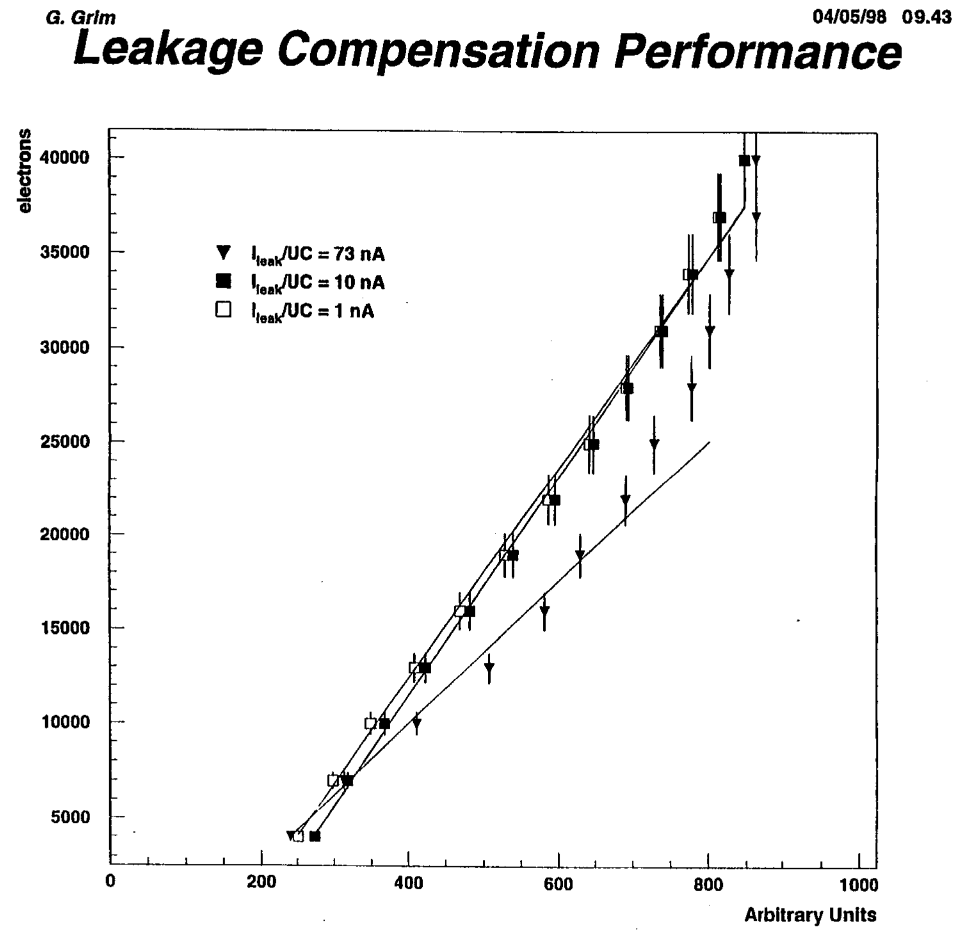
05/05/98 08.26

BFE-168 Performance





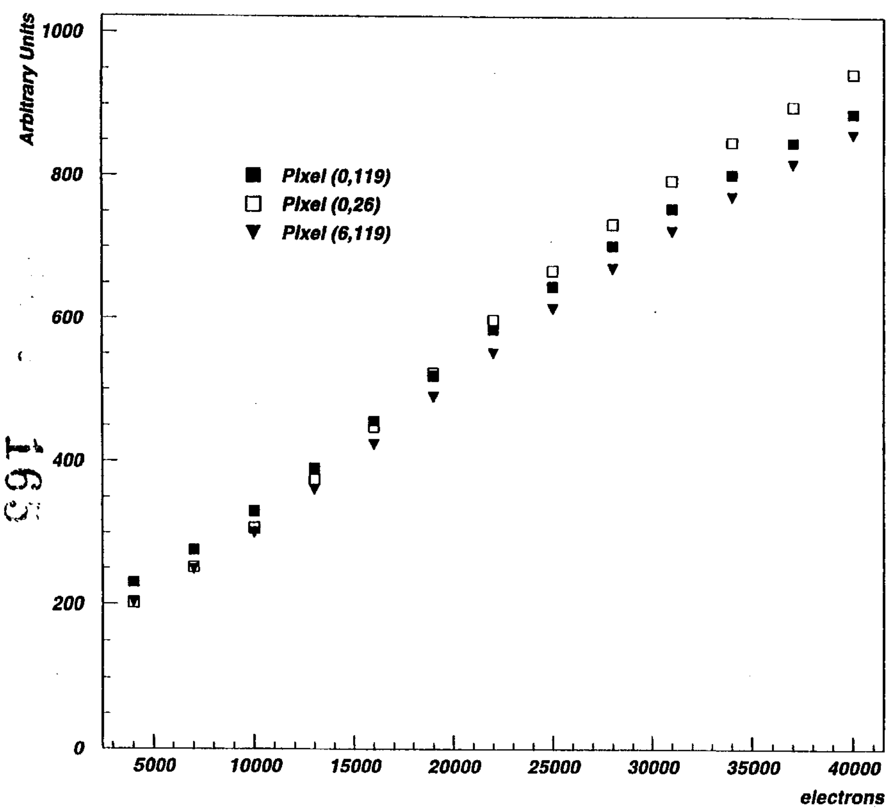
G. Grim
04/05/98 09.49
Leakage Compensation Performance
Arbitrary Units
electrons
I_{leak}/UC = 1 nA
I_{leak}/UC = 10 nA
I_{leak}/UC = 73 nA



G. Grim
04/05/98 09.43
Leakage Compensation Performance
electrons
Arbitrary Units
I_{leak}/UC = 73 nA
I_{leak}/UC = 10 nA
I_{leak}/UC = 1 nA

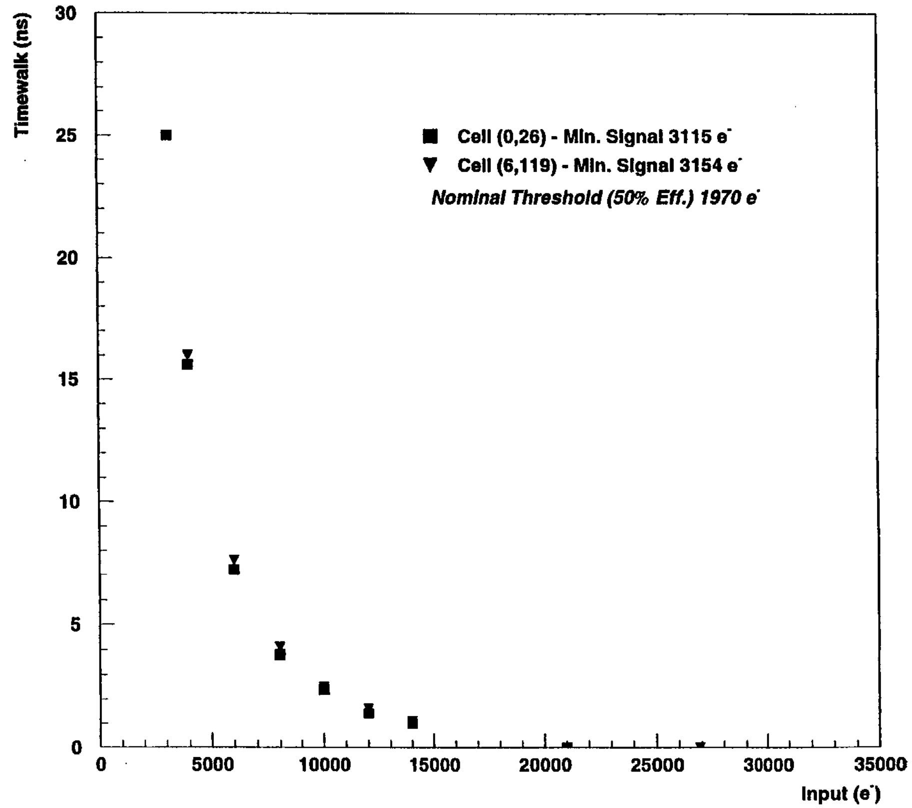
G. Grim 09/04/98 18.04

Chip-B3 UC Comparison



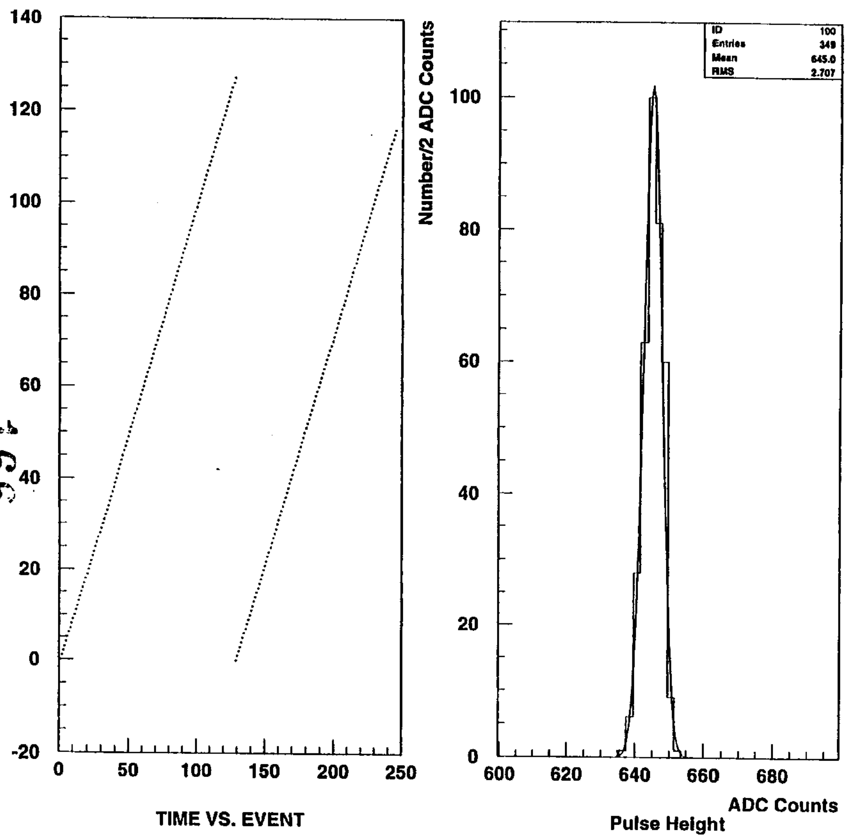
G. Grim 29/04/98 14.11

Chip-B3 UC Timewalk Comparison



05/05/98 08.12

BFE-168 Performance



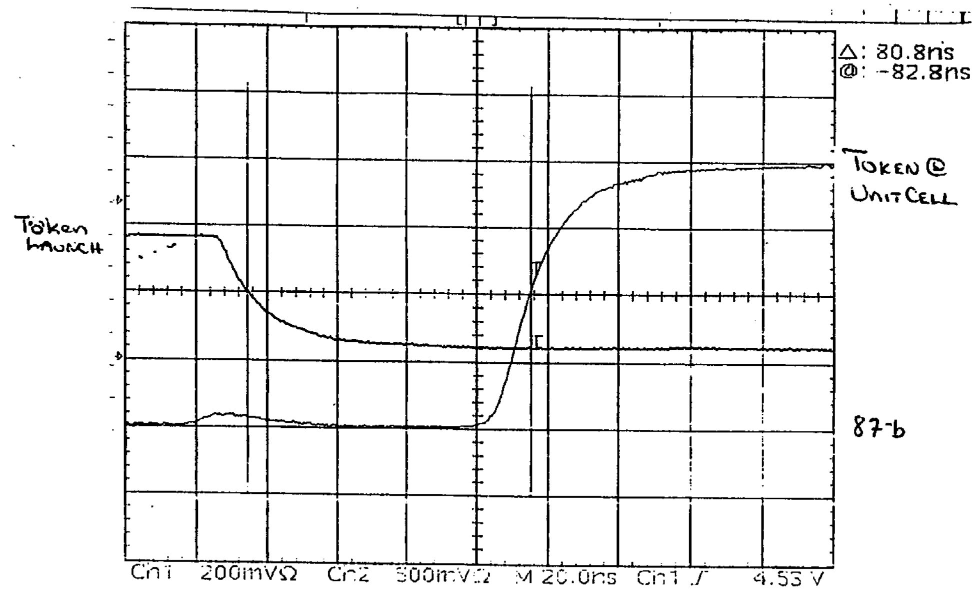


Fig. 87-b ⇒ $\frac{80.8\,ns}{120\,NS} = 0.67\,ns/UC$

Re-verified Analog Front-End Performance.

- Original Results Presented @ Hungary 1996
- Linearity Good Enough - Spec.
- Timewalk 16 ns @ 4k electrons. - Spec.
  - Dual Comparator Coincidence
- Noise of 150 e^-'s RMS ENC - Spec.

Summary of Results

- Reverified Analog-Front End Performance.
- Power Consumption
- Leakage Current Capacity
- Column Readout Design

Leakage Current Capacity

- Max. Current 73 nA/UC
- Specification of 100 nA, Goal 150 nA
- From n+/p/p+ work, observe 7 pA/μm^2 @ Room Temp.
- For 150 μm x 150 μm UC @ 0 C => 10 nA/UC Avg.

Power Consumption

	Supply (V)	*Current (mA)*	*Power (mW)*	*Power/UC (μW)*
Vdd	3.00	3.75	11.25	11.7
VddA	2.50	3.12	7.82	8.1
VddP	1.08	12.18	13.15	13.7
Total	-	-	32.20	33.6

- Power Consumption per Unit Cell in Spec!

Column Readout Functions

- Basic Design Works!
- Token Speed ~1.5 GHz (Spec. 3 GHz)
- Pixel Mask & Neighbor Logic Works
- End of Column Time Stamp Works
- Bus Speed Needs Verification

Next Step

- Conversion to Honeywell SOI
- Rad-Hard to CMS Fluences - Dave Pellett Talk
- Simulation & Layout Conversion Complete
- Submission March 1998

K. Gabathuler, PSI

CMS PIXEL READOUT ELECTRONICS

PSI - ETHZ - Aachen
P. Dick, R. Horisberger, V. Karpinski, M. Lechner, G. Pierschel, R. Schnyder

Strategy:

- Test circuits are designed in radiation hard technology in order to keep control of the area finally required for a pixel unit cell and to monitor the performance before and after irradiation.
- Before going to the complex design of a large array chip, design the most critical elements of the circuitry. Their performance determine the final concept of the readout.

Design constraints:

- 4 Tesla field offers the use of large charge sharing effect for n-pixels.
- Square pixel size of 150 μm x 150 μm implies small pixel capacitance (<100fF).
- Depletion depth of sensor > 200 μm up to 6 x $10^{14}/cm^2$.
- MIP signal >12000 electrons up to 6 x $10^{14}/cm^2$.

Design goals:

- Want to run with threshold of 2500 e up to 6 x $10^{14}/cm^2$.
- With threshold at 5 σ noise, noise level must be below 500 e up to 6 x $10^{14}/cm^2$.
- Data loss due to readout should not exceed ~1%.
- Power dissipated in readout chip should not exceed 60 μW per pixel.

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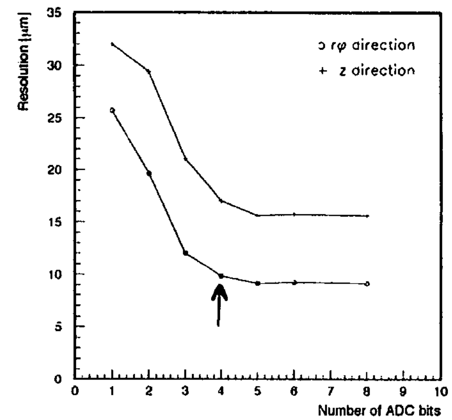
CMS PIXEL READOUT ELECTRONICS

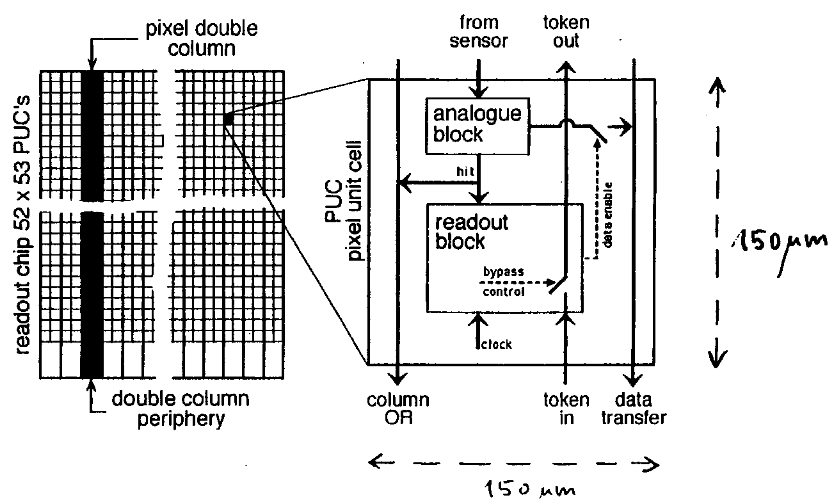
Main Features:

- Analogue Readout

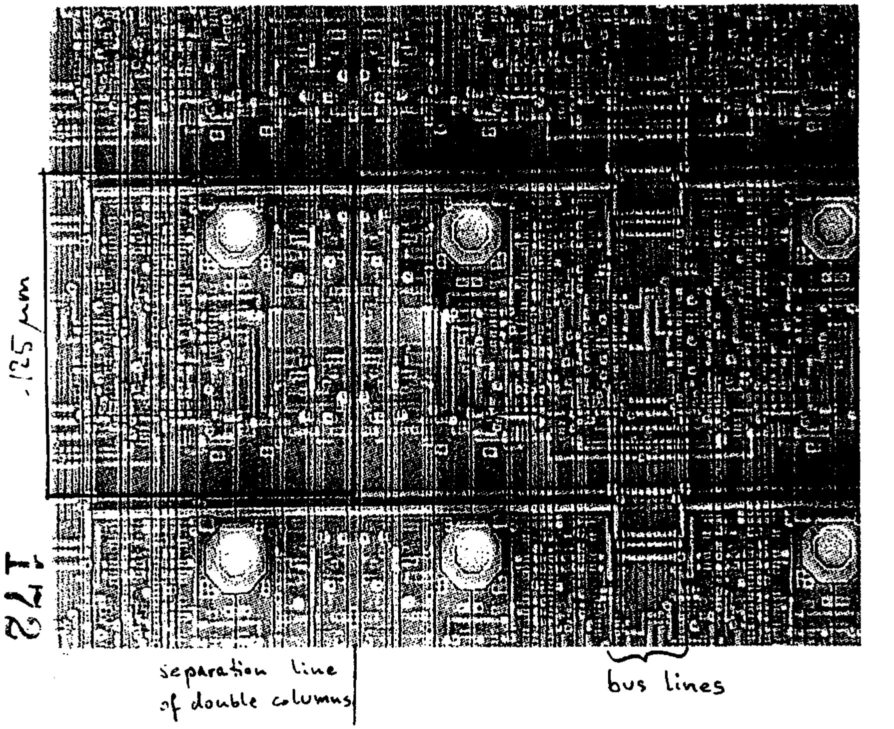


- Octal coded addressing

- Column based architecture (double columns)



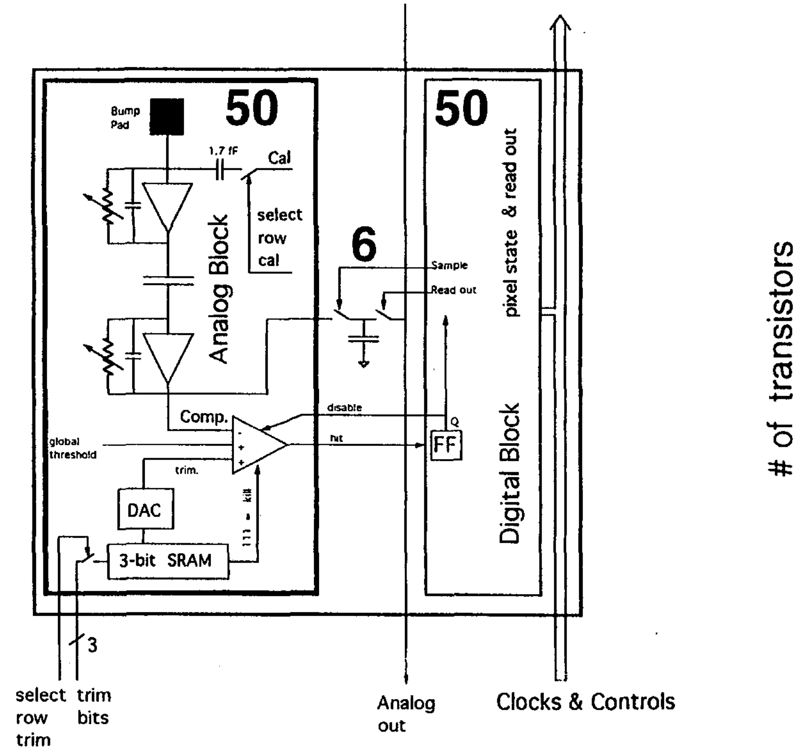
- Mirrored double column layout



- Column Drain Architecture
  Fast scan of hit pixels in a hit double column.
  Copy hits rapidly to periphery where they are stored for LT1 confirmation.

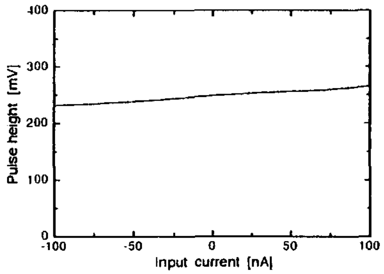
- Direct transfer of confirmed data from column periphery to counting room.

Analogue Block

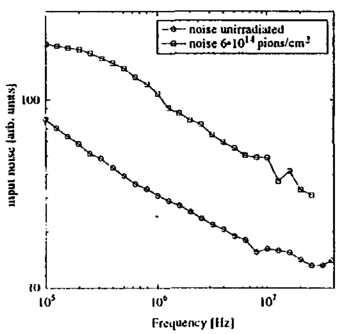


- Preamplifier&Shaper configuration
- Preamplifier feedback capacitance ~30 fF
- Preamplifier absorbs leakage current
- 20 - 30 e/mV at shaper output
- Common threshold for all pixels on chip
- Individual 3-bit threshold trim (111=kill)
- Column and row addressing scheme for trim bit programming and for applying selective calibration pulses
- Comparator disabled after hit

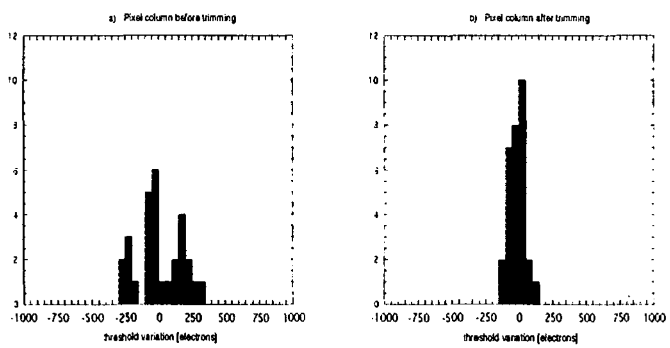
DMILL TEST CHIPS FOR ANALOGUE BLOCK



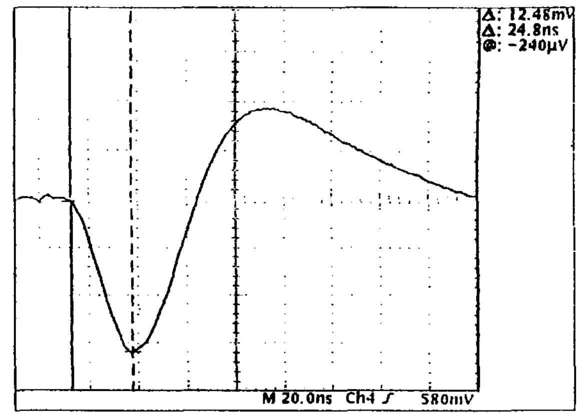
Signal variation at shaper output versus leakage current absorbed in preamplifier



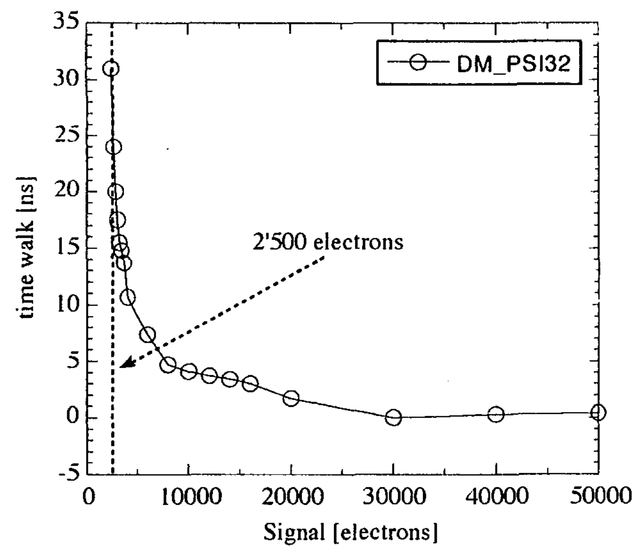
Noise increase of factor 3 after irradiation. Measured with input node capacitance of 160 fF, gives 650 e after irradiation.
For anticipated 100 fF, noise expected 400 e after irradiation.

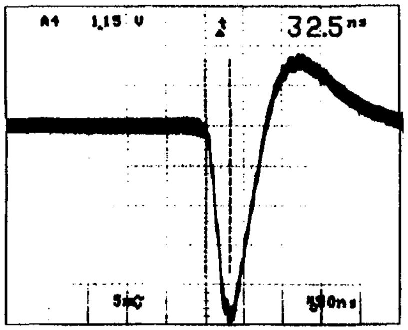


Pixel threshold distribution before and after trimming (unirradiated). Threshold ~ 1900 e, but can operate chip as low as 700 e threshold.

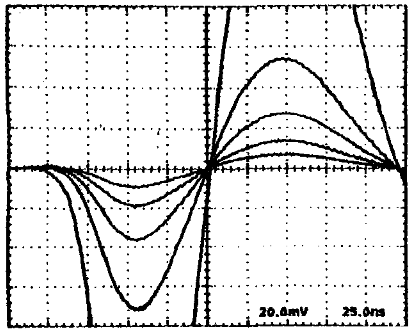


DM_PSI32, unirradiated.
Analog power ~40 µW.
Peaking time 24.8 ns.

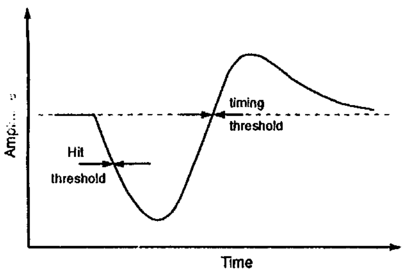


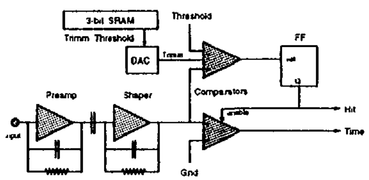


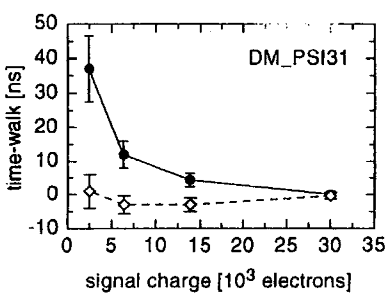
DM_PSI30, unirradiated
Peaking time 32.5 ns



DM_PSI26, irradiated with 10^{14}







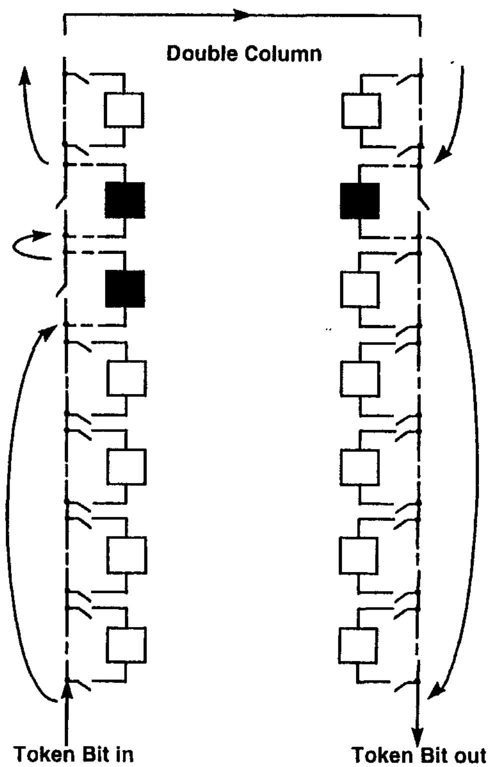
DM_PSI31, unirradiated

Zero Crossing Method

Must be checked after irradiation.

COLUMN DRAIN ARCHITECTURE

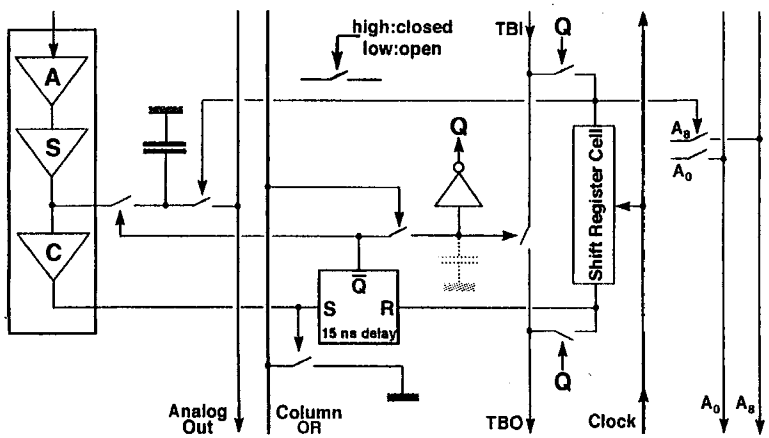
Upon a hit indicated via column OR to the column periphery, it sends a Token Bit through the column, skipping unhit pixels and stopping at hit pixels, initiating data drain to the periphery.



Travel of Token Bit up and down the double column takes about 8 b.c.

During this time more hits in so far unhit pixels in the double column from one additional b.c. must be allowed in order to reduce dead time.

CMS PIXEL UNIT CELL

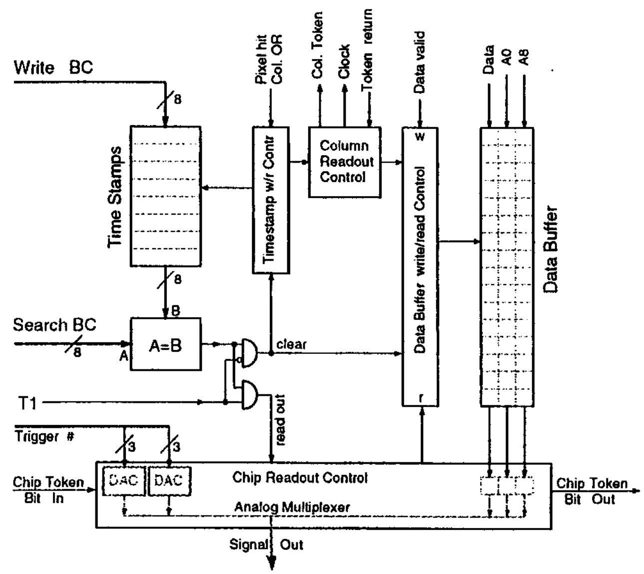


Any pixel in the column can pull the Column OR line to *LOW,* initiating a time stamp record in the column periphery . Upon sending a Token Bit on its way the column periphery resets the Column OR to *HIGH.*

The route of the Token Bit (*TBI* - TBO) is therefore only established when the Token Bit starts its travel through the double column.

During Token Bit scan # n *one* additional time stamp can be recorded and its associated hits are drained with Token Bit scan # (n+1), during which time stamp # (n+2) is allowed, and so on (double buffering).

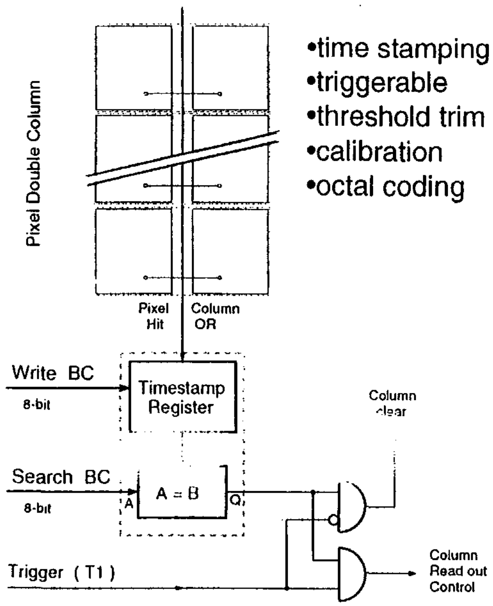
CMS PIXEL COLUMN PERIPHERY

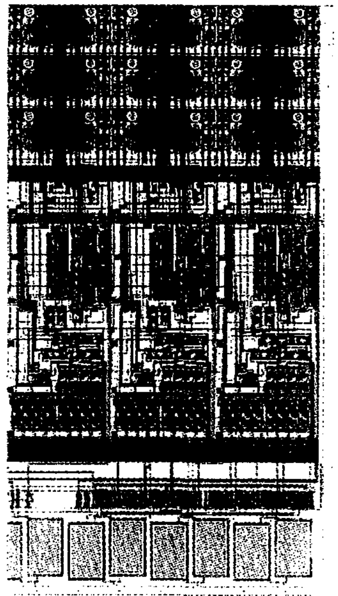


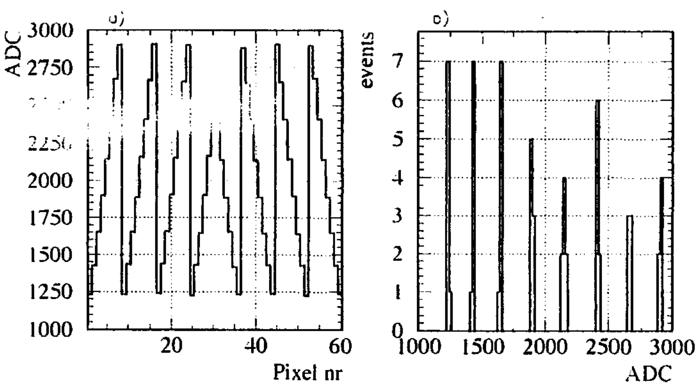
- Content of 8-bit local bunch crossing counter present in each periphery (*Write BC*). Ditto for *Search BC* which lags behind *Write BC* by 128 (1st level trigger latency)
- 8 *time stamp* registers (8-bit) organised in variable length FIFO.
- 24 data buffer cells of 3 switched capacitors. Variable association of data buffer cells to time stamp registers.
- Hand shake mechanism for Token Bit.
- Upon (*A=B and T1*) 6-bit trigger number is latched into two *DAC's* for octal coding.
- *Chip Token Bit* sent by Token Bit Manager Chip enables octal coded trigger number, pixel addresses and signal to leave the chip as a sequential analogue signal stream.

22 x 30 PIXEL CHIP

- •time stamping
- •triggerable
- •threshold trim
- •calibration
- •octal coding

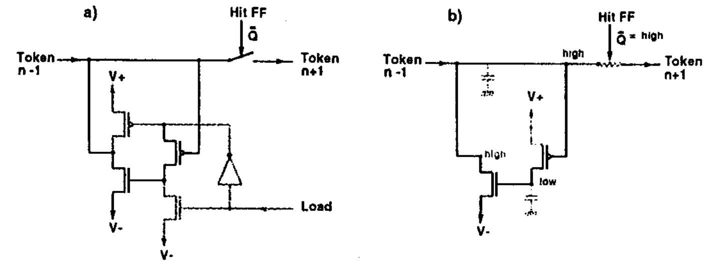


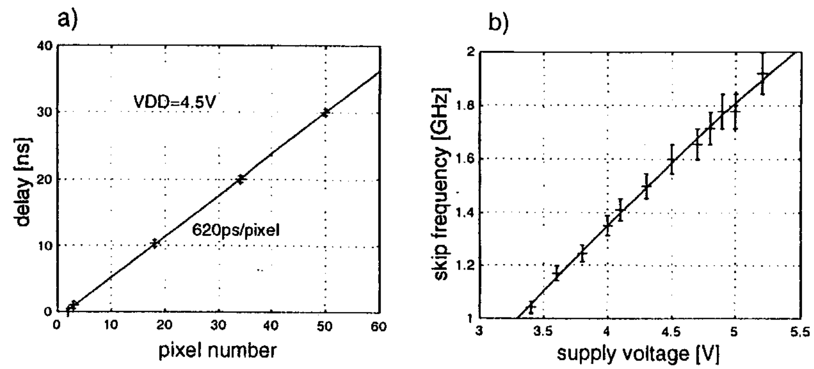




Lowe... octal coded bit of pixel address for 30 pixels of one double column. (chip unirradiated)

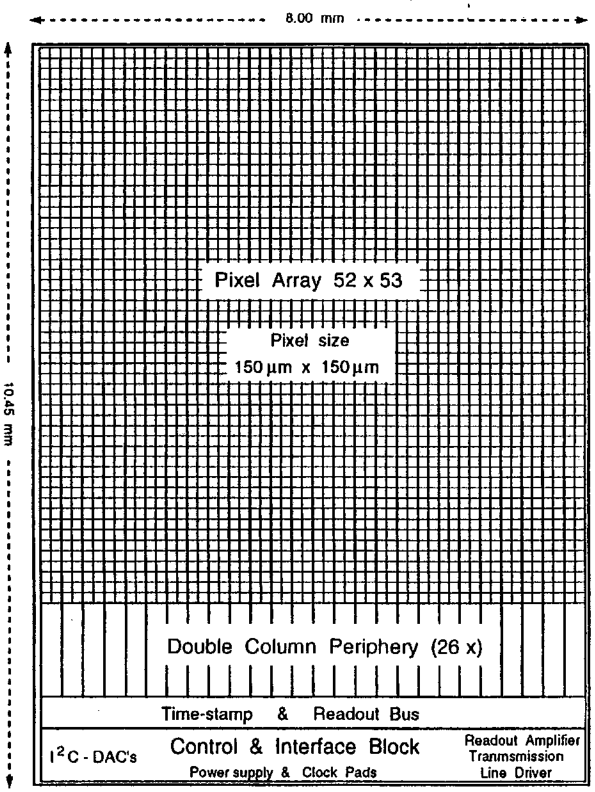
TOKEN BIT SCAN





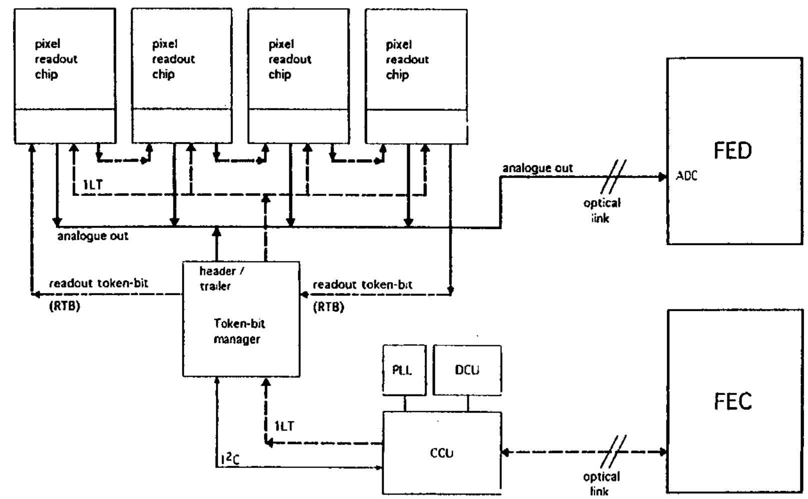
Token Bit takes 66 ns to travel through empty double column.

Crosstalk from Token Bit travelling through pixel to pixel input pad <750 electrons.



~ 380'000 transistors

READOUT OF TRIGGERED DATA



Token Bit Manager Chip

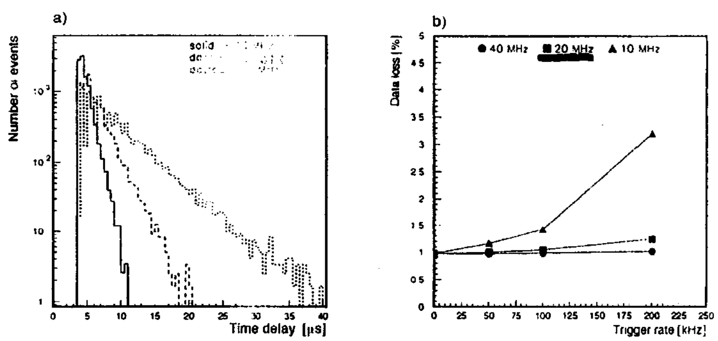
- Distributes clock and trigger signals to a group of chips.
- Manages a trigger signal stack.
- Puts data header/trailer onto the analogue out line.
- Sends Readout Token Bit according to content of trigger stack.
- Error handling and reset capabilities.

One readout frame has mixed data from different time stamps

<u>**Data Format**</u>

Data of one pixel hit	**# of octal bits**
Time stamp	2
Chip number	1
Column number	2
Row number	2
Signal	1
Header/Trailer/Marks	~2
TOTAL	**~10**

<u>**Data Transmission**</u>



Pedestal Loss of 1% is due to various losses in the raw (pre-trigger) data.

Pixel Detector for B-factories

T.E. Browder, C.J. Kenney, S.L. Olsen, S.I. Parker, S.K. Sahu*, G.S. Varner
University of Hawaii

G.P. Grim, R.L. Lander
University of California, Davis

H. Aihara, H. Tajima
University of Tokyo

H. Yamamoto
Harvard University

Abstract

Prospects for pixel detector upgrades of current e^+e^- B factories are investigated. Relevant technologies are compared. The results of some preliminary simulations and fabrication R & D are presented.

1 Introduction

B-factories are the new generation of particle accelerators capable of producing copious numbers of B-mesons. B-mesons, being heavy, have hundreds of decay modes, and therefore create a large arena for the test and measurement of Standard Model. Out of many physics topics to be studied in B-factories, test of fundamental symmetries is perhaps the foremost. The product of charge conjugation and parity (CP), which was thought to be a fundamental symmetry of nature, was found to be violated in the decay of K-mesons. Even more than 30 years after this discovery, the phenomenon of CP violation has not been observed in any other system. The Standard model, on the other hand, does allow for CP violation through complex phases in the quark rotation matrix, called Cabbibo-Kobayashi- Masakawa(CKM) matrix, which along with the magnitudes of the matrix elements, are poorly determined parameters.

The major goal of the B-factories is to discover the phenomenon of CP violation in B-meson decays, measure the CKM parameters, and therefore check if the observed CP violation can be explained within the scope of the Standard Model. These experiments have the potential to answer the very fundamental question : why is the universe that we see today is made of mostly matter, with anti-matter only scarcely present ? Such a situation can occur if there is a large enough CP violation in the physical laws of nature.

Electrons and positrons can collide to produce a quark-antiquark pair. The largest cross-section for B-mesons (a "beauty" quark paired up with any other quark) occurs at the $\Upsilon(4S)$ resonance at a center-of-mass energy of 10.58 GeV. The B-factories at (1) Cornell University, CESR ring, CLEO detector, (2) Stanford Linear Accelerator Center, PEP-II ring, BaBar detector, (3) High Energy

*Speaker & Corresponding author; E-mail - sahu@uhheph.phys.hawaii.edu
Talk presented at the Pixel 98 workshop at Fermilab during May 7-9, 1998.

Accelerator Physics Lab (KEK, Japan), KEK-B ring, BELLE detector; will all run at this energy. PEP-II and KEK-B will be asymmetric (different momenta for electron and positron beams), while CESR will be a symmetric accelerator. In Fig. 1 we show the geographic location of these B-factories and in the inset show their operating region in center of mass energy.

The decay vertices of the B-meson and its secondaries play an important role in the physics being pursued, and therefore much effort has gone into building silicon strip detectors for vertexing. Intrinsic position resolution of these detectors are typically about 5 - 15 microns, and the impact parameter resolution is typically 80 - 200 microns. For the initial discovery physics, this kind of sensitivity is enough, but as we proceed into the measurement and deeper disovery arena, much better vertexing is desirable. In Fig. 2 we show the decay lengths ($\beta\gamma c\tau$, with $\beta\gamma = 0.43$ for KEK-B) of some important particles generated at B-factories, compare them with resolutions of a common silicon strip vertex detector (SVD) and a novel silicon pixel detector (PIX) combined with the SVD. Clearly, the hybrid system (PIX+SVD) probes deep into the decay kinematics.

Both, silicon strip and pixel detectors are essentially reverse-biased PIN($p - intrinsic - n$-type) diodes. When a charged particle goes through, the ionization creates electron-hole pairs, which drift in opposite directions and create a signal when they strike the respective electrodes (see Fig 3). In the case of the strip detector, the electrodes look like strips running in orthogonal directions on p and n planes, and therefore the signal-bearing strips give the information on the position of the track. For instance, upper plane of the strip detector sketched in Fig. 3 gives the z-position measurement, and the bottom plane gives the y-position measurement. In the case of the pixel detector, however, since one of the electrodes is segmented into tiny rectangles, called pixels, both z and y measurements come from just the top plane.

2 Proposed Upgrade of SVD

In this paper, we will take the Belle detector at the KEK B-factory as a generic e^+e^- B-factory, and build our arguments around it. The same arguments can be extended to BaBar and CLEO with certain constraints.

Vertex resolution is dominated by two factors : geometry and multiple scattering. A pedagogical model with two layers of vertex detector (for the sake of simplicity) is shown in Fig. 4. The two detector planes are parallel to the beam, at radial distances r_1 and r_2. Intrinsic resolutions are σ_1 and σ_2, respectively. The goal is to make the impact parameter resolution σ_{d0} as small as possible. It comprises of two factors - geometric error (σ_{geom}) and multiple scattering error (σ_{ms}) :

$$\sigma_{d0}^2 = \sigma_{ms}^2 + \sigma_{geom}^2 \quad (1)$$

$$\sigma_{geom}^2 = \left(\frac{\sigma_1 r_2}{r_2 - r_1}\right)^2 + \left(\frac{\sigma_2 r_1}{r_2 - r_1}\right)^2 \quad (2)$$

$$\sigma_{ms}^2 = \Sigma_{j=1}^{ndet}(R_j \Delta\theta_j)^2 \quad (3)$$

$$\Delta\theta_j = \frac{0.0136}{p[GeV/c]}\sqrt{\frac{\Delta x_j}{X_0}}\left[1 + 0.038 \ln\frac{\Delta x_j}{X_0}\right] \quad (4)$$

where R_j is the radius of the inner detector(s) that need to be taken into account for estimating tracking error due to multiple scattering. It may be noted that these equations assume perpendicular incidence, and therefore a $\cos\theta$ factor enters in the denominator when slanted tracks are considered.

Examining the above equations we determine that for better vertexing :

1. r_1 and r_2 should be small, which means detectors should be as close to the interaction point as possible.

2. $(r_2 - r_1)$ should be as large as possible, which means the lever arm should be large.

3. $\frac{\Delta x_j}{X_0}$ should be small, in other words, the detector itself should be as thin as possible.

Keeping these factors in mind, we propose the following : (1) reduce the beampipe diameter (2) add two layers of *thin* pixel detector. The advantage of doing this has been simulated with a program called TRACKERR. The most relevant results are shown in Figs. 5 & 6, where the impact parameters $\sigma_{r\phi}$ and σ_z are plotted as functions of the dip angle of a 250 MeV incident pion. Intrinsic resolution of 10 μm is assumed for both, PIX and SVD detectors. The solid lines are for the SVD+PIX option with 100 μm pixel thickness, dashed lines are for the SVD+PIX option with 350 μm pixel thickness, and dotted lines are for the existing SVD only option. For the PIX option, it is assumed that one can reduce the beampipe radius to 1 cm, and that a 0.3% X_0 synchrotron/EM shield exists just outside of the beampipe.

The significant improvement in tracking and vertex resolution, especially at the low angle region is worth taking the trouble of putting a pixel detector in. Rigorous analysis on this topic may be found in [1].

In what areas do we expect physics gains ?

1. The $b \to s$ transitions, mediated by penguin diagrams are hard to separate from the $b \to c \to s$ backgrounds without good vertexing.

2. The $b \to u$ transition is a rare decay, and the matrix element V_{ub} is a poorly determined parameter. Measurement of this decay mode is made difficult by continuum background, which can be suppressed by good vertex separation.

3. Direct measurement of T-parity violation can be studied in polarization studies of $b \to c\tau\nu$. Detection and polarization measurements are difficult without excellent vertex detection.

In general, any process with a secondary vertex or where either combinatoric background is large or continuum background is large, will be easier to study with a pixel detector.

As a generic B-factory detector, we use the Belle detector at KEK B-factory to establish our point. In Fig. 7(a) cross-sectional view of the current Belle vertex detector is shown. It consists of three layers of silicon strip detectors with a 2 cm radius beam-pipe. We propose to reduce the beam pipe radius to 1 cm, and put two thin pixel layers at 1.3 and 2 cm. The resulting arrangement is shown in Fig. 8. The $r\phi$ view is given in Fig. 9. The hexagonal shape for both the layers ensures ease of mechanical fabrication, but leaves some dead space at the corners. An alternate design, shown in Fig. 10 has a hexagon-octagon shape. This has the advantage that sensors of the same size for both the pixel layers can be manufactured, thus making the yield higher.

3 Radiation Damage

Radiation damage in the B-factories is dominated by $e^{\pm}\gamma$ background from synchrotron radiation and beam-gas scattered electrons (hereafter referred to as *spent electrons*). Damage to the detector and circuit is mainly due to ionization. This differs from the type of damage at LHC, which is mostly field and gate oxide damage, as well as bulk damage due to proton, neutron or pion irradiation.

Synchrotron background is a characteristic of the machine, and the problem is different for each B-factory. In Fig. 11 we show the synchrotron radiation fans at BaBar and Belle detectors. At BaBar, the fan hits the detector region directly, and hence sophisticated masking is necessary. In Belle, the dotted lines show the 10σ synchrotron profile, and it stays clear of the detector/beampipe. Hence the beampipe radius can be reduced without being directly hit by the synchrotron radiation. In any case, we assume that synchrotron radiation can be masked, and that the majority of damage will come from spent electrons.

Spent electrons (or positrons; we will call them spent electrons in a collective sense) are produced when the beam electron scatters off a residual gas nucleus via Coulomb scattering or Bremsstrahlung. The spent particle changes direction or energy, and goes off the orbit. The new trajectory, after passing through a number of electromagnetic elements in the accelerator may hit the detector, and thus produce hits and radiation damage. Simulations of such backgrounds have been performed at all the three B-factories, and details of the results may be found in the proceedings of the First and Second Workshops on Backgrounds at Machine-Detector Interface([2]). For Belle, the results are summarized in Fig. 12, where expected the dose is plotted as a function of the radial distance from the beamline. The position where the pixel detector will be gets upto a MRad of dose per year, which would be too much for conventional strip detectors and associated electronics. Although the electronics could be made rad-hard, the large capacitance and large leakage current of strip detectors would render them inoperable at such high doses. Again, the occupancy would be too high for a strip detector.

Getting the detector and the electronics rad-hard upto at least 5 MRad is conceivable with current technology, thanks to success in development of radhard electronics for LHC.

It is worthwhile to mention that the backgrounds are a strong function of the beam emittance. A representative diagram of beam emittances at PEP-II, CESR and KEK-B is given in Fig. 13. The very low emittance at KEK-B makes it a lot easier to put a pixel detector close to the beam.

4 Possible Options

The B-factories will start their runs in early 1999. We plan to install the pixel upgrade after two years of initial running, which means we have to make a working detector by the end of the year 2000. Keeping this goal in mind, we have evaluated several options for vertexing technology.

- **Diamond Pixels :** It would be the best detector option, given its radiation hardness. But the technology is currently being developed, and there aren't multiple vendors of the detector grade material to ensure uninterrupted supply. This option would be too risky for this project.
- **Thin Silicon Strips :** These are a possible option, although signal to noise is a problem. Some groups have produced such detectors with partial success. Advantage is that one can use commercially available Viking VH1 radhard chips with these detectors. This is a potential *intermediate* upgrade option.
- **Thin CCDs :** CCDs have been used in HEP experiments and backthinned CCDs can be presumably used for this purpose. But the charge transfer (shift register) mechanism limits the capability of operating the detector at high background rates. The signal would be swamped in backgrounds during charge transfer.
- **Thin Silicon Pixels (bump-bonded) :** This is a potential option for us, and the rest of the paper is written taking this as the default. By choosing this, we are flying on the wings of ATLAS/CMS expertise.

- **Thin Silicon Pixels (Monolithic) :** With lower capacitance than bump-bonded ones, these have better S/N performance. This could be a potential option if the technology can be made rad-hard. This option is still under study.
- **Thin Slicon Pixels (3D) :** This is a novel innovation in silicon detector technology. But it is in the process of being developed, and would clearly be too ambitious for this project.

We are currently carrying out R & D for the bump-bonded thin silicon pixel option.

The proposed manufacturing process of the detector is described in Fig. 14. One starts with a 500 μm readout wafer and a 70 - 100 μm detector wafer. The detector is then backed up with wax by a 300 μm dummy wafer. Indium bumps are deposited on both sides, and pressure bonding is performed. The sandwich is cut with diamond saws to the desired size, and by dissolving the wax the dummy support is removed. The readout wafer is then back-thinned by cold reactive plasma etching down to 50 μm or less. One is then left with a complete thin detector ready to be installed.

In the Belle detector, the acceptance is from 17° to 150°, and therefore the rule $L = 5R$, where R is the radial distance of the detector from the beamline and L is the minimum physical length of the detector, applies (see Fig. 15). Since we want to put the detectors very close to the beamline, with R less than 2 cm, a whole sensor can be comfortably carved out of a 4 inch or at worst 6 inch wafer, both of which are standard. Such a "one-piece" detector eliminates the need of inter-sensor wire bonding, and simplifies the structural issues greatly.

5 Some Rules of Thumb and "a" Readout Architecture

The pixel upgrade we propose need not have any time-stamp information, since the trigger will be provided by the silicon strip and TOF detectors. With only charge information needed, the number of transistors, capacitors and resistors will be small, and therefore the size of the pixel can be made small. We envision a 50 × 50 μm^2 pixel size. Bump bonds are reliably done at diameters of 20 μm or large, and could comfortably fit into this pixel dimension. With 100 μm thick detector, the number of e-h pairs produced per MIP will be about 8000. In order to get good position resolution, the readout has to be analog and we need to get the charge sharing information from neighboring pixels. Assuming a 3×3 pixel clustering scheme, we should be sensitive up to about 20% of the total charge, which corresponds to 1600 electrons. Using the canonical S/N = 10/1, we get 160 electrons as the ENC of our electronics, which is achievable with current CMOS technology.

The readout/Integration time and dynamic range of the electronics depends on the degradation of the detector and electronics due to radiation. A useful parameter is the dark current. A good detector will have a dark current of the order of 10 nA/cm^2. A few MRad of dose will increase it to about 50 nA/cm^2. On a 50 × 50 μm^2 size pixel, this corresponds to 0.25 pA - 1.25 pA of dark current. With the 160 ENC number discussed in the last paragraph, the time becomes 160 e^-/ 1.25pA = 20 μsec. This means the integration time can be as long as 20 μsec even though the beam crossing is only every few nano seconds.

Since the physics event rate is less than 10 kHz and the event multiplicity is less than 8 for B-factories, the above scheme should work well.

A simple proposed architecture for readout is shown in Fig. 16. It is a modified version of an original design by Aw, Kenney and Parker. One sensor module consists of typically 2000 rows and 200 columns. When a row is hit and the charge collected is larger than the threshold, then the address of that row is encoded. During each scan cycle, the control loops over the encoded rows, and strobes all the columns of that row to be read out in parallel. These 200 signals can then be digitized, and may be filtered and/or delayed through an SCA/FPGA for a quick quality scan before being dumped into the database. Some multiplexing and zero-suppression may be required at this step if the power consumption becomes too large. All the analyses can be done offline.

6 Experience with Thin Wafers

At the Center for Integrated Systems(CIS), Stanford and the Fabrication Lab at UC, Davis we have done some rudimentary work on thin wafers. Starting from 300 μm, wafers have been thinned down to 70 μm by chemical etching. Processes such as dump rinsing, spin rinsing, spin resist, lithography, wet oxidation and dicing have been tested with good yield. Cold reactive plasma etching has been done without doing any visible damage to bumpbonds. Processes such as metallization and bump bonding will be tested on these thin wafers in near future.

In Fig. 17 we show a picture of lithography done on a thin wafer. The structures visible are about 20 μm wide. In Fig. 18 we show the cross-section of a diced thin wafer, still supported by the dummy wafer with wax.

7 Future Directions

The following goals are set for the installation of a pixel detector at the KEK B-factory. These are highly contingent upon manpower and financial resources.

- All processing techniques for thin wafers will be established this year (1998). The production will either be done by ourselves or vended to any interested manufacturer with the technology transfer.
- A diode prototype will be made by the end of 1998.
- Charge drift simulation for thin pixels and device optimization for readout will be done by the spring/summer 1999.
- A readout chip will be fabricated by mid 1999.
- A full prototype will be ready by the end of 1999.
- Assuming the backgrounds permit, a full detector will be made in 2000 and installed at the end of the year.

Acknowledgement

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[1] "Track Origin Reconstruction Resolution with a future Belle Pixel Detector", T.E. Browder *et al.*, To be published as a Belle Note (http://bsunsrv1.kek.jp).

[2] Proceedings of the First and Second Workshops on Backgrounds at the Machine Detector Interface, Hawaii 1995 (Ed. T.E. Browder, UH-511-838-96, available from www.phys.hawaii.edu/~beam/proceedings.html), 1997 (Ed. T.E. Browder and S.K. Sahu, in print at World Scientific, partial contributions available from www.phys.hawaii.edu/~beam/papers.html)

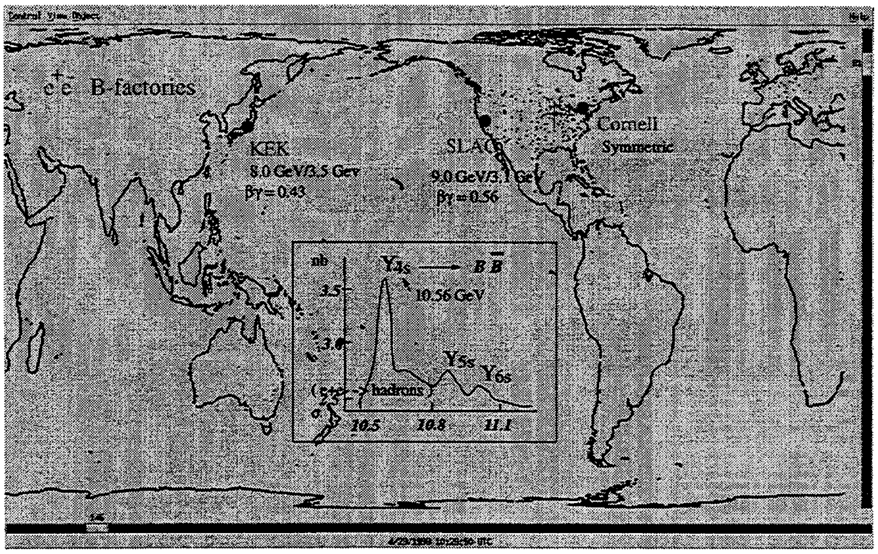


Figure 1: Geographical location of the e^+e^- B-factories. The inset shows the operating energy at $\Upsilon(4S)$ resonance.

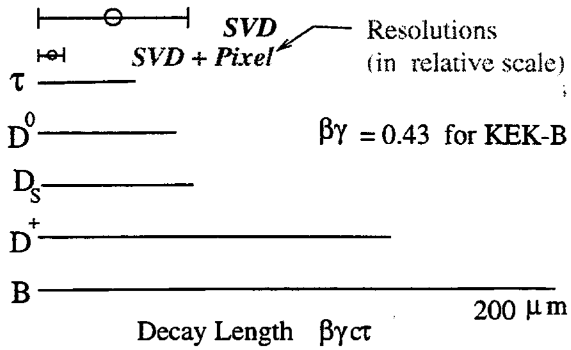


Figure 2: Decay lengths of some particles in relative scale, compared with resolutions offered by SVD and SVD+Pixel. Both SVD and PIX are assumed to have intrinsic resolution of 10 μm. SVD has 350 μm wafers, and PIX has 100 μm wafers. SVD option assumes a 2 cm radius beampipe, whereas the SVD+PIX option assumes a 1 cm beampipe.

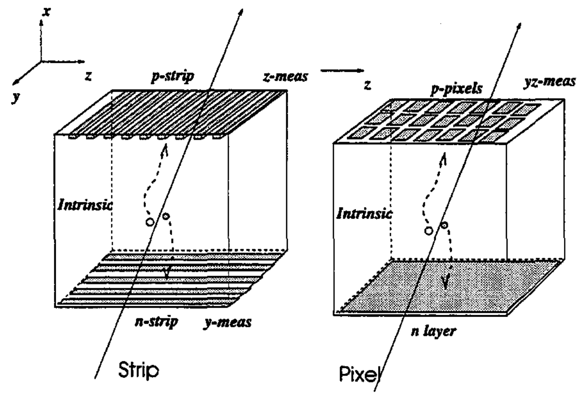


Figure 3: Conceptual comparison between silicon strip detectors and silicon pixel detectors. The arrow represents a charged particle, and the two circles represent an electron-hole pair out of thousands created. The electron drifts to the n-side (the detector is always reverse biased), and the holes drift to the p-side, generating a signal current upon arrival.

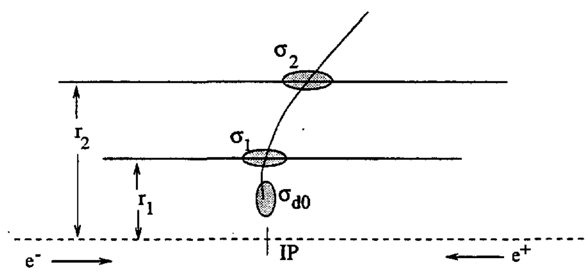


Figure 4: Model of a two-layer vertex detector.

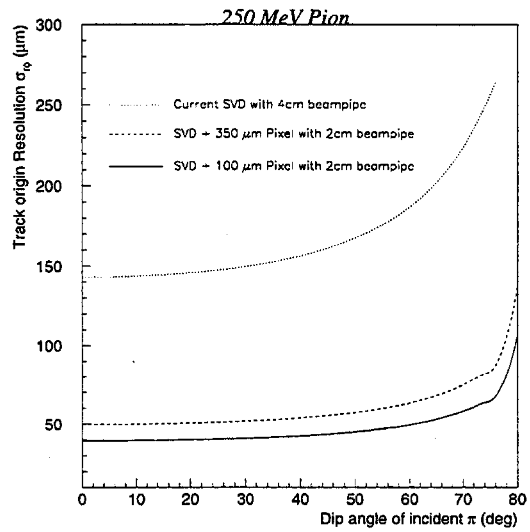


Figure 5: Impact parameter resolution in $r\phi$ plane as a function of dip angle for pions of different momenta.

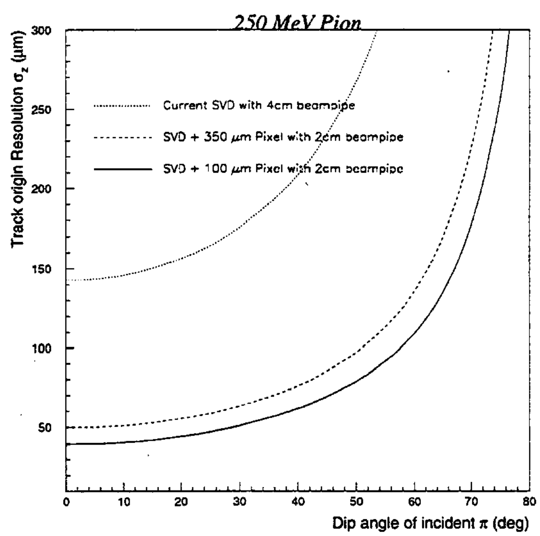


Figure 6: Impact parameter resolution in z direction as a function of dip angle for pions of different momenta.

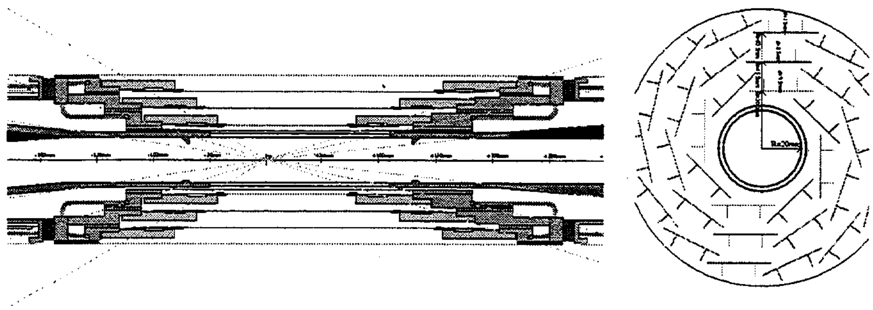


Figure 7: xz and $r\phi$ views of the current Belle silicon vertex detector (SVD).

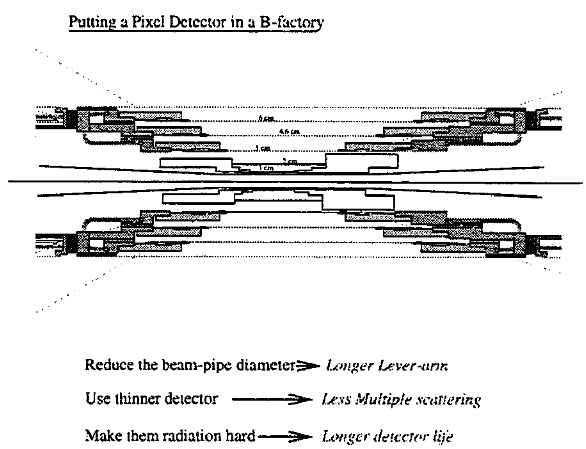


Figure 8: xz view of the proposed pixel detector upgrade at Belle.

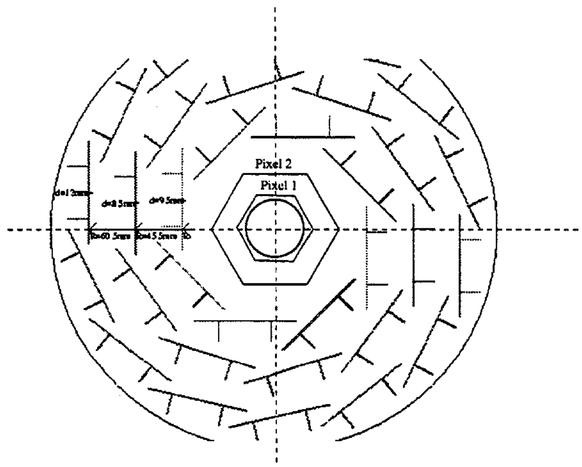


Figure 9: $r\phi$ view of the proposed pixel detector upgrade at Belle.

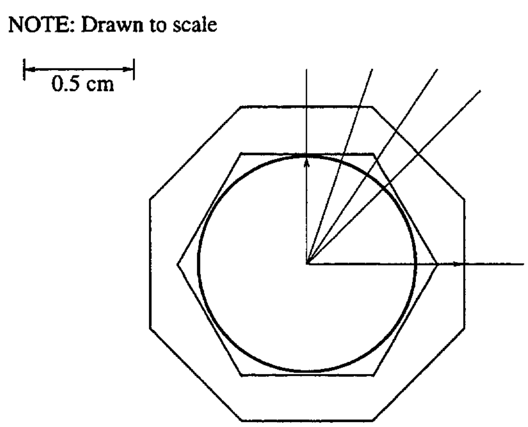
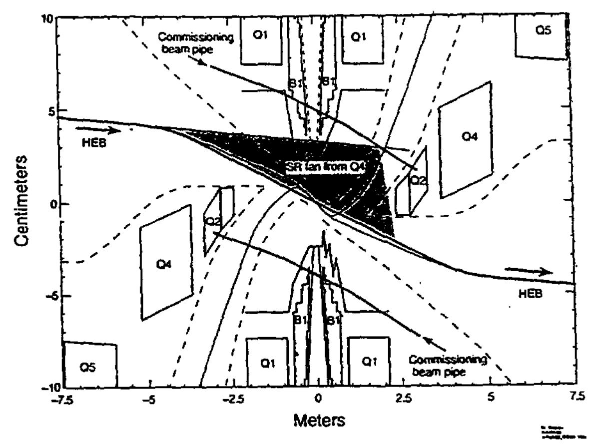


Figure 10: $r\phi$ view of another option for a pixel detector upgrade at Belle.



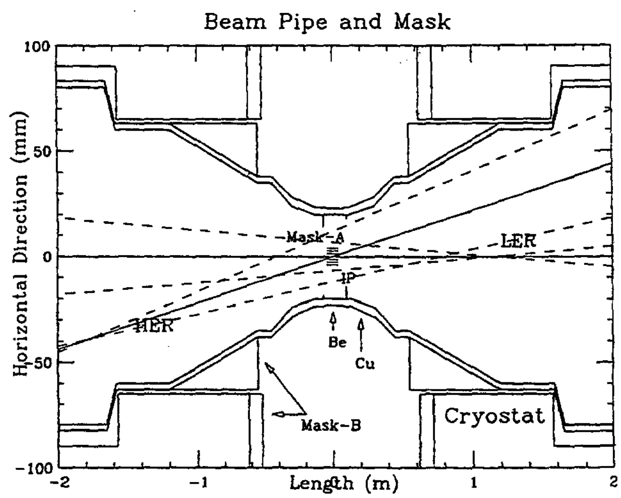


Figure 11: Synchrotron radiation fans at BaBar (top) and Belle (bottom). Dotted lines for Belle represent 10σ contours.

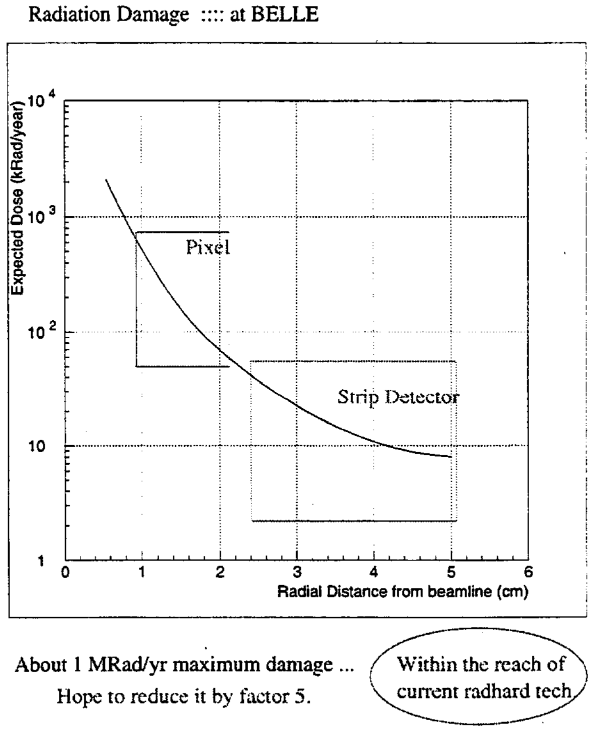


Figure 12: Radiation dose as a function of radial distance due to spent electrons at Belle.

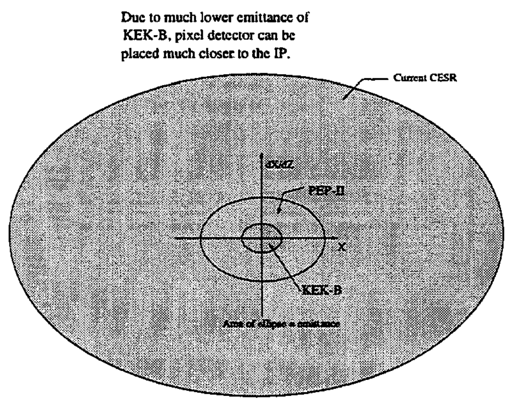


Figure 13: Beam emittance in the three B-factories in a relative scale. The area of the ellipse is a measure of the emittance.

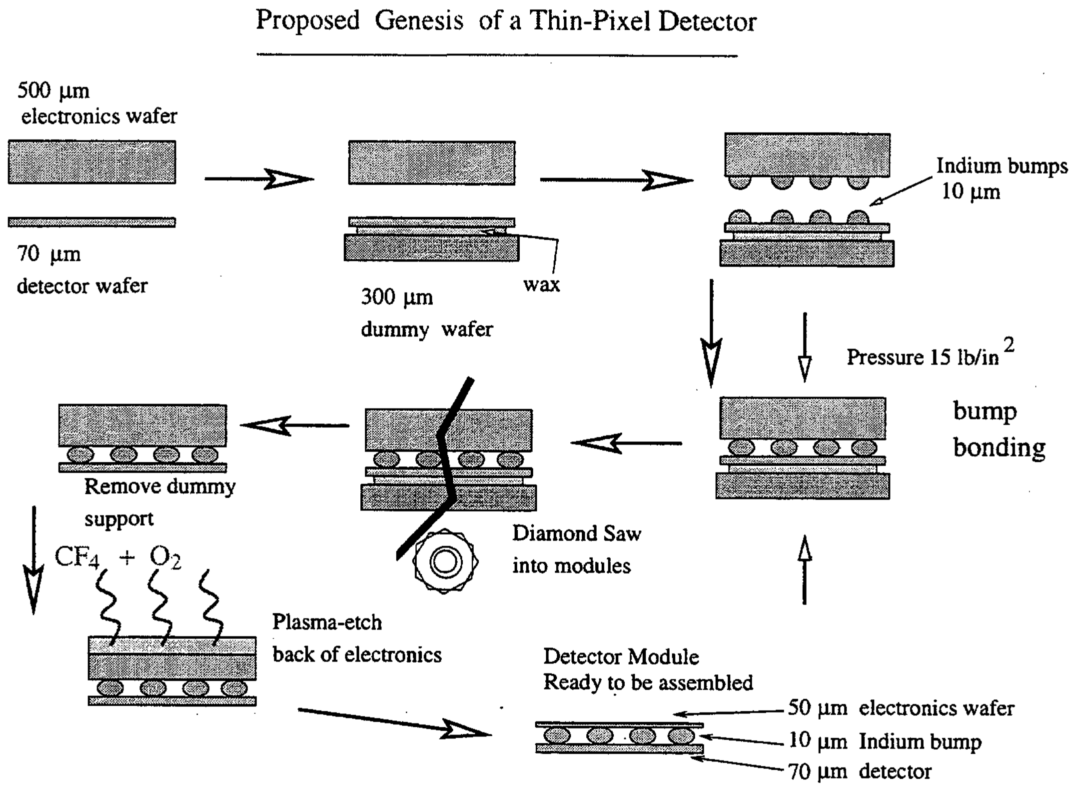


Figure 14: Proposed production process of a thin bump bonded pixel detector.

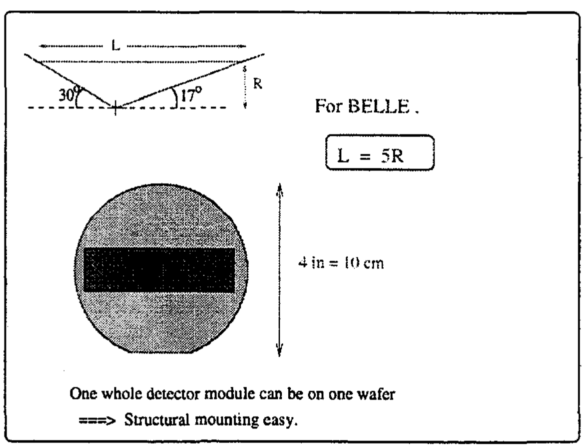


Figure 15: At small radii, the whole pixel sensor can be accomodated on a single wafer : the $L = 5 \times R$ rule.

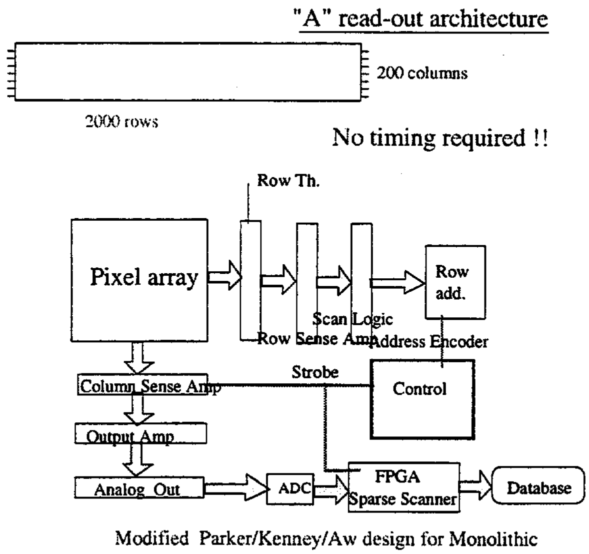


Figure 16: A simple proposed readout architecture for B-factory bump-bonded pixels.

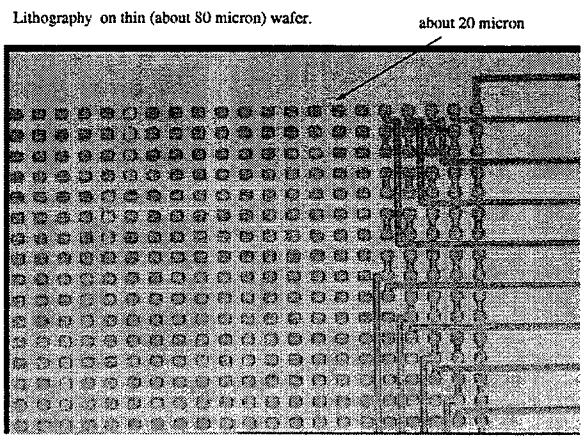


Figure 17: Lithography on a thin pixel. The smallest features are about 20 μm wide.

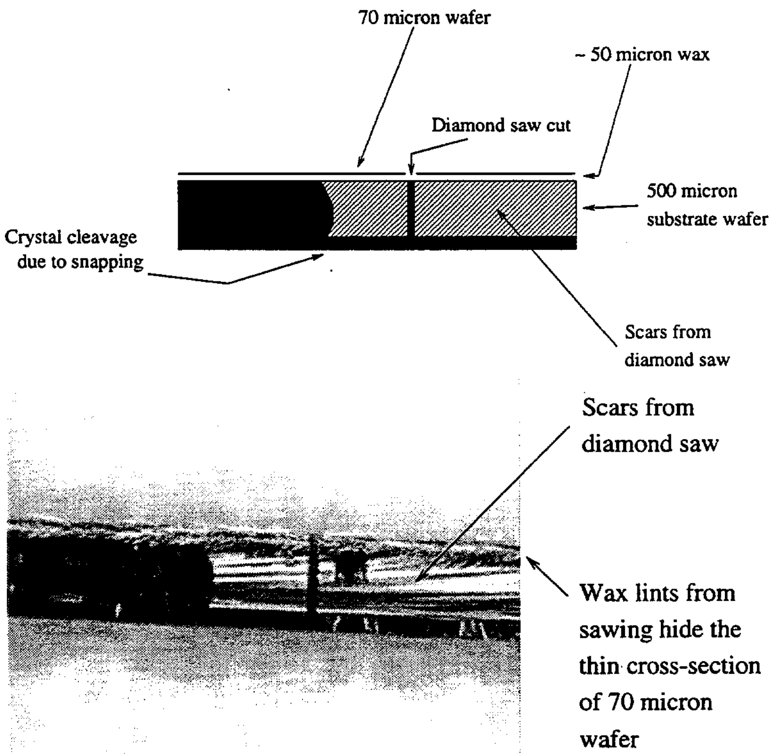


Figure 18: A cross-section of a diced thin wafer supported by a dummy wafer with wax.

Study of Radiation Damage to Honeywell RICMOS-IV SOI Transistors by Charged Hadrons [1]

G.P. Grim and D.E. Pellett
Physics Department, UC Davis, Davis, CA 95616

Abstract

We present preliminary results of an exposure of Honeywell RICMOS-IV SOI transistors to 2×10^{14} 63.3 MeV protons at the UCD cyclotron radiation test beam (27 Mrad (Si)). In terms of surface damage, this corresponds to almost twice the dose expected for the CMS pixel detector during its useful life at the LHC collider. The irradiated transistors include n-channel MOSFETs similar to the front-end transistors of a pixel readout we have designed for use at the next generation of detectors at hadron colliders. Data are presented on radiation-induced changes in threshold, transconductance, maximum voltage gain and noise for MOSFETs produced in a developmental SOI run. The preliminary results indicate that the readout front end would continue to function satisfactorily in the CMS radiation environment.

I. INTRODUCTION

The next generation of vertex detectors at colliders such as the Large Hadron Collider (LHC) at CERN will be subject to extreme radiation doses from high energy charged hadrons. For example, the inner part of the CMS pixel vertex detector, on which we are collaborating, is expected to be penetrated by of order 6×10^{14} such particles during its useful life [1], [2]. It is important to understand the limits of performance of the readout electronics under such conditions. For example, we have designed a pixel readout suitable for LHC applications [3]. The input transistor for the charge-sensitive amplifier is expected to be the component most sensitive to damage. In our design, this is an NMOS device with $w = 8.4\ \mu m$ and $l = 0.8\ \mu m$. A candidate radiation-hard technology for implementing the readout is the Honeywell SOI RICMOS-IV process [4]. This has been used successfully for radiation-hard digital circuitry, but its applicability for our analog use needs to be investigated.

For radiation tests, we have used Honeywell process monitor bars which include PMOS and NMOS transistors with nominal values of $w = 10\ \mu m$ and $l = 0.8\ \mu m$. The bars were specially processed to yield p-channel MOSFETs hard to a dose of 50 Mrad [5]. The gate oxide thickness was 15 nm, the barrier oxide thickness, 370 nm, and the effective gate length, 0.65 μm. We measured the $I - V$ characteristics and threshold shifts of these devices as a function of radiation dose and the noise in the frequency range 1-3 MHz for unirradiated devices and devices irradiated to 27 Mrad.

[1] Partially supported by US DOE contract DE-FG-03-91ER40674

II. MEASUREMENT TECHNIQUES

A. *Irradiation and Testing*

The devices were irradiated in the proton radiation test beam at the UC Davis Crocker Nuclear Laboratory (CNL) cyclotron [6]. The beam energy was 63.3 MeV. The fluence was monitored to 10% accuracy using a secondary emission monitor calibrated using a Faraday cup. The beam profile was approximately uniform over a 7 cm diameter, much larger than the devices under test. The dose rate was 2.3 Krad (Si)/s. Irradiation was done under bias ($V_{DS} = V_{GS} = 1\ V$ for NMOS and $V_{DS} = V_{GS} = -1\ V$ for PMOS devices) and in an argon atmosphere. Device parameters were measured with the beam off at 5 Mrad intervals using a Hewlett-Packard 4145B semiconductor parameter analyzer controlled by an Apple Macintosh computer running a LabVIEW [7] program.

B. *Preliminary Noise Measurement*

The input-referred noise amplitude in the frequency range 1-3 MHz was measured under operating conditions similar to that of the pixel readout front-end transistor. For this, a low-noise transimpedance amplifier calibrated using a signal generator and resistors was employed in conjunction with a Tektronix 2712 spectrum analyzer. Noise measurements were made approximately one month after the irradiation.

III. RESULTS

A. *Shift of Characteristic Curves and Thresholds*

Changes under irradiation in the device performance ($I - V$ characteristics and thresholds) are shown in Figures 1 through 3. In general, larger changes were observed in the first 15 Mrad than in the reminder of the exposure.

B. *Changes in Transconductance and Maximum Gain*

Graphs of transconductance divided by drain current before irradiation and after the full 27 Mrad dose are shown for the n-channel and p-channel transistors in Figures 4 and 5, respectively. Figures 6 and 7 show corresponding results for maximum voltage gain, g_m/g_o. The front-end transistor in the pixel readout is an n-channel MOSFET and has an operating point in the neighborhood of 10 μA. Here, the transconductance falls by approximately 20% and the maximum gain by 40% of the original values.

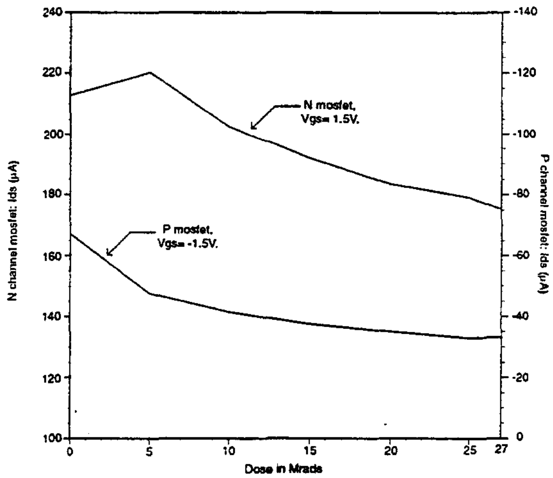


Figure 1: Typical shifts of I_{DS} for fixed V_{GS} due to irradiation.

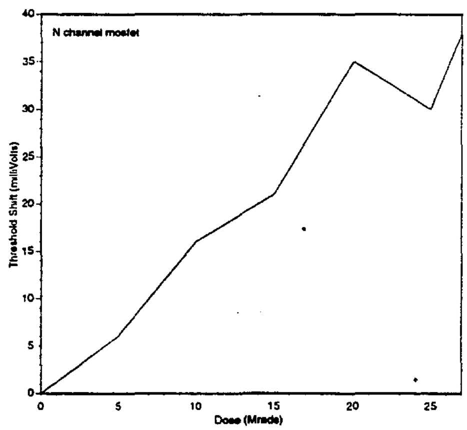


Figure 2: Threshold shift for the NMOS device as a function of dose.

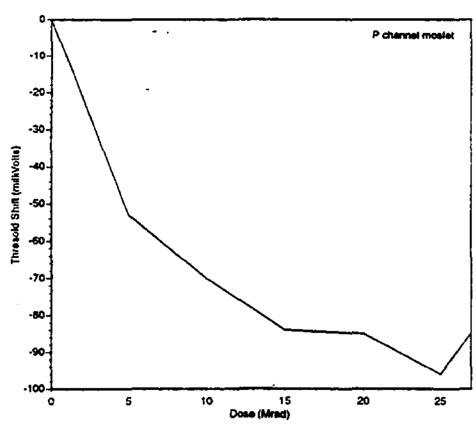


Figure 3: Threshold shift for the PMOS device as a function of dose.

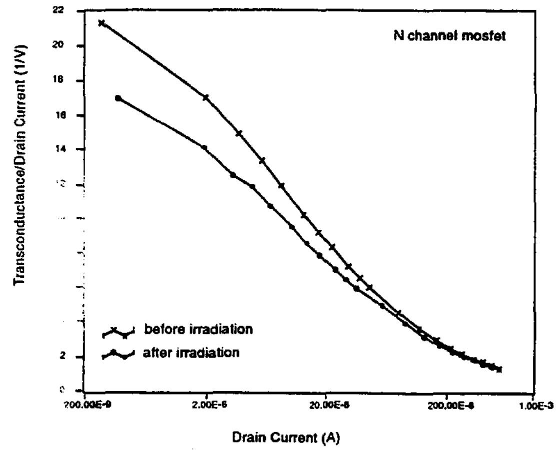


Figure 4: Plots of g_m/I_D before and after a dose of 27 Mrad (Si) for the n-channel transistor.

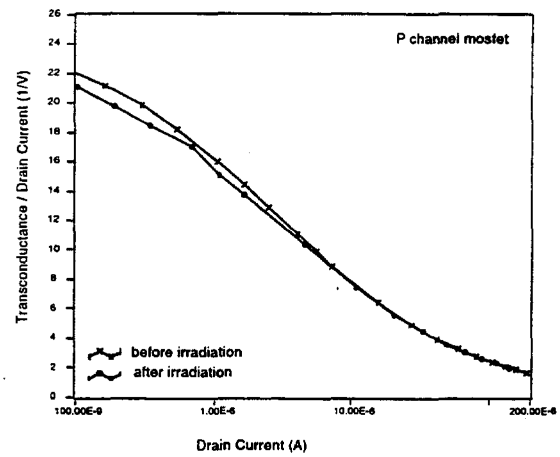


Figure 5: Plots of g_m/I_D before and after a dose of 27 Mrad (Si) for the p-channel transistor.

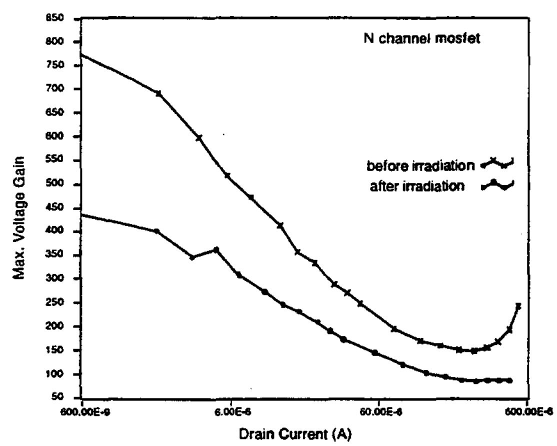


Figure 6: Plots of $A_v(max) = g_m/g_o$ before and after a dose of 27 Mrad (Si) for the n-channel transistor.

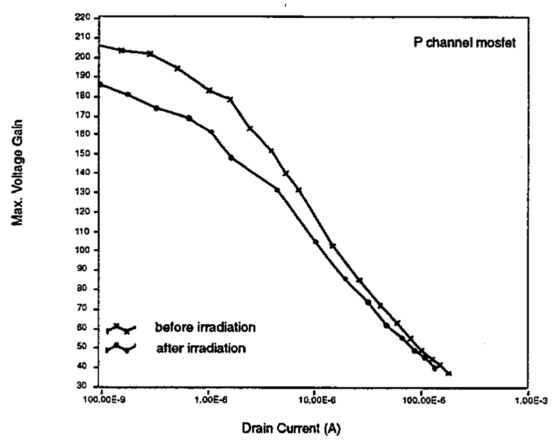


Figure 7: Plots of $A_v(max) = g_m/g_o$ before and after a dose of 27 Mrad (Si) for the p-channel transistor.

C. *Preliminary Noise Measurement*

Noise measurements before and after irradiation at a center frequency of 2 MHz are listed in Table 1.

Table 1
Noise Measured at 2 MHz

FET $(type)$	Dose $(Mrad)$	g_m (μS)	v_N $(nV/\sqrt{Hz})$	v_{N_0} $(nV/\sqrt{Hz})$
NMOS	0	140	20	9
NMOS	27	125	40	9
PMOS	0	88	22	11
PMOS	27	95	32	11

The measurement conditions correspond to the operating point of the input transistor, $I_D = 10\ \mu A$ and $V_{DS} = 500\ mV$. The spectra in the interval 1-3 MHz were observed to be flat. In Table 1, v_N is the measured rms noise voltage per $\sqrt{\text{Hz}}$. An estimate of the thermal noise expected from the channel resistance, $v_{N_0} = \sqrt{(0.67)4kT/g_m}$, is included for comparison. Prior to irradiation, v_N is approximately twice v_{N_0} for both the n- and the p-channel devices. After a dose of 27 Mrad, there is a further increase of 100% in v_N for the n-channel device and 50% for the p-channel.

These effects may be understood in the context of a recent model for excess apparent white noise in SOI MOSFETs proposed by F. Faccio *et al.* [8], in which the excess comes from thermal noise associated with the body resistance, increasing as the body resistance increases. The input-referred noise amplitude was observed to change as the body resistance was varied via the body or backgate bias. This provides a possible method for reducing the noise. In our case, the body resistance can vary in response to radiation-induced positive charge in the buried oxide. We are currently carrying out more detailed noise measurements and investigating these effects in the Honeywell devices.

IV. Conclusions

Our preliminary conclusion is that the pixel front-end would continue to operate in the LHC environment. Noise remains a primary concern since the discriminator threshold needs to be approximately five times the expected noise level to prevent overloading the data acquisition system with random hits. More detailed noise measurements and circuit simulations are currently underway, including measurements of the effects of body and backgate biasing on noise.

V. Acknowledgements

We are grateful to Dr. C. Castaneda of the UC Davis Crocker Nuclear Laboratory (CNL) for assistance with the test beam and to CNL for granting development time for this run. We wish to thank the UCD Physics Department Electrical Engineer, B. Holbrook, for developing the noise measurement apparatus. It is a pleasure to acknowledge useful comments, information and suggestions from S.T. Liu and M. Flanery of the Honeywell Solid State Electronics Center and from P. Seller.

VI. References

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[6] The proton radiation test beam at CNL was set up and instrumented through a joint effort of CNL and the U.S. Naval Research Laboratory.

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Performance of a CCD tracker at room temperature

T. Tsukamoto (Saga Univ.)

T. Kuniya, H. Watanabe (Saga Univ.);
A. Miyamoto, Y. Sugimoto (KEK);
S. Takahashi, N.Tamura (Niigata Univ.);
K. Abe, T. Nagamine, Y. Shirasaki (Tohoku Univ.);
T. Aso (Toyama National College of Maritime Technology)

1

Outline

- Introduction
- HPK CCD
- Experimental setup
- Response to charged particles
  - S/N, detection efficiency, energy resolution
  - Position resolution
- Comparison with EEV CCD
- Summary

2

Advantage of CCD for tracking device

- **Pixel detector**
  - **unambiguous reconstruction/high granularity**
- **Thin ←extremely low capacitance**
  - **less multiple scattering**
- **Serial readout**
  - **small number of channels**
- **Continuously sensitive**
  - **no intrinsic limitation as regards trig. rate**
- **Other R&D**
  - **driven by commercial interest (video) as well as X-ray astronomer, etc.**

3

Vertex detector application in future LC

- **Low repetition rate ~150Hz ↔ serial r/o**
- **Highly collimated jets ↔ pixel detector**
- **Backgrounds ↔ pixel detector**

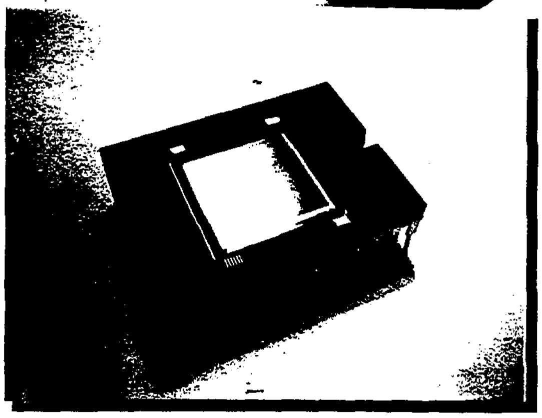
Operation at room temp. (~0°C) ⇒ compact cooling system

- **to reduce material**
- **to keep mechanically stable**
- **to avoid interference with the beam monitor**

4

Hamamatsu (HPK) CCD

- **Feature**
  - Full frame transfer type
  - 2phase CCD
  - MPP operation to reduce dark current
- **Developed for scientific researches**
  - Low light level measurements (e.g. spectroscopy)
  - X-ray astronomy



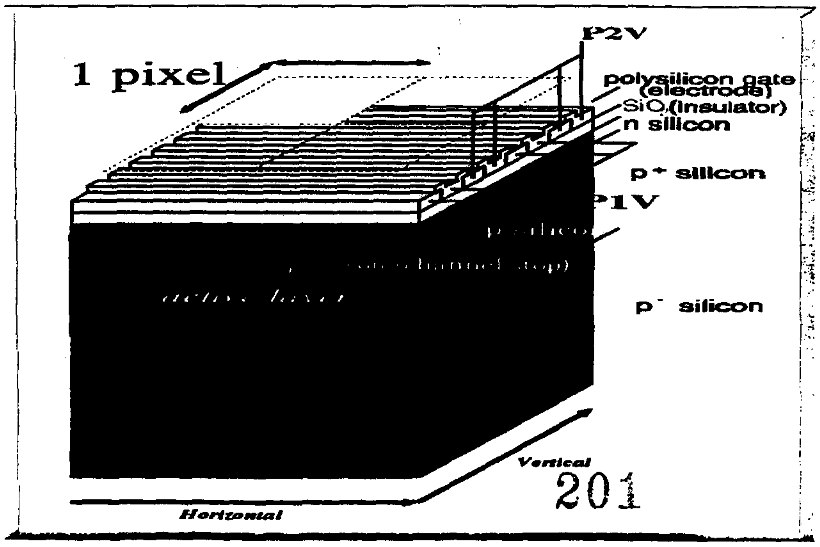
⇒ How about MIP detection?

Application for high energy physics

especially at higher temperature

Structure of CCD

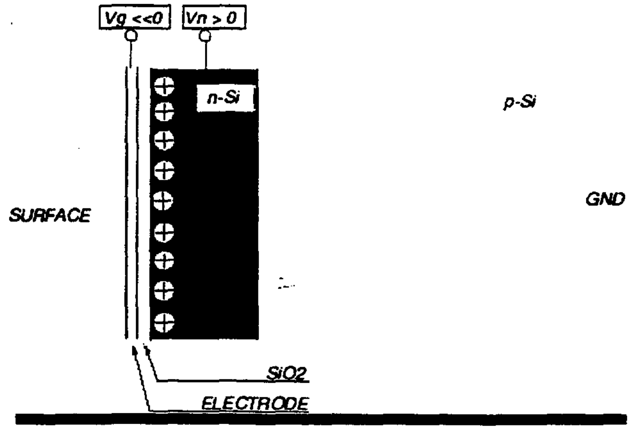
- **HPK S5466: Full Frame Transfer Type (2phase)**



MPP(Multi Pinned Phase) Operation

"Inverted Operation" in other words

- **Holes are accumulated under Si/SiO_2 interface.**
- **Thermal excitation of electrons is significantly suppressed.**



⇒ Reduction of the dark current by one order of magnitude

7

Specification

- **CCD: Hamamatsu S5466**

Type	2phase FFT-CCD
#pixels	512×512
Sensitive area	24μm×24μm
Active layer in depth	~10μm
Sensitivity	2.0μV/electron
Charge transfer eff.	>0.99995

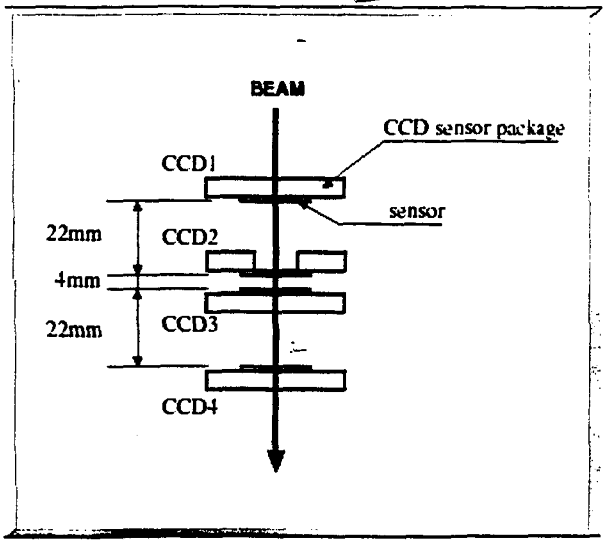
- **Driver: Hamamatsu C5934-1010**

Gain	×55
H-clock	250Hz
V-clock	62.5Hz

8

Experimental setup

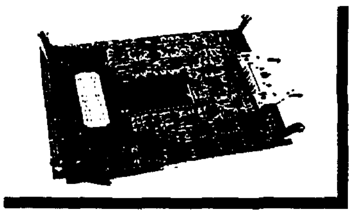
- **4 layers**
  - **to reduce random hits**
  - **minimize multiple scatterings**
    - **a special package w/ a hole**
    - **CCD2 & CCD3 as close as possible**
- **KEK PS T1 line**
  - **4 sec/cycle**
  - **2.0GeV, 1.0GeV, 0.5GeV (π^-)**



9

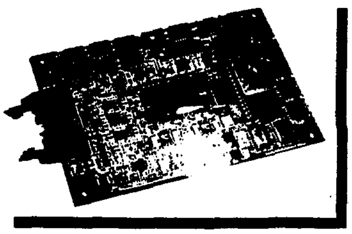
Setup

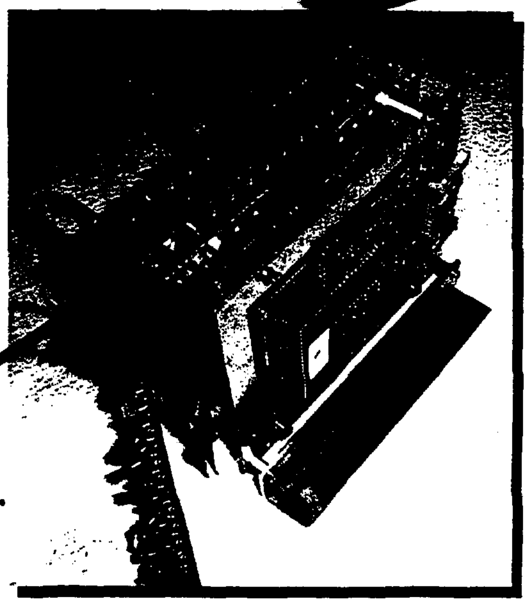
- **Standard CCD**



1.2mm Al_2O_3 behind the chip

- **Special CCD w/ a hole**

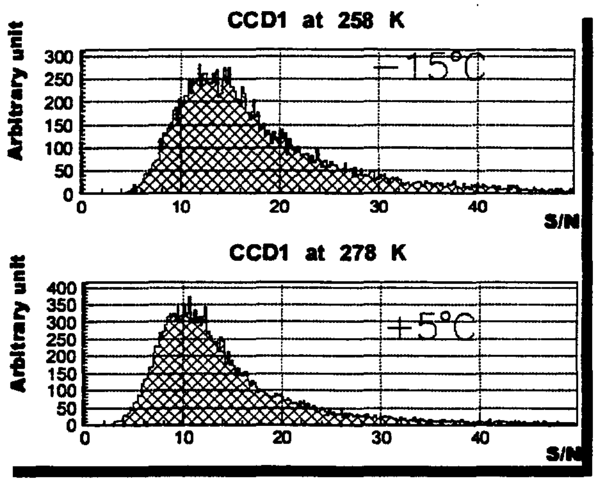


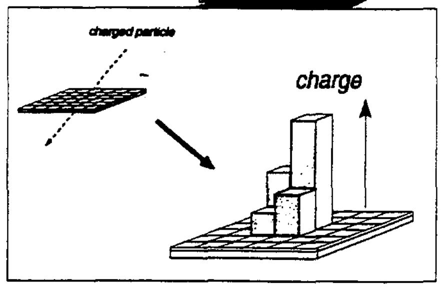


2nd layer

Response to Charged Particles

- 2x2 clustering
- S/N

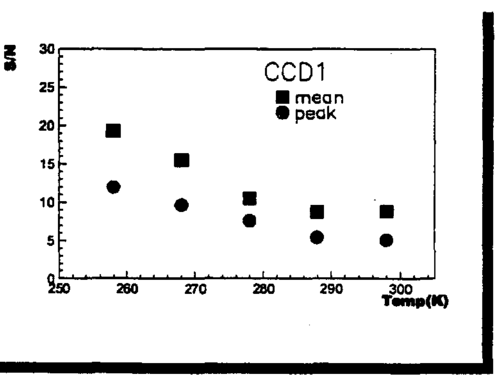




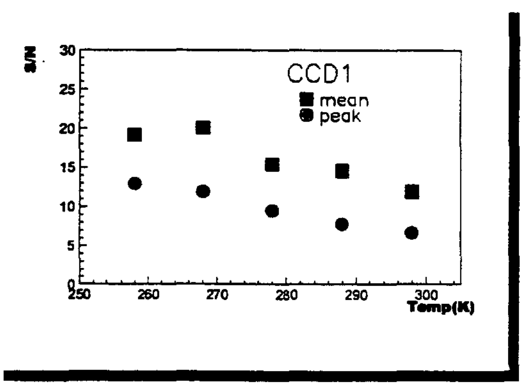
11

S/N as a function of temperature

- 4sec readout cycle



- 1.3sec readout cycle

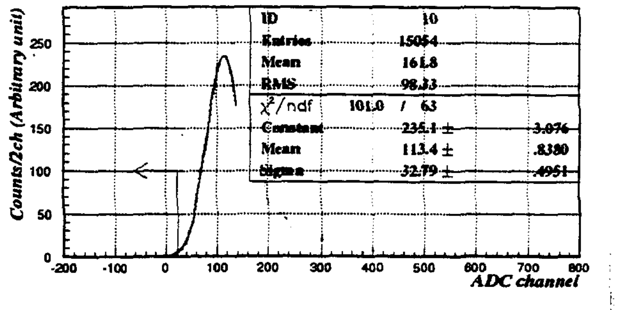


12

Detection Inefficiency for MIP

- **Detection inefficiency**

  assume Gaussian shape in the low energy side of Landau

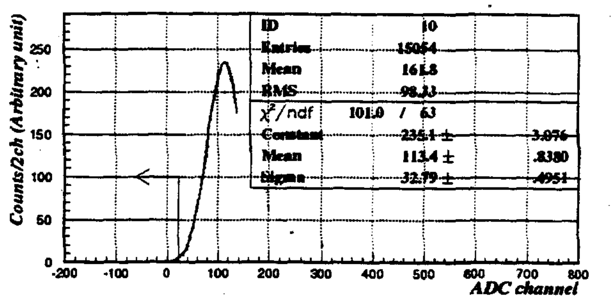


Temp.	Inefficiency (%)
−15℃	0.00±0.03(stat)±0.03(sys.)
+5℃	0.05±0.04(stat)±0.04(sys.)

Energy Resolution for MIP

- **Energy resolution**

[redacted]



Temp.	Ereso (%)
−15℃	28.9±0.5
+5℃	33.2±0.5

Position Resolution

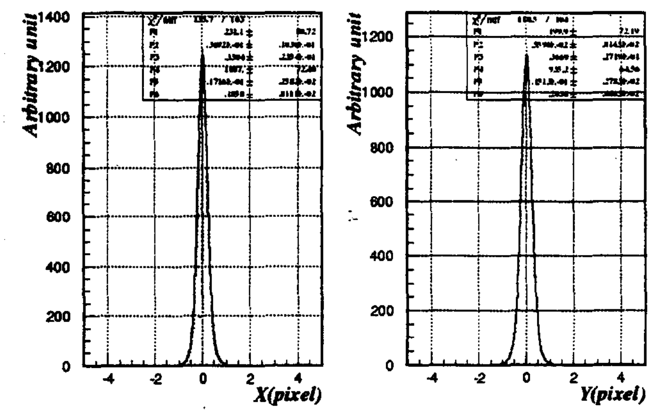
- **After the careful alignment...**

- **Position resolution**

Two components seen

⇓

can fit to double Gaussian



Charge sharing ↔ Position resolution

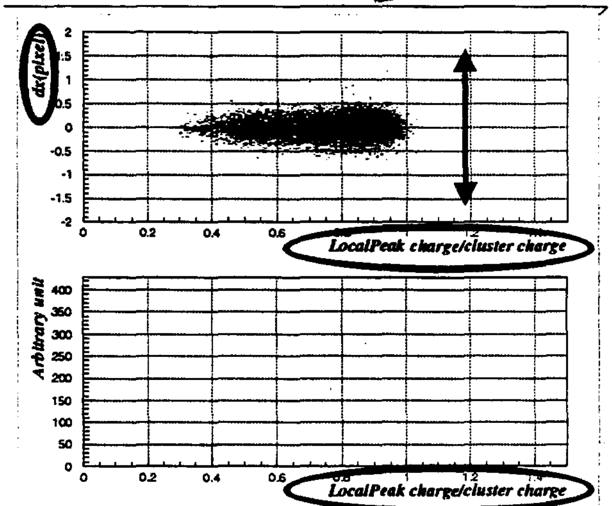
- **Charge sharing**

[redacted]

As "ratio" gets close to 1,

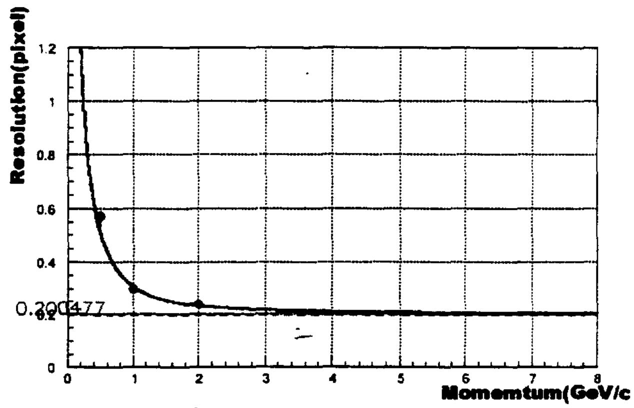
Position resolution gets worse.

$\because 1/\sqrt{12}$ component increases



Momemtum dependence of position resolution

- Position resolution as a function of p
- Fits well to the formula (multiple scattering)



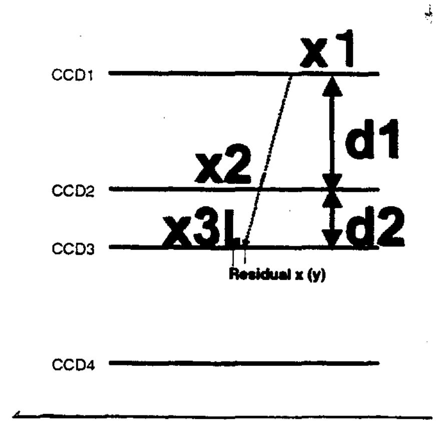
Resolution
→ 0.20 ± 0.01 pixel

Intrinsic Resolution

- **Assuming all the sensors have the same resolution,**

$$(\sigma_{obs})^2 = (\sigma_2)^2 + \left(1 + \frac{d_2}{d_1}\right)^2 (\sigma_1)^2 + \left(\frac{d_2}{d_1}\right)^2 (\sigma_0)^2$$
$$= 2.56 \cdot (\sigma_{intrinsic})^2$$

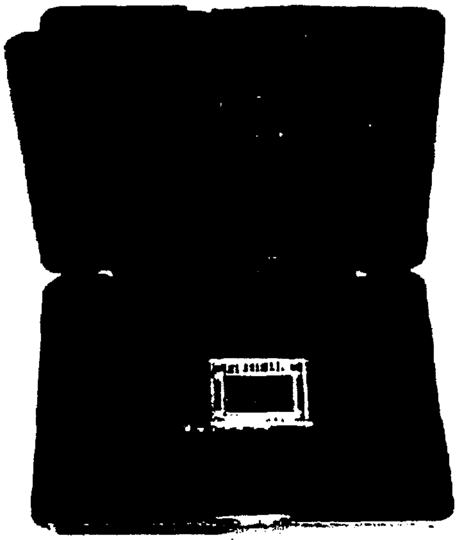
where $\sigma_{intrinsic} = \sigma_0 = \sigma_1 = \sigma_2$



- $\sigma_{intrinsic}$= **3.0±0.2μm** (weighted σ w/ double Gaussian)
- $\sigma_{intrinsic}$= **3.6±0.2μm** (RMS)

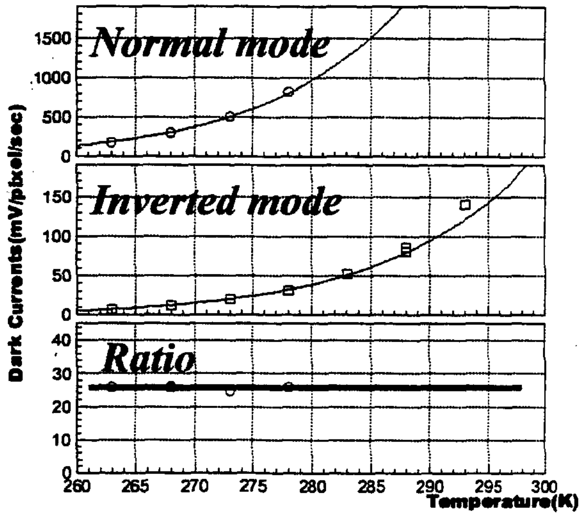
EEV CCD

- **CCD 02-06**
  - **#pixels: 385(H)×578(V)**
  - **pixel size: 22μm×22μm**
  - **active depth: 20μm**
- **Two operation modes**
  - **normal mode**
  - **"inverted mode" ="MPP mode" in HPK**



EEV normal mode v.s. inverted mode

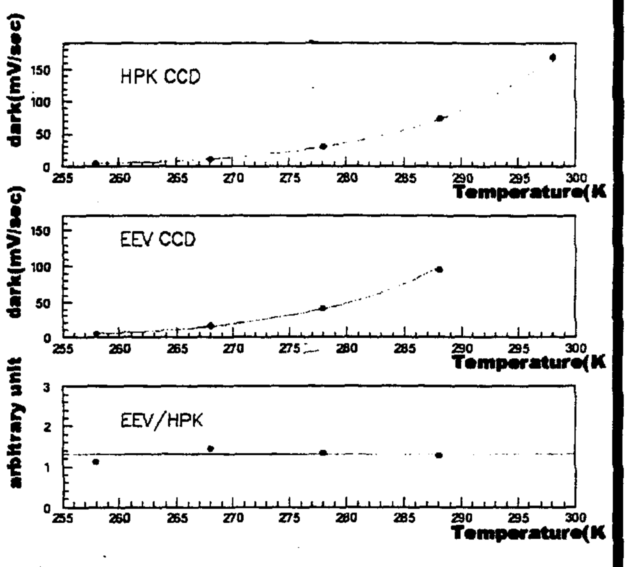
- **Dark current**
- **Suppression factor ~25**



Comparison of the dark current

- HPK(MPP) vs EEV(inverted)
- Similar in mV
  EEV = HPK×1.3
- But measured gain
  EEV = HPK×0.5

Dark current in electrons
for CCD's under our study
EEV = HPK × 2.5



Summary

- MIP's are successfully detected using HPK CCD
- Operation at room temperature ~0°C
  - S/N >10 up to +5°C
  - efficiency very close to 100%
  - position resolution: 3.0μm
- Comparison with EEV CCD
  - Both "MPP" and "inverted" mode suppress the dark current by one order of magnitude

Future prospects

- Tracking performance of EEV CCD will be examined in June.
- Radiation damage
  - affects CTE(Charge Transfer Efficiency)
  - CTE measurements are on-going.
  - Irradiation with a strong ^{90}Sr will take place in the near future.

A medical imaging system based on a GaAs pixel detector read-out by a single-photon counting VLSI electronics.

P. Maestro

Dipartimento di Fisica and INFN, Pisa, Italy

Abstract

GaAs pixel detectors have been studied and tested to choose the best ones regarding charge collection properties and to improve the ohmic contacts deposition technology. With a 36-channels read-out electronics operating in single-photon counting mode, images of low-contrast details on a standard mammographic phantom have been collected, showing better imaging capabilities of this detector in comparison with the typical film-screen systems at the energy of the mammographic clinical X-rays tube.

Real application of this system in early diagnosis of the breast disease requires the extension of the detector sensitive area and the development of a VLSI read-out electronics, capable of handling many thousand channels and bump-bonded to the GaAs pixels. A front-end chip (MEDIPIX) has been designed by the CERN micro-electronics group and electric threshold measurements have been performed using a custom read-out system composed of three standard VME boards and a C language software.

1 Digital mammography

Radiography is based on the measurements of the differential attenuation of X-rays passing through non-uniform biological tissues. In standard radiography a photographic emulsion is used to detect the photons transmitted through the patient, together with a fluorescent screen which improves the detection efficiency. The film carries all of the information contained in the image, which is displayed as an optical density pattern [1].

The term "digital radiography" indicates systems capable of recording images in numerical form and of handling the data after the acquisition. The image is made of an array of pixels, each one associated with a grey level deriving from the analog to digital conversion of the detector signals. Then an image

processing software, improving contrast resolution and signal-to-noise ratio, allows digital radiography to obtain different views of the examined tissue with a single patient exposure and to increase diagnostic informations. Moreover the choice of a detector more sensitive to radiation than the screen-film system can reduce the dose to the patient.
Mammography in particular would largely take advantage of an improved performance in terms of contrast, due to the little difference in the X-rays attenuation coefficients between healthy breast tissues and tumourous masses (as large as few mm), which makes the early detection of the disease dramatically difficult [2].

2 The detector choice

Gallium Arsenide is a good candidate in the construction of a detector for medical imaging. Its high Z-number (31, 33) implies a great photoelectric absorption cross-section in the diagnostic energy range (20-60 KeV), and a consequent higher detection efficiency with respect to silicon, in spite of the fact that the latter exploits a more consolidated development technology.
At the mammography X-rays average energy (20 KeV) a GaAs 200 μm thick detector shows a 100% efficiency, greater than either a 300 μm thick silicon detector (about 24%) or a film-screen system (about 55%). Germanium, though being more favoured due to its higher Z, is excluded from this kind of applications because of the low required temperature operation.
Gallium Arsenide offers also the advantages of a great resistivity (order of $10^8 \Omega \cdot$ cm), which reduces the leakage current, and of a high electron mobility, which means faster detector response signals [3].

GaAs detectors differ for construction technique and kind of ohmic contact. These technologies are often empirically developed by industry and aim at the improvement of the charge collection and efficiency properties of the detectors.
The most used methods of growing GaAs crystals are the Liquid Phase Epitaxy (LPE) and the Liquid Encapsulated Czochralski (LEC). The LPE GaAs detectors show on one side a maximal bias indipendent charge collection efficiency (c.c.e.), thanks to the absence of trapping and recombination centers in the crystal (such as in silicon detectors), and on the other side a low detection efficiency, because the material built in this way is characterized by a thin depth [3, 4]. On the contrary, the LEC GaAs detectors are thicker and then more efficient, but worse regarding the charge collection properties, because of the high concentration of crystal impurities. Therefore the c.c.e. can be increased developing new ohmic contacts on LEC SI-GaAs crystals, which intensifies the electric field in the depletion region [5, 6].

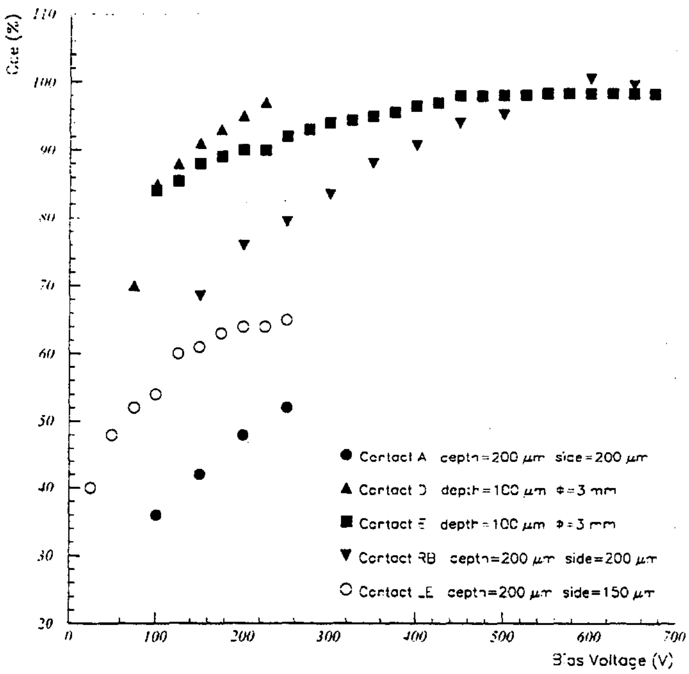


Figure 1: *Charge collection efficiency as a function of the bias voltage of six GaAs detectors, differing for ohmic contact type, thickness and geometry. The measured errors are 5% on the detectors called A, RB, LE, 12% on D and E.*

Concerning the read-out electronics, the approach we have considered is a single photon counting system, which allows to reach a better contrast definition than an integrating readout system ([7]). The pixel detector architecture is the most suitable topology for a 2-dimensional reconstruction of the image. Each pixel has linear dimensions of the order of hundred microns, so to meet the stringent requirement of submillimetric spatial resolution in the imaging applications, and is read-out by a corresponding electronics channel.

A first prototype of digital mammography detector has been built; it consists of a 36-pixels LEC SI-GaAs 200 μm thick detector, with ohmic contacts studied to obtain a complete c.c.e. (fig. 1) [8, 9], and of a discrete-components electronics, where each channel has a preamplifier, a shape amplifier, a discriminator with externally adjustable threshold and a counter.

Images of low-contrast details on a standard mammographic phantom have been obtained by this system (fig. 2). It has been verified that the GaAs detector can "see" details with contrasts lower than 3%, limit achievable by traditional film-screen systems [10].

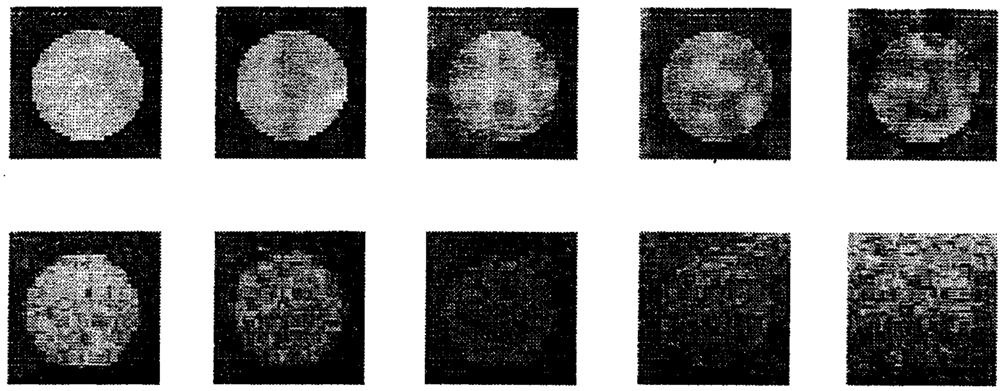


Figure 2: *Details no. 1-5 from the TORMAS phantom: nominal contrast here are from left to right respectively 8.5%, 5.5%, 3.8%, 2.6% and 2.0 %. The upper images are produced with 36-pixels GaAs detector, the lower ones with a traditional film-screen system. Distance focus-detector 64 cm. Exposure 12.5 mAs.*

3 The Front-End Electronics and Read-Out System

In order to cover surfaces of diagnostic interest a front-end chip (MEDIPIX) has been designed to read-out the GaAs detector with thousands of pixels [11]. The chip is derived from the OMEGA3 chip [12], developed at CERN. MEDIPIX contains 64×64 square cells with side 170 μm, each one provided with a bump-pad (24 μm diameter) on which the corresponding single pixel of the detector is to be bump-bonded. The chip has been built with SACMOS 1μm technology, by FASELEC (Zurich). The total area covered by the chip is 1.7cm^2, consequently a wider major surface can be obtained assembling many chips in ladders.

Figure 3 shows a scheme of the MEDIPIX architecture. Each channel is composed by a charge sensitive preamplifier, a comparator with an externally set threshold, a shaping delay and a 15-bit pseudo-random counter. The preamplifier receives as input, either the detector signal, via the bump-bonding pad, or a test signal from an external pulse generator.

The operation mode of each cell is configured via 5 bits. This array of 5×4096 bits is called mask. The chip is self-triggering i.e. after a reset, the comparator is sensitive to signals larger than the threshold. In addition to a common threshold (the same for the 4096 pixels), each pixel threshold can be separately adjusted, with a 3-bit resolution, so to compensate for non-uniformities among channels (three of the five bits in the cell's mask).

Moreover 5 currents have to be externally set as analog biases to MEDIPIX: two of them are used to fix the working point of the preamplifier, one sets the length of the shaped signal, two adjust the levels of the common and single channel thresholds. The single-photon counting is performed by the chip at a

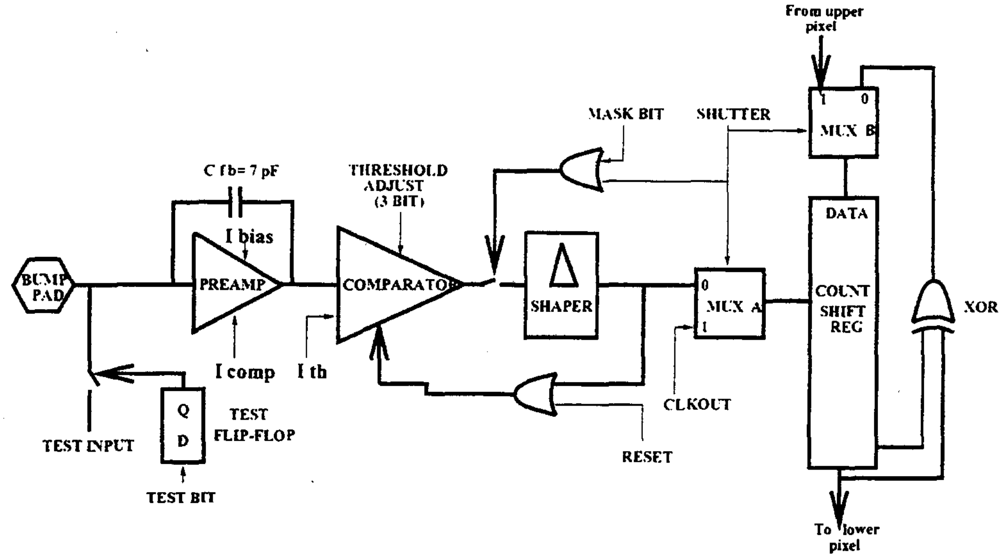


Figure 3: *MEDIPIX: chip electric scheme.*

maximum acquisition rate of 500 kHz, while its maximum read-out frequency is 10 MHz.

MRS (MEDIPIX Read-Out System) is the read-out system, designed and produced in collaboration with LABEN (Italy) to test and handle data from MEDIPIX. MRS is based on standard VME and consists of 3 boards: the VMEboard, the MOTHERboard and a custom CHIPboard.
The present CHIPboard hosts two chips and contains the circuits to transmit the analog currents MEDIPIX needs. The MOTHERboard is a stand-alone card without active elements but only containing the digital buffers for the differential signal transmission from VMEboard to chip. The VMEboard is a standard 6U single slot VME card divided into two parts; the analog one with the DACs generating the analog biases and the power supplies for MEDIPIX, and the digital one containing all the system logic controls and organized in four FPGA (Master, Decoder, Mask-Data and Counter-Data).
MRS allows four operation phases:

1. SETUP phase. This includes the mask loading, the setting of the analog biases and power supplies to the chip, the counters reset.

2. ACQUISITION phase. MEDIPIX acquires data from the detector.

3. TEST phase. MEDIPIX acquires data from a pulse generator interfaced to the system.

4. READOUT phase. The system stops acquisition and reads the chip counters.

The software to control MRS (Medisoft) has been written in C on a OS9 environment. It has a menu structure which allows the operator to select and execute the different routines in the four operation phases and to implement new functions which prove useful during the test of the system, without changing the main architecture of the software itself.

4 Electric threshold calibration of MEDIPIX

A set of MEDIPIX chips on a wafer have been electrically tested, before being bump-bonded to the detector.

After checking the digital part of each chip (writing and reading-out masks on the counters), the correct working values of the analog biases have been searched and then the pixels thresholds in each MEDIPIX have been calibrated sending pulses from a generator to the test input (1 mV pulse corresponds to about 100 electrons charge on the test capacitance of 16 fF).

The threshold should be set as low as possible because the goal is to detect signals of about 4000 electrons i.e. the charge collected by a 90% efficient GaAs detector every time a 20 keV photon is stopped in the crystal; a 5 standard deviations cut means to have a threshold of 2500 e^- with a noise of 300 e^-. So the first operation is to set a common (to all 4096 pixels) threshold low enough to avoid wrong counts induced by electronic noise (fig. 4).
Then the fine threshold adjustment has been performed setting the 3-bit mask so to narrow the distribution (fig. 5). In this way the final result is an average threshold in the most performing chips of 1400 electrons, with a 80 electrons spread on the 4096 pixels, better than the initial requirements.

5 Conclusions

Test on the "brick" obtained by the bump-bonding of the GaAs pixel detector to MEDIPIX will start in the next months and will consist first of the threshold calibration of each pixel using radioactive sources, and then of the production of phantoms images, such as it has been done with the 36-channels prototype. At the same time Montecarlo simulations are being run in order to evaluate (in terms of low dose, minimum image faking and costs) the best detector's scanning configurations, when more "bricks" will be assembled to form a sensitive area of mammographic interest (typically 18 $\times$ 24 cm^2).

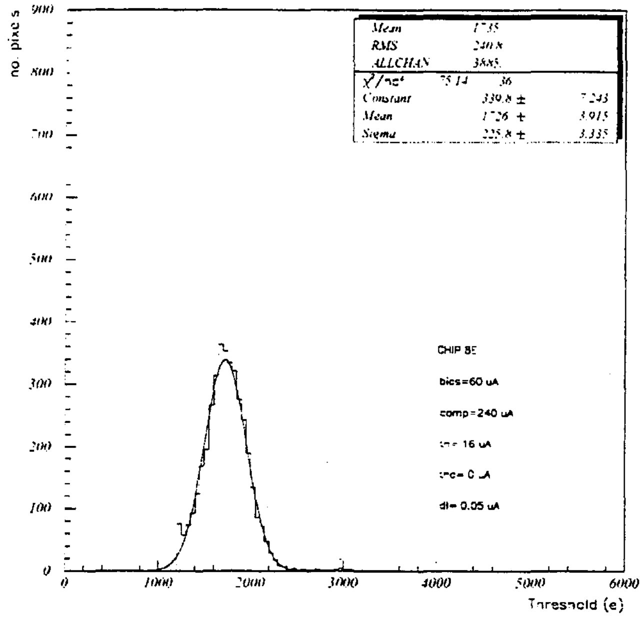


Figure 4: *Distribution of thresholds for the MEDIPIX named 8E (from the position on the wafer) with the common setting of threshold current.*

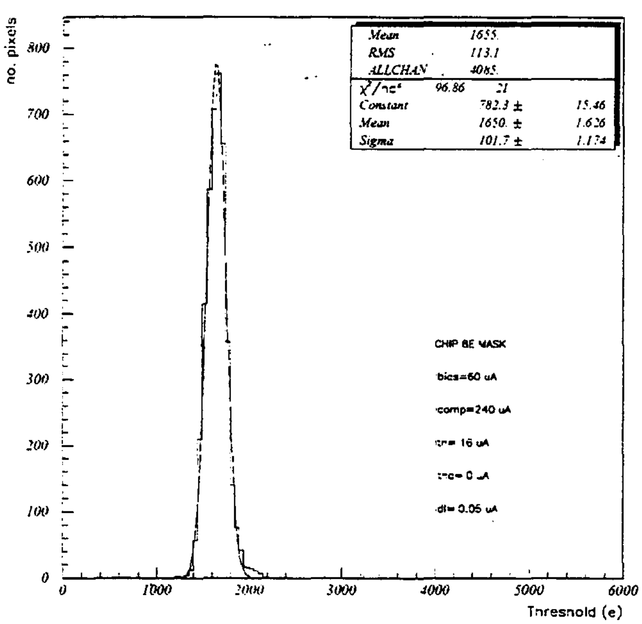


Figure 5: *Distribution of thresholds for the MEDIPIX 8E after the threshold currents adjustment in each single pixel.*

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A 5 Million Frame per Second Radiography System Using High Energy Protons

The author list, which is fairly long is:

H.-J. Ziock, K. J. Adams, K. R. Alrick, J. F. Amann, J. G. Boissevain, M. L. Crow, S. B. Cushing, J. C. Eddleman, C. J. Espinoza, T. T. Fife, R. A. Gallegos, J. Gomez, T. J. Gorman, N. T. Gray, G. E. Hogan, V. H. Holmes, S. A. Jaramillo, N. S. P. King, J. N. Knudson, R. K. London, R. P. Lopez, J. B. McClelland, F. E. Merrill, K. B. Morley, C. L. Morris, C. T. Mottershead, K. L. Mueller, Jr., F. A. Neri , D. M. Numkena, P. D. Pazuchanics, C. Pillai, R. E. Prael, C. M. Riedel, J. S. Sarracino, H. L. Stacy, B. E. Takala, H. A. Thiessen, H. E. Tucker, P. L. Walstrom, G. J. Yates, J. D. Zumbro
(Los Alamos National Laboratory, Los Alamos, NM 87545)

E. Ables, M. E. Aufderheide, P. D. Barnes Jr., R. M. Bionta, D. H. Fujino, E. P. Hartouni, H.-S. Park, R. Soltz, D. M. Wright
(Lawrence Livermore National Laboratory, Livermore, CA 94550)

M. Amman, JF. Beche, E. Beuville, V. Douence, L. Fabris, F. Goulding, N. Madden, J. Millaud, B. Turko, J. Walton, J. Zaninovich
(Lawrence Berkeley National Laboratory, Berkeley, CA 94720)

S. Balzer, P. A. Flores, R. T. Thompson
(Bechtel, Nevada, Los Alamos Operations, Los Alamos, NM 87545)

R. Prigl, J. Scaduto, E. T. Schwaner
(Brookhaven National Laboratory, Upton, NY 11973)

A. Saunders
(University of Colorado, Boulder, CO 80309)

J. M. O'Donnell
(University of Minnesota, Minneapolis, MN 55455; current address: Los Alamos National Lab)

Abstract:

We have developed a technique for taking multiframe radiographic images of dynamic objects up to hundreds of g/cm^2 thick using high energy protons as the probing particles. The technique is capable of simultaneously determining the amount, location, and types of material present in the object. The basic principles of the technique will be presented as will be radiographs taken using 10 GeV protons at the Brookhaven AGS, and 800 MeV protons at the Los Alamos LANSCE facility. Finally detector system concepts for this application will be presented.

The work presented in the poster session is covered in detail in two papers which are to appear in Nuclear Instruments and Methods as part of the proceedings of the 3rd International Symposium on Development and Application of Semiconductor Tracking Detectors, Melbourne, Australia, December 9-12, 1997. The preprints of those papers, LA-UR-98-1015 and LA-UR-98-1368, are included herein.

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DETECTOR DEVELOPMENT FOR DYNAMIC PROTON RADIOGRAPHY

H.-J. Ziock, K. R. Alrick, R. A. Gallegos, J. Galyardt, N. T. Gray, G. E. Hogan, V. H. Holmes, S. A. Jaramillo, N. S. P. King, T. E. McDonald, Jr., K. B. Morley, C. L. Morris, D. M. Numkena, P. D. Pazuchanics, C. M. Riedel, J. S. Sarracino, G. J. Yates, J. D. Zumbro
[Los Alamos National Laboratory (LANL)]

M. Amman, JF. Beche, E. Beuville, V. Douence, L. Fabris, F. Goulding, N. Madden, J. Millaud, B. Turko, J. Walton, J. Zaninovich
[Lawrence Berkeley National Laboratory (LBNL)]

ABSTRACT

The development of high frame rate imaging charged particle detector systems for proton radiography at an advanced hydrotest facility (AHF) is discussed. The detector systems being developed are to be capable of providing a movie of dynamic events with inter-frame times as short as 200 nanoseconds and with spatial resolutions of 1/2 mm or better. Initial results from beam tests of a 1024 frame 8^2 pixel silicon detector prototype device and a four frame 1024^2 pixel electro-optically shuttered camera system will be presented.

INTRODUCTION

A promising new technology, proton radiography, for performing dynamic radiography on thick objects (100's of gm/cm^2) is being developed as part of the US Science Based Stockpile Stewardship program. The general concept of proton radiography (PRAD) is addressed in a separate paper in these proceedings[1]. In this paper we discuss the detector systems being developed for the PRAD project. The detector performance that we hope to achieve is given in Table 1. The detector development effort is broken into two separate parts. The first is aimed at providing limited multi-frame capability in a short time scale for rapid experimental verification of the PRAD concept. The second is longer term and addresses the full set of requirements given in Table 1, and if possible maintains a flexible design, capable of expanding to go beyond those requirements as they are likely to be a moving target. Before proceeding to the details of the detector development effort, we briefly review the basic detector options and their limitations.

Protons, being charged particles, themselves interact with the detector medium leaving an ionization trail that can be detected directly or indirectly. In ionization detectors, gaseous or solid state, the positively charged ions and negatively charged ions or electrons of the ionization track are separated and collected to form the signal directly. For silicon detectors it takes 3.6 eV of energy loss by the incident particle to generate one electron-hole (eh) charge pair on the average, although the fundamental energy loss mechanism for charged particles involve ~17 eV quanta[2]. The specific ionization energy loss for a minimum ionizing particle (MIP) in silicon results in an average of about 80 eh pairs per μm. The other means of signal generation is indirect, such as in a scintillator where the ionization is turned into light, which is collected and turned back into a second electric signal by, for instance, a photocathode or a photodiode. This entire process is rather inefficient, requiring on the order of 100 eV of energy loss in plastic scintillator to produce a photon which is difficult to collect and turn back into an electrical signal. The specific ionization in the plastic scintillator we used resulted in about 17,000 photons emitted into 4π steradians per cm of plastic scintillator for a MIP. Mirroring the back surface of the scintillator is at best only about 80% efficient so one can only achieve about 15,000 forward (into 2π steradians) photons.

Table 1: Detector Performance Goals	
Frames to be read out	~ 100 or more
Time spacing of frames	~ 200 nsec
Duration of frame (strobed)	~ 10 nsec
Spatial resolution at object	~ 1/4 mm pixel
Region to be imaged	~ 10 cm
Mass density accuracy	~ 1% or better
Particles detected / element	≥ 25,000
Maximum signal per pixel	~ 250k particles
Accuracy	~ 12 bit

LIGHT COLLECTION

Schematically a light based detector system for PRAD will resemble what is shown in Fig. 1. Light is generated in a scintillator, which is located in the image plane of the PRAD magnetic lens[3], reflected by

LA-UR-98-1015

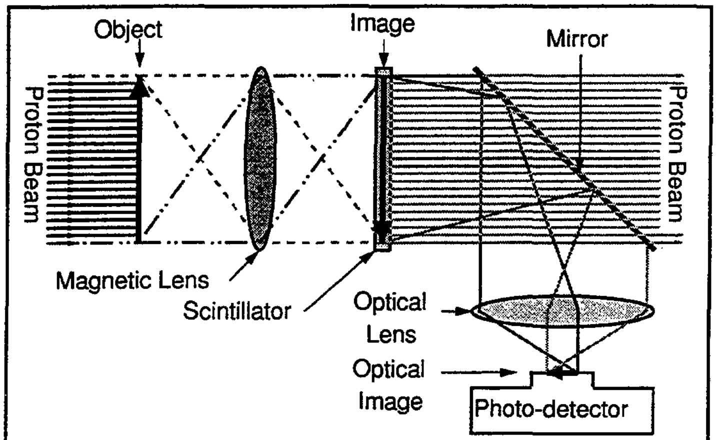

Fig. 1. Schematic of a PRAD light imaging system.

a 45° mirror out of the path of the proton beam, and then collected and imaged by an optical lens onto the photo-detector plane that creates the electrical signal. The above assumes that the photo-detector is itself sensitive to charged particles and must therefore be out of the proton beam. Although one could in principle use fiber optics to carry the light directly from the scintillator to the photo-detector, and thereby avoid the use of the mirror and lens, in practice this results in undesirable complications. First, the clear fiber array must have the same dimensions as the scintillator which according to Table 1 is on the order 10 cm on an edge if we assume that the magnetic lens is an identity lens. In bending the fibers at 90° to the beam direction, in order to get them out of the beam requires a depth for the clear fiber array of at least 1/2 the scintillator edge dimension and in reality it will be somewhat larger, especially if a 90° kink can't be made and instead one needs a smooth bend. These clear fibers will introduce a substantial amount of undesirable material in the beam creating background problems. This would severely limit the feasibility of using multiple planes of detector. The second problem is that Cerenkov light will be generated in the clear fibers. This becomes a problem as the fibers are being diverted to exit the region of the beam. At that point, light will be generated in clear fibers which are not connected to the ones that the proton will strike in the scintillating fiber array, resulting in an additional background problem. The Cerenkov problem can be minimized as the Cerenkov light is emitted in a forward direction and is broadband. This would however require the complication of using narrow bandpass filters for the scintillation light and choosing the proper fiber geometry.

Instead of trying to cope with all the problems associated with a fiber readout, we decided to use the mirror–lens coupled solution which has its own, but much more straight forward problem, namely the small amount of light captured by a lens system. This is especially true when the lens is operated with a magnification which is less than unity as is required when the photo-detector such as a microchannel plate (MCP), proximity focus diode (PFD), or CCD is much smaller in size than the object being imaged.

An optical lens system is used to form an image of the downstream face of the scintillating fiber array on the light detection device. The lens also serves the purpose of demagnifying the object to a size such that the image fits onto the detector. A lens does this rather inefficiently, capturing only a very small fraction of the light generated. The fraction of the light emitted in a forward direction (into 2π) that is captured by a lens which accepts a cone of half opening angle θ is simply

$$fraction = 1 - \cos(\theta). \quad (1)$$

Using various relationships for optics, the half cone acceptance angle for a lens system can be rewritten as

$$\theta = \mathrm{atan}\{ 1 / [2F(1 + 1/M)] \} \quad (2)$$

where F is the f - number (F#) of the lens (= focal length / effective diameter) and M is the magnification (typically less than unity in our application). Thus the fraction of forward light (0° to ±90°) accepted by a lens system from a point source is

$$fraction = 1 - \cos\{\mathrm{atan}[M/(2F(1 + M))]\} \quad (3)$$

The angle θ is still not the half cone angle into which light is emitted by the scintillator, as the light is refracted to larger angles on leaving the high index scintillator into the air. The emission angle in the scintillator θ', which the lens accepts is thus considerably smaller than the already small acceptance half cone angle of the lens by an amount

$\theta' = \mathrm{asin}\{[\sin(\theta)]/n\}$, where n is the index of refraction of the fiber core (we take n = 1 for air). (4)

Putting this all together, one finds:

$$fraction = 1 - \cos\{\mathrm{asin}[\sin(\mathrm{atan}\{ 1 / [2F(1 + 1/M)]\})/n]\} \approx (M^2) / [8n^2F^2 (1 + M)^2], \quad (5)$$

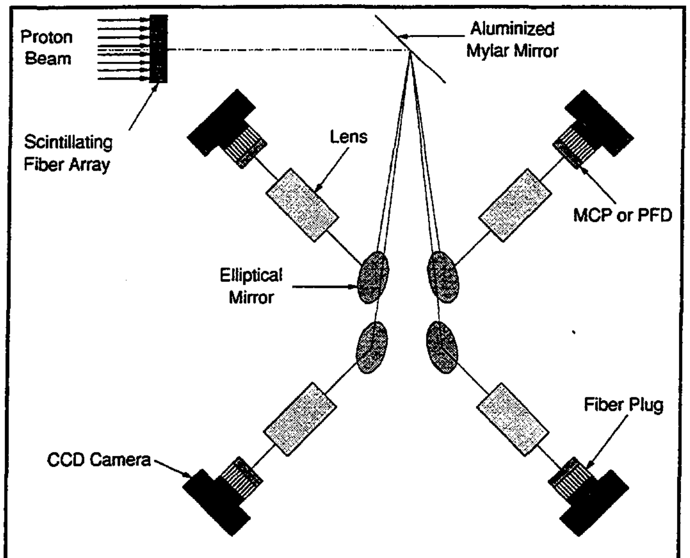

Fig. 2. Schematic of the 4-frame detector system. The cameras and lenses were in a common horizontal plane which was below the proton beam.

where the last result makes use of the small angle approximation for the trigonometric functions. Putting in values representative of those we used ($M = 1/5$, $F = 1.8$, $n = 1.6$) gives *fract* $= 4 \times 10^{-4}$. This value is then further reduced by a number of other factors. These include a packing fraction associated with the active part of the scintillating fiber array (typically < 70%) and the light transmission of the optical system which is < 90%, especially for the blue light emitted by the scintillator. The largest factor is however the quantum efficiency of the light detector which is on the order of 20% for a photocathode and 35% for a CCD. When all the inefficiency factors are taken together, they reduce the overall efficiency of the system another factor of about 10. Taking the total number of forward photons, which in the case of a 2 cm scintillator for MIPs is 30,000 and multiplying by the lens acceptance and other inefficiencies results in about one detected photoelectron per proton and thus very poor counting statistics.

SHORT-TERM SOLUTION

In order to allow us to address a number of issues concerning multi-frame dynamic radiography we developed a limited frame camera system capable of recording images separated by 1 μs or less. Due to the limited development time available, we used off-the-shelf hardware. Our initial attempt involved the use of an IMCO ULTRANAC[4] framing camera. A framing camera consists of a photocatode from which the emitted electrons are accelerated and electrostatically focused to form an image on a downstream, long decay time phosphor screen. Horizontal and vertical electrostatic deflection plates between the photocathode and phosphor screen are used to move subsequent images to fresh locations on the phosphor screen. After some initial tests, this approach was discarded. We found the photocathodes in all our in-hand framing cameras (which were originally bought to be used in experiments dealing with the longer wavelength part of the visible spectrum) were nearly blind to the very blue light emitted by the standard plastic scintillators. Also the small diameter of the photocathode (18 mm diameter) required a reduced lens magnification resulting in even less light. We also had concerns about the potential for distortion in the image caused by space charge effects at the cross-over point of the electromagnetic lens in the framing camera. Stray magnetic fields from the proton imaging lens also distorted the framing camera image.

Our next attempt was based on a set of cooled slow scan CCD cameras, each coupled to a gated image intensifier for shuttering. The shuttering of the different cameras was time phased so that each camera recorded a different time (~ 40 ns burst of protons). The schematic of the camera system adopted is shown in Fig. 2. It should be noted that in this configuration each camera looks at an independent part of the solid angle, thereby avoiding any beam-splitter induced loss of light. The electronic shuttering is based upon our earlier work[5, 6] in electro-optic shuttering of microchannel plate image intensifiers (MCPIIs) by gating their photocathode emission. For some of the cameras we opted for proximity focus diodes[7] (PFDs), which we gated by switching their bias voltage on and off[8]. The intensifiers also provided gain for these weak photon flux experiments and provided wavelength shifting between input and output images for optimal spectral matching to the CCD. Because of the broad requirements for imaging camera system performance, such as wide dynamic range, variable gain, signal-to-noise, and tradeoffs between gain and resolution requirements, we decided to use both DEP[9] MCPII and Proxitronic PFD intensifiers, to exploit and evaluate the features of each type. The MCPIIs have higher gain and faster shuttering with lower high voltage and gate pulse amplitude requirements. The PFDs have higher QE, higher resolution and lower noise, but require much higher bias and gate potentials. Both have adequate dynamic range to effectively use the CCD pixel well capacity. We are still evaluating tradeoffs between the two intensifier types[10]. Results of a dynamic shot using this camera system are shown in Fig. 3, which shows the propagation of a detonation wave in a 28.5 mm radius piece of high explosive (HE).

LONG-TERM SOLUTION

For an AHF class detector system we took an approach which was modular in design and allowed for an evolving set of performance requirements. To demonstrate the basic concept we built a pair of 8 × 8 pixel detector systems designed to meet or exceed all the performance requirements given in Table 1, with the exception of pixel size. Our pixel sizes were (1 mm)^2 and (0.5 mm)^2. There is no problem with building

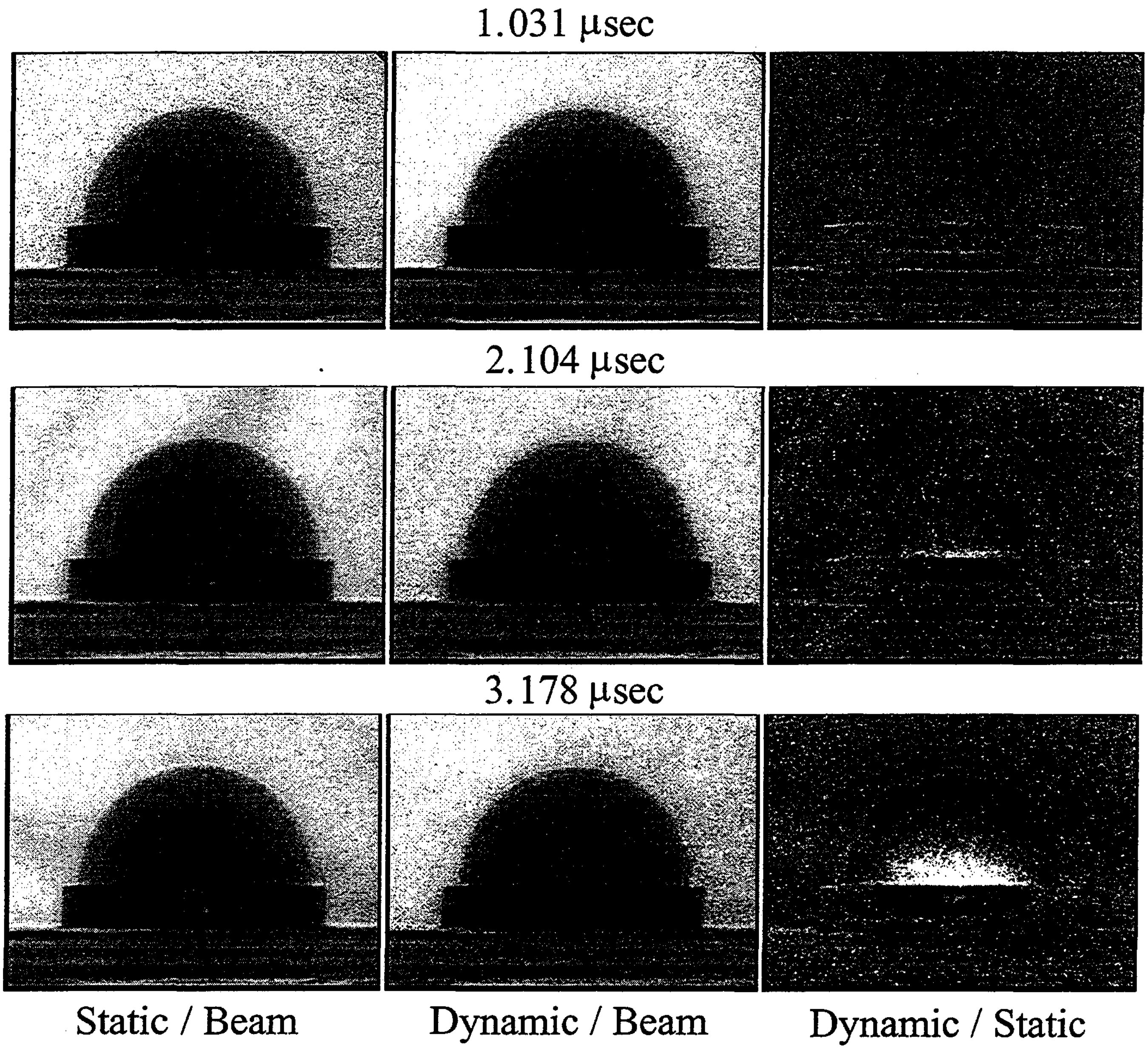

Fig. 3. Ratio images of proton radiographs taken by the detector system. Each row corresponds to a different camera. The fourth camera was unfortunately disabled by a lightning strike shortly before these radiographs were taken. The three different columns correspond to beam normalized radiographs of the static object (left column), beam normalized radiographs of the object as it was exploding (center column), and ratios of the dynamic to static images (right column), which emphasize differences between the static and dynamic radiographs. The given times are relative to detonator breakout.

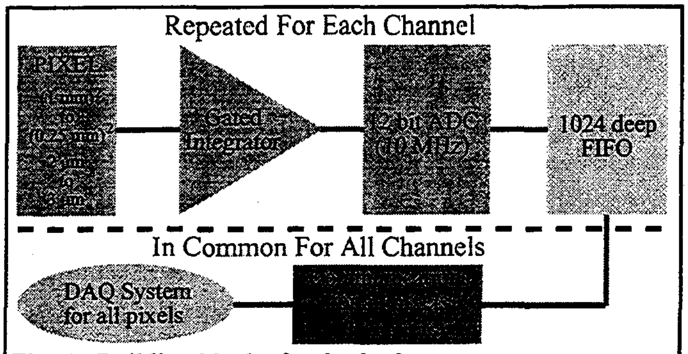

Fig. 4. Building blocks for the 8 × 8 system.

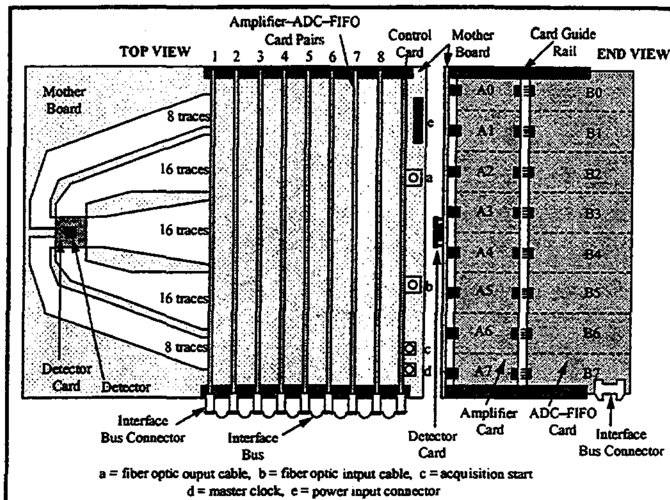

Fig. 5. Sketch of the layout of the 8 × 8 system.

smaller pixel sizes. The problem is instead in the high density interconnections which we were not prepared to address at this stage of the effort. The resulting small prototype was largely designed and constructed by LBNL.

The building blocks of the 8 × 8 system are shown in Fig. 4. For every pixel we had an individual low gain gated integrator, followed by a 10 MHz 12-bit pipelined ADC (Analog Devices AD9220), followed by a 1024 deep first in first out (FIFO) memory unit. In common to these 64 channels of electronics was a control card. This provided the proper phasing of the clock signal which was derived from the accelerator RF system, the trigger signal that started the data storage in the FIFO's and the readout circuitry that read back the 1024 readings from each of the 64 FIFO's. Each reading was then sent via a fiber optic link to the data acquisition computer on command via a CAMAC card once the exposure set was complete. The entire system was built using discrete off-the-shelf components. The hardware configuration is shown in more detail in Fig. 5 and was centered around a Motherboard into which we could plug different samples of the 8 × 8 detector. Into the Motherboard we also plugged 8 pairs of cards, each card pair servicing 8 pixels. The card pairs consisted of the gated integrator / driver card which in turn fed the ADC-FIFO card. The 9th card that plugged into the Motherboard was the control card mention above. A schematic of the gated integrator is shown in Fig. 6.

The silicon *pin* detectors themselves were of a very special design which made use of epitaxial processing by Lawrence Semiconductors[11]. The detectors were made effectively very thin because we were concerned about the potential for collapse of the detector bias field and the very large current spikes that might have otherwise occurred when on the order of 100,000 protons hit each and every pixel every proton burst. The detectors consisted of a 500 μm thick very heavily *n*-doped silicon substrate (few × 10^{19} dopant atoms/cc), on top of which a 2 or 3 μm thick epitaxial layer of more lightly doped *n*-type material (~10^{15} dopant atoms/cc) was grown, and which during operation formed the active (*i*-type) part of the detector. Doping profiles of two of the wafers are shown in Fig. 7. Ion implanted *p*-type regions were

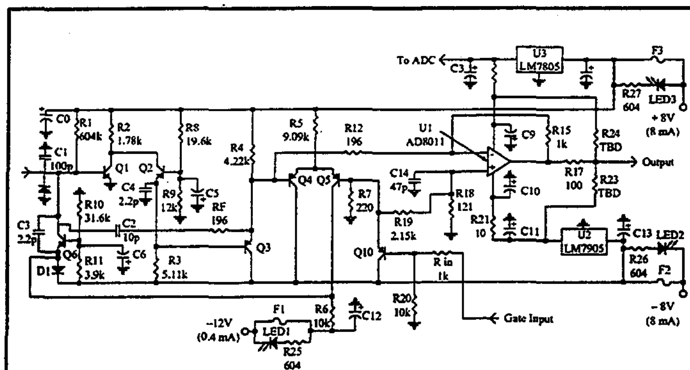

Fig. 6. Schematic of the gated integrator. The charge gain for the amplifier is about a factor of 5.

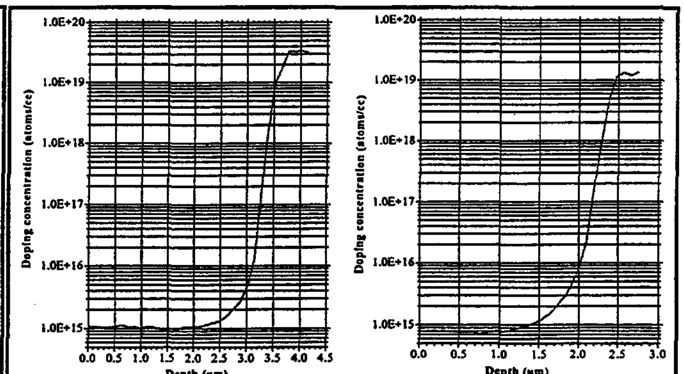

Fig. 7. Doping profiles for one of the 3 μm and one of the 2 μm epitaxial detector wafers.

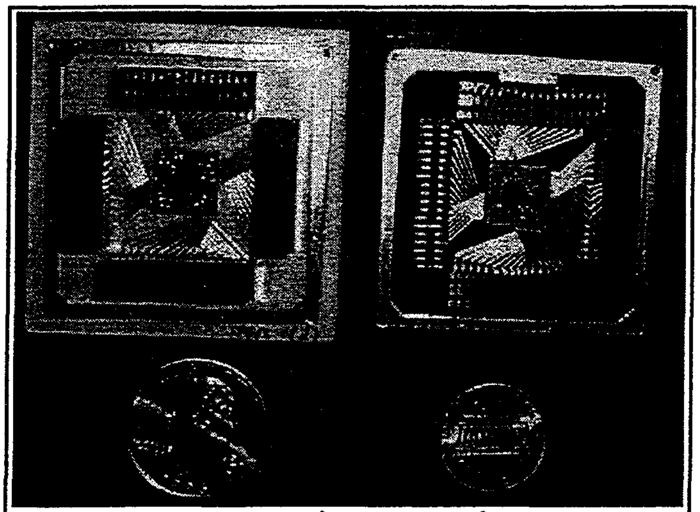

Fig. 8. Detectors of $(1\ mm)^2$ and $(0.5\ mm)^2$ pixel sizes.

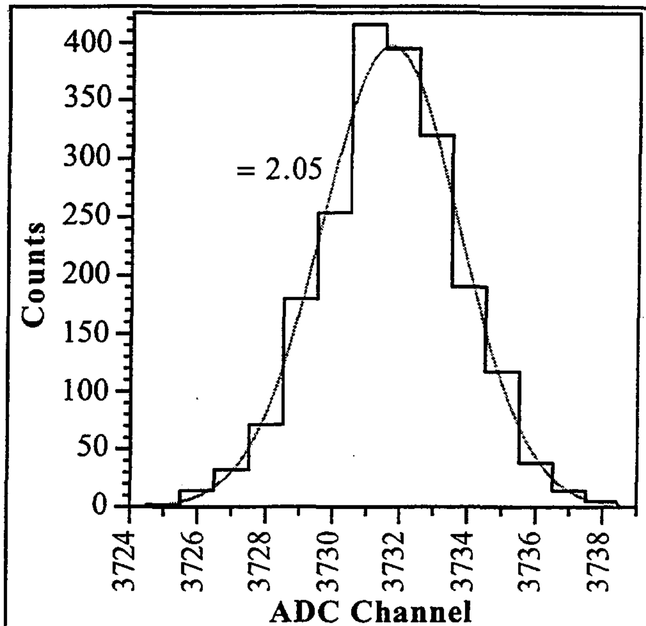

Fig. 9. System performance at 5 MHz with DC input.

then used to make the individual pixels. These were in turn sputtered with aluminum contacts to which the wire bonds were made. The detectors were glued to small ceramic cards (Fig. 8) which had connectors along their periphery to allow them to be plugged into the Motherboard. Despite the thinness of the active detector layer, substantial signals (160 to 240 eh pair on average) were generated for each proton, which is to be compared to the single photoelectron per proton from the scintillator based system discussed earlier. The detectors were biased at a few volts, with the bias being applied to the substrate side. The pixels side was connected to the electronics, which was designed to offer a very low input impedance up to very high frequencies. (Subsequent measurements showed that the epitaxial (active) layer of the detectors was fully depleted by the internal junction voltage.)

Leakage currents across the detector wafers varied. Occasional pixels showed leakage currents in the 10 μA range. However, sub-nanoamp values were far more common and a number of 8×8 pixel regions were found on the wafers in which all the pixels had sub-nanoamp leakage current values. For comparison, the proton beam induced signal currents in the pixels were in the 10 to 100 μA range.

The performance of the detectors and readout electronics is shown in Figs. 9 to 14. Fig. 9 shows the performance during a bench test of the electronics chain when it was clocked at 5 MHz with a DC voltage level through a resistor providing the injected input charge. The rms deviation is ~2 ADC counts, (4095 = full scale). A similar noise level was seen with the system in the experimental area and reading out a detector just before or after beam bursts arrived. Fig. 10 shows the linearity of the system response averaged over all 64 pixels as a function of proton beam intensity. The horizontal axis gives the proton beam intensity as measured by a toroidal pickup coil (arbitrary scale units with an obvious zero offset) and the vertical axis gives the 64 pixel average ADC value. The spread in the points is largely due to noise in the pickup coil circuit. Fig. 11 shows the time response of the system. The 800 MeV proton beam at the Los Alamos Neutron Scattering Center (LANSCE) for our tests was run in a chopped mode with a frequency of 1/72 of the fundamental accelerator frequency of 201.25 MHz resulting in a chopped beam burst once every ~ 358 ns. The 358 ns mode could be further gated to give a proton burst once every N x 358 ns (N = integer). For Fig. 11, two detector response curves are shown, one with N=2 and the other with N=10. The detector system itself took readings once every 358 nsec. As can be seen, the detector responded fully to the beam time structure. Fig. 12 shows a picture of a vertical resolution pattern taken with a $(0.5\ mm)^2$ pixel detector. The object imaged consisted of 1/2 mm wide slots with a pitch of 1 mm cut into a heavy metal plate. The resolution pattern was placed in the object plane of the magnetic lens system of our radiography setup[1]. The detector plane coincided with the image plane of the magnetic lens and immediately downstream of it we placed a phosphor image plate. The relative alignment of the detector and resolution pattern can be seen in the image plate picture (the left half of Fig. 12). The central

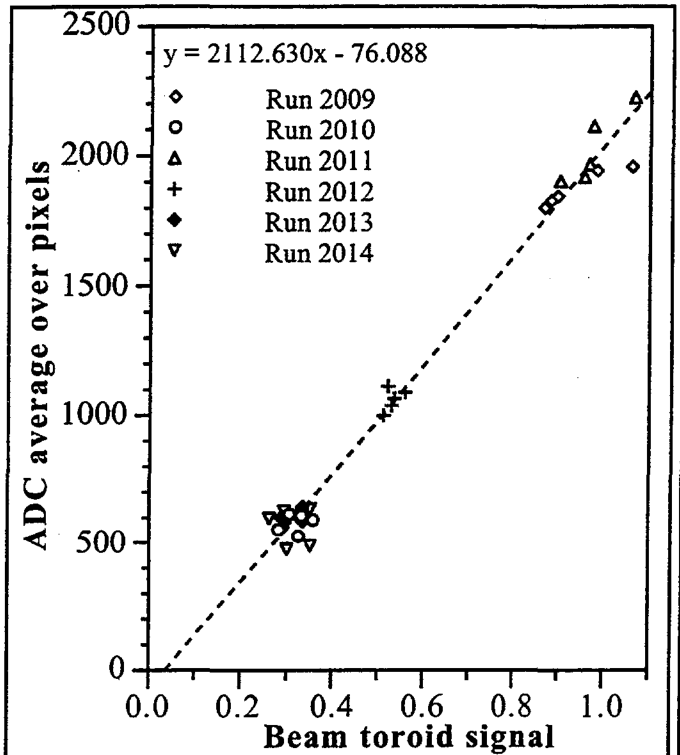

Fig. 10. Detector response as a function of beam intensity.

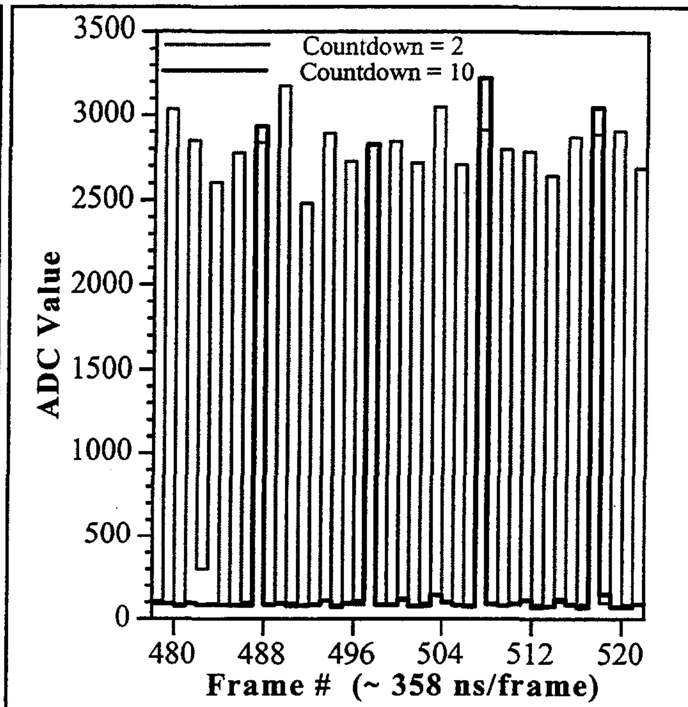

Fig. 11 Time response of the detector system for a beam burst every 2×358 ns and for a burst every 10×358 ns. The inter-frame time was 358 ns.

square subsequently superimposed on the image is the location of the detector proper as determined from the pin locations of the connectors of the detector card. The pins can be seen along all 4 edges of the image plate picture. The right hand image is a plot of the ADC values from the 64 pixels of the silicon detector and very clearly shows the resolution pattern.

Finally, Figs. 13 and 14 show the results of a dynamic experiment. The image plate inset in Fig. 13 shows a picture of a short cylindrical piece of HE seen from its side. A steel plate (the dark area) was glued to the top of the HE. At the bottom of the HE, the detonator is visible. The location of the silicon detector can be ascertained from the pins of the chip carrier. The silicon detector systems overlapped the HE with 6 or 7 rows of pixels, and overlapped the steel with two or one rows of pixels respectively. For this test both of our 8 × 8 detector systems were used, with about a 1 cm gap between them. Fig. 14 shows the output of the two systems (S1-S8 = system 1, S10-S18 = system 2). The two systems were misaligned by about one row as is evident when comparing the low numbered row regions (1-3).

Both systems had (1 mm)^2 pixel detectors. For system 1, all 64 pixels were operating, whereas system 2, had four bad pixels. Fig. 13 shows the response of both of the two systems averaged over all good pixels and plotted on an arbitrarily normalized scale. The beam toroid signal is shown as the gray step function shaped curve. Also shown is the response of detector system 1 but with the individual frames normalized by the beam toroid values. The beam toroid signal shows that the beam was turned on at frame 37. A proton burst arrived once every 358 ns, the same as the frame spacing for the pixel systems. The HE was initiated at the time indicated by the vertical line at frame 146. Several μs after initiation, the detonation wave reached the region of the steel plate and began pushing it out of the field of view of the detector system. This is indicated by the steep rise in the transmitted proton beam intensity seen by the detectors. At the about same time the detonation wave broke out of the HE surfaces and the reaction products (gases) began to dissipate boosting the detector signal even more. The proton beam attenuation change due to the gas expansion is rapid at first but slows with time as the gas becomes more dilute. Nonetheless, even many hundreds of frames after the detonation, the expansion of the gas is still evident. The sudden dip starting at frame 447 is due to a 3 frame programmed interruption of the beam used to demonstrate proper operation of the system.

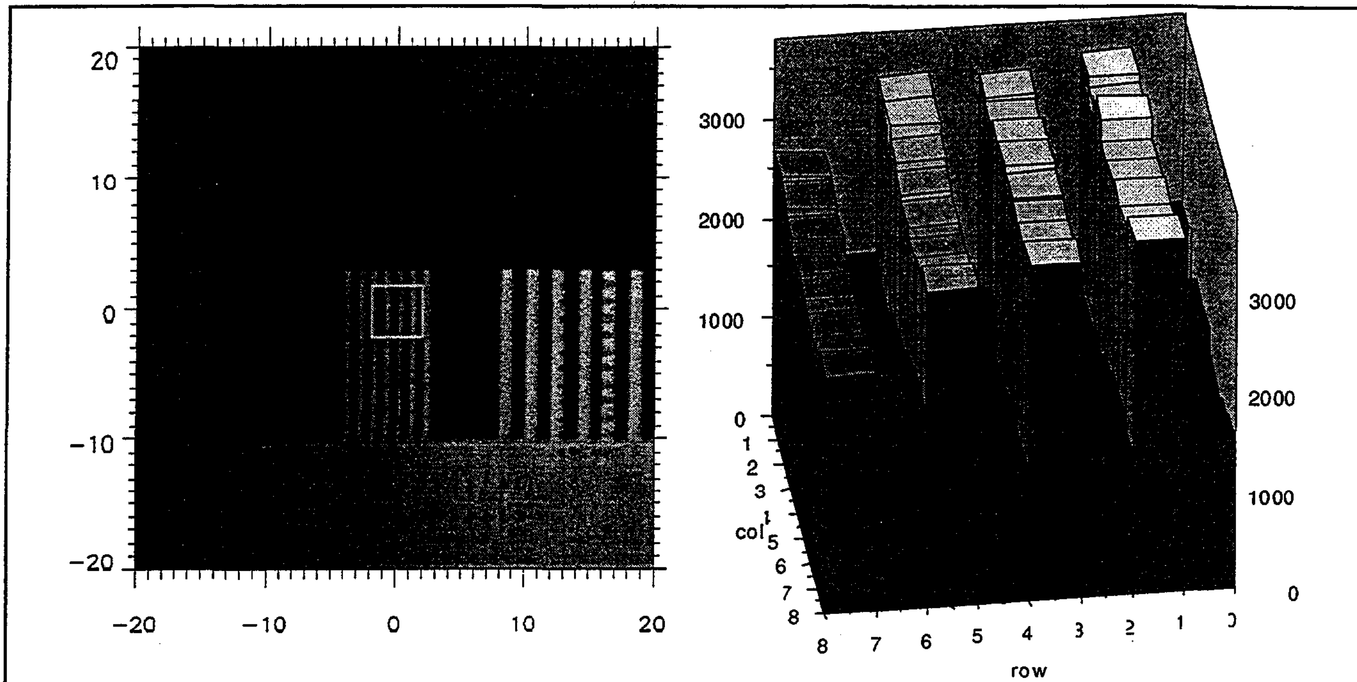

Fig. 12. The left image shows an image plate picture of a vertical resolution pattern. The scale is in mm. The two parallel rows of slightly darker small spots near all 4 edges of the image are the connector pins of the card holding the silicon detector. These were used to determine the detector location which is indicated by the small square near the center of the image. The right image shows the output of the 8 × 8 pixels in units of ADC counts.

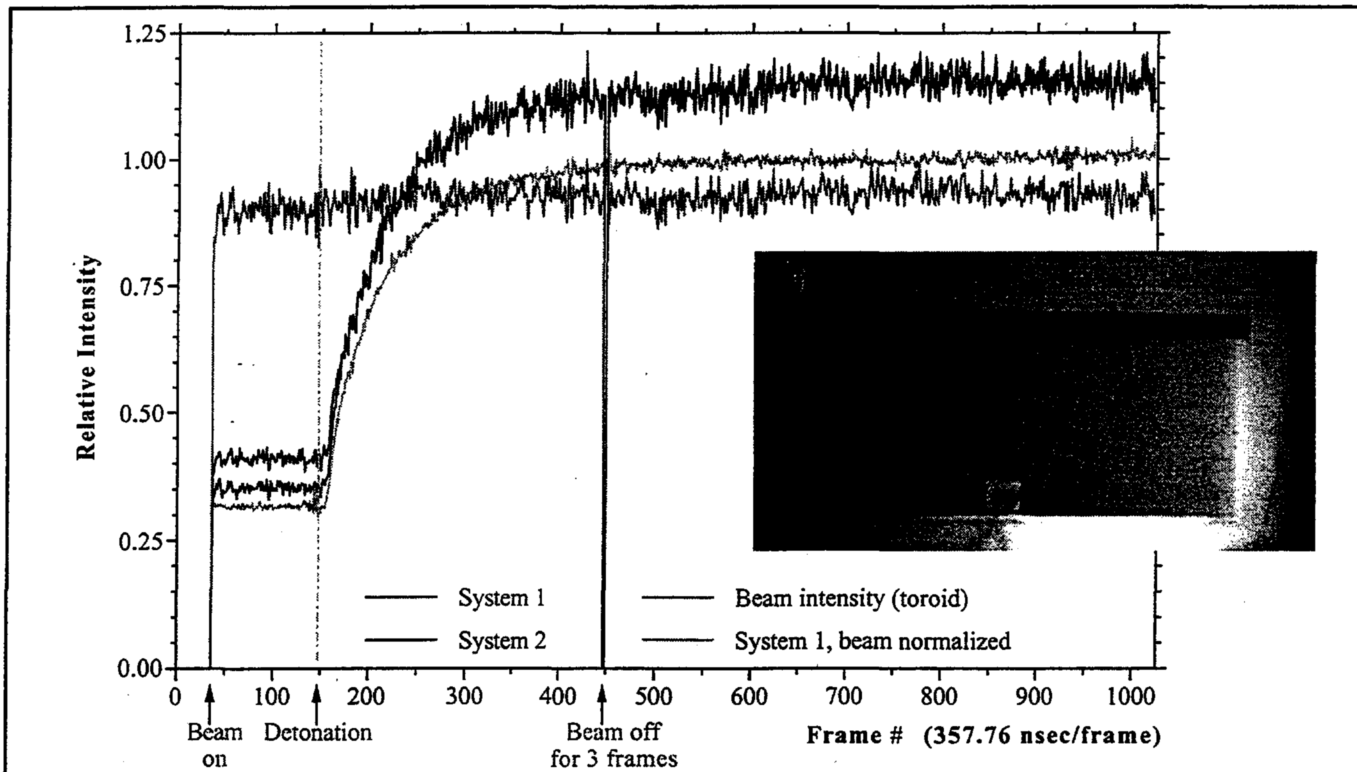

Fig. 13. The average pixel response of the detector system to the detonation of the piece of HE shown in the inset.

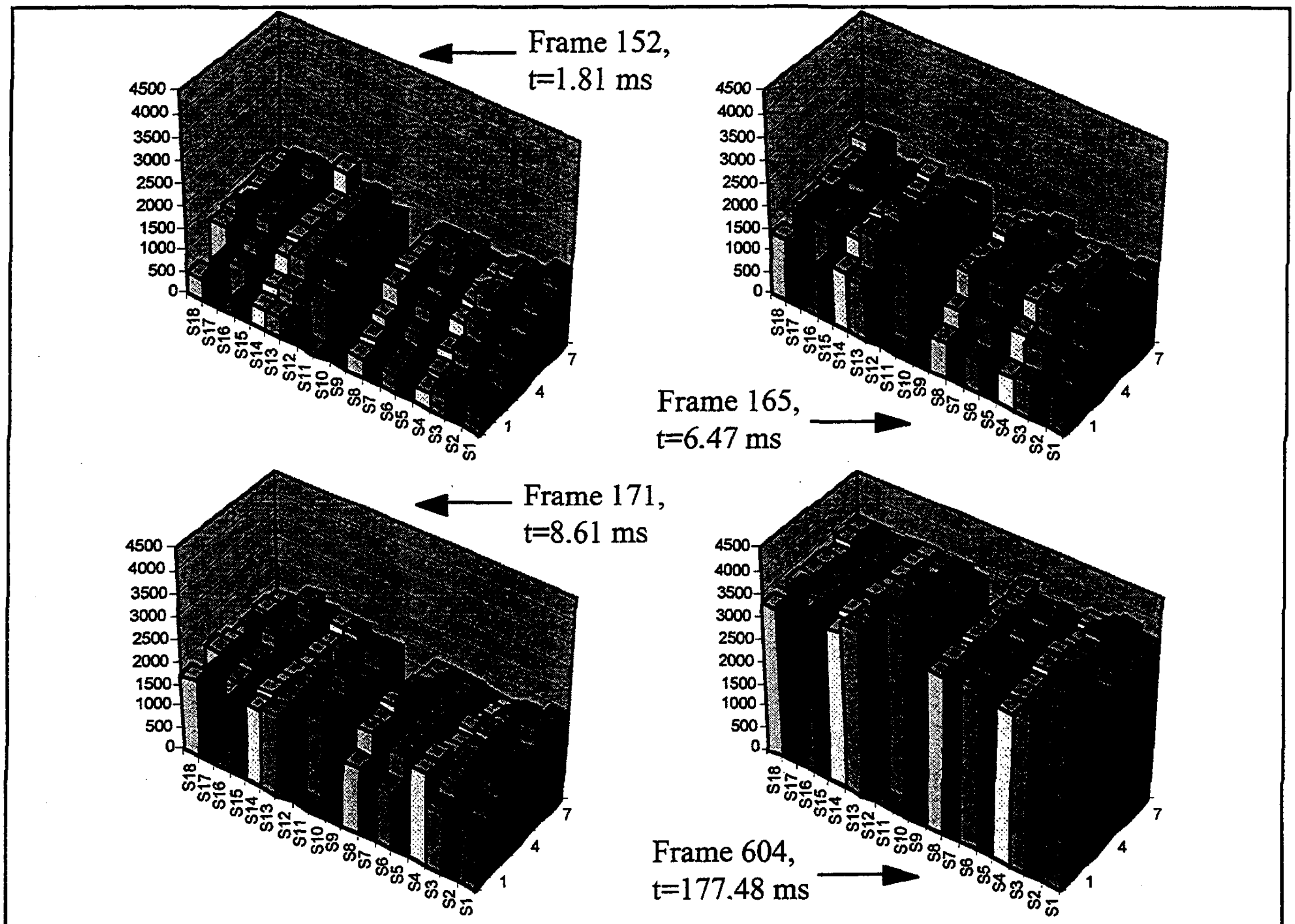

Fig. 14 Individual frames from the dynamic radiograph set shown in Fig. 13. The two 8 × 8 systems are plotted side by side.

PROBLEMS

Fig. 15 shows several sequential frames of pixel detector output of what should be a very uniform beam spot. Although this is what is seen on the average, also apparent are a number of relatively large and random fluctuations in pixel response. A systematic characterization of these fluctuations is shown in Fig. 16 in which is plotted a distribution of ratios of pixel values from a large number of frames and a large number of pixel pairs. (Frame to frame beam intensity changes, and different pixel gains were corrected for before the ratios were taken.) The rms width of the distribution is seen to be over 9%. Although there are relatively large fluctuations in energy deposition in thin detectors as given by the Landau distribution[12] or variants thereof[13] for single protons, when averaging over a large number, N, of protons per pixel, the pixel fluctuations should be a factor of $N^{1/2}$ *smaller than the individual proton* fluctuations. As such even a 100% fluctuation level for single proton measurements should result in only a 0.58% fluctuation in pixel response and therefore cannot be the cause of the problem. Another explanation is in order as we had $N \approx 30{,}000$ for the results shown in Fig. 15 & 16.

An alternative explanation lies in nuclear interactions of protons in the silicon pixels themselves. Starting with the inverse of the nuclear collision length in silicon of $(70.6\ \mathrm{g/cm^2})^{-1}$, multiplying by the density of silicon and an active detector thickness of 2.0 μm, and assuming 30,000 protons incident on a pixel in a single frame, gives a probability of 0.20 that a nuclear interaction will occur per pixel per frame. When this is folded with Poisson counting statistics, the probability of no nuclear interactions in a given pixel in a given frame is 82%, whereas 18% of the time one or more nuclear interactions take place. This is significant. One additional criterion must be satisfied for this to explain the observed effect, namely the

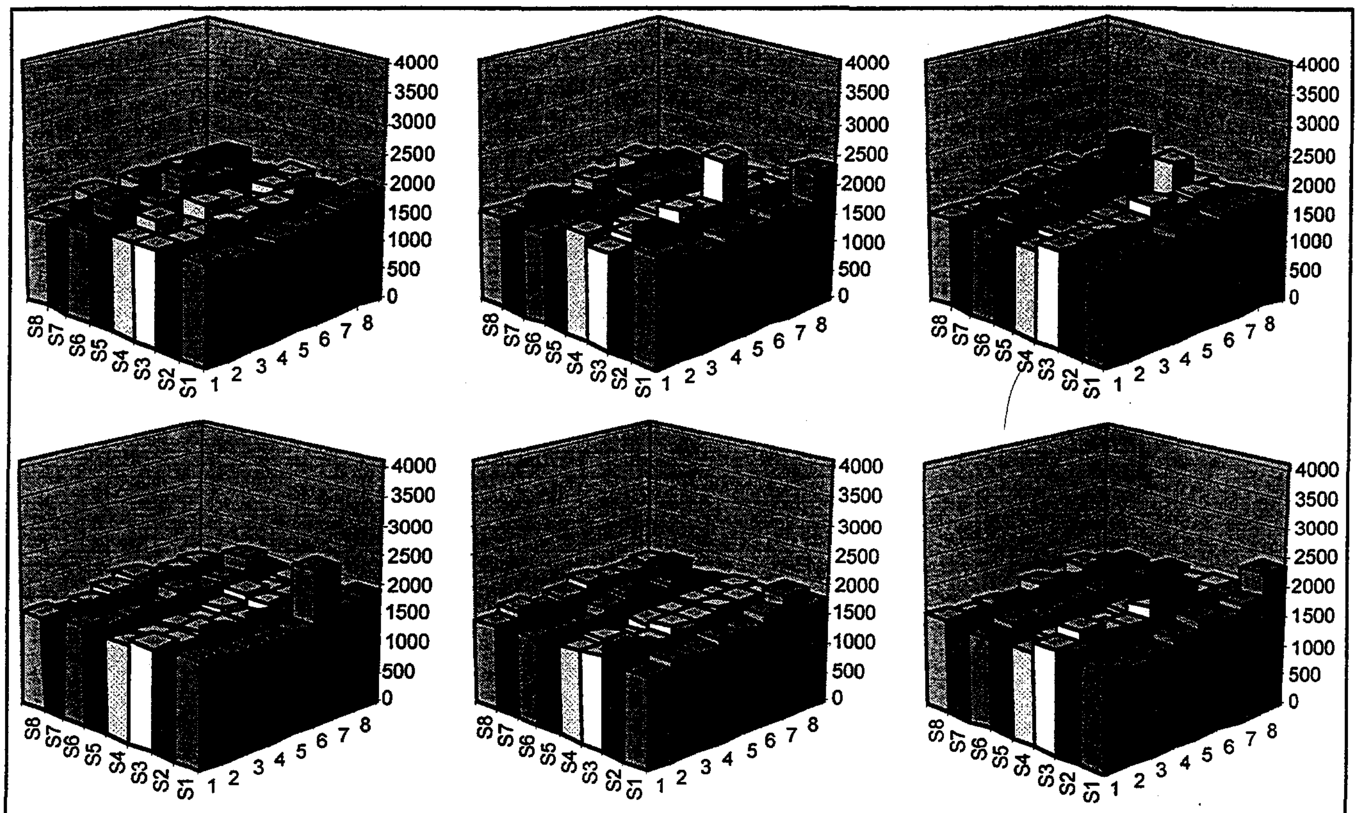

Fig. 15. Sequential frames of the smooth proton beam spot demonstrating random fluctuations in pixel response.

nuclear collision must result in a very large energy deposition in the active part of the detector. If instead the nuclear collision solely produced a single high energy secondary particle, that particle would look like any of the 30,000 incident protons and as such would result in a 1 in 30,000 part fluctuation in the signal, clearly not what is required. What is needed instead is a slow heavy recoiling particle which is capable of depositing a significant amount of its energy even in a very thin active layer. This could easily be done by a recoiling residual nuclear fragment. If we assume a knockout of a single nucleon from a silicon nucleus in which the Fermi level had a typical value (300 MeV/c), the recoiling nucleus would have an average momentum of 300 MeV/c. Translating that momentum into the kinetic energy of a mass 27 amu fragment, we find a value of 1.8 MeV, which would be easily be stopped by 2.0 μm of silicon. Comparing this energy deposit with that of the 30,000 protons, which on average each deposit about 500 eV, or 15 MeV in total, we find that a single nuclear interaction can easily cause a 12 % fluctuation. This number is of the order of magnitude required to explain the phenomenon.

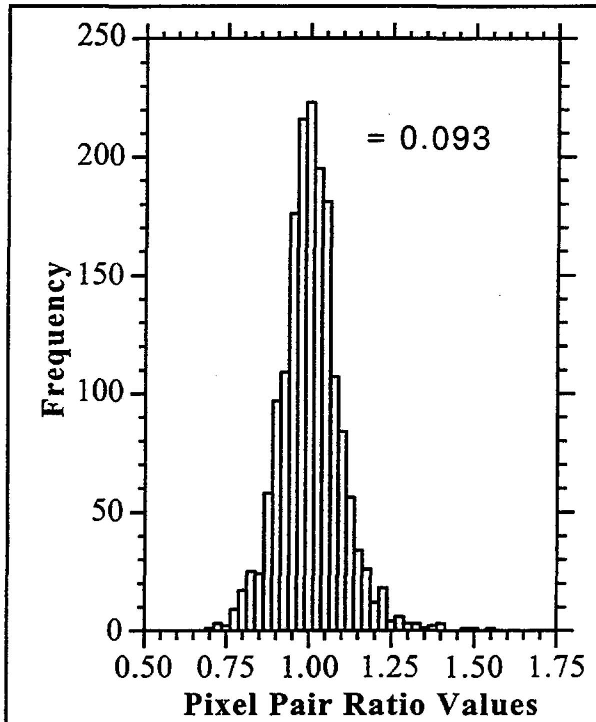

Fig. 16. Ratios of pairs of pixel values from a large number of frames and pixel pairs. Mean differences in pixel response and beam intensity were corrected for.

Several options are available to deal with this problem. A number of these are based on trying to reduce the detector thickness thereby decreasing the probability of a nuclear interaction. The limiting detector thickness value is probably around 1 μm, which would decrease the effect by a factor of two from that calculated above. Another approach is to subdivide each resolution element in the image to a large number of pixels. One then keeps the proton beam intensity per resolution element about the same. This decreases the number of protons per pixel by the number of pixels per resolution element. The probability of a nuclear interaction per pixel changes by the same amount. While this is occurring the fractional change in signal caused by a nuclear interaction in a pixel goes up by the number of pixels/resolution element, making those "bad" pixels even more readily apparent. Those pixels are then rejected, and only the "good" pixels in a resolution element are used. If desired, the loss in the counting statistics due to the few bad pixels in a resolution element can always be compensated for by increasing the beam intensity slightly. A variant of this scheme[14] subdivides things in time as opposed to space, for instance sending 10 bursts of protons separated by 20 ns, each of 1/10th the nominal intensity and each one being read out, as opposed to 1 nominal burst every 200 ns.

An alternative to the above approach of trying to decrease the probability of a nuclear interaction is to go in the opposite direction and thereby effectively averaging out the effect of the fluctuations. For instance, in plastic scintillator, the inverse of a nuclear collision length is $1/(58.4\ \mathrm{gm/cm^2})$. Multiplying this by the density of the material, a thickness of 2 cm, and assuming 30,000 protons incident per pixel, one finds on the average 1000 protons have nuclear interactions. Thus the statistical effect of the interactions are reduced by a factor of $1000^{1/2}$ or about 32 over that of a single interaction. At the same time, the relative effect of a single nuclear interaction collision is greatly reduced. The normal energy deposition of a high energy proton in 2 cm of plastic scintillator is 4 MeV, about equal to the kinetic energy of a recoiling 11 amu fragment with a momentum of 300 MeV/c. The fact that this approach works can be seen by doing a pixel ratio analysis for some of the scintillator based images taken with CCD cameras discussed earlier. Such an analysis shows an rms width of just over 2%, and the majority (~80%) of that is due to the poor photon counting statistic per proton and lower number of protons per pixel.

FUTURE PLANS

Planned upgrades for the short-term CCD based system include expanding it to an 8 frame capability, and using larger diameter PFD's (40 mm vs. 25 mm) in order to increase the magnification and thereby the amount of light available and hence improving the counting statistics of photoelectrons per proton. The larger diameter PFD's will also be operated at higher voltages and therefore increased gain to make up for the loss of light that will occur in the tapered fiber optic bundle which connects the PFD to the ~ $(25\ \mathrm{mm})^2$ CCD. For the long-term system several paths are being pursued. We have designed an application specific integrated circuit (ASIC) which is based on the CMOS process and has been implemented in a

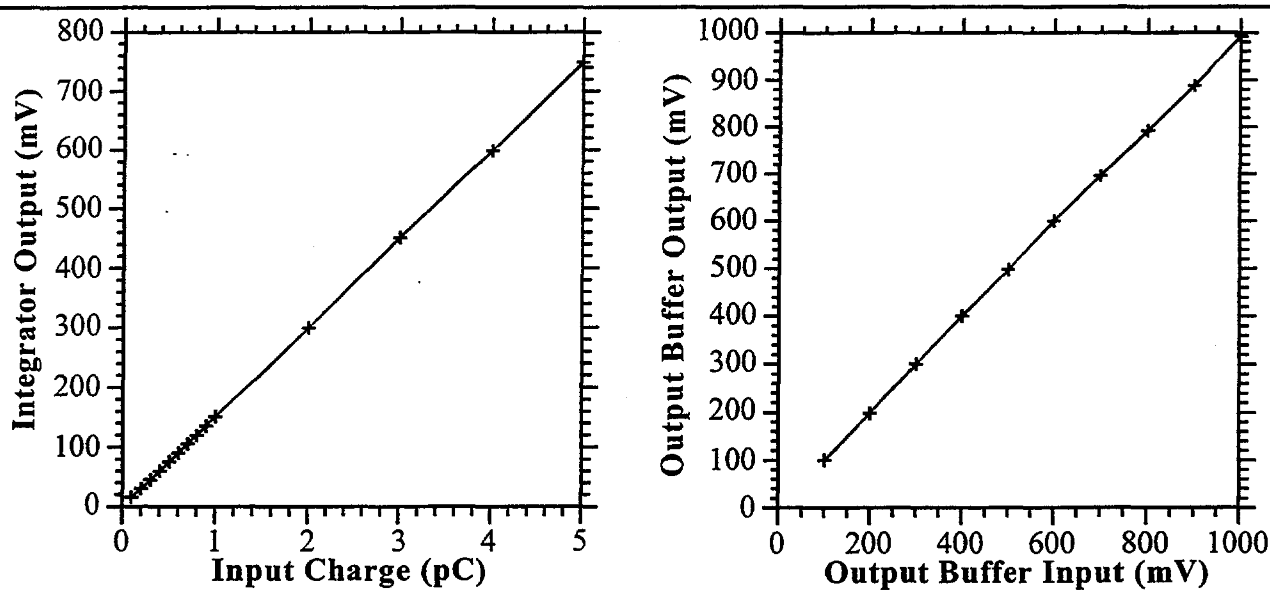

Fig. 17. Measured linearity of the response of the new ASIC chip components. The left plot is for the gated integrator and the right plot is for the output buffer circuit.

0.5 μm HP MOSIS run. The chip has 4 gated integrators which multiplex their output to an included analog memory unit. The chip then sequentially feeds the 4 analog values via a driver circuit into a separate 12 bit 40 MHz pipelined ADC. Initial performance evaluations of the ASIC chip as shown in Fig. 17 look promising. The new ADC / ASIC chip combination are planned to form the basis of a new 10,000 pixel prototype system which will be used to look at system issues. In the longer term we still need to solve the interconnect problem for $(1/4\ \mathrm{mm})^2$ or smaller pixels.

We will evaluate several solutions to the apparent nuclear interaction problem. We have built some small photodiode arrays compatible with the LBNL electronics, which are presently being coupled to a fiber optic array. It should be pointed out that the electronics built by LBNL were designed to be fully compatible with the use of a photodiode detector as opposed to the solid state ionization detectors. Since silicon photodiode arrays can be built much larger and more cheaply that CCD detectors, it is possible to use a lens system with unit magnification as opposed to the magnification of 1/5 that was required for the CCDs. Referring back to eq. (5), this results in about a factor 9 more light. At the same time blue sensitive photodiodes have quantum efficiencies of at least 80%[15] buying us about a factor of 4 over the photo-cathodes on our MCPs or PFDs. Using the value of 1 photoelectron per proton derived earlier for our scintillator based system, we would now be about a factor of 36 better, or at just under 1/2 the signal that would be gotten from a 1 μm thick silicon ionization detector.

Along the line of reducing the probability of nuclear collisions in a pixel in the time domain, we are considering building a version of the electronics which would use a single 40 MHz ADC to look at individual pixels once every 30 to 40 ns. We will also look at reducing the detector thickness to 1 μm.

CONCLUSIONS

We have constructed a 4 frame electro-optically gated CCD based camera system capable of operating at speeds of better than 1 frame/μs, and producing high resolution images. This system is already being used to evaluate the proton radiography concept. We have also designed, built, and beam tested a 64 pixel silicon detector based system that meets all the current performance requirements for the final AHF system with the exception of pixel size and some aspects of noise performance. The noise performance issue is apparently not in the electronics, but instead is linked to nuclear interactions of the probing proton beam in the detector and the very high proton beam intensity we have. Several solutions to this problem seem to exist and will be evaluated in detail in the near future.

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THE PROTON RADIOGRAPHY CONCEPT

H.-J. Ziock, K. J. Adams, K. R. Alrick, J. F. Amann, J. G. Boissevain, M. L. Crow, S. B. Cushing, J. C. Eddleman, C. J. Espinoza, T. T. Fife, R. A. Gallegos, J. Gomez, T. J. Gorman, N. T. Gray, G. E. Hogan, V. H. Holmes, S. A. Jaramillo, N. S. P. King, J. N. Knudson, R. K. London, R. P. Lopez, J. B. McClelland, F. E. Merrill, K. B. Morley, C. L. Morris, C. T. Mottershead, K. L. Mueller, Jr., F. A. Neri , D. M. Numkena, P. D. Pazuchanics, C. Pillai, R. E. Prael, C. M. Riedel, J. S. Sarracino, H. L. Stacy, B. E. Takala, H. A. Thiessen, H. E. Tucker, P. L. Walstrom, G. J. Yates, J. D. Zumbro
(Los Alamos National Laboratory, Los Alamos, NM 87545)

E. Ables, M. E. Aufderheide, P. D. Barnes Jr., R. M. Bionta, D. H. Fujino, E. P. Hartouni, H.-S. Park, R. Soltz, D. M. Wright
(Lawrence Livermore National Laboratory, Livermore, CA 94550)

S. Balzer, P. A. Flores, R. T. Thompson
(Bechtel, Nevada, Los Alamos Operations, Los Alamos, NM 87545)

R. Prigl, J. Scaduto, E. T. Schwaner
(Brookhaven National Laboratory, Upton, NY 11973)

A. Saunders
(University of Colorado, Boulder, CO 80309)

J. M. O'Donnell
(University of Minnesota, Minneapolis, MN 55455; current address: Los Alamos National Lab)

ABSTRACT

Proton radiography is a new tool for advanced hydrotesting. It is ideally suited for providing multiple detailed radiographs in rapid succession (~ 200 ns between frames), and for work on thick systems (100's of g/cm^2 thick) due to the long nuclear interaction lengths of protons. Since protons interact both via the Coulomb and nuclear forces, protons can simultaneously measure material amounts and provide material identification. By placing cuts on the scattering angle using a magnetic lens system, image contrast can be enhanced to give optimal images for thick or thin objects. Finally the design of a possible proton radiography facility is discussed.

INTRODUCTION

We have developed a versatile new technique for obtaining a large number of flash radiographs in rapid succession. Our work is in support of the US Department of Energy's Science Based Stockpile Stewardship (SBSS) program and, in particular, is aimed at developing a concept for the Advanced Hydrotest Facility (AHF). The cessation of all underground nuclear weapons tests by the United States in accord with a proposed Comprehensive Test Ban Treaty has presented a significant challenge for the Department of Energy (DOE) nuclear weapons program with respect to certifying the performance, reliability, and safety of US nuclear weapons. The AHF is to be the ultimate above ground experimental tool for addressing physics questions relating to the safety and performance of nuclear weapon primaries.[1] In particular, the goal of the AHF is to follow the hydrodynamic evolution of dense, thick objects driven by high explosives.

The radiographic technique we developed uses high energy protons as the probing particles. The technique depends on the use of magnetic lenses to compensate for the small angle multiple Coulomb scattering (MCS) that occurs as the charged protons pass through the object under study. The use of a magnetic lens turns the otherwise troubling complications of MCS into an asset. Protons undergo the combined processes of nuclear scattering, small angle Coulomb scattering, and energy loss, each with its own unique dependence on material properties {atomic weight, atomic number (Z), electron configuration, and density}. These effects make possible the simultaneous determination of both material amounts and material identification. This multi-phase interaction suite also provides the flexibility to tune the sensitivity of the technique to make it useful for a wide range of material thicknesses.

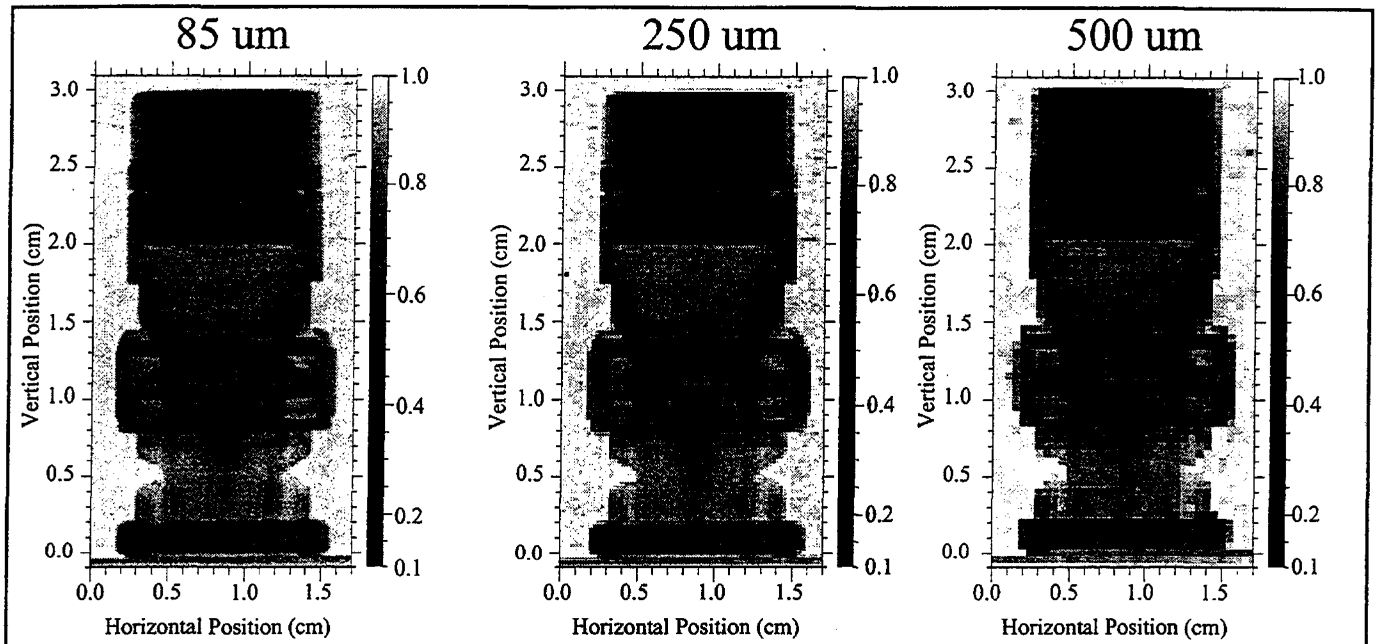

Fig. 1. A digitized phosphor image plate[3] proton radiograph of a 50Ω BNC terminator. The initial image (left) was digitized with (85 μm)^2 pixels. For the central and right images, pixels in 3-by-3 and 6-by-6 areas from the left image were summed.

The magnetic optics provides a means of maintaining unit magnification between the object and the image and the ability to move the image and hence detector planes far from the explosive object under test. This greatly improves the signal to background value and reduces the complexity of the blast protection scheme for the detectors. The magnetic lens system also provides the capability to change the angular acceptance, which is crucial for the ability to perform material identification and to tune the sensitivity for objects of very different thicknesses.

Protons offer a number of other advantages as probing particles in radiography as they can be detected with 100% efficiency and the same proton can be detected multiple times by multiple detector layers. For applications, such as those foreseen at the AHF, where thick dense dynamic objects need to be radiographed multiple times in very rapid succession, protons are nearly ideal solutions as they are highly penetrating, and the proton sources (accelerators) naturally provide the extended trains of short duration, high intensity beam bursts that are required. A single accelerator can easily provide enough intensity to allow the beam to be split many times to provide the multiple beams needed for simultaneous views of the object allowing 3-D tomographic "movies" to be made, the ultimate goal of the AHF.

The following sections of this paper will present an overview of the principles of high energy proton radiography (PRAD), their implementation, and how these mesh with the currently perceived performance requirements for the AHF. In addition, some of our initial PRAD results using both the 800 MeV beam available at the Los Alamos Neutron Scattering Center (LANSCE) and a secondary 10 GeV proton beam at the Alternating Gradient Synchrotron (AGS) at the Brookhaven National Laboratory (BNL) will be given. Finally, a possible design for an AHF is examined. In a separate paper[2] in these proceedings, we discuss the detector development effort associated with our work on PRAD.

GOALS

Performance requirements for the AHF are given in Table 1. In addition to the high frame rate requirements, high resolution images are needed. A feeling for resolution can be gathered from Fig. 1, in which pixels from a proton radiograph image have been averaged to ever coarser bins. The high resolution, high contrast capabilities must be achieved even for radiographs of "thick"

Table 1: Desired AHF Performance Parameters	
Spatial Resolution	better than 1 mm (FWHM)
Object thickness	up to 100's of g/cm^2
Thickness accuracy	~ 1% pixel by pixel
Interframe spacing	from ~ 100 ns to many μs
# of frames	at least 10
Velocities to freeze	speeds of km/s
Views for 3D imaging	4 to 16

objects, where "thick objects" are measured in units of 100's of g/cm^2. Thick objects strongly attenuate the beam of probing particles in their region of maximum thickness, and potentially produce large amounts of background by scattering particles from thinner regions of the object into the area of the image corresponding to the thickest part of the object where few direct particles penetrate. Background issues are further complicated by the need to view the object simultaneously from several directions, leading to the potential for scattering particles from one source into the detectors corresponding to another source. Tied to the requirement for high precision measurements is the desire to obtain maximum precision with a limited budget of probing particles. This is further constrained by the dynamic range of the detector system, which must count the number of transmitted particles in both the thin and thick regions of the object. In the following section, the properties of the ideal probing particle will be derived, and we will show that protons come very close to being such particles.

DESIRED PARTICLE ATTENUATION LENGTH

With a fixed budget of incident particles, one can calculate the ideal attenuation length (λ) for the probing particles when radiographing an object of a given thickness (L). The ideal attenuation length will be the one that minimizes the fractional error in the difference between the number of particles transmitted by two regions of the object that differ in thickness by an amount T. We start by assuming simple exponential attenuation of the beam by the object

$$N(L) = N_o\exp(-L/\lambda), \tag{1}$$

where N_o is the number of incident particles per pixel, which is assumed to be known. The difference in the number of particles transmitted through the two regions is given by

$$N(L) - N(L+T) = N_o\exp(-L/\lambda) - N_o\exp(-(L+T)/\lambda) = N_o\exp(-L/\lambda)\,[1 - exp(-T/\lambda)]. \tag{2}$$

The error in the result given by eq. (2) is simply the square root of the sum of the squares of the errors in each of the terms in the difference. Since, from counting statistics, the square of the error in $N(L)$ is simply $N(L)$, we have

$$error\ in\ difference = [N(L) + N(L+T)]^{1/2} = [N_o\exp(-L/\lambda)]^{1/2}\,[1 + \exp(-T/\lambda)]^{1/2}. \tag{3}$$

In the limit of $T \rightarrow 0$, $\exp(-T/\lambda) \rightarrow 1 - T/\lambda$, and eqs. (2) and (3) become respectively

$$N(L) - N(L+T) = N_o\exp(-L/\lambda)\,[T/\lambda] \tag{4}$$

$$error\ in\ difference = [N(L) + N(L+T)]^{1/2} = [N_o\exp(-L/\lambda)]^{1/2}\,[2]^{1/2}. \tag{5}$$

Taking the ratio of eq. (5) to eq. (4) in order to get the fractional error gives

$$fractional\ error\ in\ difference = [2N_o\exp(-L/\lambda)]^{1/2} / \{N_o\exp(-L/\lambda)\,[T/\lambda]\} = 2^{1/2}T^{-1}\lambda N_o^{-1/2}\exp(L/2\lambda). \tag{6}$$

Taking the derivative of that with respect to λ and setting the result to zero in order to find the value of λ that minimizes the fractional error gives

$$(d/d\lambda)\,[fractional\ error\ in\ difference] = (2N_o)^{-1/2}T^{-1}\exp(L/2\lambda)\,[1 - L/2\lambda] = 0. \tag{7}$$

Solving for λ, we find

$$\lambda = L/2, \tag{8}$$

namely the optimal attenuation length is one half the object thickness. Thus for thick objects measured in units of 100's of g/cm^2, one wants attenuation lengths measured in the same units, not in 10's of g/cm^2. Table 2 gives nuclear interaction lengths for high energy protons (above kinetic energies of ~800 MeV nuclear interaction length values are largely energy independent) and attenuation lengths for 5 MeV x-rays (which have approximately the maximum penetrating depths in high Z materials). Also presented are the resulting *fractional error in difference* values as calculated using eq. (6) and assuming N_o = 100,000 and $T = 0.01*L$ (i.e. a 1% thickness difference effect). Since this fractional error must be less than one for there to be any chance of seeing the thickness difference, the table clearly demonstrates the advantage of protons for thick, high Z objects.

MULTIPLE COULOMB SCATTERING

Unlike x-rays, protons undergo a random walk as they pass through an object due to the myriad of small angle charged particle collisions they have with the atoms in the object. This multiple Coulomb scattering (MCS), at first glance appears to be a great disadvantage for proton radiography since the protons no

Table 2: Nuclear interaction lengths for protons and x-ray attenuation lengths[4] and the *fractional error in difference* values for a 1% thickness difference and 100,000 incident particles per pixel.

	High Energy Protons (~≥ 1 GeV)				5 MeV x-rays			
material	hydrogen	graphite	iron	lead	hydrogen	graphite	iron	lead
λ (g/cm^2)	50.8	86.3	131.9	194.0	21	38	34	23
X_o (g/cm^2)	63.05	42.70	13.84	6.37				
L (g/cm^2)								
10	2.51	4.09	6.13	8.90	1.19	1.94	1.76	1.28
20	1.38	2.17	3.18	4.57	0.76	1.11	1.02	0.79
50	0.74	1.03	1.43	1.97	0.62	0.66	0.63	0.61
100	0.61	0.69	0.86	1.12	1.02	0.63	0.66	0.90
200	0.81	0.61	0.63	0.73	5.49	1.18	1.44	3.98
500	6.23	1.40	0.79	0.63	2779.31	24.46	47.46	1081.10

longer travel in a straight line, and an image, unless taken immediately downstream of the object, will be blurred because of the angular dispersion. (Even immediately downstream of the object, some blurring due to the random walk will be evident.) To first order, the plane projected MCS angular distribution of the protons leaving the object is a Gaussian characterized by a root mean square (*rms*) plane projection deflection angle θ_o which is given by the expression[4]

$$\theta_o(z) = 0.0136 \text{ GeV } (\beta cp)^{-1} (z/X_o)^{1/2} [1 + 0.038 \ln(z/X_o)] \qquad (9)$$

where c is the velocity of light, βc is the velocity of the proton, p is its momentum, and z/X_o is the thickness of the object, z, measured in units of radiation length, X_o. It should be noted that as the β of the proton approaches one, θ_o depends inversely on the momentum of the proton, and only grows as the square root of the object thickness. (The logarithmic term is on the order of 10% and has been ignored here.) The MCS has two effects. The first is the random walk itself, which leads to the limited blurring previously mentioned and is characterized by plane projection *rms* deviation, y, of the proton from its unscattered location by the time it reaches the end of the object. That is given by

$$y(z) = 3^{-1/2} z\, \theta_o(z). \qquad (10)$$

The second is the additional blurring due to the random direction of the protons from MCS as they leave the object and travel to the detector, which will be located a non-zero distance from the object. The first effect can be dealt with by simply raising the proton beam momentum. To set the scale, for proton beams of 2, 5, 20, and 50 GeV/c beam, for a 20 radiation length object which is 10 cm thick, y = 2.16, 0.80, 0.20, and 0.08 mm respectively. As seen from eqs. (9) and (10), the results improves linearly as the beam momentum is increased, but grow worse as the product of the linear thickness of the object and the square root of the thickness of the object in radiation lengths. Since the object one wants to radiograph has a known thickness, by choosing a sufficiently high momentum, the blur can be reduced to any desired value. The *rms* angles θ_o for the same geometry and beam momenta are 37.4, 13.8, 3.4, and 1.4 milliradians respectively. Since we intend to look at explosively driven dynamic objects, the detectors need to be quite distant from the object. Thus the second effect must be dealt with by a different means. The solution here relies on the fact that protons are charged and therefore their trajectories can be bent by a magnetic field. More specifically, one builds a magnetic lens. The center of the object is then placed at the object plane of the long focal length magnetic lens. Similar to an optical lens, the magnetic lens collects all the protons within its solid angle acceptance, and, regardless of their angle of emission from a point in the object plane, puts them all back at the corresponding point in the image plane.

MAGNETIC LENS AND MATERIAL IDENTIFICATION

The overall magnetic lens system we have designed[5] is shown schematically in Fig. 2. The two imaging lens cells thereof are inverting identity (–I) lenses. These cells are each comprised of four identical quadrupole magnets operated at identical field strengths, but alternating polarities (+ – + –). They have the feature that at the center of the gap between the two middle magnets of a cell, the protons are sorted radially solely by their scattering angle in the object, regardless of which point in the object plane they originated from. This allows one to place a collimator at that location and use it to make cuts on the MCS

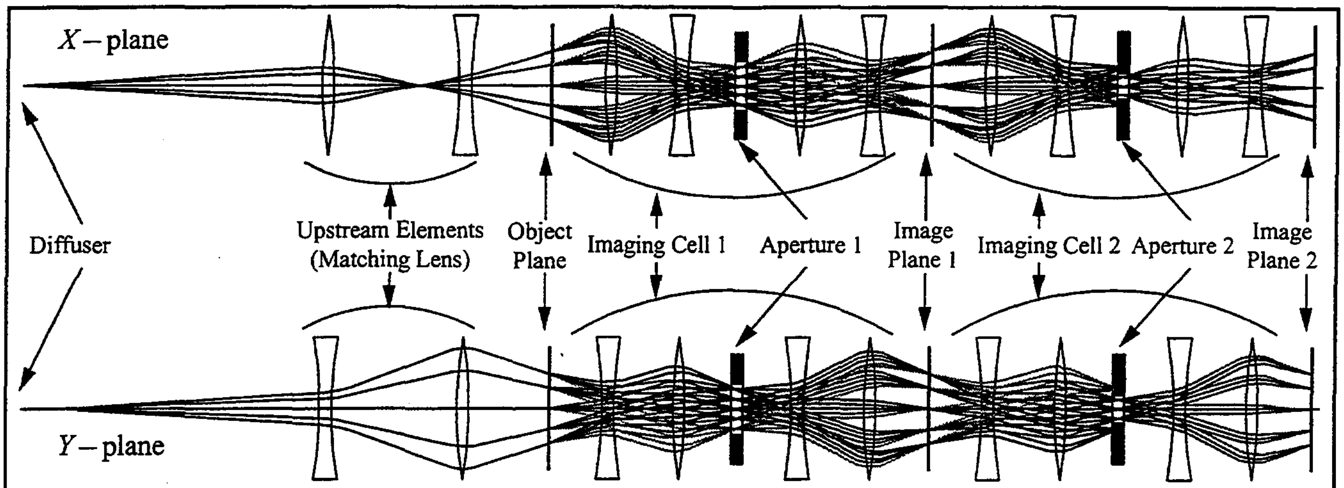

Fig. 2 Schematic of the PRAD magnetic lens system showing both the X and Y views. The beam is first prepared with a diffuser and matching lens to meet optics requirements. It then passes through the object being radiographed. The transmitted beam passes through an iris, or aperture located in the middle of the 4-quadrupole −I magnetic lens cell and is focused on the first detector. It then enters the second identical −I lens cell, which this time has a smaller diameter iris, and is focused on a second detector. Together, the two detectors provide the information needed to reconstruct both the density profile and material composition of the object.

angle in the object. As noted previously, the scattering angle distribution is approximately a Gaussian with a width, which, by eq. (9), depends on the number of radiation lengths of material the protons passed through. With the collimator, one can limit the transmitted particles to only those with an MCS angle less than the cut angle (θ_c). The number of transmitted particles N_c after such a cut is given by

$$N_c \approx N\int_0^{\theta_c} \frac{1}{2\pi\theta_o} \exp\left(-\frac{\theta^2}{2\theta_o^{\,2}}\right) d\Omega \approx N\left[1 - \exp\left(-\frac{\theta_c^2}{2\theta_o^2}\right)\right], \text{ or } \frac{N_c}{N} \approx \left[1 - \exp\left(-\frac{\theta_c^2}{2\theta_o^2}\right)\right] \tag{11}$$

where N is the number of incident particles. Note that when $\theta_c >> \theta_o$, $N_c = N$, as expected. Using eq. (9) for θ_o, ignoring the small logarithmic term, and solving for z/X_o gives

$$\frac{z}{X_o} \approx \frac{-\theta_c^2}{2\left(\frac{13.6 \text{ MeV}}{\beta cp}\right)^2 \ln\left(1 - \frac{N_c}{N}\right)} \tag{12}$$

If we now build a lens system which consists of two of the −I lenses set back to back, the first with an aperture sufficient to pass essentially all the particles scattered by MCS (but not those scattered by inelastic nuclear interactions), the second with its aperture set so that it cuts into the MCS distribution, and then place detectors at the image planes of the two lenses, we get two independent measurements. The first depends on the number of nuclear interaction lengths of material in the object, while the second depends on the number of radiation lengths of material in the object. Since the values of nuclear interaction length and radiation length have different dependencies on material type as shown in Table 2, we are in a position to determine both the amount of material in the object and what that material is. If the object has transitions from one material type to two material types and then from two to three material types, ..., we can unfold the object in terms of material types and thickness for each material. (Note that a 1 to 2 material step followed by a 2 to 3 material step can be unfolded, but a sudden 1 to 3 material step cannot be unfolded.)

It should also be noted that by using a single magnetic lens with just a MCS angle cut, one can achieve high contrast proton radiography even when the object is too thin to provide good contrast using nuclear attenuation. Just as was the case for nuclear exponential beam attenuation, for pure MCS based radiography of a given thickness object, there is an ideal cut angle that maximizes sensitivity to changes in object thickness. The value of that optimal cut angle can be determined by the same process as lead to eq. (8), but for an attenuation that is given by eq. (11). Thus by changing the aperture to provide that optimal

MCS angle cut, one can tune the system to provide optimum sensitivity, regardless of the object thickness. This was done for the image shown in Fig. 1.

As can be seen in Fig. 2, the magnetic lens system has some additional elements upstream of the object. The proton beam passes through a thin diffuser, which gives a small angular divergence to the beam and then passes through a set of magnets, which introduces a correlation between the radial position of a proton in the object plane and its angle. This is done to reduce magnetic lens induced aberrations in the identity lens cells. These aberrations are both geometric and chromatic in nature. For the particular momentum to which the lens is tuned, the relation between the location of a particle in the object plane, x_{object}, and its location in the image plane, x_{image}, for a magnetic lens is given by

$$x_{image} = R_{11}x_{object} + R_{12}\phi_x, \tag{13}$$

where ϕ_x is the angle of the particle in the x-plane relative to the axis of the lens, and the R's are constants, which characterize the magnetic lens. A similar equation holds for the y-coordinate. If instead of having beam particles with a single momentum (p), the particles have a spread in momentum, δp, eq. (13) becomes

$$x_{image} = (R_{11} + \Delta R_{11}' + \textit{higher order terms})x_{object} + (R_{12} + R_{12}'\Delta + \textit{higher order terms})\,\phi_x, \tag{14}$$

where $\Delta \equiv \delta p/p$ and the R′ coefficients are distortion constants for the lens. When an object is placed in the object plane, several things happen to the transmitted proton beam. First, the protons lose energy and thus momentum; their final average momentum p, being less than their incident momentum p_o. The momentum loss in the object is not single valued, but instead covers a range $\pm\,\delta p$ due to random nature of the energy loss process and variations in the thickness of the object. Also, through MCS, an angular divergence is introduced to the beam, which is characterized by θ_o, as given by eq. (9).

We are free to arrange the incident proton beam so that all the particles incident on the object plane have a relation between their angle and location in that plane given by $\phi_x = wx$. Combining this with the effect of the MCS, we have $\phi_x = wx + \theta_o$ for the outgoing beam. Assuming the magnetic lens is tuned to the average momentum of the transmitted protons, eq. (14) becomes

$$x_{image} = R_{11}x_{object} + R_{12}\phi_x + (R_{11}' + wR_{12}')x_{object}\Delta + R_{12}'\theta_o\Delta + \textit{higher order terms.} \tag{15}$$

Making use of the fact that we have a –I lens, which implies $R_{11} = -1$ and $R_{12} = 0$, and ignoring the *higher order terms*, eq. (15) becomes

$$x_{image} = -x_{object} + (R_{11}' + wR_{12}')x_{object}\Delta + R_{12}'\theta_o\Delta. \tag{16}$$

We note that if we choose w such that $w = -R_{11}'/R_{12}'$, the $x_{object}\Delta$ term in eq. (16) becomes identically equal to zero, and thus all position dependent chromatic aberration terms vanish. The matching magnets upstream of the object are used to establish that correlation, w, between x and ϕ_x. Thus eq. (16) becomes

$$x_{image} = -x_{object} + R_{12}'\theta_o\Delta, \qquad \text{provided:} \qquad w = -R_{11}'/R_{12}'. \tag{17}$$

In addition to the matching lens establishing the desired correlation between incident particle angle and location at the object plane, the lens provides some other useful functions. It further expands the incident beam allowing one to illuminate a large object, without making the upstream diffuser very thick. It also helps maintain a very uniform acceptance across the full field of view of the imaging lenses.

MOMENTUM SCALING

The remaining distortion term in eq. (17) is given by

$$\Delta x = x_{object} + x_{image} = R_{12}'\,\theta_o\Delta, \tag{18}$$

which is characterized by the chromatic aberration coefficient of the lens, R_{12}', and the product $\theta_o\Delta$. For high momentum protons (> 1 GeV/c), the momentum loss is essentially independent of beam momentum. Therefore the fractional momentum bite of the beam, Δ, scales inversely proportional to the beam momentum. Likewise from eq. (9), the angle θ_o is also inversely proportional to the beam momentum. Thus the spatial resolution of the magnetic lens system improves as the square of the beam momentum.

Other factors also effect the overall spatial resolution that can be attained in proton radiography. There is the spatial resolution of the detector system, which is essentially independent of momentum. There is also the effect of the non-zero thickness of the object, which by eq. (10) degrades the resolution. As discussed earlier, this effect scales as $1/p$. If there is a vessel to contain the explosive blast in an AHF application,

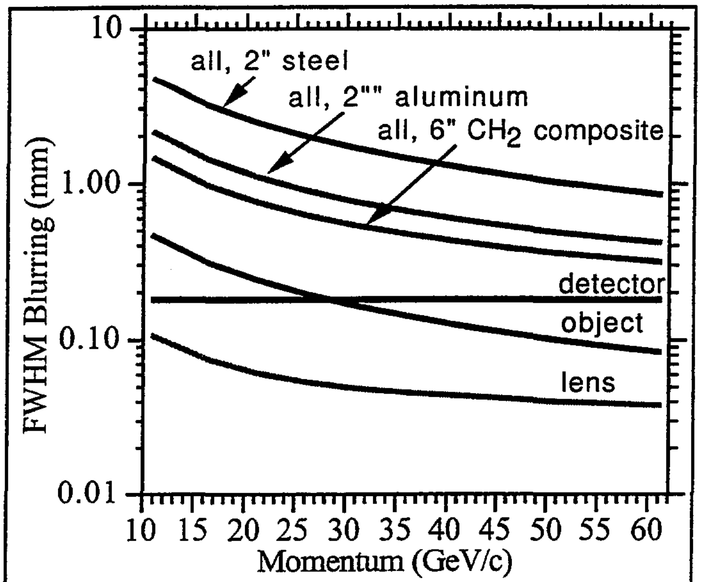

Fig. 3. The momentum scaling for the various terms effecting spatial resolution. Shown are possible individual contributions from the detector, object, and lens, and the overall contribution when these are combined with different containment vessels values.

the MCS of the incoming and outgoing beams in the vessel walls will produce a similar effect, but this time linearly dependent on the separation between the object and the containment vessel wall. Due to the relatively large value of this distance, this will likely be the dominant term effecting spatial resolution. The MCS in the vessel wall will change the value of the outgoing proton angle, which cannot be corrected for by the magnetic lens. This characteristic angle change multiplied by the distance from the object to the vessel wall will be the amount of blur introduced. (If the vessel wall is closer to the image plane than the object plane, the relevant distance is the vessel wall to image plane separation.) The characteristic angle involved is again given by eq. (9) and thus scales as $1/p$. As eq. (9) also shows, it depends on the thickness of the vessel wall in units of radiation length, and therefore it is important to use thin, low-Z materials. The vessel wall thickness is less important for the incident beam, since there it affects the desired correlation between the incident particle location at the object and the particle angle there. This correlation was to remove the chromatic spatial aberrations from the lens, which were already a higher order effect. In Fig. 3 we plot the expected overall spatial image blurring as a function of beam momentum for the various terms and various containment vessel walls.

PROTON DETECTION

Protons, being charged particles, directly excite the detector medium, predominantly through Coulomb interactions with electrons in the medium. They thus generate a signal even for an extremely thin detector. Because of the mass difference between protons and electrons, there is very little deflection of the protons by the detector, and therefore very little in the way of a detector produced background problem. In contrast, x-rays, being uncharged, do not directly ionize the detector material as they pass through it. As a matter of fact, it takes one x-ray attenuation length for 63% of the x-rays to interact and generate a charged particle, which then leaves the excitation trail that a detector sees. X-rays predominantly interact through large angle scattering, and due to the large required detector thickness are likely to have secondary interactions that produce backgrounds in the detector. Since protons can be detected by very thin detectors, no similar problem exists for them. Also in a thin detector, the proton is virtually undeflected and therefore can be used for a second (or third) time, such as in a second magnetic lens system for MCS material identification. Furthermore, multiple planes of detectors can detect the same proton, thereby achieving redundancy. The thinness of the proton detectors also makes them essentially blind to neutral secondary particles generated in the object (neutrons and γ-rays), thereby reducing the potential for other background problems.

BACKGROUNDS

Backgrounds in the case of proton radiography are very small, as we have verified both in Monte Carlo studies and in experiments. This results from the relatively long values of interaction (attenuation) lengths for protons and the large standoff distance for the detectors from the object, which is due to the magnetic lens system. The magnetic lens also provides filtering of off-momentum background particles. At the same time, the thin detectors are essentially blind to neutral secondary particles, which would otherwise dominate the relatively small background. In neither proton nor x-ray radiography are the "attenuated" particles cleanly removed from the beam. Some fraction of the "attenuated beam" will undergo one or several hard interactions in the object and/or surrounding material and still hit the detector in a location that is uncorrelated to their ideal path through the object. Thus they contribute a background signal in the detector, which is indistinguishable from the real signal, thereby masking or greatly diminishing one's sensitivity to the small effects one is looking for in the object. This is clearly a signal to background issue. The signal depends on the ability to get a substantial number of particles directly through the thickest part of the object, and thus requires a very large number of incident particles for a thick object. The background level depends on a combination of factors, the most important of which are the variation in thickness across the object in terms of scattering or attenuation length, the probability of scattering in a given amount of material, and the number of incident particles.

The background will clearly be worst when the object is thick and there is a considerable variation in thickness across the object. At the thickest part of the object there will be very little signal as the beam is strongly attenuated. In the thinner parts of the object, scattering of the beam will occur with some of the scattered particles deflected into the detector region corresponding to the thickest part of the object and potentially causing a large fractional background there. Thus ideally one would like to tailor the beam intensity to be highest at the thickest part of the object, and to have the thickness of the object roughly comparable to the attenuation length of the material of which the object is made. This is exactly what one has in proton radiography. The upstream diffuser used to impart the small angular divergence to the incident beam produces an approximately Gaussian shaped beam profile which is peaked at the center of the beam where one can locate the thickest part of the object. The width of the Gaussian can also be adjusted by changing the diffuser thickness, depending on whether a more uniform or more peaked beam is desired. Furthermore, the interaction length of the protons is, or can be, well matched to the thickness of the object. In contrast, for x-rays, there is typically a poor match of attenuation length to object thickness, especially for thick objects. Also, since the x-ray source is essentially a point source, the beam intensity is nearly uniform across the object. In practice, for x-ray images, a graded collimator of varying thickness can be built that is matched to the object so the collimator – object combination present a uniform thickness to the x-ray beam. However, in the case of dynamic radiography, that becomes problematic at best. An added complication occurs when one has multiple beam lines and detectors needed to perform 3-D reconstructions of the object. Crosstalk between the different beam lines and detectors can then occur. Furthermore, additional beam is incident on the object due to the multiple beam lines. For protons the magnetic lens maintains the signal intensity between the object and the detector plane, while particles failing to pass the angular acceptance cut of the lens are either stopped internally in the lens, or fall off in intensity as the distance from the object to the detector squared. With the long length of the magnetic lens, there is virtually no background from other beam lines.

A numerical example of the background issue dramatically demonstrates the difference between protons and x-rays. We will use a very simplistic model that demonstrates the gross features of the issue. We take an object which has a maximum thickness L, and a minimum thickness of fL, where $f < 1$. The signal at the thickest part of the object is given by eq. (1)

$$signal \equiv S = N_o \exp(-L/\lambda). \qquad (19)$$

For a calculation of the background we again start with eq. (1), and substitute the distance the proton has penetrated into the object (x) in place of L. We then calculate the differential of that in order to calculate, as a function of x, the number of protons which undergo a scattering in a length dx. Ignoring the leading minus sign, which indicates a loss of particles from the incident beam, this gives

$$dN(x) = N_o \lambda^{-1} dx \exp(-x/\lambda). \qquad (20)$$

Next we calculate the number of those $dN(x)$ scattered particles that make it out of the object. We do this at the thinnest part of the object where the distance the particles still have to travel to get out of the object is $fL - x$. (We ignore the fact that the particles are now traveling at an angle to their original direction and therefore have a somewhat greater distance to travel.) This calculation is again done using eq. (1) and we find the number of *surviving scattered* $\equiv SS$ particles to be

$$SS = dN(x) \exp[-(fL-x)/\lambda] = N_o \lambda^{-1} dx \exp(-x/\lambda) \exp[-(fL-x)/\lambda] = \{N_o \lambda^{-1} \exp(-fL/\lambda)\} dx. \qquad (21)$$

Integrating eq. (21) over the thickness of the object at its thinnest location (*i.e.* $x: 0 \to fl$) gives

$$total\ SS = N_o \lambda^{-1} fL \exp(-fL/\lambda). \qquad (22)$$

To find the *background* we just need to multiply the *total surviving scattered* value by the detector fractional acceptance at the region of thickest part of the object for those scattered particles. We take this to

Table 3: Signal to background values assuming $H = 0.001$.										
material	$\lambda_{nuclear}$ (g/cm^2)	$\lambda_{5\ MeV\ x\text{-}ray}$ (g/cm^2)	L (g/cm^2)	f	$(S/N_o)_{nuclear}$	$(S/N_o)_{x\text{-}ray}$	$S/B_{nuclear}$	$S/B_{x\text{-}ray}$	$R_{nuclear}$	$R_{x\text{-}ray}$
iron	131.9	34	304	0.2	0.1	1.32E-04	344	0.4	6.3	1269.2
iron	131.9	34	212	0.2	0.2	1.94E-03	857	5.4	3.6	147.7
iron	131.9	34	91	0.2	0.5	6.79E-02	4143	216.3	1.7	8.6
iron	131.9	34	304	0.5	0.1	1.32E-04	275	2.6	3.2	87.0
iron	131.9	34	212	0.5	0.2	1.94E-03	556	14.1	2.2	22.7
iron	131.9	34	91	0.5	0.5	6.79E-02	2040	193.9	1.4	3.8
lead	194.0	23	447	0.2	0.1	3.67E-09	344	4.60E-05	6.3	5595334.9
lead	194.0	23	312	0.2	0.2	1.27E-06	857	7.07E-03	3.6	52062.9
lead	194.0	23	135	0.2	0.5	2.89E-03	4143	8.0	1.7	107.5
lead	194.0	23	447	0.5	0.1	3.67E-09	275	6.24E-03	3.2	16496.5
lead	194.0	23	312	0.5	0.2	1.27E-06	556	1.66E-01	2.2	886.8
lead	194.0	23	135	0.5	0.5	2.89E-03	2040	18.4	1.4	18.6

be H. Thus we find the *signal* to *background* value $\equiv S/B$ is given by

$$S/B = N_o\exp(-L/\lambda) / [H\, N_o\lambda^{-1} fL \exp(-fL/\lambda)] = \lambda(HfL)^{-1}\exp[-(1-f)L/\lambda]. \qquad (23)$$

In Table 3 are given some values of the S/B for different materials, values of L, and values of f, both for 5 MeV x-rays and high energy protons. Also given are the beam transmission probabilities (S/N_o) at the thickest part of the object. We take $H = 0.001$. It should be noted that due to the limited momentum transmission of the magnetic lens in proton radiography, the value of H for protons should be less than that for x-rays, improving the S/B value for protons relative to that for x-rays beyond the values shown.

A related issue addressed in Table 3 is the dynamic range required for the detector. If a uniform intensity beam is incident on the object, the ratio, R, of the signal intensity at the thinnest part of the object to that at the thickest part of the object (ignoring background) is given by

$$R = N_o\exp(-fL/\lambda) / [N_o \exp(-L/\lambda)] = \exp(\,(1-f)L/\lambda). \qquad (24)$$

As Table 3 shows, R can be quite large for x-rays, especially when λ is small compared to L. In looking at these values and considering the detector dynamic range and sensitivity, it is important to keep in mind that the detector must, in addition, be able to see on the order of a 1% change in object thickness at the thickest part of the object.

The preceding calculations do not deal with the production of secondary particles in the object due to nuclear interactions. We examined this issue in a Monte Carlo study which used the latest version of the LAHET[6] code, which in turn uses FLUKA[7] to simulate the nuclear scattering and particle secondary production. In the study, a zero diameter beam of 50 GeV protons was incident normal to a slabs of ^{238}U of different thicknesses. At the downstream face of the slab we recorded all outgoing particles. For those particles, their particle type, location, and 3-momentum were recorded. Neutrons were tracked down to kinetic energies of 20 MeV. Due to the inability of LAHET to directly deal with γ-rays, and electrons and positrons, these were ignored. The predominant source of γ-rays will be π^0 decays, whose number will be about the same as those for π^+ or π^-, the dominant secondary charged particles. As the π^0 decays essentially instantaneously, into two γ-rays, by the above arguments, their number will initially be about equal to the number of secondary charged particles. However, the γ-rays will be strongly attenuated in the object, and the few surviving γ-rays will be spread over a large angular region and thus outside the angular acceptance of the magnetic lens system. Since they are also nearly invisible to the detectors, their omission should have a negligible effect on the results. Fig. 4 gives the angular distribution of all the particles making it out of the back of the slab sorted by particle type. Fig. 5 shows a similar plot, but for outgoing particle momentum. Both figures are for 500 g/cm^2 of uranium, a very thick object, where the background problem will be most severe. In Table 4, we record the signal and background values for cuts on the outgoing particle angle and momentum for different slab thicknesses. We consider signal particles to be protons which have angles inside the outgoing angle cut, and a momentum which is greater than the expected average momentum of protons exiting the slab minus 5%. As can be seen, secondary particles contribute very little, and the dominant secondary particles are neutral and thus essentially invisible to the detector.

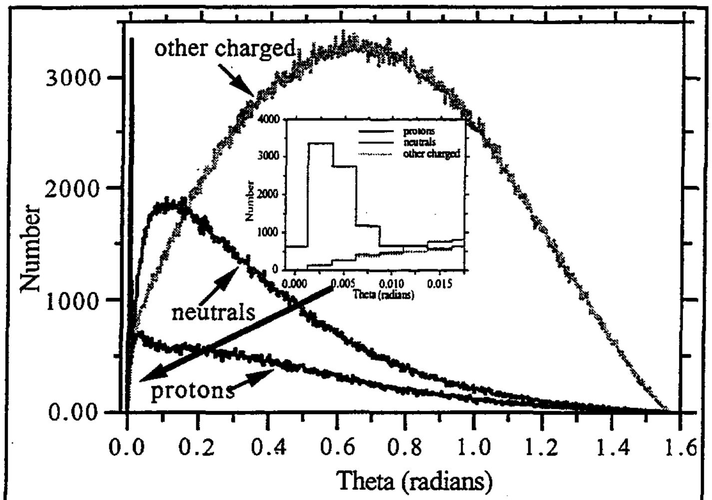

Fig. 4. Histograms of the number of outgoing particles of a particular type as a function of scattering angle for 100,000 incident 50 GeV protons on a 500 g/cm² slab of ^{238}U.

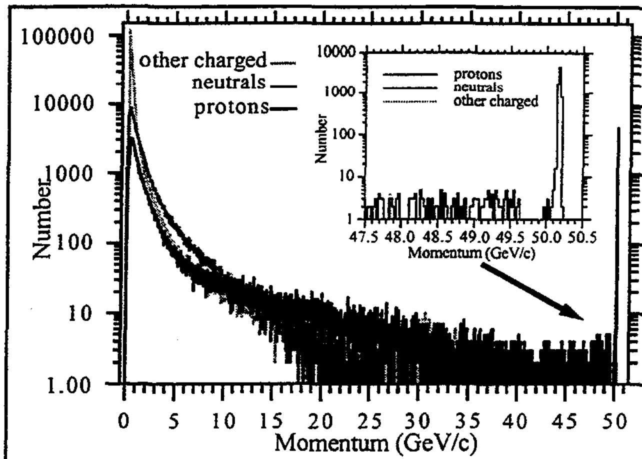

Fig. 5. Histograms of the number of outgoing particles of a particular type as a function of momentum for 100,000 incident 50 GeV protons on a 500 g/cm² slab of ^{238}U.

EXPERIMENTAL WORK

We have carried out a number of experimental tests of the PRAD concept using magnetic imaging lenses. Some of these tests were carried out at the LANSCE facility, making use of its 800 MeV chopped proton beam. The 800 MeV beam energy is too low to allow for the study of thick objects in which nuclear attenuation is important. This is due to the large dispersion in momentum loss by the protons at 800 MeV, both directly and as a result of variations in object thickness. As discussed earlier, this results in poor lens performance and hence a blurred, poor quality image. However, by looking at thinner objects, we could still study the MCS part of the PRAD concept, the actual performance of the magnetic lens system, and by making use of the pulsed nature of the proton beam (one pulse every $N\times358$ ns, N = integer), take a sequence of radiographs of explosively driven events.

The ability to take high contrast, high resolution images using a MCS angle cut for a thin object is demonstrated by the image shown in Fig. 1, which is a static radiograph taken using a phosphor image plate as a detector. The object is a 50 Ω BNC terminator that is only 1.4 cm in diameter. The resistor and its leads inside the metal case of the terminator are clearly visible, as are the internal screw threads. Even submillimeter features are sharp. Radiographic images of a dynamic event are shown in Fig. 6. The object is a 58 mm diameter half-sphere of high explosive (HE) which is in the process of detonating. These images were again made with phosphor image plates. Four different explosive shots were fired to produce the four radiographs, with the proton beam timed to arrive at different times relative to the detonation initiation time. The different times are (top to bottom) 0.99 μs, 1.90 μs, 2.50μs, and 3.25μs after detonation initiation. Also shown are the results of a reconstruction of the object from those radiographs. The position of the shock front (the glitch in Fig. 6) associated with the detonation is seen to progress between the different radiographs. The shock front is seen to correspond to about a 30% increase in local

Table 4: Particle generation & survival in the given amount of ^{238}U

	no cut	10 mrad θ cut	47.9 GeV/c momentum cut	momentum and θ cut
50 g/cm²				
protons	151840	77756	77015	76761
neutrals	211620	633	21	11
other charged	196658	837	0	0
100 g/cm²				
protons	182034	60733	59584	59184
neutrals	448298	1017	36	14
other charged	331171	1364	0	0
200 g/cm²				
protons	212593	36998	35597	35134
neutrals	883247	1318	45	23
other charged	473650	1691	0	0
500 g/cm²				
protons	168694	8209	7473	7160
neutrals	1319912	935	11	5
other charged	397354	1044	0	0

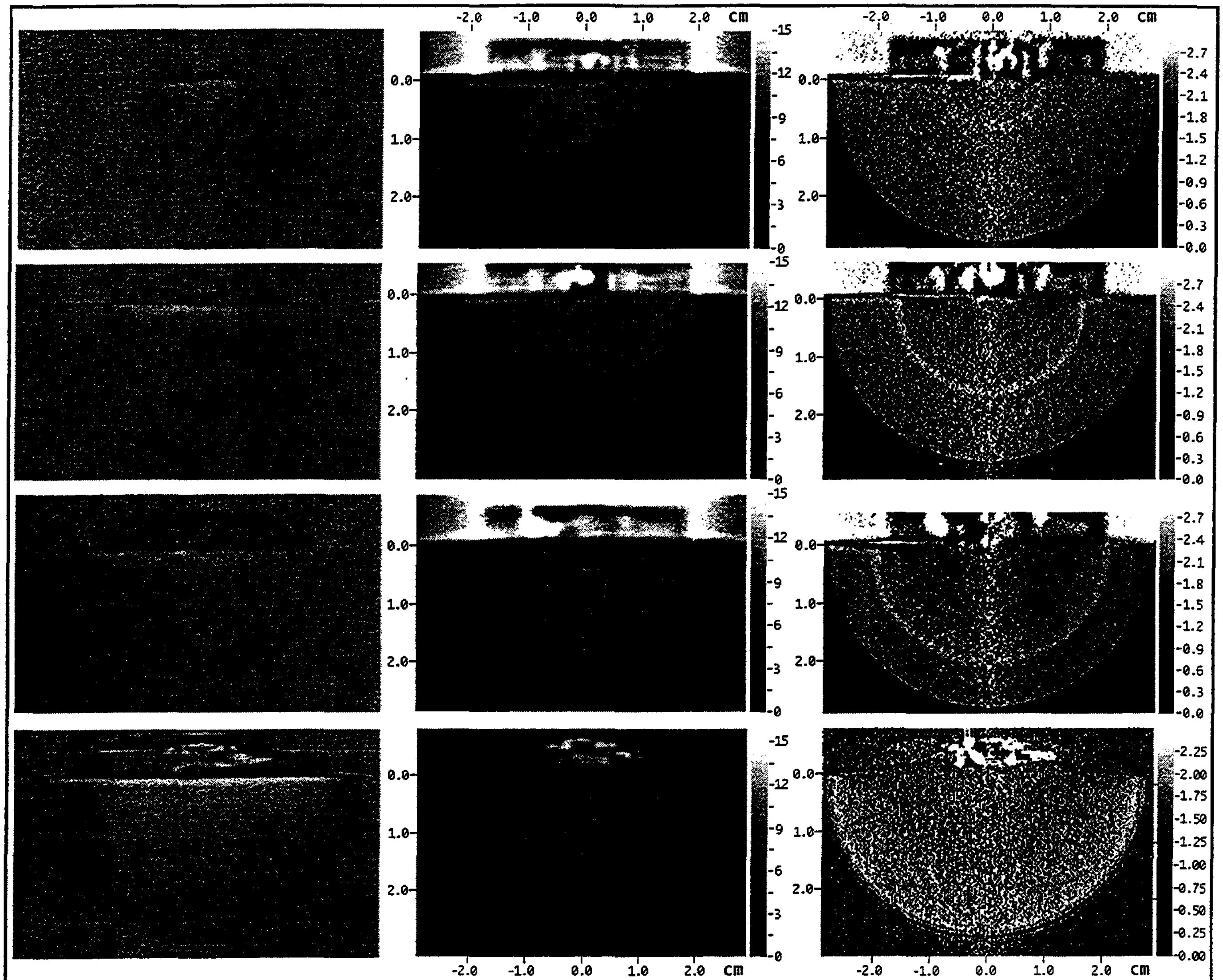

Fig. 6. Original data and reconstructions from phosphor image plate proton radiographs of a hemispherical piece of HE at different times following detonation (top to bottom: 0.99 μs, 1.90 μs, 2.50μs, and 3.25μs after detonation initiation). The left column is the ratio of a radiograph at the given time after detonation initiation to an identical radiograph taken prior to detonation. The central column gives the unfolded amount of material in units of g/cm^2 using the measured beam attenuation, the known radiation length for the HE material, and the known MCS angle cut. The right column is a reconstruction of the density of the material obtained using the preceding results and a hemispherical object shape. The reconstruction starts at the left and right edges of the object and works towards the vertical centerline of the object, resulting in the increased error seen towards the centerline.

density. Behind the shock front a rarefaction can also be seen. For the above images, the collimator inside the magnetic lens was set to provide a MCS angle cut of 10 milliradians.

To test the PRAD concept at higher energies, we made use of a 10 GeV secondary proton beam at the AGS at BNL. The various components of the experimental setup are shown in Fig. 7. As a secondary beam line was being used, the instantaneous proton beam flux was low, allowing us to use wire chambers to track the protons individually from upstream of the object location to the image plane of the magnetic lens. Images were made with both the wire chambers and phosphor image plates using long exposure times. One of the objects we imaged, also shown in Fig. 7, is known as the French Test Object (FTO) and consists of concentric spherical shells. The outer shell is a density 1/2 g/cc plastic foam and covers the radial region between 6.5 and 22.5 cm. The next inner shell is copper and is in the region between 4.5 and 6.5 cm. The third shell is a tungsten alloy and covers the region between 1 and 4.5 cm leaving an air

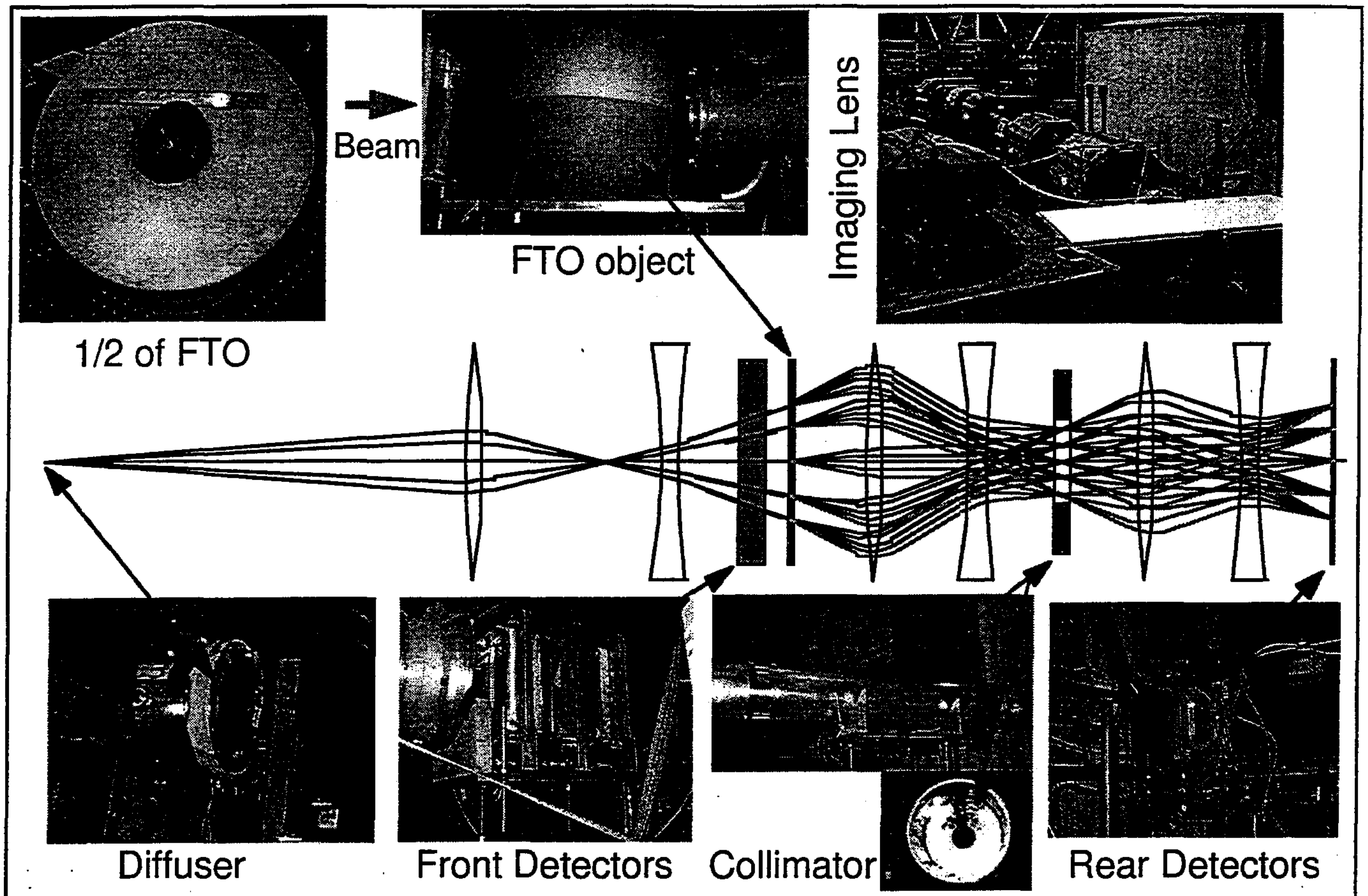

Fig. 7 Schematic of the PRAD magnetic lens system and actual components for EXP. 910 at the BNL AGS. The beam is first prepared with a diffuser and matching lens to meet optics requirements. Next the beam is measured just upstream of the object by the front detectors after which it passes through the object being radiographed. The transmitted beam passes through an iris, or aperture, located in the middle of the 4-quadrupole -I magnetic lens system and is focused on the rear detectors. The runs with different angle cuts were done separately using different collimators. The data from these runs provide the information needed to reconstruct both the density profile and material composition of the object.

cavity in the center. The maximum object thickness is 213 g/cm^2, just tangent to the central cavity. The magnetic lens system had an effective horizontal and vertical aperture of about ± 7 cm. Two sets of images were taken of the FTO, one with a collimator corresponding to $\theta_c \sim 9$ mrad, and the second with a collimator corresponding to $\theta_c \sim 4.5$ mrad. The first collimator passes nearly all of the MCS distribution but not the nuclear inelastically scattered particles, whereas the second cuts substantially into the MCS distribution. The resulting image plate radiographs are shown in Fig. 8. Fig. 9 shows the radial distributions resulting from those radiographs and the "radiographs" of the beam intensity incident on the object. The results of a reconstruction of the object are shown in Fig. 10 and are given in Table 5, which also gives the actual locations of the changes in the material type and the Particle Data Book[4] values for the nuclear interaction lengths and radiation lengths of the relevant materials. The results clearly demonstrate the ability to unfold material type and thickness.

We also used the wire chamber data to study background issues. The beam energy, although still a factor of about 5 less than that being discussed for the AHF, is sufficient to address most of the background problems, as one is well above the particle production threshold energies that will be most relevant at 50 GeV. The wire chambers consisted of multiple planes providing both X and Y information, which could in turn be used to provide particle direction information. As the magnetic lens used was a – I lens, summing the proton position at the object plane and the image plane should ideally give a value of zero regardless of the proton position in the object plane. This is shown in Fig. 11, where scatterplots of $YSUM = Y_{object} + Y_{image}$ versus $XSUM = X_{object} + X_{image}$ are given. Also shown are scatterplots of the particle scattering angle vs. $XSUM$. The upper left plot has a linear intensity scale showing that the vast

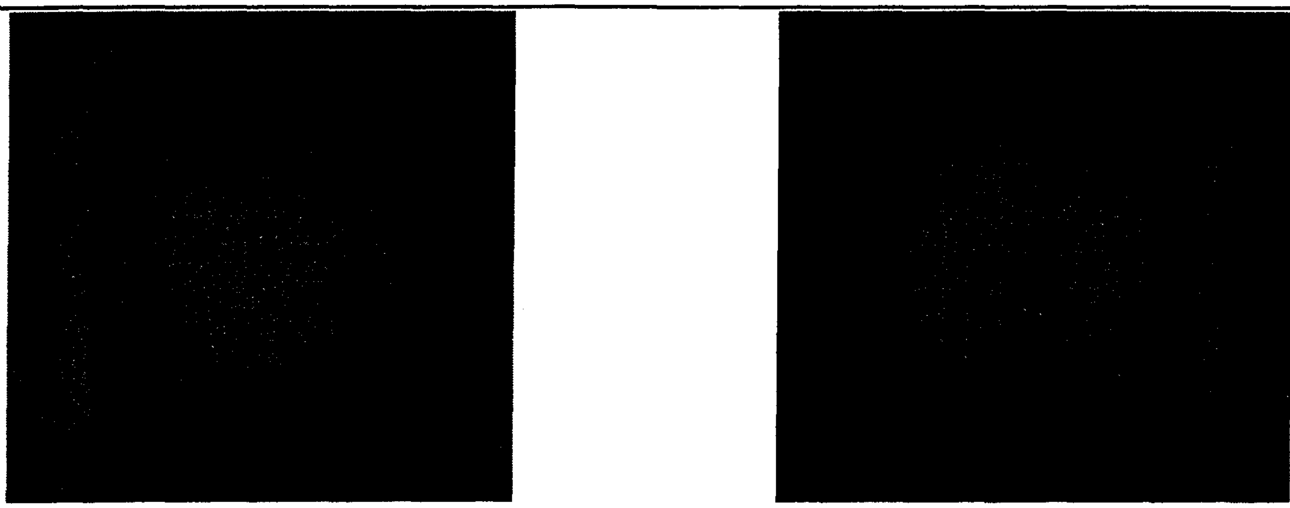

Fig. 8 Results from proton radiograph image plate pictures of the FTO. Shown are "negatives" of the beam distribution normalized images. The left (right) image corresponds to the ~9 (~4.5) mrad collimator. The slightly trapezoidal shaped region is the field of view of the magnetic lens. The outer edge of the copper shell nearly fills the field of view.

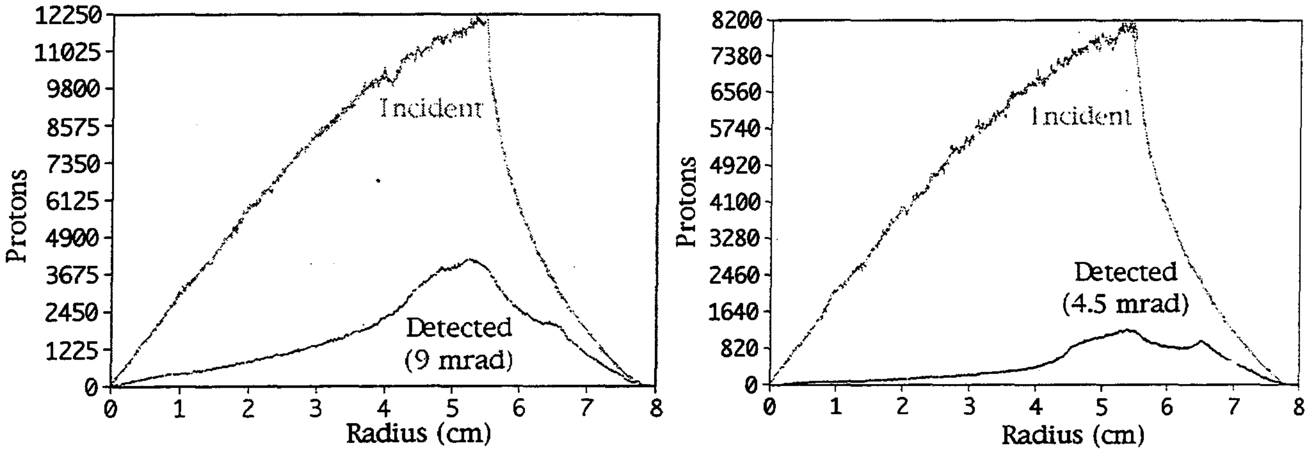

Fig. 9. Radial distributions for the radiographs of FTO similar to those given in Fig. 8, but using the wire chamber data. The left (right) plot is for the 9 (4.5) mrad collimator. The upper (lower) curve is the number of incident (transmitted) particles. The drop to zero in the radial distributions as zero radius is approached is simply a solid angle effect.

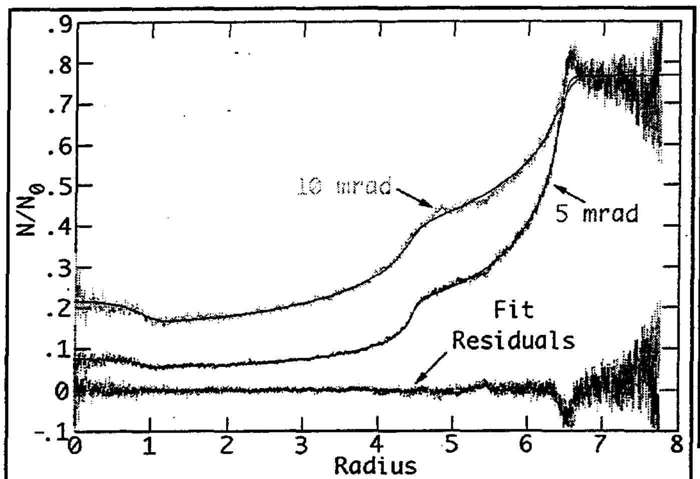

Fig. 10. Fits to the transmission data for the FTO. The upper two curves are the measured transmission vs. radius. The bottom overlaid curves are the residuals of the two fits.

Table 5: Fitting results.

Material	Radius (cm)	λ (cm)	X_0 (cm)	
Void	0.98	–	–	Fit
	1.00	0.0	0.00	Real
Tungsten	4.48	10.5	0.38	Fit
alloy	4.50	10.1	0.37	Real
Copper	6.47	14.2	1.10	Fit
	6.50	15.1	1.42	Real
Foam	–	–	–	Fit
	22.50	160.0	84.00	Real

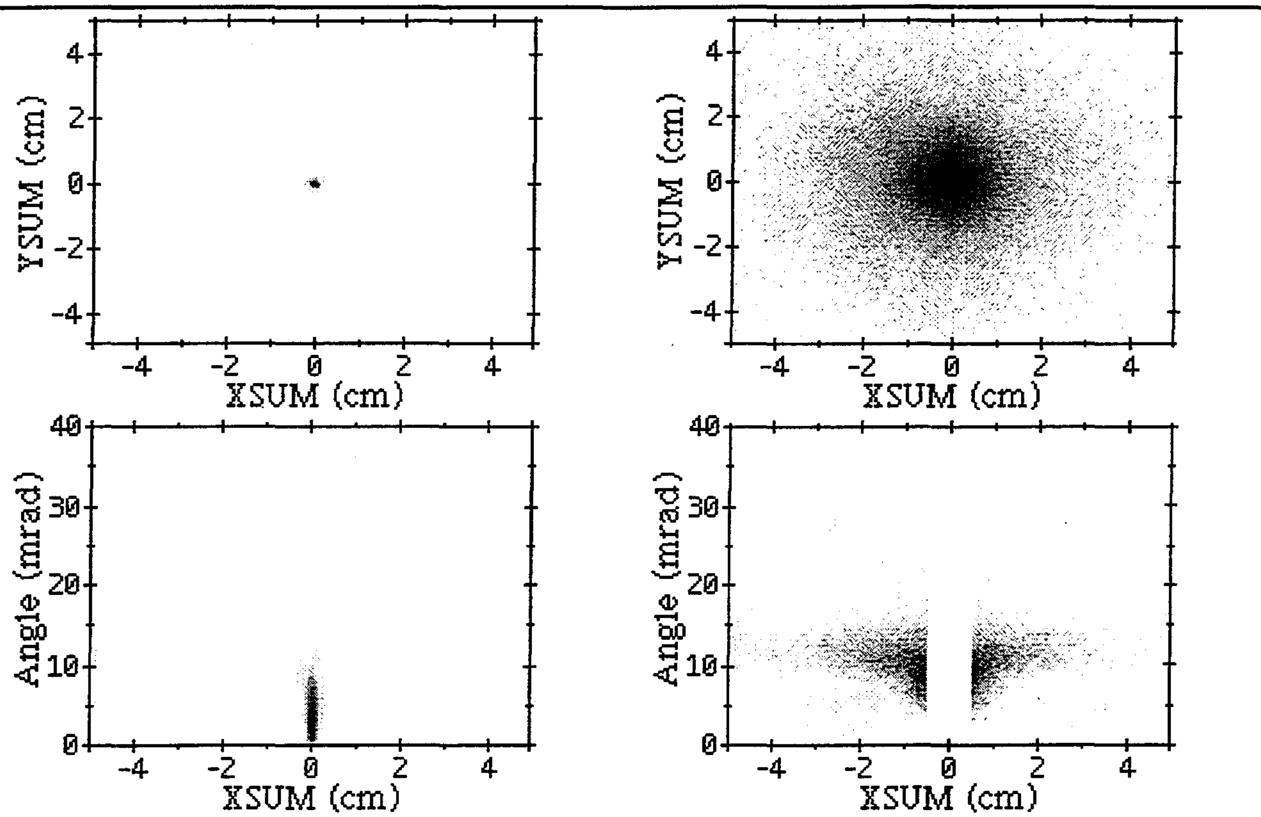

Fig. 11. Top left: two-dimensional histogram of XSUM vs. YSUM on a linear scale; top right on a logarithmic scale; bottom left: XSUM vs. scattering angle on a linear scale; bottom right: on a logarithmic scale with the additional restriction that both $|XSUM|$ and $|YSUM|$ be larger than 5 mm.

majority of events are not "problem" events. The upper right plot is the same data, but plotted on a logarithmic intensity scale to highlight the "problem" events. The bottom left plot shows on a linear intensity scale the proton scattering angle in the object as a function of $XSUM$ and demonstrates that the lens also performs well over the relevant range of scattering angles. The bottom right plot shows the same distribution but on a logarithmic intensity scale and only for "problem" events. The "problem" or background events are defined as those that have both $|XSUM| > 5$ mm and $|YSUM| > 5$ mm. (This explains the missing events in the $|XSUM| \leq 5$ mm region of the plot.) The information on background is more qualitatively given in the histograms shown in Fig. 12. The events shown are from a radiograph of the FTO, where only those events that at the object plane were within a horizontal band of ± 5 mm height centered on the FTO were used. It should be noted that the events considered passed all the way through to the imaging lens and to a trigger counter located behind the wire chambers at the image plane. (This explains the shape of the object plane distributions in Fig. 12, where the central air cavity and copper to tungsten transitions are evident.) The left column gives the X-distribution of those particles measured at the object plane, whereas the right column is for the same particles, but measured at the image plane. Each plot has two curves. The upper curve (darker) curve is for all events, whereas the lower (lighter) curve is for the background events as defined previously. There were several problems with the experimental setup which caused larger than expected backgrounds. One problem was inadequate shielding upstream of the object which allowed particles outside the "field of view" of the upstream lens to reach the object and image plane. Another problem was that the incident beam was by mistake not centered on the object; the majority of the beam actually missing the object and hitting the upstream magnets. The third problem was inadequate thickness for the collimator, which allowed some of the protons that hit the collimator to still reach the image plane. With the use of the wire chamber data, these types of events could be removed. This is shown in the lower two rows of histograms in Fig. 12. The measured "expected" background to signal values can be read off of the bottom row histograms and are on the order of a few percent. A more careful set-up would no doubt have improved these values.

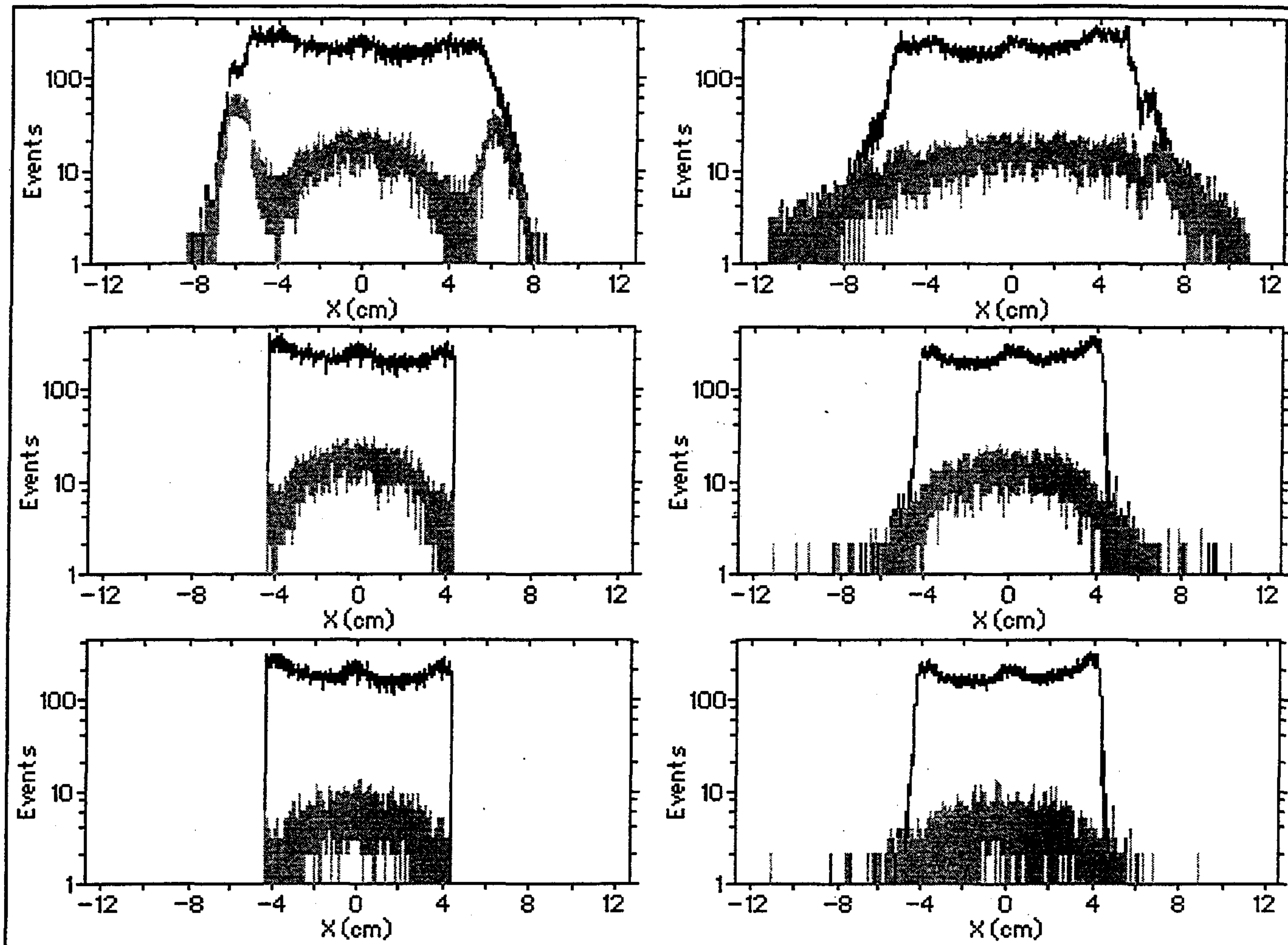

Fig. 12. Left: histograms of X positions at the object plane for events within a 1 cm high band in Y centered on the FTO at the object plane. Right: histograms of positions at the image plane. Top: all events. Middle: events required to be in the lens field of view at the object. Bottom: events also required to be within the collimator acceptance. The upper lines are the signal plus background. The lower lines are the background.

AHF PROTON ACCELERATOR COMPLEX

The AHF will be required to produce transmission radiographic images with high spatial and temporal resolution From 4 to 16 simultaneously-illuminated views and 25 or more time-separated exposures per view are desired. The desired beam-pulse structure needs to be flexible, with 10^{10} to 10^{11} protons in a 10-20 nsec-long pulse per view. A programmable time separation between pulses in each view which varies from a minimum of about 100 nsec to a maximum of many microseconds. These requirements lead to the use of a low-duty-factor, slowly cycling proton synchrotron with a flexible multipulse beam-extraction system, feeding into a multistage beam-splitting transport system that transmits proton pulses to the test facility.

The total number of protons in the ring is approximately 10^{13}. This number follows from the following arguments. If we want pixel by pixel measurements that have an accuracy of 1 part in A, we need A^2 particles per pixels from counting statistics arguments alone. Allowing for other measurement errors such as those associated with the detectors, we need to boost the number of particles by a factor of B. The beam is attenuated by the object by a factor of C, thus we need A^2BC particles per pixel in the incident beam. Taking into account the area of the object we need an additional factor D given by *(area of object) / (area of a pixel)*. If we now have E views, assume losses in the beam splitting chain are a factor of F overall, and record G frames per view, the machine must deliver $A^2BCDEFG$ protons in a shot. Going back to Table 1, and taking round number values, we have $A \sim 100$, $B \sim 2$, $C \sim 5$ (the Gaussian shaped

Table 6. Twelve-View Beamline Summary	
Total splitter sections	4
Total straight cells	120
Total bend cells	232
Quadrupole Length (m)	704
bore radius (cm)	0.5
gradient (T/m)	2.5
Number of Dipoles	928
Dipole Length (m)	2.0
gap (cm)	5.0
field (T)	4.2

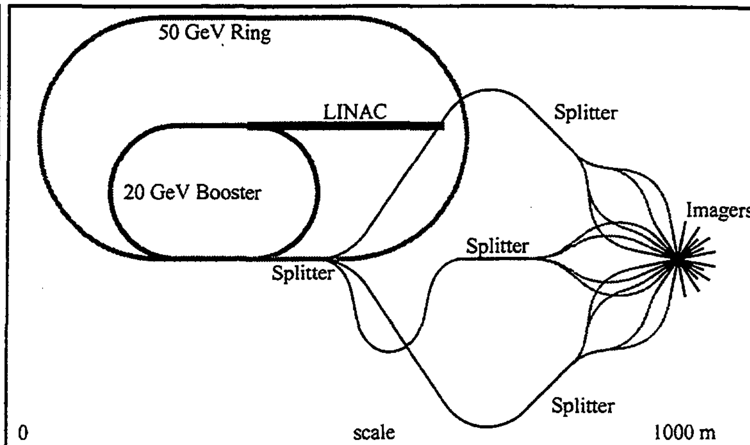

Fig. 13. Layout of the entire facility for 12 views, showing the linac, booster, main ring, and beamlines.

beam centered on the thickest part of the object helps here), $D \sim (10\ \text{cm}/250\ \mu\text{m})^2 = 160{,}000$, $E \sim 16$ (beam splitting in our design is in multiples of 2), $F \sim 2$, and $G \sim 25$, which approximately yields the 10^{13} value.

The nominal beam energy of 50 GeV is set by object thickness and also by the thickness of the vessel (windows) that must contain the blast. The present study is based on an 800-MeV linac, such as available at LANSCE, which injects an H^- beam directly into a 50 GeV synchrotron. Numerous proton synchrotrons in the energy and/or intensity range needed for PRAD are presently in operation around the world. Thus the technology required for a PRAD accelerator has already been demonstrated. A conceptual point design for a system that can meet the above requirements has been presented elsewhere[8]. The synchrotron is fairly conventional, except for use of a lattice with an imaginary transition γ and certain features of the achromatic arcs.

There are two design parameters of a PRAD synchrotron that need some particular attention. First, simplicity of operation and low intensity suggests that a booster stage can be avoided. However, a critical parameter is the magnetic field at injection time. For a 50 GeV synchrotron operating at 1.7 Tesla at full energy, the magnetic field at injection time with 800 MeV injection is 0.05 Tesla. This is thought to be about the minimum practical field. Thus 50 GeV is the maximum practical energy for injection by the existing LANSCE linac at Los Alamos. For a higher energy PRAD synchrotron, either a booster synchrotron, or a higher energy injection linac would be required. (If constructed on a greenfield site, a lower energy linac plus a small booster would be a more cost-effective injector solution.)

The second issue concerns beam extraction from the high-energy synchrotron. If single-turn extraction is chosen, then a pulse train of length equal to the circumference of the synchrotron is delivered to the experiment. For a 1.5 km typical circumference of a 50 GeV synchrotron, this amounts to a total pulse train length of 5 microseconds. The bunch frequency in this train is the rf frequency of the synchrotron. We presently favor a 5 MHz rf frequency, thus providing bunch spacing of 200 ns. Loss-less extraction is possible if the kicker rise time is less than 200 ns, which is obtainable with today's technology.

If single-bunch extraction were to be installed, it would be possible to make a quite flexible program of pulse delivery that extends from spacing of 200 ns up to seconds. The total number of pulses available in the reference scheme would be 25 pulses. For this mode of operation, it is likely that a well-terminated single step kicker of 50 Ohm characteristic impedance would be used. For variable proton burst spacing, a modulator capable of providing 25 pulses with variable pulse spacing would have to be developed. Although no such modulator presently exists, it is believed that its development is not likely to present any obstacles to construction of the facility.

Both beam transport and beam splitting are performed in the beam transport system (see Fig. 13). The beamlines are achromatic and isochronous; the latter feature is enforced by symmetry. In the present example, there are 12 beamlines illuminating the target from different angles, both in-plane and out-of-plane. At the end of each beamline, there is a 45-m target-illuminating section that includes a diffuser and magnetic quadrupoles that prepare the beam size and convergence angles for object illumination. On the opposite side of the object containment chamber from each illuminating section, there are magnetic imaging systems and detector arrays. The transport system parameters for the above design are listed in the Table 6 exclusive of the matching and imaging lenses.

CONCLUSION

We have reviewed the basic concept of proton radiography and found that it should perform extremely well and have substantial advantages of x-ray based radiography in the case of thick (100's g/cm^2) objects. In the case of thin objects, it still performs very well, with added bonus that it can be tuned to give high contrast images regardless of how thin the object is. An added feature of proton radiography is the ability to measure, not only the amount of material (as in standard radiography), but also the composition of the radiographed object in terms of material identities. These predictions have been confirmed in beam tests. The proton accelerator needed for a future Advanced Hydrotest Facility is not beyond the scope of existing proton accelerators. Furthermore proton accelerators naturally have the strobed pulse nature needed to follow rapidly evolving dynamic events and can do so for an extended period of time.

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Overview of Radiation Hardness of Silicon Detectors for HE Physics*

B. Dezillie and Z. Li
Brookhaven National Laboratory, Upton, NY 11973-5000

*This investigation was done as a part of work established and supported by the Rose Collaboration (RD48, CERN), and was supported in part by the U.S. Department of Energy: Contract No: DE-AC02-98CH10886.

Abstract

The status of the on-going work in radiation damage and hardness of silicon detectors for high-energy physics experiments is summarized. Recent progress in defect engineering for rad-hard silicon detectors, including low (FZ and CZ) and medium (FZ) starting resistivity silicon, Epi-Si (medium and high resistivities), and non-standard processing (as compared to standard planar processing), will be presented. The results are reported in terms of reverse current, depletion voltage as a function of fluence and annealing time after irradiation.

1. Introduction

Recently tremendous interests have been generated towards the usage of non-standard silicon materials and processing steps for detectors in extreme radiation environment (i.e. LHC). Some of more promising approaches are: 1) usage of medium (~ 1 kΩcm) and low (≤ 500 Ωcm) resistivity n-type silicon as starting material; 2) usage of epitaxial silicon materials; 3) incorporation of impurities in silicon materials during growth and/or during detector processing to getter radiation-induced defects that cause detector degradation; and 4) non-standard detectors processing steps as opposed to the usual planar processing technology. In this paper, the effect of starting resistivity, growth parameters, Epi-Si, and processing parameters on the detector electrical properties, in particular on the effective impurity concentration (N_{eff}), will be summarized and systematically presented.

2. Experimental conditions

2.1 Test structures

The first set of epitaxial (Epi) n-type wafers, with thickness (d) of 100 and 150 μm, was made on 300 μm thick CZ substrates by MACOM (USA). Canberra (Belgium) has processed all MACOM epitaxial samples with the planar technology. Samples labelled C50 → C83 are single round diode areas varying from 0.08 to 2.19 cm^2 [1, 2]. Samples labelled C142-C-A1/A3/B3-# were processed using the CERN II mask design with various structures (pads, strips, pixels).

The second set of Epi-Si wafers (n- and p-type with different thickness: 100, 150 and 200 μm) was grown on 600 μm CZ substrates by ITME (Poland) [3]. Most wafers in this set were grown at a growing rate of 1 μm/min. Some wafers in the set (thickness = 100 μm) were grown at a growing rate of 0.5 μm/min to check the effect of growing rate on radiation hardness. Some wafers in this second set have been processed by the MESA technology by DIOTEC (Slovakia Republic) [4] and cut to single diode test structures of 0.25 cm^2. Some other wafers in the second set were processed by Canberra with the traditional planar technology using the CERN II mask set.

Float-Zone (FZ) silicon detectors with different resistivities have been manufactured by Wacker and processed at BNL, using the standard BNL mask set for test diodes.

Czochralski (CZ) silicon wafers with an initial resistivity of 100 Ω cm have been manufactured by Polovodice (Czech Republic) and processed at BNL.

Parameters of Epi-Si samples studied here are listed in Table I and II. Table III gives the parameters, as well as radiation fluences, of Epi, FZ, and CZ silicon samples for the study of the initial resistivity effect on radiation hardness of detectors.

Table I Initial characteristics and names for n-type epitaxial samples (Conduction: n-type)

Manufacturer	Producer	Epitaxial thickness (μm)	Resistivities [Ωcm]	Substrate thickness (μm)	Naming convention
MACOM	Canberra	120	960	300	C50
		110	500 - 860	300	C52 → C72
		100	600 - 800	300	C73 → C83
		100	800	300	C142-C-B3-1 → 20
		100	800	200	C143-C-B3-1 → 20
		150	2000	300	C144-C-A3/B3-1#
		150	2000	300	C145-C-B3-1 → 20
		150	2000	300	C146-C-#
ITME	Canberra	105	~2200	600	I3-C-B3-1 → 10
		90	~4000	600	I14-C-B3-1 → 10
		150	~10.000	600	I23-C-B3-1 → 10
		185	~12.500	600	I33-C-B3-1 → 10
ITME	DIOTEC	105	1800 - 4200	600	I1→ 9-B-1 → 30
		90	6000 - 7250	600	I11→19-B-1→ 30
		150	5500 - 7450	600	I21→ 29-B-1→ 30
		185	2800 - 3600	600	I31→ 39-B-1→ 30

Table II Initial characteristics and names for p-type epitaxial samples (Conduction: p-type)

Manufacturer	Producer	Epitaxial thickness (μm)	Resistivities [Ωcm]	Substrate thickness (μm)	Naming convention
ITME	DIOTEC	105	390 - [illegible]20	600	I1P→ 9P-B-#
		93	1300 - [illegible]250	600	I11P→19P-B-#
		142	1700	600	I21P→ 29P-B-#
		200	3250 - 4500	600	I31P→ 39P-B-#

Table III The characteristics of samples used in the study of the effects of the initial resistivity on the radiation hardness

Wafer number	Type	Initial resistivity (Ωcm)	Thickness (μm)	$V_{fd.0}$ (V)	Fluence (n/cm^2)
796	CZ	100	325	2700	7×10^{14}
795	FZ	500	265	650	7×10^{14}
C143	Epi	630	100	50	4×10^{14}
C153	Epi	2k	150	36	4×10^{14}
799	FZ	5k	400	90	7×10^{14}

2.2 Irradiation facilities

Proton irradiation has been performed at the Proton Synchrotron (PS) at CERN. The beam energy was 24 GeV (hardness factor = 0.5 * (1 MeV neutron) [ROSE]). The average flux during an entire irradiation was approximately 3×10^9 cm^{-2} s^{-1}. Detectors were irradiated in fluence steps up to a maximum fluence of 4×10^{14} cm^{-2}. Measurements have been taken after each fluence step. Irradiation with 7 to 10 fluence steps usually took around 3 days. The irradiation temperature was 26 °C and measurement and storage temperature was 20 °C.

1 MeV neutron irradiation has been performed within a 24-hour period at the University of Massachusetts at Lowell (USA) and some additional samples were irradiated by 10 MeV neutrons at PTB (Germany).

2.3 Characterisation techniques

Electrical characteristics of samples were obtained from the current-voltage (I-V) and capacitance-voltage (C-V) measurements using a Keithley 487 High Voltage Source Measuring Unit and a Hewlett Packard 4263A Impedance Analyser operating at 10 or 100 kHz. The full depletion voltage (V_{fd}), normalised to a 300 μm diode thickness, is deduced from the C-V curve. The leakage current was obtained from the I-V curve at full depletion. All data presented in this paper have been corrected for self-annealing and normalised to 20°C following [5].

After irradiation, the first annealing measurement has been performed after 10 days of room temperature annealing. Then the detectors were heated in several steps for 1-3 h at 80°C, in order to accelerate the annealing process. The annealing time is then expressed in equivalent room temperature time.

2. Results and discussions

2.1 The effect of material growing and processing

. Growth rates were varied to see if this altered the oxygen and carbon concentrations in the epitaxial layer. Based on some defect kinetic modelling [6], higher oxygen and carbon concentrations were predicted to lead to a more radiation hard material.

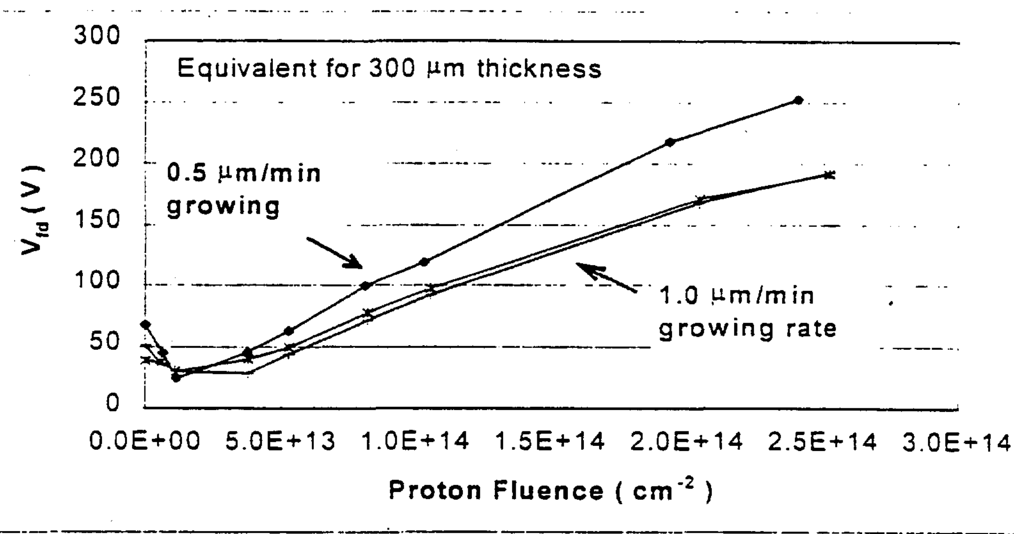

Figure 1: The full depletion voltage (Vfd) as a function of proton fluence for ITME Epitaxial detectors with different growing rates (0.5 and 1 µm/min)

Figure 1 shows V_{fd} as a function of proton fluence for two ITME detectors of 100 and 150 µm thick with a growing rate of 1 µm/min, one ITME detector of 100 µm thick with a growing rate of 0.5 µm/min. It is clear that the rate of increase with fluence (Φ) for detectors with higher growing rate is much smaller than that for detectors with lower growing rate. This may be explained by gettering/sinking effect of irradiation-induced defects by thermal defects. During the growth with a higher growing rate, more defects are likely to form in the material. More defects in the starting material lead again to a more radiation hard material due to possible gettering/sinking effect of radiation induced defects by as-grown defects [7, 8]. However, there was now clear correlation between the oxygen and carbon impurities (measured by SIMS (Secondary Ion Mass Technology) by EVANS Europe) and the radiation hardness of the detectors. The diffusion of defects during the growing process is nearly identical for 100 and 150 µm thick epitaxial layers.

Figure 2 illustrates the volume leakage current as a function of proton fluence for ITME diodes with different growing rate and one MACOM detector of 150 µm thick [2]. All these detectors have been processed in identical conditions by ion-implantation by Canberra. Coherent with the result of the full depletion behaviour after the irradiation (Fig. 1), the leakage current is higher for ITME detectors grown with a lower growing rate. The alpha value for the MACOM sample is much lower than the alpha value for the ITME samples. However, no details about the MACOM growing procedure are known. Nevertheless there exists a clear difference the two manufacturers, indicating strong processing dependence.

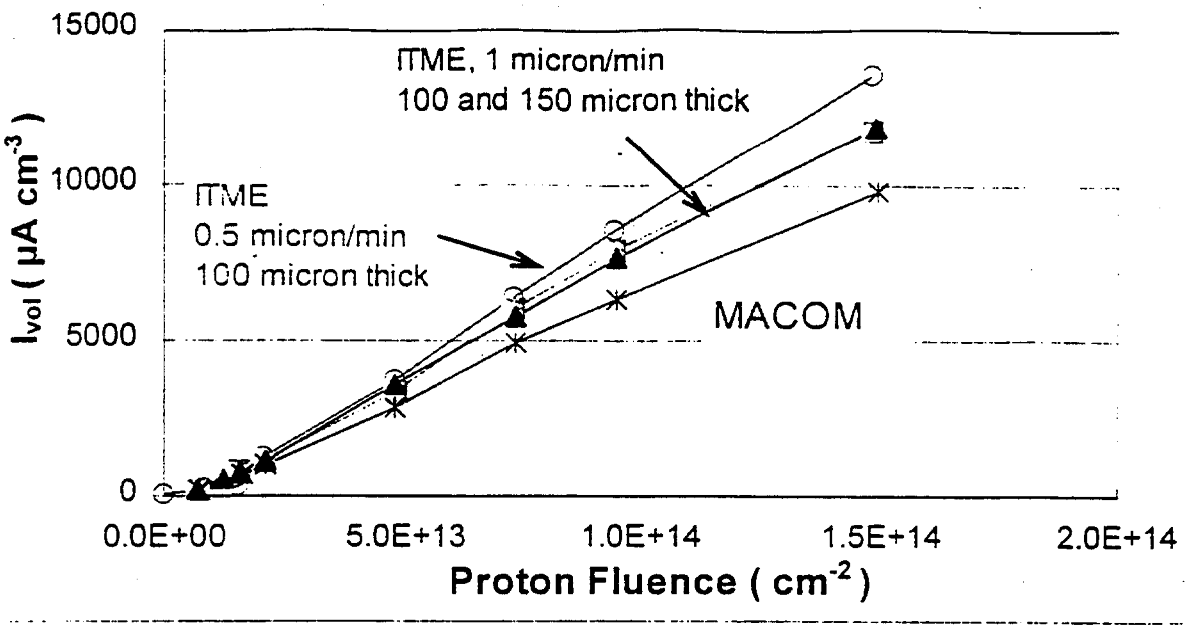

Figure 2: The leakage current as a function of proton fluence for ITME diodes with different growing rates and one MACOM diode, all processed by ion-implantation.

Figure 3 shows the SIMS results (measured by EVANS Europe) for a processed MACOM and an unprocessed ITME detector. The oxygen concentrations are identical for both (in the order of $5x10^{16}/cm^3$), but the carbon concentration for the more radiation hard MACOM sample is three times lower than the ITME sample. This result indicates that high carbon concentration – in contrast to what the modelling predicts - have a negative influence on the radiation hardness.

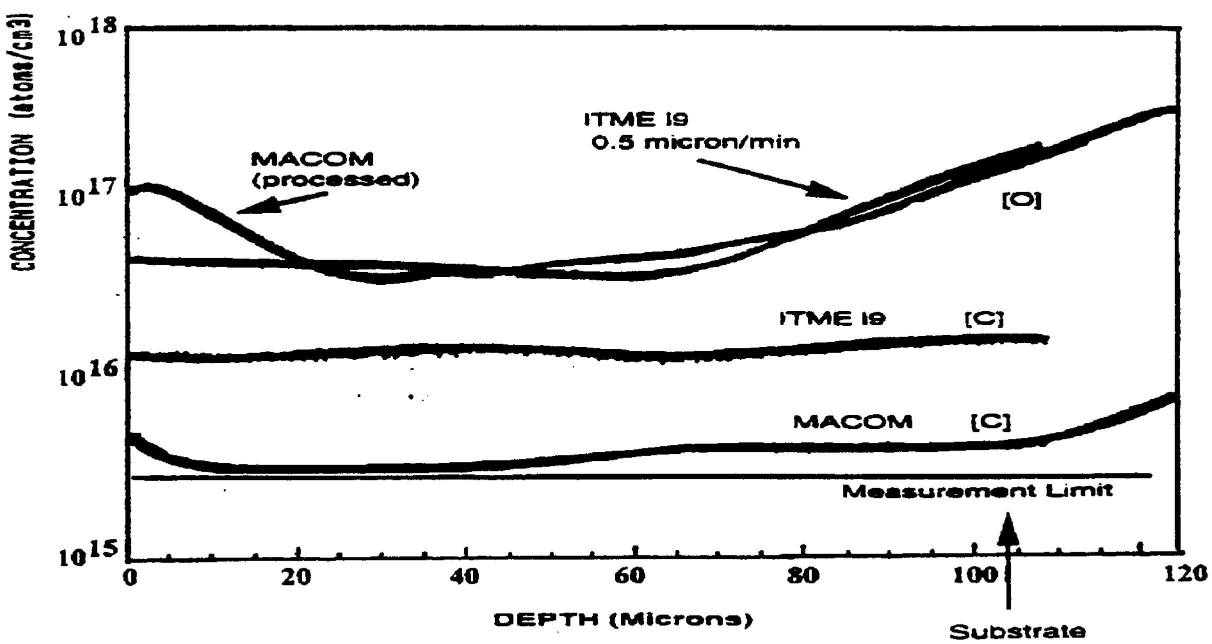

Figure 3: SIMS analysis of a processed MACOM and unprocessed epitaxial wafer.

The structure and orientation of the crystal lattice could also play a role in the defect kinetics and the radiation hardness of the material. It is known that MACOM changed the crystal orientation from <111> to <100>. Detectors with <111> crystal orientation are more radiation hard than those with <100> crystal orientation. But the direct influence of crystal orientation on the radiation hardness is not clear since detectors grown with the <100> orientation have also higher initial resistivity, which, as we will describe in the following section, would also have strong effects.

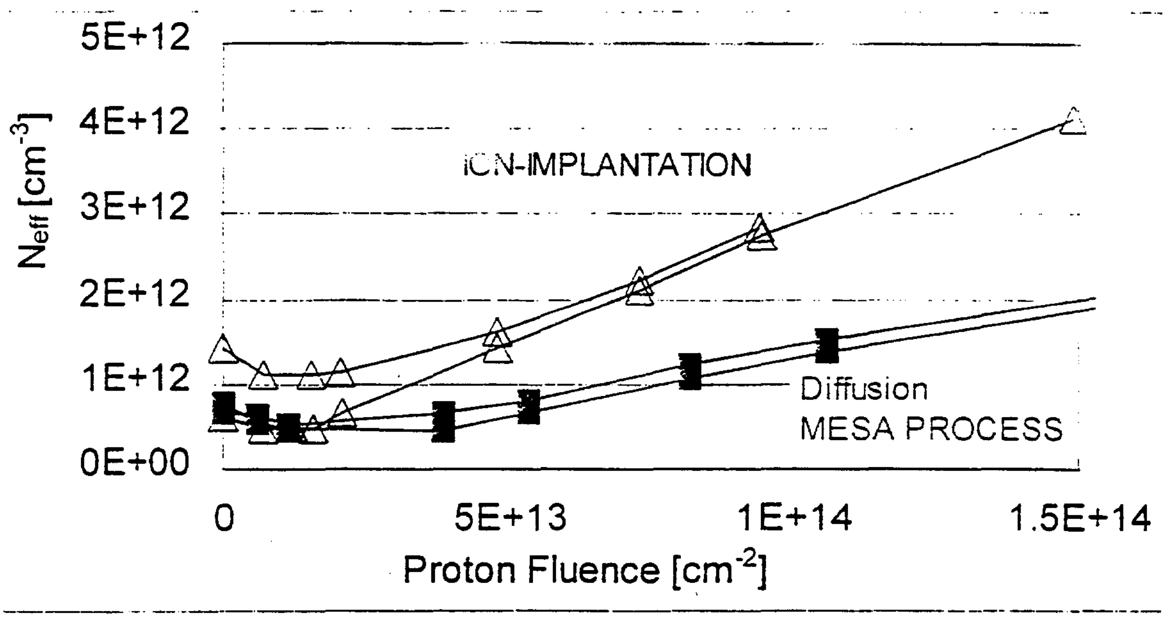

Figure 4: The effective impurity concentration as a function of proton fluence for MESA and Planar processed diodes from the same material.

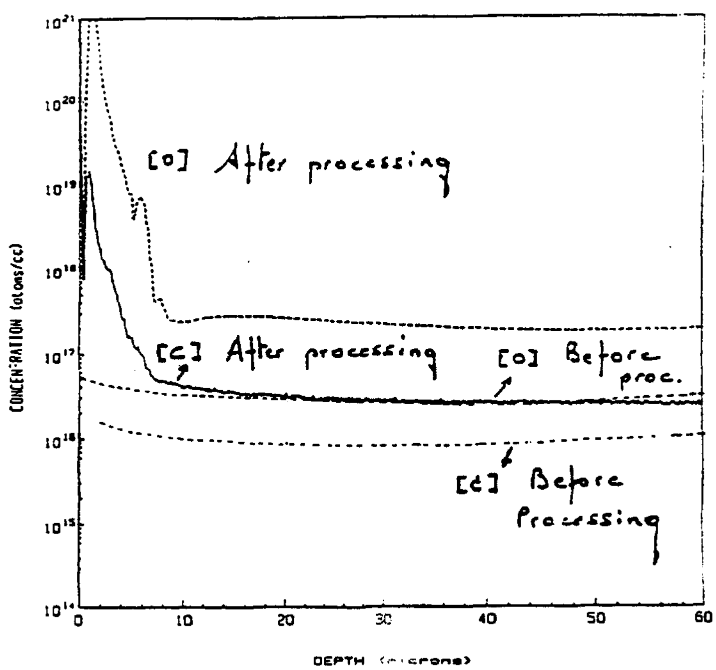

Figure 5: SIMS measurements by EVANS Europe. Depth profiles for an ITME, 100 mm thick (1 µm/min growing rate), n-type epitaxial material. A large increase of [O] and [C] is observed.

As shown in Fig. 4, epitaxial as well as FZ diodes processed with MESA method are twice as radiation hard as those processed by planar technology. SIMS measurements show a huge increase of oxygen and carbon concentration after the MESA processing, as shown in Fig. 5. We should note here that, MESA method could also introduce other impurities as well as defects in detectors during processing, since it is a highly invasive technology [4]. However, the strong influence of processing-induced impurities/defects on the radiation hardness is once more observed.

Some epitaxial diode have also been irradiated under a constant bias (150 volts) [2], which was set to be larger than V_{fd} at anytime during irradiation. No difference in alpha and beta (β) values between biased and non-biased epitaxial detector has been observed (e.g. Fig 6 shows V_{fd} vs. fluence). During the annealing process after irradiation, the biased detector was held continuously at the same bias voltage (even during the heating period to accelerate the annealing process). Figure 7 gives the alpha evolution as a function of equivalent time at room temperature (RT). Again, no effect of the bias has been observed during the annealing process of both alpha and beta values.

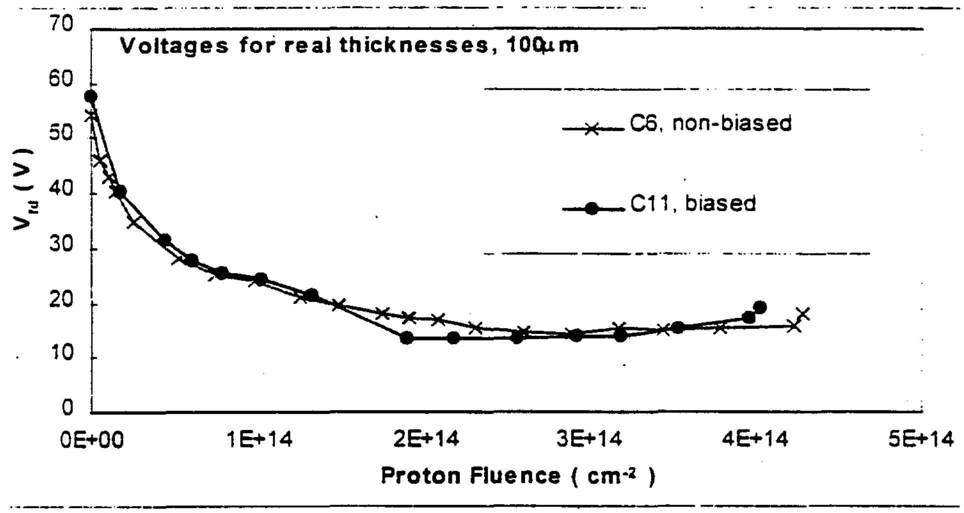

Figure 6: The full depletion voltage for real diode thickness (100 µm) as a function of proton fluence for MACOM epitaxial detectors.

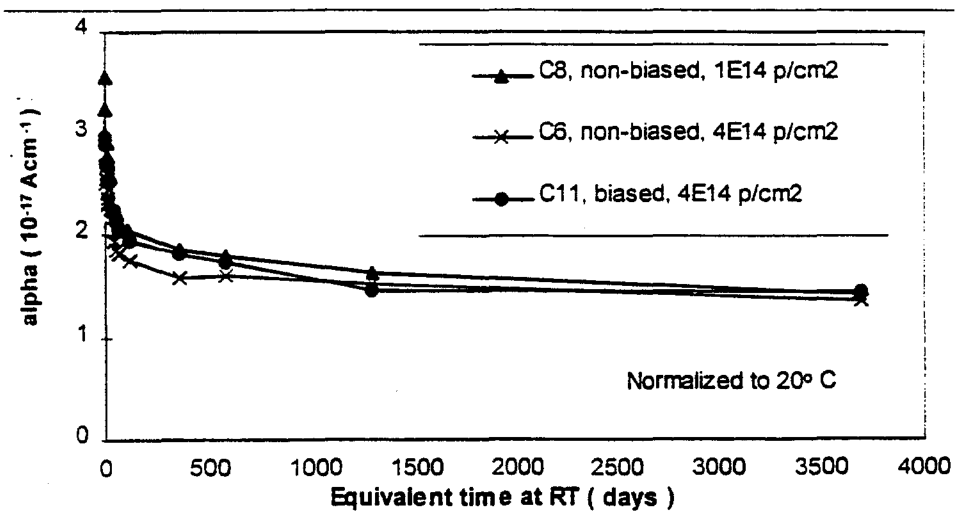

Figure 7: The damage constant alpha versus equivalent time at RT for biased and non-biased MACOM epitaxial detectors.

Table IV gives an overview of alpha and beta values for detectors made with the different epitaxial materials and processes.

The alpha factor is determined as: $\alpha = \Delta I_{vol} / \Phi$. The beta factor is calculated from the equation: $N_{eff}(\Phi) = |N_{D,0}\, e^{-c\Phi} - N_{A,0} - \beta\Phi|$, with $N_{A,0}$ the initial acceptor concentration. $N_{D,0}$ the initial donor concentration and c the removal rate of donors.

Table IV: Overview of the alpha and beta values for different Epitaxial detectors.

Manufacturer	**Device**	α **(10^{-17} A cm^{-1})**	β **(10^{-3} cm^{-1})**	ϕ_{inv} **(p/cm^2)**	$N_{eff,0}$ **(cm^{-3})**	ρ_0 **(Ohm cm)**
N-TYPE						
MACOM Epi	C50	4	-	2.0E+15	4.6E+13	940
	C78	5.7	7.48	2.0E+15	6.8E+13	740
	C142-C-6	4.4	1.1	2.5E+15	7.2E+13	580
	C142-C-8 (Biased)	4.4	1.1	2.5E+15	7.2E+13	580
	C144-C-A3-20	6.87	1.37	~2.1E13	2.0E+13	2100
ITME Epi	I1-B-2 (0.5 μm/min)	5.33	15	1.1E+14	9.9E+12	4200
	I11-B-2	4.16	10.4	1.2E+14	5.7E+12	7250
	I21-B-2	4.24	10.9	1.4E+14	7.5E+12	5500
	I31-B-2	4.88	-	2.7E+14	1.5E+13	2800
	I2-C-20 (0.5μm/min)	9.68	> 40	~2.0E+13	1.1E+13	3800
	I12-C-20	8.39	~ 27	~2.0E+13	1.9E+13	2230
	I22-C-20	8.36	27	~2.0E+13	5.8E+12	7150
	I32-C-20		38.6		3.3E+12	12650
Wacker FZ	M18	7.2	28	2.4E+13	4.0E+12	11500
	M160	5.4	18.9	1.1E+14	6.9E+12	6000
P-TYPE						
ITME Epi	I1P-B-1 (0.5μm/min)	-	-		3.2E+14	390
	I11P-B-2	4.7	9.3		9.1E+13	1400
	I21P-B-2	4.9	9.6		7.3E+13	1700
	I31P-B-2	-	10.2		2.4E+15	3450
Wacker FZ	CP	5.8	13.2		2.4E+12	5800

Interesting as well is the behaviour of the p-type ITME epitaxial detectors. Figure 8 shows V_{fd} vs. proton fluence for 100, 150 and 200 μm thick p-type epitaxial detectors. Surprisingly, in contrast to results from the standard high resistivity FZ p-type detectors [9], we have observed an initial decrease of V_{fd}, similar to the donor removal/compensation effect observed in n-type detectors. One almost has to assume a radiation-induced "acceptor removal" to explain this effect. However, a new model base on the interaction of two deep levels predicts such behaviour in p-type silicon detectors [10]. We should note that this process is still not totally understood yet. The beta factor for these three p-type epitaxial diodes is nearly identical (see Table IV).

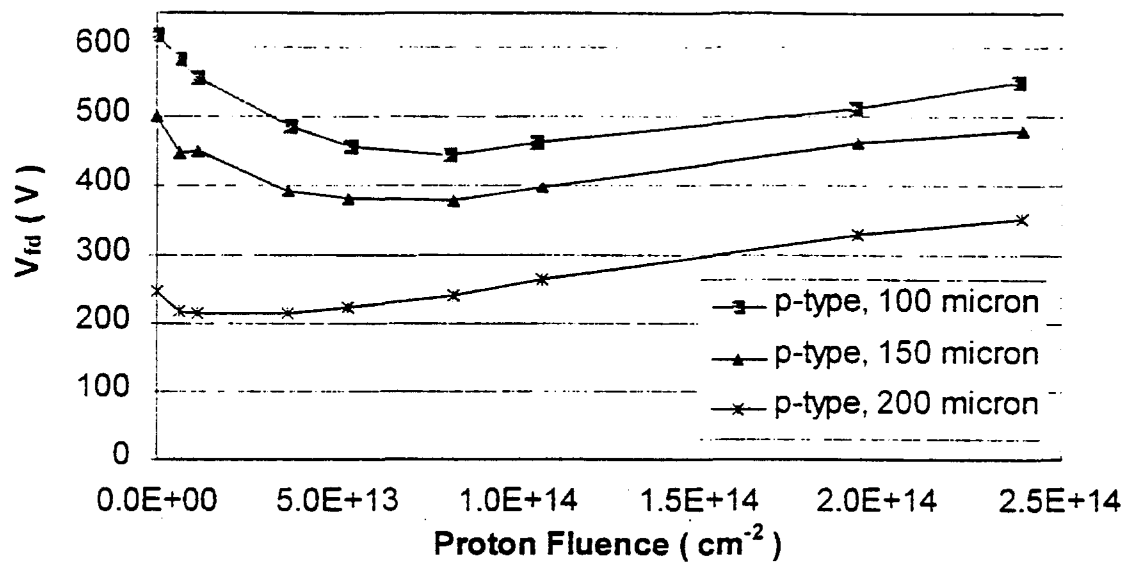

Figure 8: The full depletion as a function of proton fluence for p-type ITME Epitaxial detectors.

1.2 The effect of the initial resistivity

Comparing the behaviour of low and high resistivity MACOM epitaxial diodes, it has been observed that the low resistivity detectors are more radiation hard. In general, differences in initial doping concentration as well as differences in crystal orientation and growing conditions could cause these differences in radiation hardness. It is well known now that lower initial resistivity material inverts at a higher fluence, with inversion fluence nearly proportional inversely to the initial resistivity. The donor removal rate is much lower than previously thought if it exists at all. Higher initial donor concentration helps to provide positive space charge to compensate the radiation-induced negative space charge duo to deep acceptors.

In order to fully understand the effect of initial resistivity on the detector radiation hardness, some low resistivity CZ and FZ diodes (see Table III) have been irradiated and heated for the study of N_{eff} (effective impurity or space charge concentration, $N_{eff} = 2\varepsilon\varepsilon_0 V_{fd}/ed^2$) behaviour as a function of fluence and time [11]. Figure 9 illustrates V_{fd} as a function of neutron fluence for 630 Ω cm Epi, 2 kΩ cm Epi, and a 5 kΩ cm FZ. The inversion fluence is nearly the same for FZ and epitaxial diodes with similar initial resistivities (ρ_0). However, at higher fluences (> 4 10^{14} n/cm^2), the increasing rate of N_{eff} is somewhat lower for epitaxial detectors than that for FZ detectors with similar ρ_0,

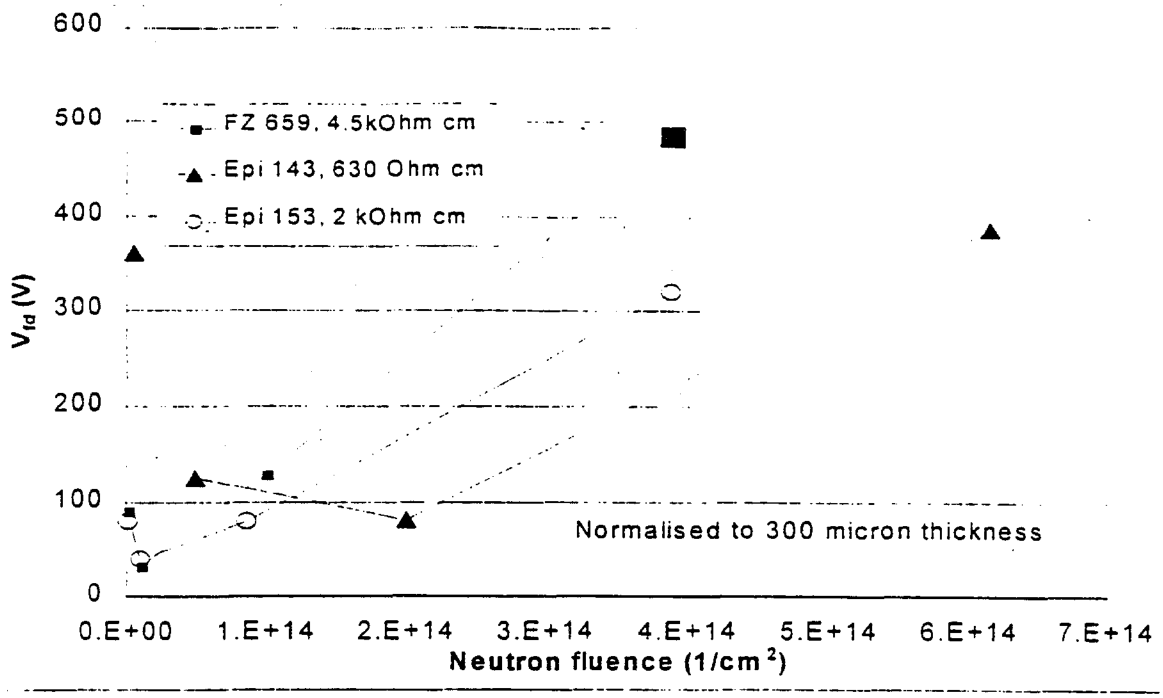

Figure 9: The effective doping concentration as a function of neutron fluence, for CZ, FZ and EPI detectors with different initial resistivities.

indicating that there may be increased radiation hardness for Epi-Si duo to its processing. For both FZ and Epi detectors, the overall N_{eff} after 10 years reverse annealing at equivalent room temperature is higher for detectors made with larger initial resistivities silicon materials [12]. This behaviour is consistent with the compensation model of deep acceptors in which the "donor removal" plays no role [13].

Acknowledgements

The authors would like to thank Prof. G. Lindström and M. Moll from Hamburg for performing neutron irradiation on some samples used in this study. Some detector data have been taken during the collaboration with the CERN ECP/MIC group. In particularly, one of the authors, Dezillie, would like to thank F. Lemeilleur for his supervision. Also the work of the CERN group in preparing the proton irradiation's at the PST7 is greatly appreciated.

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Pixel Sensors for ATLAS

Sally Seidel
Department of Physics and Astronomy
University of New Mexico
Albuquerque, New Mexico 87131, USA

for the ATLAS Collaboration

8 May 1998

Abstract

The design and fabrication of the First Prototype Pixel Sensors for ATLAS has been completed. The wafers include two large rectangular structures, called tiles, as well as numerous smaller structures. Each tile accepts 16 readout chips and is compatible with the prototype module design. Most of the smaller structures are compatible with single readout chips. The designs of all of these prototype devices are explained with attention to the goals and constraints that guided design choices.

1 Overview of the ATLAS Pixel Sensor Program

The ATLAS Experiment at the CERN LHC will include a silicon pixel detector as its innermost tracking chamber. The detector will consist of three layers of rectangular sensors arranged in a cylindrical ("barrel") pattern coaxial with the beamline, and 2×5 layers of identical sensors assembled into disks. The detector will require 1508 barrel sensors and 720 disk sensors.

The pixel detector must survive for 10 years in the hostile radiation environment of the collider. The sensors closest to the beam will receive more than 10^{15} minimum ionizing particles/cm^2. The anticipated need to operate the sensors partially depleted after some point in their radiation lifetime is the dominant factor in the choice of n-type implants in n-type substrate. As radiation damage to the bulk will require increasingly higher operating voltages during the detector's lifetime, the requirement of operating these sensors at high voltage without electrical breakdown or microdischarge is important to the design. Some features of the design also reflect the desire to provide bias to every pixel without attaching the readout integrated circuit. This is expected to facilitate testing of the sensors prior to bonding and to guarantee a uniform electric field in the sensor active area in cases of failure of a bump bond. To minimize multiple scattering of tracks in this, the innermost of ATLAS's detection systems, the inner layer will be fabricated from sensors of 200μm thickness while the outer two layers and the disks will use 250μm sensors.

The production sensors for the ATLAS barrels will be 2 readout chips wide and 8 readout chips long. The readout chips will have 24 columns and 160 rows; each pixel cell will have dimensions $50 \times 300\mu\text{m}^2$. Consequently, the active area for a barrel sensor will be 16.4×60.4 mm^2. The overall dimensions of the barrel sensor depend upon the module concept (still in development) but will lie in the range 16.4×62.4 mm^2 to 21.4×67.8 mm^2. Disk sensors will use the same technology as barrel sensors but will have a slightly different shape.[1]

The ATLAS pixel sensor design program includes fabrication of First Prototypes and Second Prototypes prior to production sensors. First Prototypes were designed in 1997, fabricated by CiS Institut für Mikrosensorik e.V. and Seiko Instruments Inc., and are now under study within ATLAS. The Second Prototypes are expected to be designed and ordered prior to January 1, 1999. Pre-production sensors will be designed and ordered in 1999 so that production sensors can be ready for assembly in 2000.

This document primarily concerns the First Prototypes. The First Prototype wafers contain 2 large structures, called Tile 1[1] and Tile 2[1, 2], 17 smaller sensors which examine additional design options and which can each be read out by a single amplifer chip, and a variety of process test structures. Design details of the two tiles and important features of some of the other structures are described below.

2 The Design of the First Prototype Sensors

2.1 Introduction

Figure 1 shows the layout of the (4-inch diameter, 280μm thick) First Prototype wafer. Figure 2 (including its Details A, B, C, D, E, and F) illustrates the n-side of Tile 1 after processing. Figure 3 shows a bond pad region. Figure 4 (including its Details A, B, and C) illustrates features of Tile 2. Figure 5 shows the Tile 2 i/o bus structure. Figure 6 shows the guard rings. Figure 7 illustrates the second metal pattern. Figure 8 shows the structure known as the bias grid.

2.2 Cell Geometry

On the accompanying figures, rows are labelled in the horizontal direction, columns in the vertical. The active area of each tile is divided into 16 units, a unit being defined as a group of pixels that use a common amplifier chip. The geometry of each pixel cell in the First Prototypes is characterized as follows:

- Number of pixel cells per readout chip: 164×18
- Total number of pixel cells: 47232 ($= 16 \times 164 \times 18$)
- Pixel cell dimensions: $50 \times 400 \mu m^2$. (This is larger than the production sensors' pitch in order to match the prototype electronics.)
- Cells that lie in columns which would not be adjacent to a chip's bump pads if they were 400μm long are elongated to 600μm. (See Figure 2, Detail B, and Figure 4, Detail B.)

2.3 n-side Isolation and Implant Dimensions

The principal difference between the two tiles is their technology for n-side isolation. Tile 2 uses p-spray[3], and Tile 1 uses p-stops. On the First Prototype wafers, regions that use the different isolation techniques are separated by a low precision mask.

In Tile 1, the n-type implants are isolated from one another by p-stops of the individual, or "atoll," design. This choice provides a low inter-pixel capacitance. Pairs of units are additionally surrounded by a common p-stop frame. The dimensions of Tile 1 implants are as follows:

- n^+ implant width: 23μm
- p^+ implant width: 5μm
- gap between n-type and p-type implants: 6μm
- gap between neighboring p^+ implants: 5μm.

Complete dimensions of the structures on Tile 2 are shown in Figure 4, Details A and B. For each pixel cell, the mask width of the central n-implant is 13μm, while the floating n-implant that surrounds it is 6μm wide. The spacing between those structures is 6μm. The floating implant serves to keep the distance between implants (and consequently the inter-implant electric field) small without compromising the relatively large distance, and hence low capacitance, between neighboring channels. In both tiles, corners are rounded to reduce electric fields. (See for example Figure 2, Detail D.)

2.4 n-side Guard Ring

The design of both tiles' n-side edge region (see Figure 6) is guided by the concern to minimize the possibility of electrical arcs between the sensor and the electronics which are only a bump's diameter away. There is an inner guard ring which consists in a metallized n^+ implant. On Tile 1 the implant has width 86.5μm; on Tile 2 the width is 90μm. On Tile 2 this inner ring can be used for biassing the whole array (see Section 2.12). Beyond the inner ring is an outer region covered with n^+ implant. The inner ring and outer region are separated by a gap. On Tile 1, that gap has total width $30\mu m$ and is unimplanted. To provide electrical isolation, a $10\mu m$ wide p-stop is placed in the center of the gap. On Tile 2, the gap is $8\mu m$ wide, and electrical isolation is provided by the p-spray implant which covers the whole device.

Contact pads to the n-type implant appear in the four corners of the tile. On each tile, one of these contact pads bears a label so that the orientation of the tile is uniquely specified. The outer n-implant is grounded externally.

2.5 p-side Guard Ring

Both tiles use the same design[4] for their p-side guard ring. The multi-guardring structure contains 22 rings with a pitch that varies from $20\mu m$ near the sensitive area to $50\mu m$ near the edge. The p-implant is $10\mu m$ wide in every ring while the gap increases from the center to the edge. The metal overlaps the implant by half of the gap width on the side of the ring facing the sensitive area. The entire guard ring structure is $525\mu m$ wide.

2.6 Double Metal

A second metal layer is being tested on 30% of the First Prototypes. Devices with and without double metal do not differ in any aspect of their design other than the double metal itself, the insulator, and the addition of vias to allow access through the insulator to first metal pads. In the First Prototype program, double-metal is being tested in some (redundant) busses on Tile 2 and as routing of signals from pixels at the edge of units to preamplifiers above neighboring implants. The busses run parallel to the long side of the sensor and are located between bump bond pads and the active area. Figure 5 shows a detail of the bus structure on Tile 2.

The narrowest line in Metal 2 is $10\mu m$ wide and 1.5–2.0 μm thick. The minimum Metal 2 spacing, which is not critical, is greater than $20\mu m$. In the bus structure, Metal 2 has width 20–50 μm. The contact holes are $3 \times 10\mu m^2$ in the masks. Metal on the first layer has thickness 1.2–1.5 μm. The insulator material varies with manufacturer: one vendor uses SiO_2; the other, polyimide. To maintain flatness of the bump pads, vias are not located beneath them. Figure 7 shows the second metal design.

Devices that have Metal 1 but not Metal 2 are completely functional. In the devices with both metal layers, the outermost four rows of pixels are not connected by bumps directly to their preamplifiers (i.e., their bump pads have no vias). Signals from pixels in those rows are instead routed in Metal 2 to neighboring pixels by using the same metal pattern as appears in Metal 1 in the sensor's central region.

2.7 As-cut Dimensions

The wafers containing the tiles are provided by their manufacturer without dicing in order that they may be bumped first. To accommodate the busses, Tile 2 is wider than Tile 1. After dicing, the dimensions of the tiles are:

Tile 1 (default): 18.6×62.6 mm^2, and

Tile 2 (default): 24.4×62.6 mm^2.

It may be necessary to increase the distance between the guard ring and scribeline in order to guarantee sufficient radiation hardness. To provide for this possibility, a second scribeline is included which would give the tiles the following dimensions:

Tile 1 (enlarged): 19.4×63.4 mm^2, and

Tile 2 (enlarged): 24.4×63.4 mm^2.

2.8 Metallization

On Tile 1, the first metal has width 14μm on the pixels. The metal width on the inner guard ring is 6μm narrower than the implant. The masks for the metallization over the implant of Tile 2 show a width of 12μm, 1μm less than the mask width of the implant.

2.9 Pads

The bond pads are twenty-sided polygons (approximating circles). On Tile 1 the implant has mask diameter 21μm, or processed diameter approximately 23μm. On Tile 2 the implant has mask diameter 18μm. On both tiles the first and second metals have diameter 20μm.

Bond pads are placed at the end of each pixel cell. This layout anticipates a mirrored electronics layout. The closely spaced bond pads are 50μm apart. (See Figure 2, Details A and B). A cross section of a bond pad region is included in Figure 3.

Some pixels have no bond pads. Those cells will have no preamplifier directly above them and so must have their signals routed to bond pads on pixels a few rows away in the same column. For both tiles, the routing will use a single metal layer. Figure 2 Details C and E show the routing for Tile 1 while Figure 4 Details B and C show it for Tile 2.

Bias pads are placed in several locations on the inner n^+ guard ring. They form two extra rows with the same 50μm pitch as the pixels have. See Figure 2, Detail F for an example of n-side bias pad placement. Probing pads are placed on the inner guard ring in the region between adjacent units (see Figure 2, Detail F).

2.10 p-side (Back Side) Design

This information concerns both tiles. A p^+ implant is continuous in the area covered by pixels. The aluminization has $30 \times 100\mu\mathrm{m}^2$ apertures to facilitate stimulating the cells from the p-side with a laser.

2.11 Passivation

The passivation must be compatible with technologies for applying bumps for bonding. A 1μm thick silicon nitride layer is used. The openings in the passivation for bump bonding have 12μm diameter.

2.12 Bias Grid

To maximize the yield on assembled modules, it is beneficial to test sensors under bias prior to attaching the amplifier chips. A bias grid is integrated into Tile 2 (see Figure 8) to allow every channel to be biased on a test stand without a chip and without contacting the implants directly. A bus between every pair of columns connects to a small n^+ implant "dot" near each pixel. When bias is applied (through a probe needle) to the grid via the inner guard ring of the n-side, every pixel is biased by punchthrough from its dot. (The use of p-spray facilitates this technology since the elimination of need for photolithographic registration permits the distance between n-implants to be small and hence keeps the punchthrough voltage low.) Once a chip has been attached, the grid is no longer used for biassing the cells. It nonetheless maintains any unconnected pixels (i.e., bad bumps) near ground potential. The punchthrough dot sacrifices 0.8% of the pixel's active area.

2.13 Tolerances

The following tolerances are required:

- Uniformity of thickness: $\pm 10\mu$m
- Mask alignment: $\pm 2\mu$m

2.14 Sensor Electrical Properties

The following is a summary of the required electrical properties:

- Initial depletion voltage: 50–150V
- Initial maximum operating voltage: ≥ 200V
- Initial leakage current at $V_{\text{depletion}} + 10$V: < 100 nA/cm^2
- Initial oxide breakdown voltage: ≥ 100V.

2.15 Processing

The following processing requirements are made:

1. n^+ implant dose: $> 10^{14}/\text{cm}^2$.
2. concerning n-side isolation:
   - for Tile 1, the p^+ implant dose is $\geq 10^{13}/\text{cm}^2$.
   - for Tile 2, the p-spray effective dose in silicon is $(3.0 \pm 0.5) \times 10^{12}/\text{cm}^2$.
3. Back (p-side) contact dose: $> 10^{14}/\text{cm}^2$.
4. Implant depth after processing is $\geq 1\mu$m.

2.16 Radiation Hardness

The following specifications will be required of Second Prototype and production sensors. They are not required of First Prototype sensors. The properties of irradiated First Prototype sensors are nonetheless being studied.

The production sensors must have the following performance after an irradiation of 10^{15} p/cm^2:

1. Breakdown voltage: > 500 V.
2. Depletion voltage (for 300μm sensors): < 800 V.
3. Leakage current (measured at $-5°$ C) after one month of annealing at 20° C (for 300μm sensors): < 125μA/cm^2 or < 25 nA per pixel cell.

3 Design Variations Studied on Single-chip Sensors

On each wafer, three of the seventeen single-chip sensors have all of the design features of Tile 1. Three others have the features of Tile 2. Among the remainder, two evaluate a common p-stop design, one combines the common p-stop with p-spray, one studies a variety of p-stop geometries, and one evaluates three different bricking patterns. In the region of the wafer that uses p-spray, there are an additional 3 devices which explore techniques for minimizing cross talk, implementing bricking, and modifying implant geometries and gap sizes.

"Bricking" is the offsetting of pixel cells in neighboring rows by half a pixel length. Bricking improves the z resolution for double hits and reduces the cross talk coupling by distributing the capacitance over four neighboring cells rather than two. The challenge to the implementation of bricking comes from the fact that bricked sensor cells are not directly adjacent to the bump pads of the mirrored bump pad geometry of the (nonbricked) readout chip. Several solutions to this problem are being examined on the single-chip sensors. In one option, the bump pad is placed above a neighboring channel's implant and then routed in single metal to the implant which requires connection. This option produces cross talk between the two implants involved. In a second option, the routing between implants is accomplished in second metal. In the third option, called "partial bricking," routing is avoided entirely by staggering the implants only at their ends which have no bump pads. This option complicates pattern recognition slightly. The three bricking options are illustrated in Figures 9, 10, and 11.

4 Testing

Acceptance testing is being done by ATLAS only. The wafer has test structures for monitoring flat band voltage, layer thickness, implant resistivity, aluminum sheet resistance, etching uniformity, and alignment.

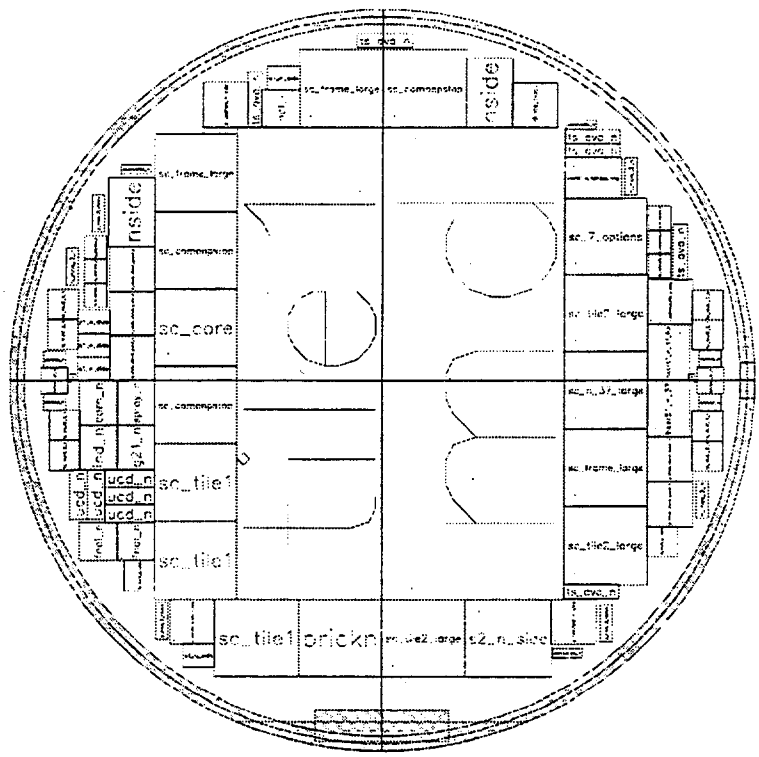

Figure 1: The layout of the 4-inch First Prototype wafer.

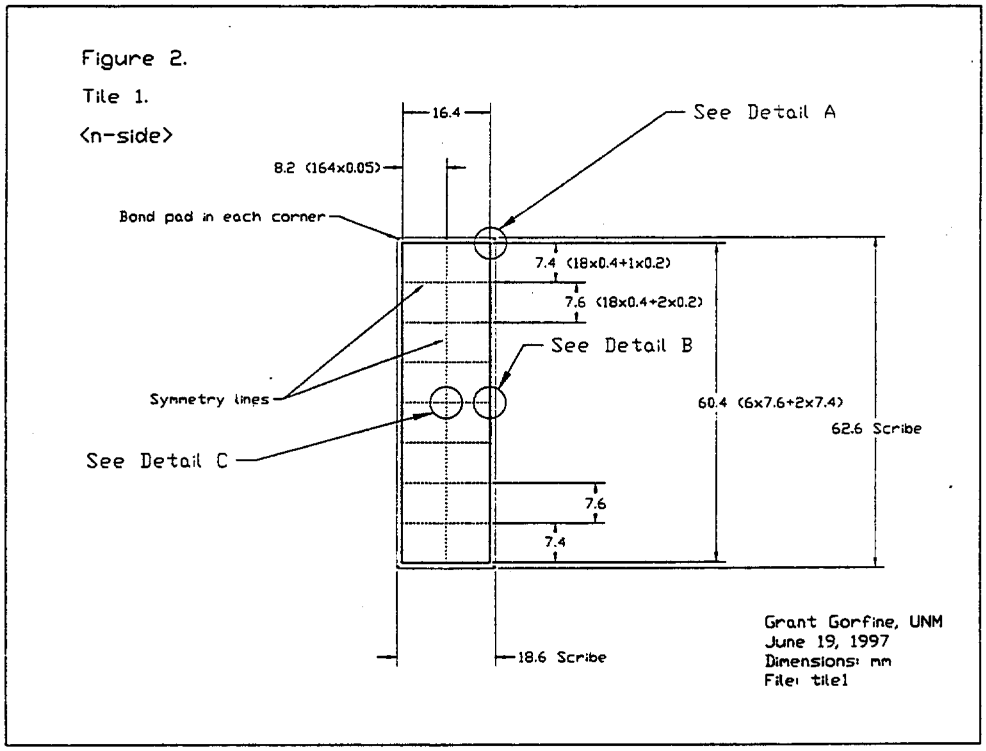

Figure 2: The Tile 1 concept.

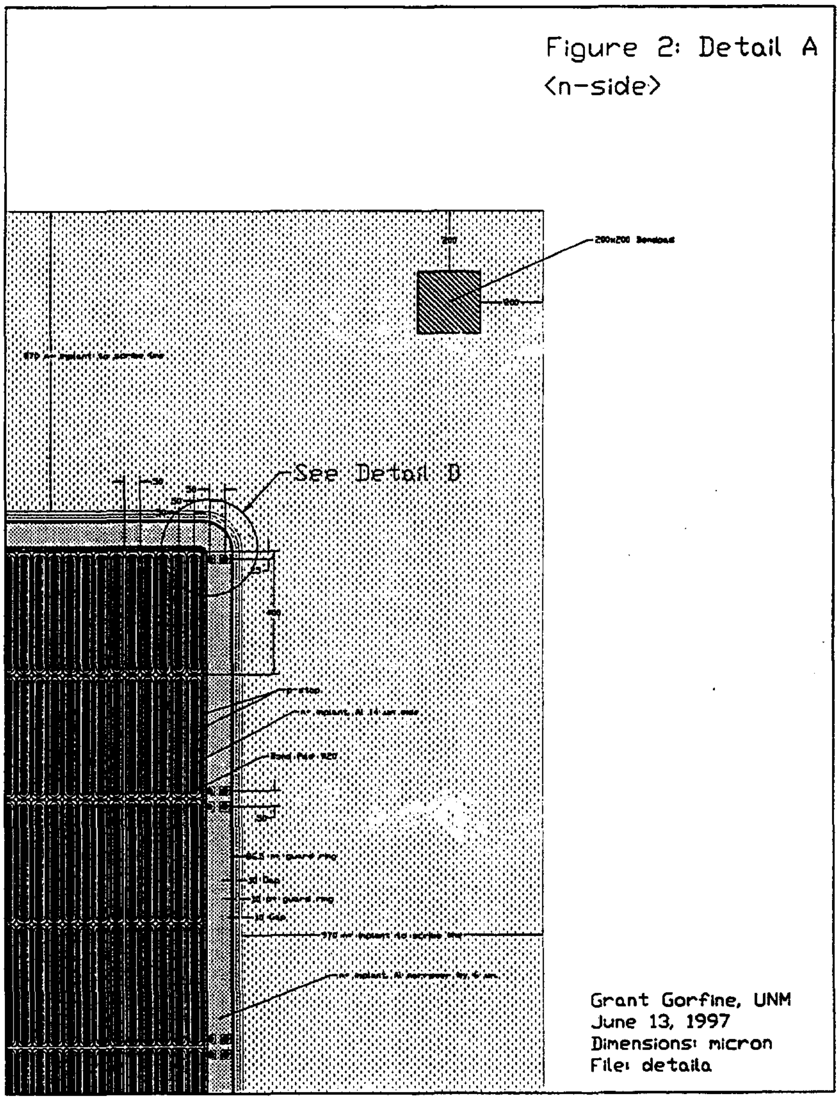

Figure 2a: Corner detail of Tile 1.

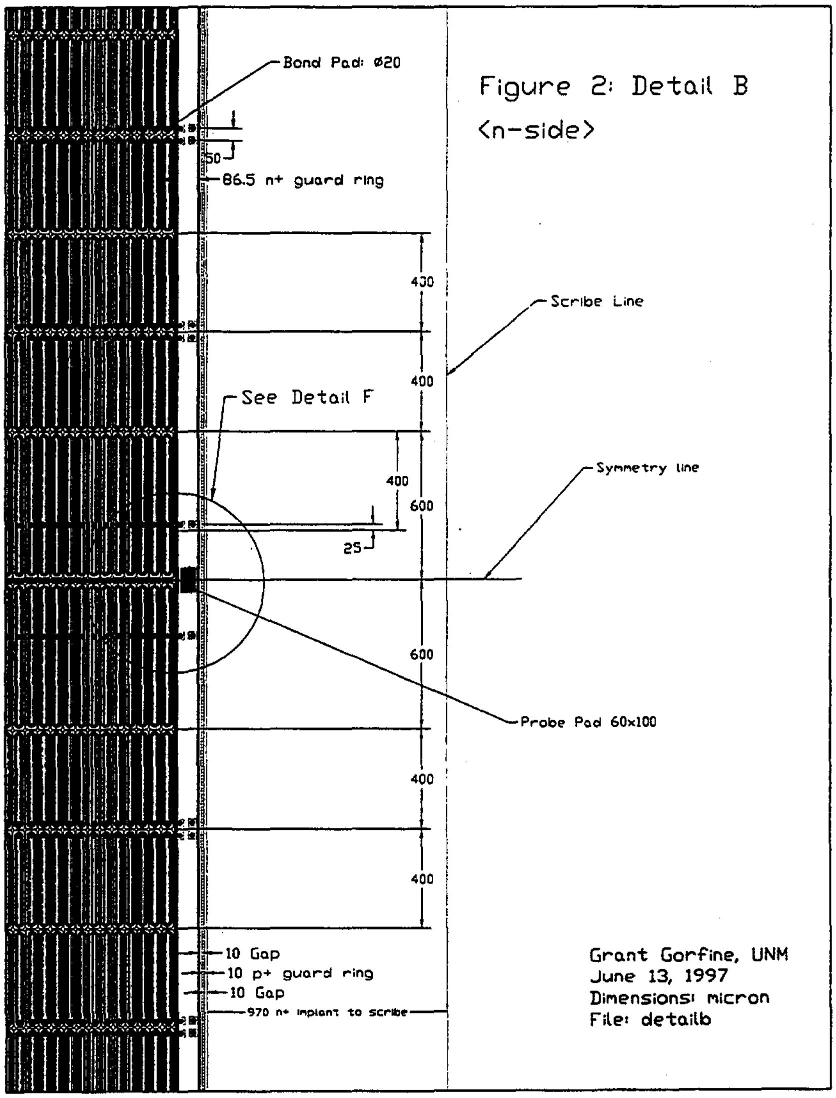

Figure 2b: Detail of Tile 1 showing a region between units in which cells of length 600 μm are used.

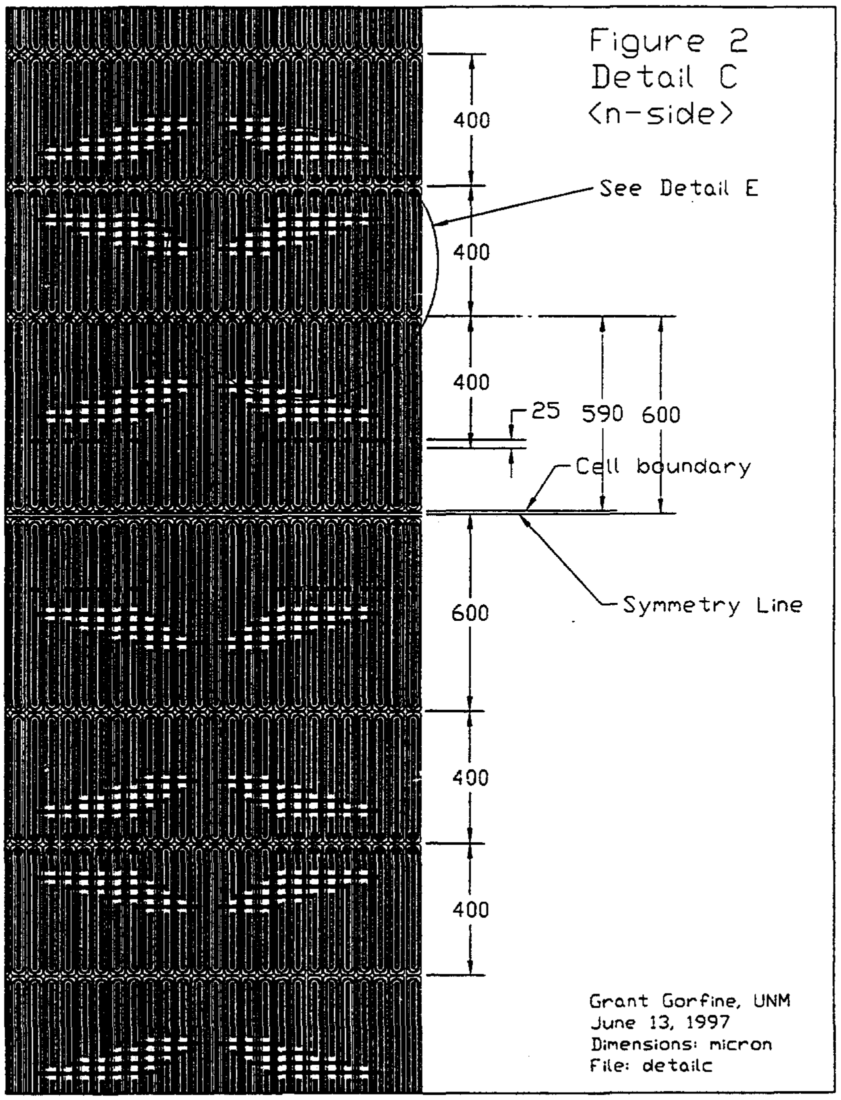

Figure 2c: Detail of Tile 1 showing first metal traces which route signals from implants at the edges of their units to the preamplifers above neighboring implants.

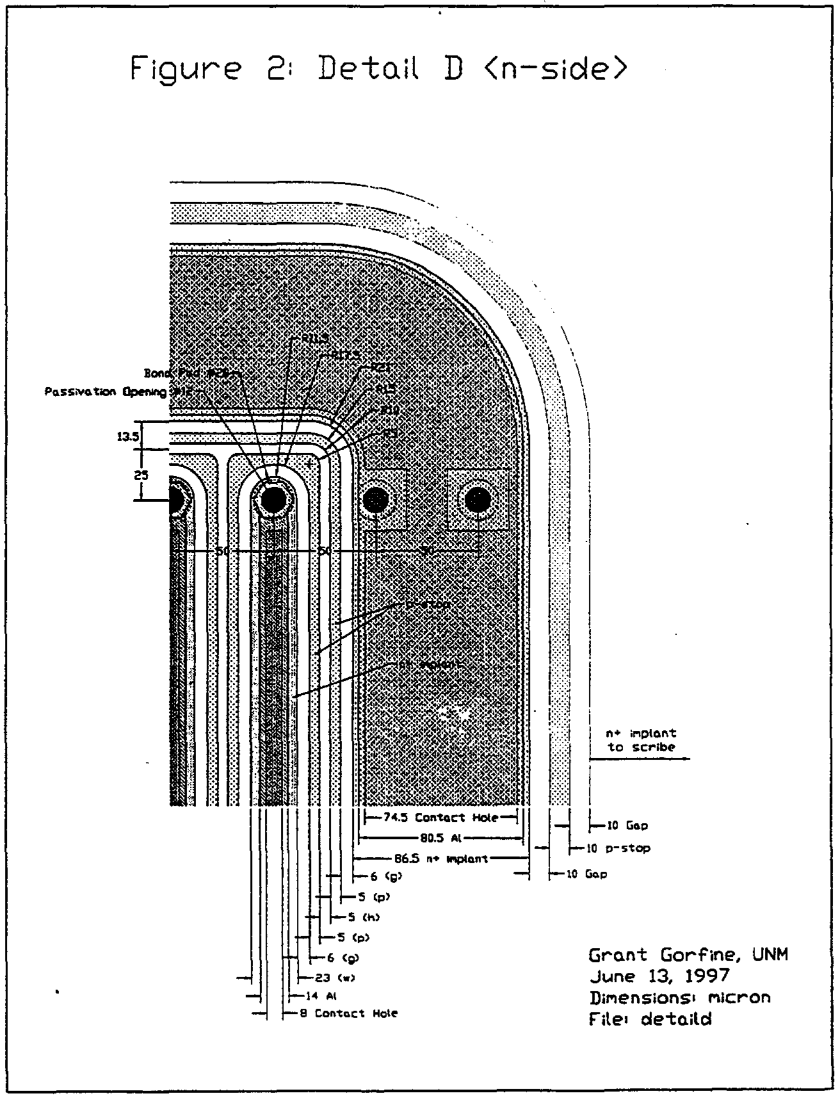

Figure 2d: Detail of Tile 1 showing the corner of the n-side guard ring and the isolation implants.

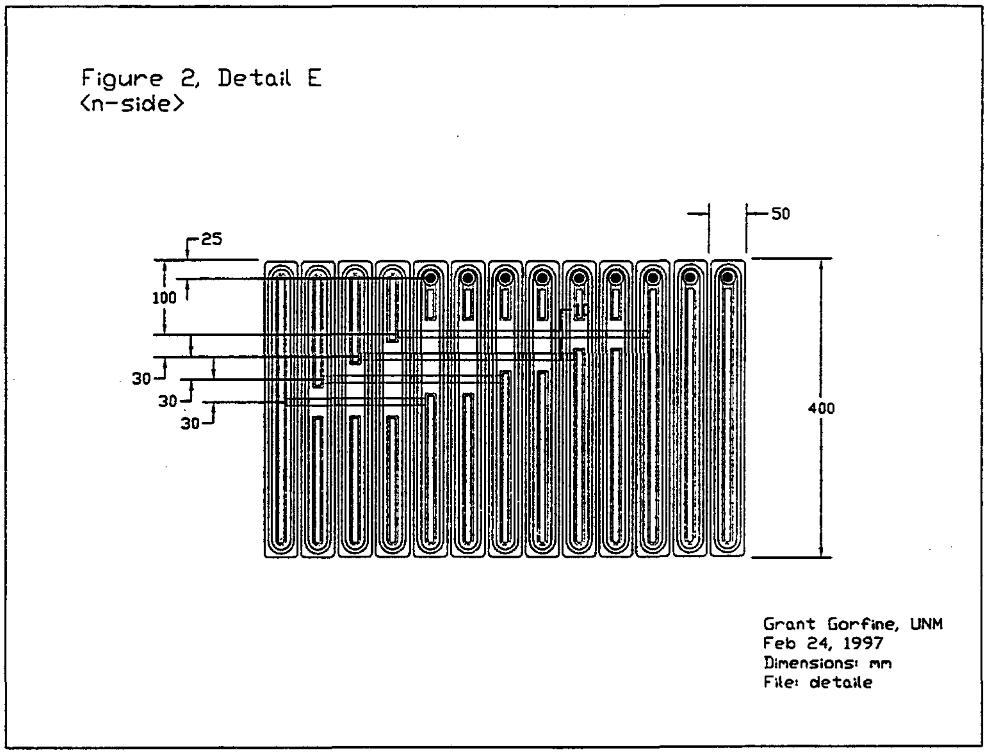

Figure 2e: Detail of Tile 1 showing the first metal near the edge of a unit.

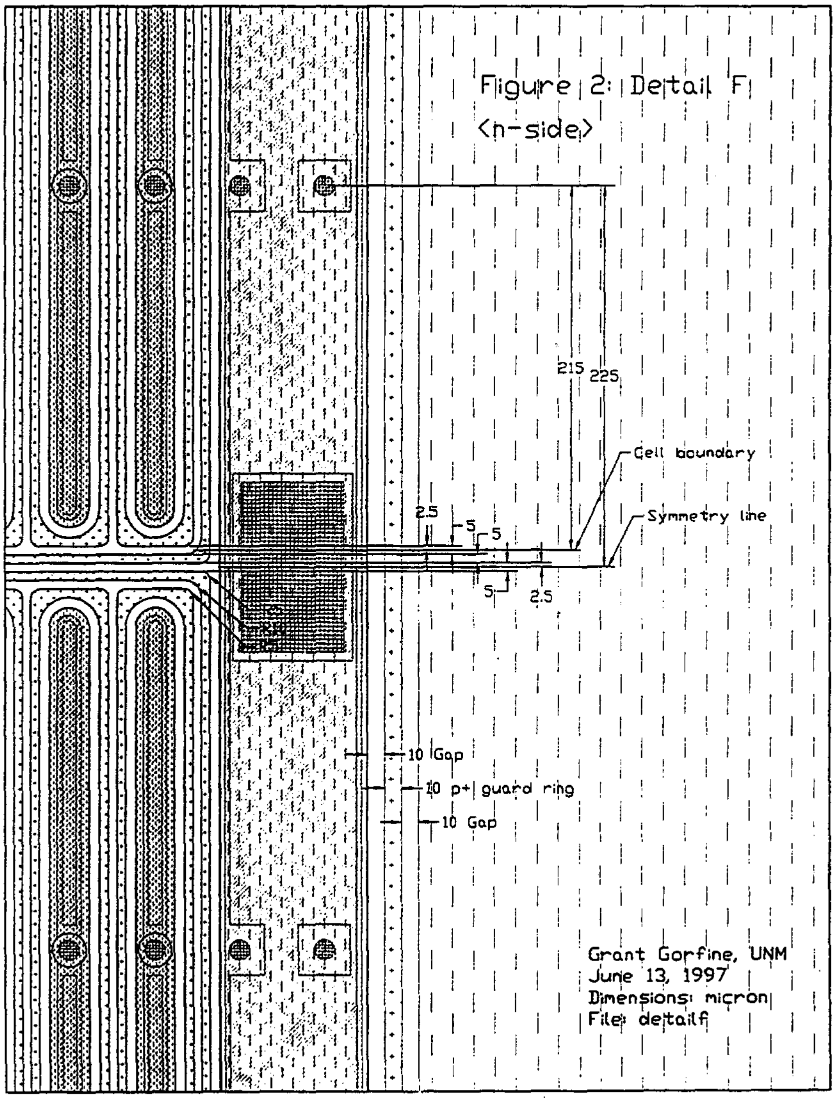

Figure 2f: Detail of Tile 1 showing the structure of isolation implants at the boundary between units.

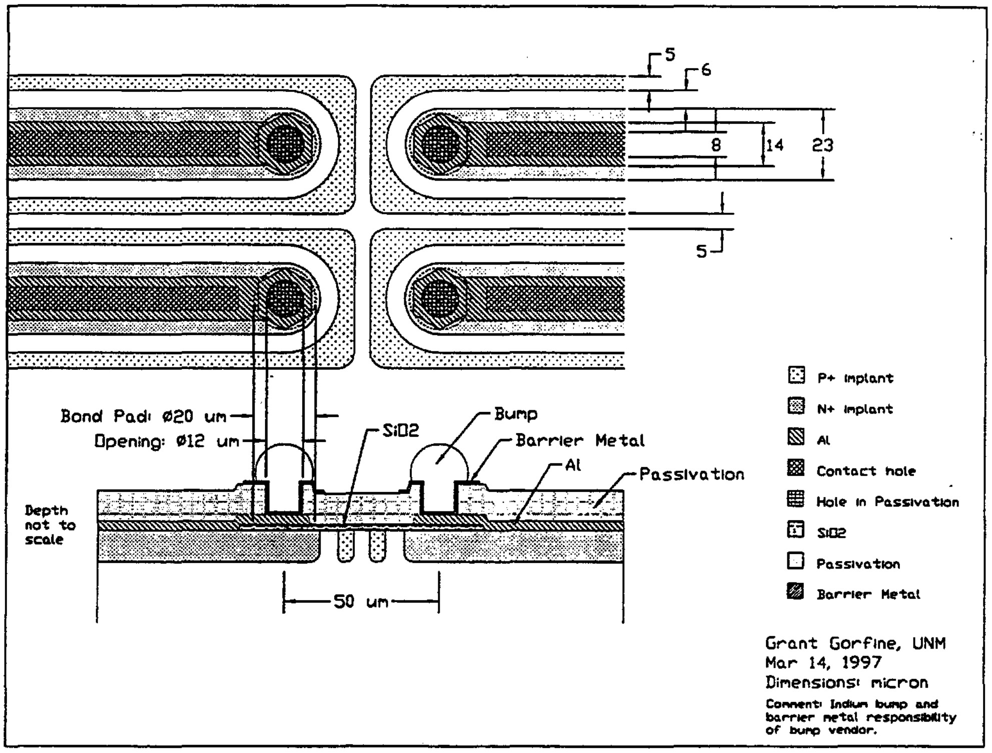

Figure 3: Concept of a Tile 1 bond pad region.

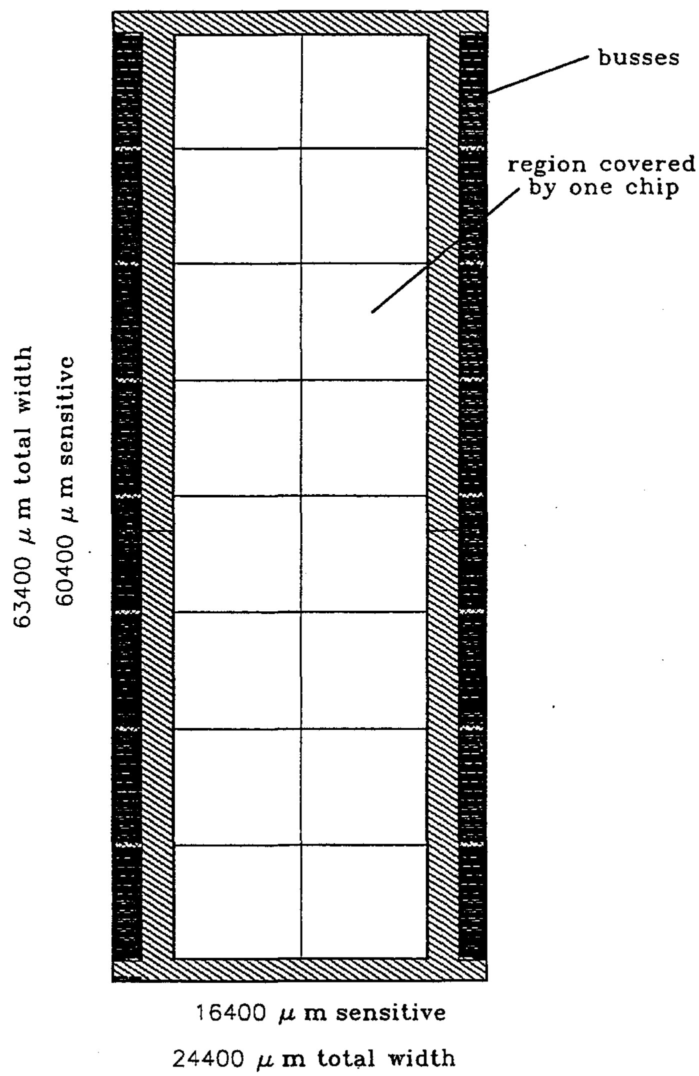

Figure 4: The Tile 2 concept.

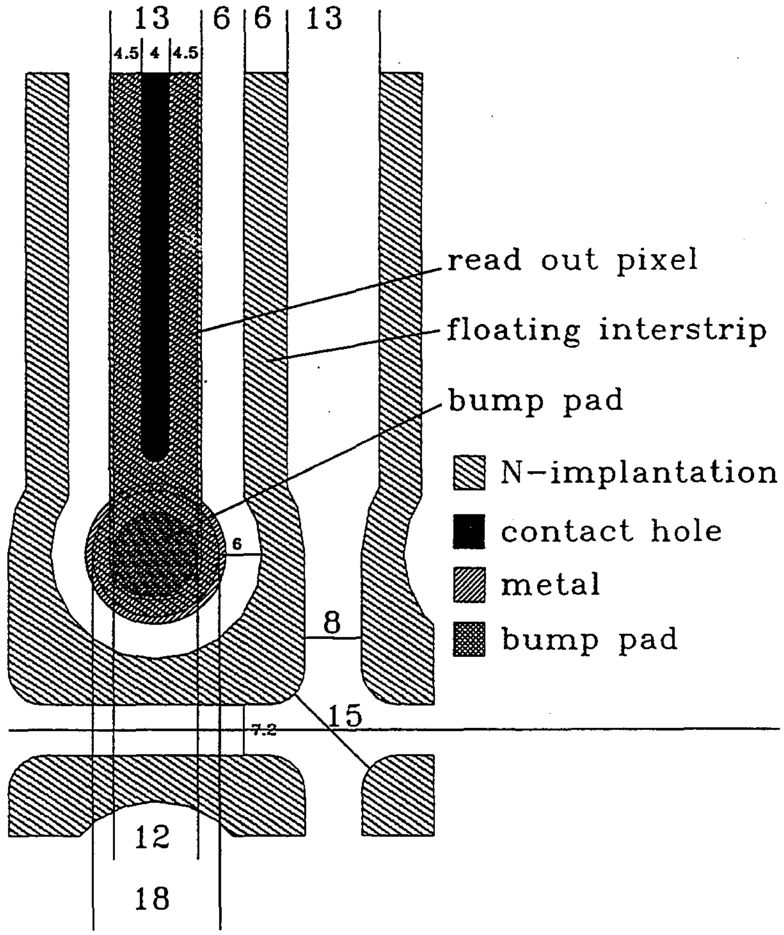

Figure 4a: Portion of a pixel cell in Tile 2.

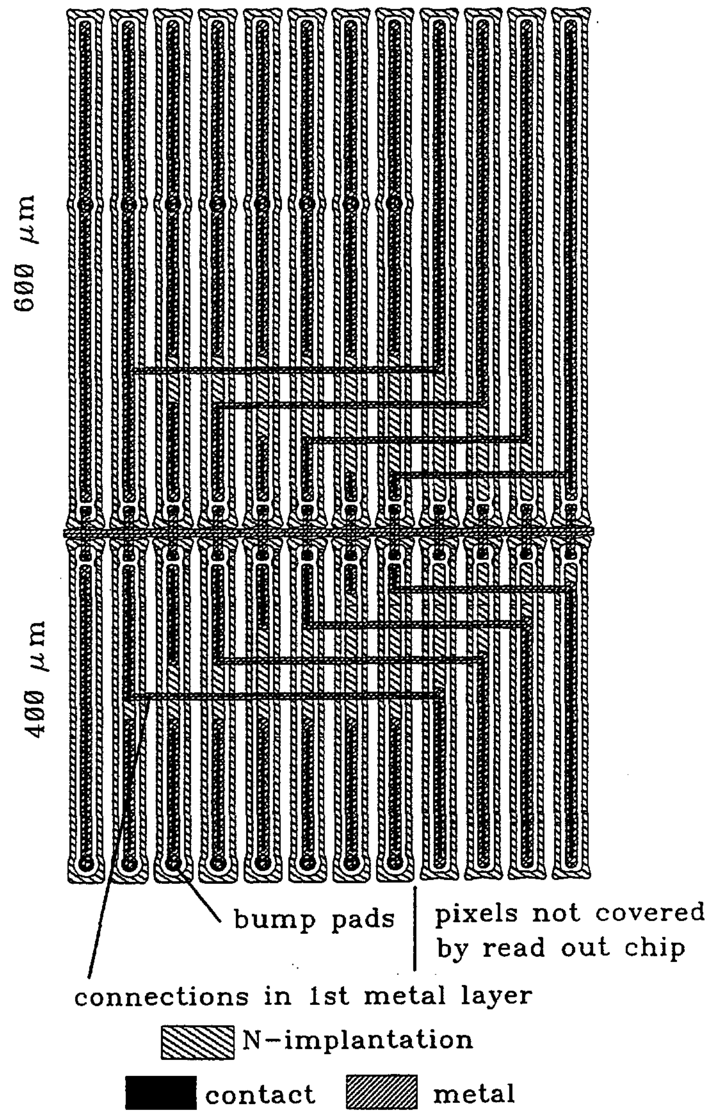

Figure 4b: Detail of Tile 2 showing first metal traces which route signals from implants at the edges of their units to the preamplifers above neighboring implants.

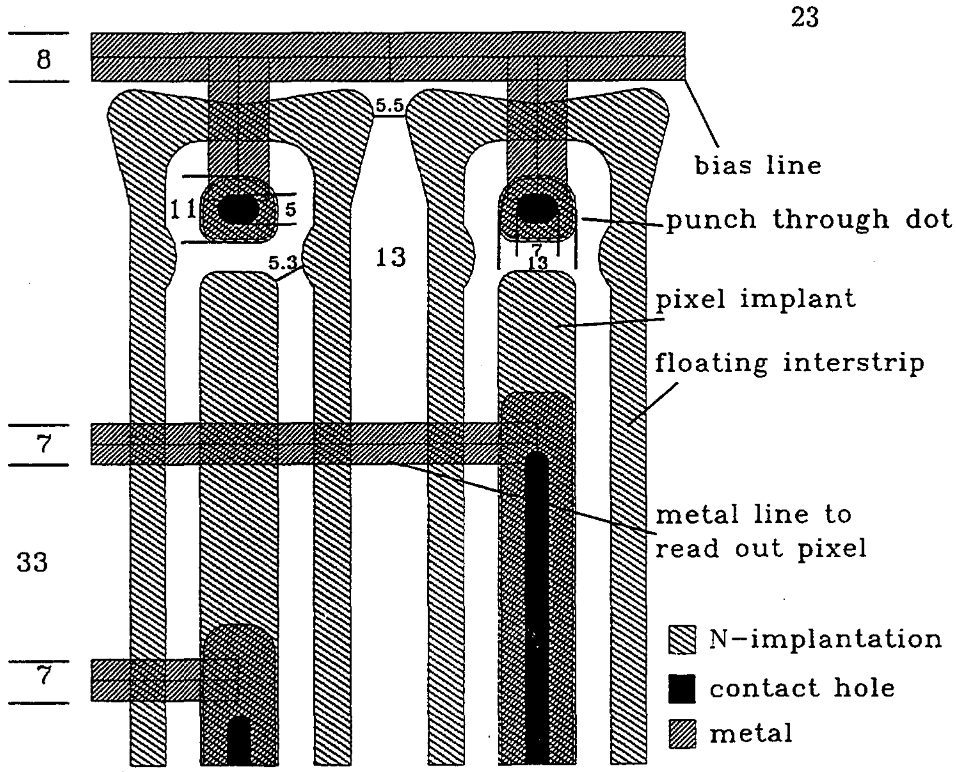

Figure 4c: Section of the Tile 2 multiplexing scheme.

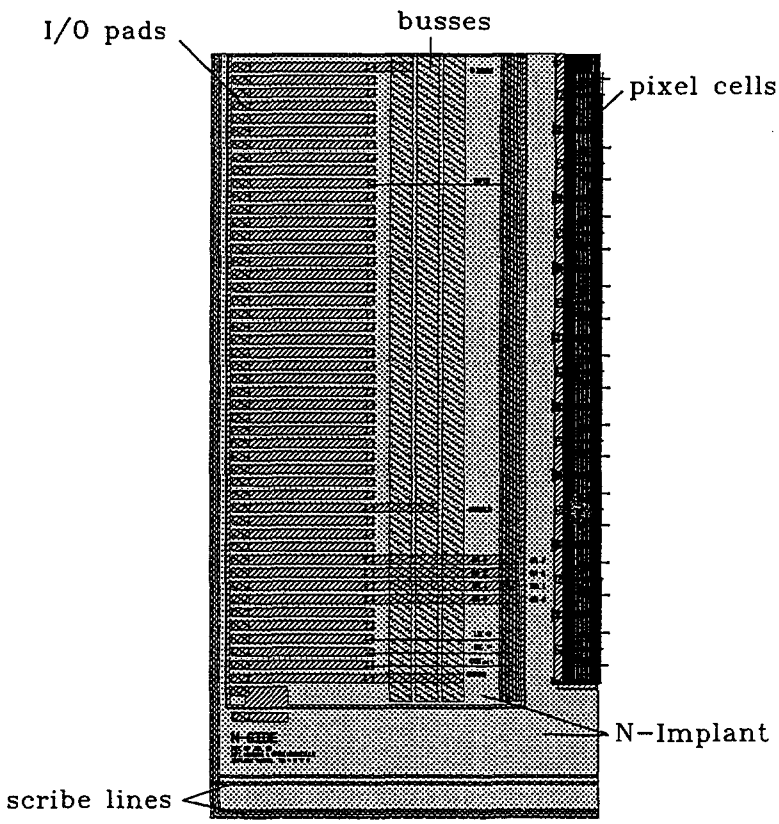

Figure 5: I/O busses on Tile 2.

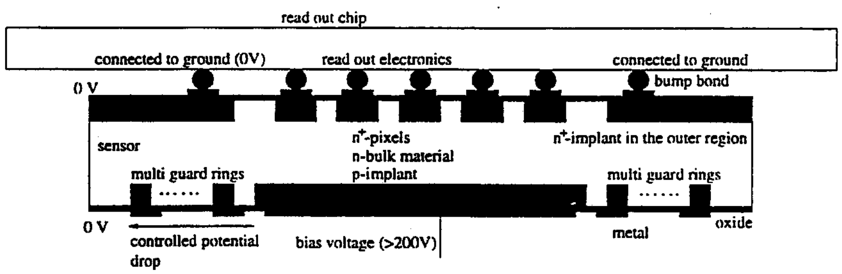

Figure 6: A cross section of a tile showing the guard rings.

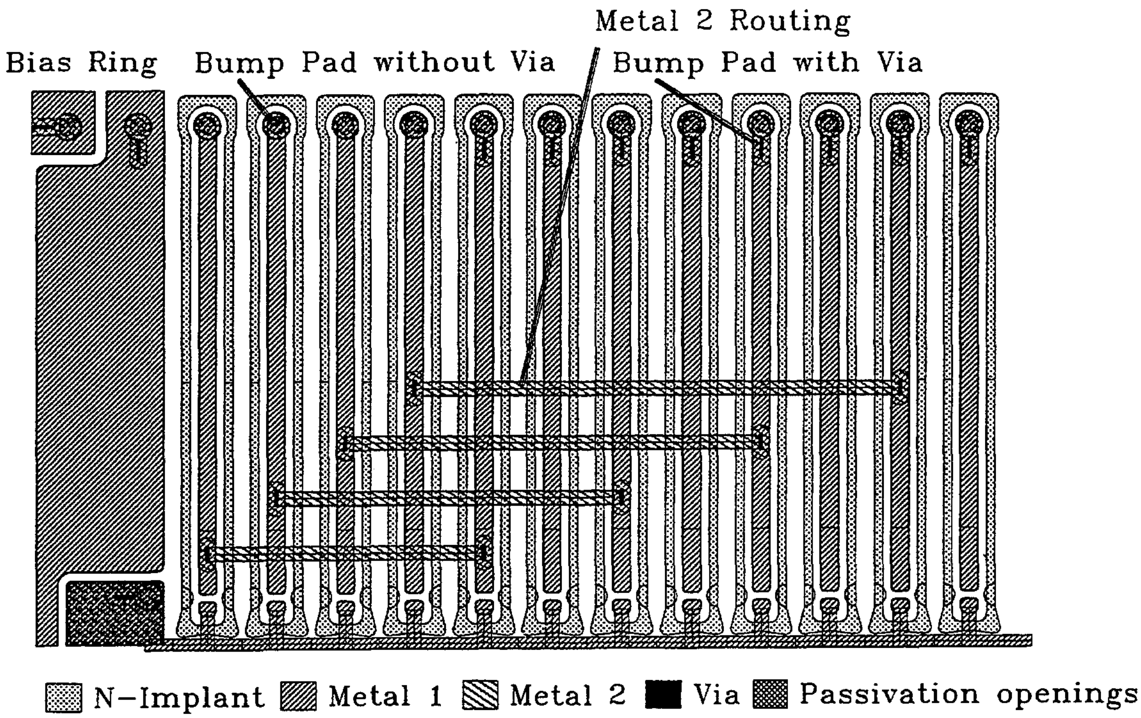

Figure 7: The Metal 2 routing.

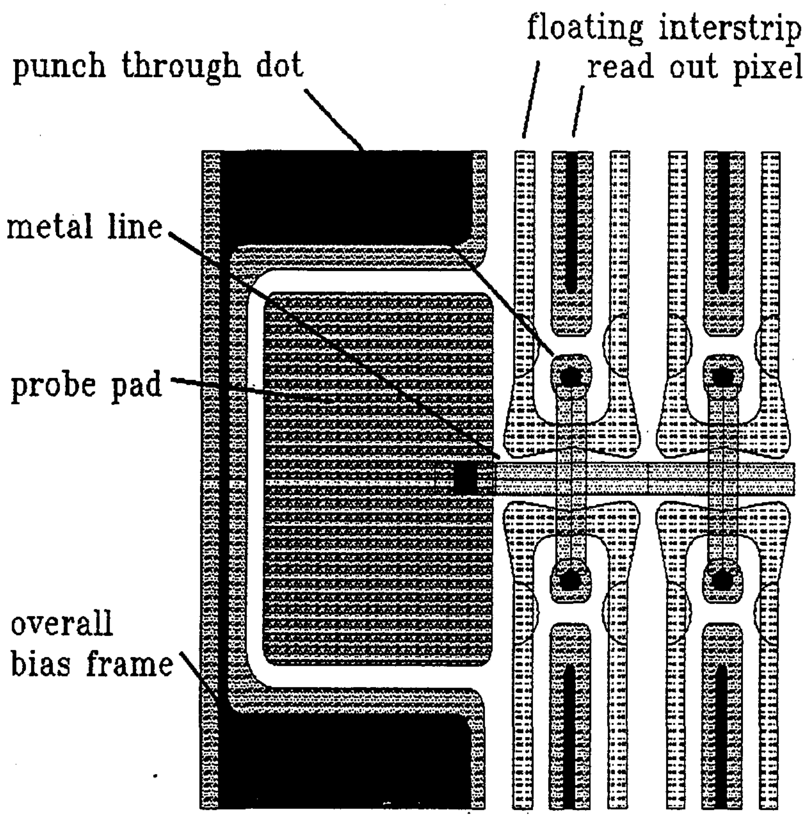

Figure 8: A section of the bias grid.

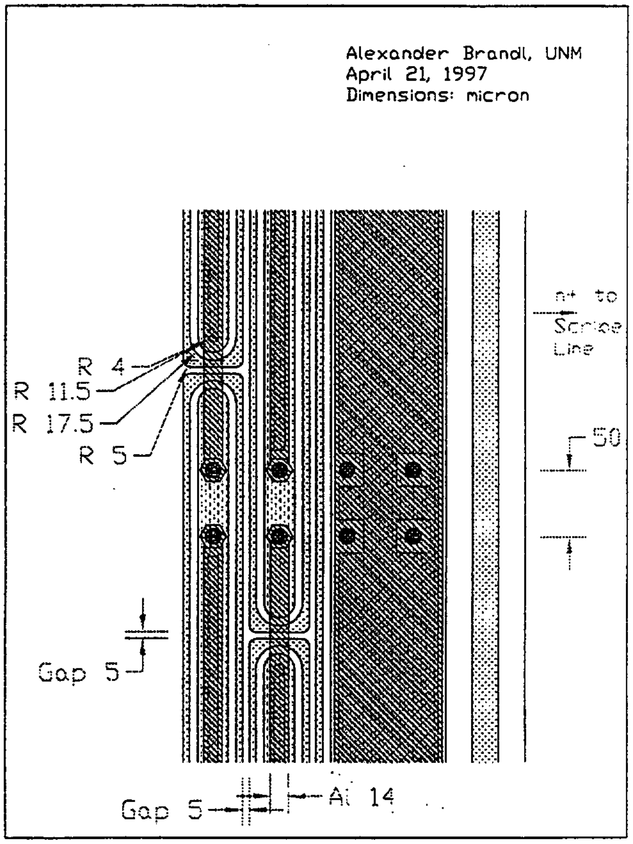

Figure 9: Bricking with single-metal routing.

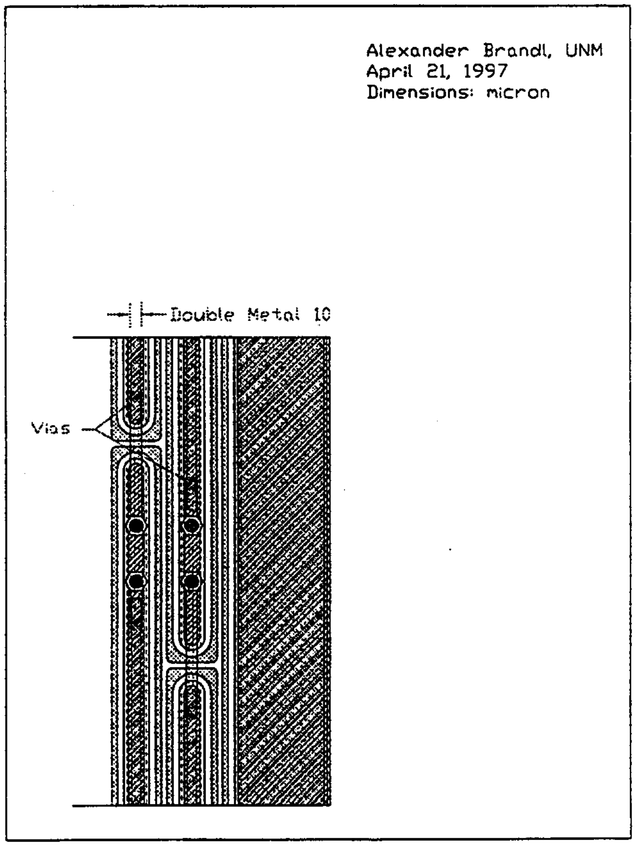

Figure 10: Bricking with double-metal routing.

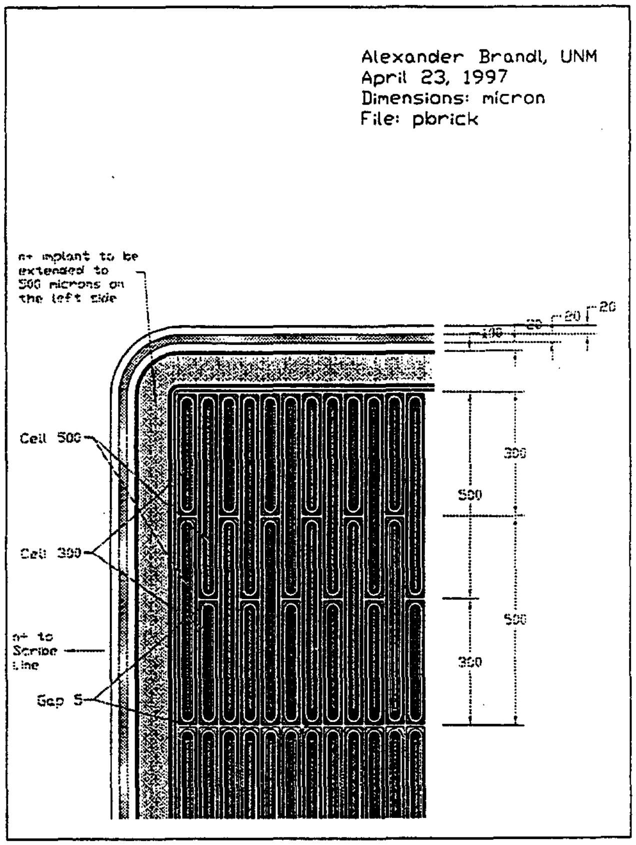

Figure 11: Partial bricking.

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PIXEL98 Workshop

Sensors for CMS Pixel Detector

Chih-Yung Chien

Johns Hopkins University

FNAL, May 6-9, 1998

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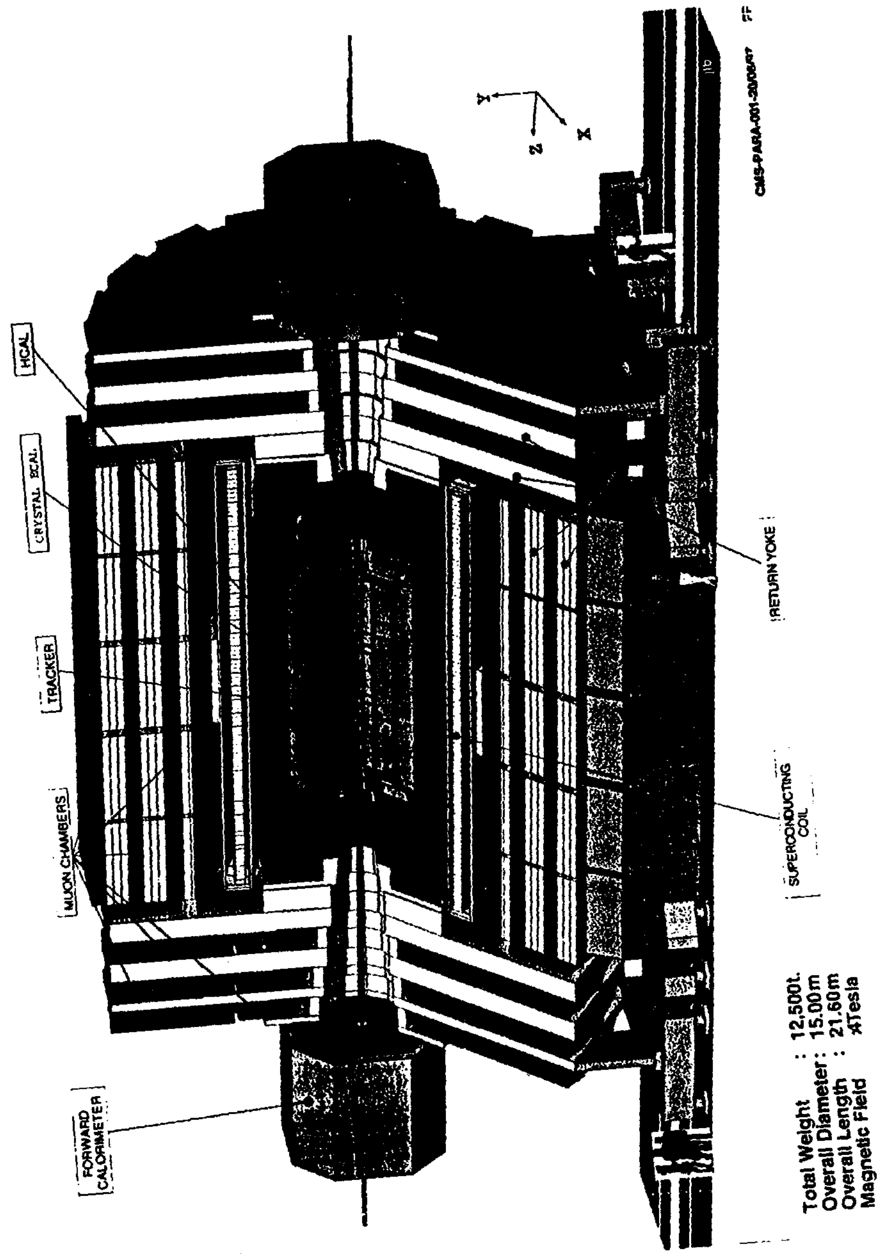

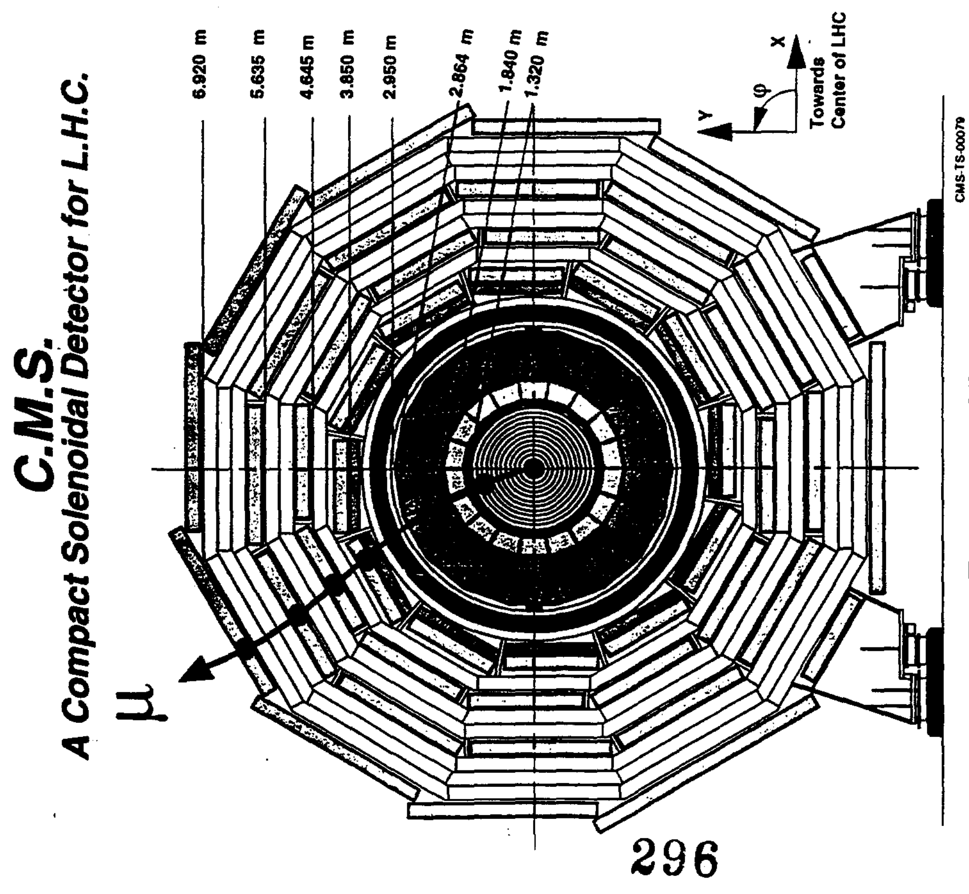
C.M.S.
A Compact Solenoidal Detector for L.H.C.
μ
6.920 m
5.635 m
4.645 m
3.850 m
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1.840 m
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Y
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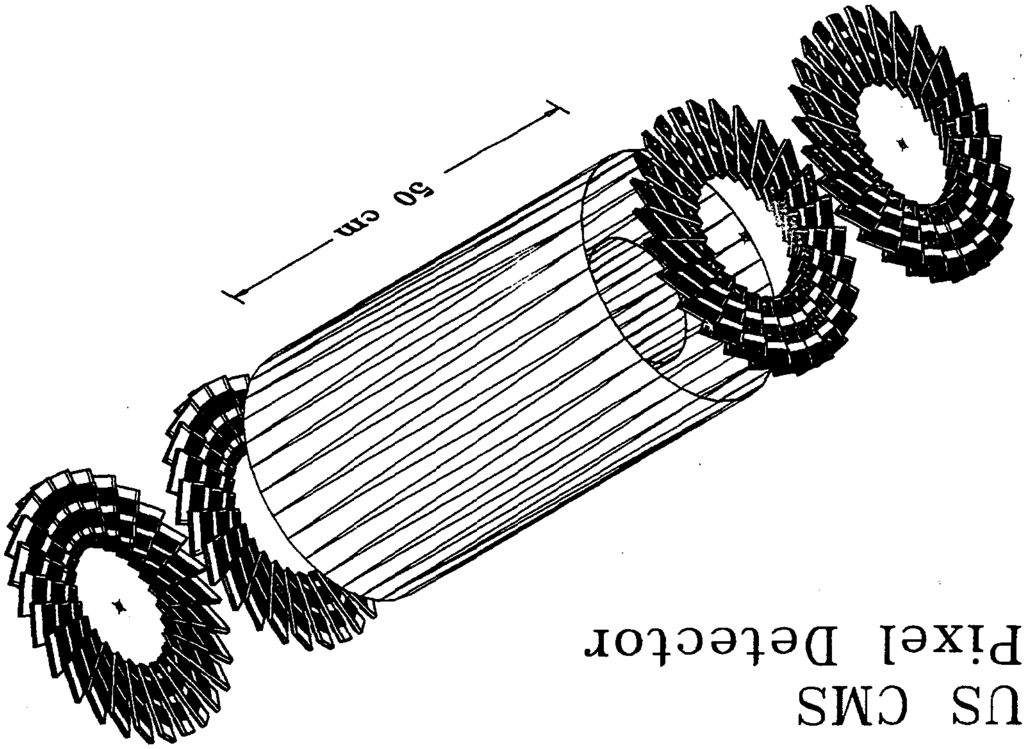
Transverse View


50 cm
US CMS
Pixel Detector

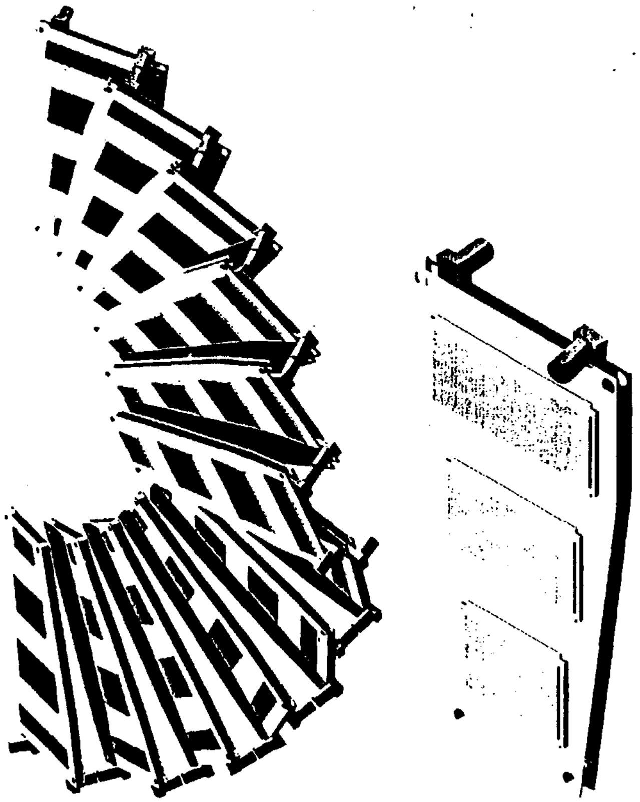
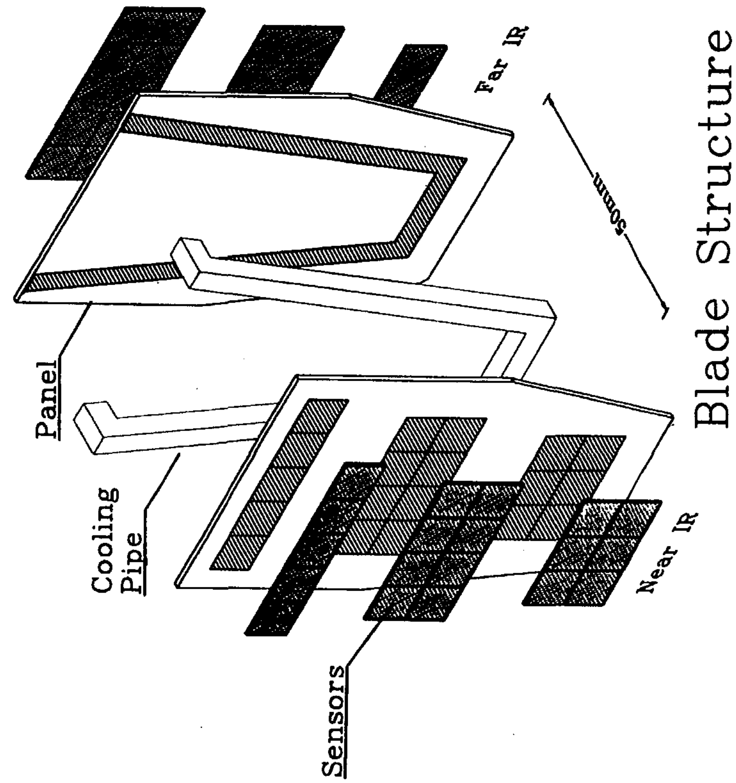


Figure 4: The turbine blade geometry to one disk of forward pixels.



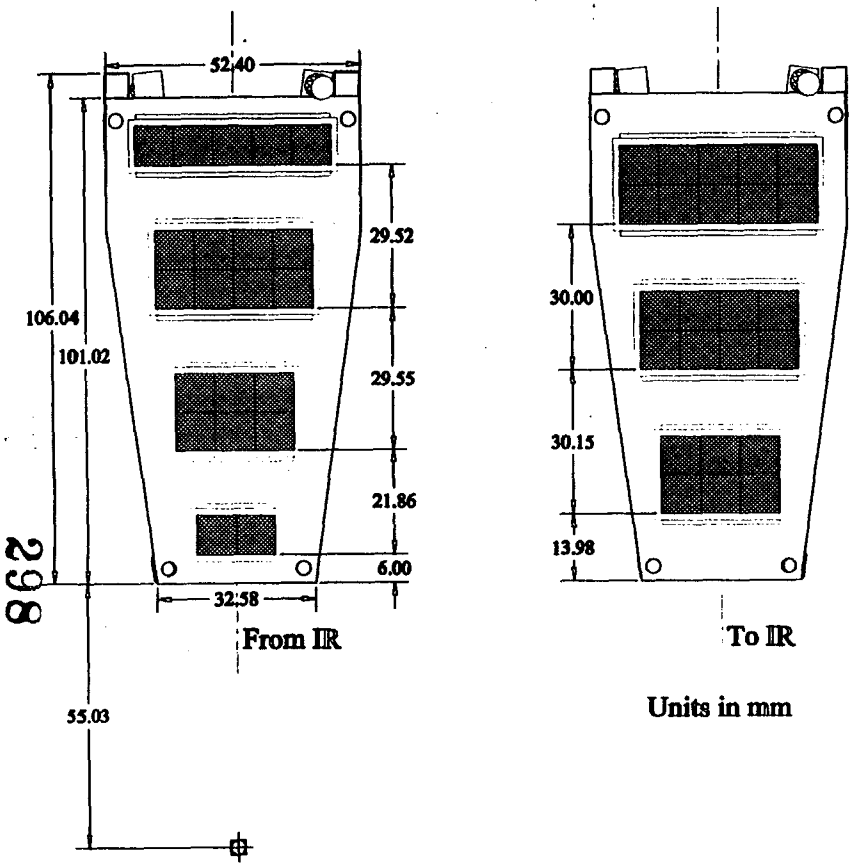


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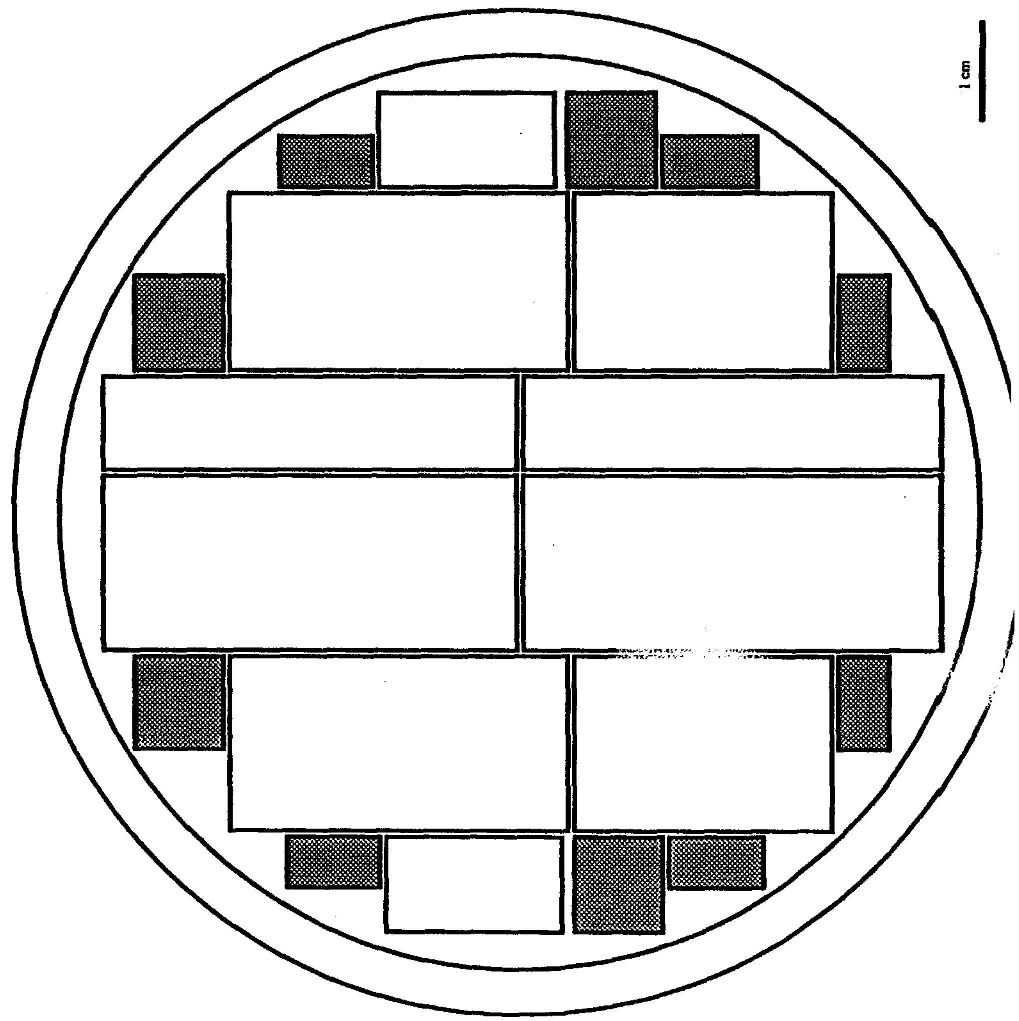
Figure 10: The dimensions of the blades and the sensor arrays.



Total number of sensors needed

4 disks x 24 = 96 blades
each blade has 2 panels consisting of :
7 sensors with 45 readout chips
(each chip reads out 53x52 150micronx150micron pixels)

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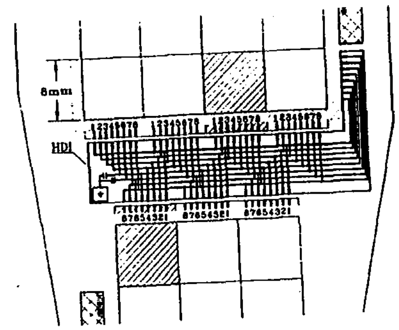
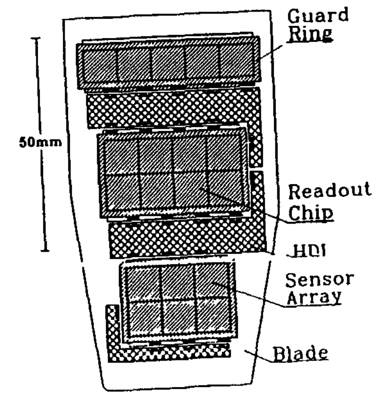
type	readout chips	no. pc.	sensitive area cm x cm r (rphi)	physical size cm x cm r (rphi)
A	2	1	0.795 x 1.560	0.935 x 1.700
B	6	2	1.605 x 2.260	1.745 x 2.400
C	8	2	1.605 x 3.210	1.745 x 3.350
D	10	1	1.605 x 3.960	1.745 x 4.100
E	5	1	0.795 x 3.960	0.935 x 4.100
Total	45	7		

These 7 sensors fit in a 4" silicon wafer.
→ need 96 wafers of good sensors to be installed into 4 disks. plus spares.



High Density Interface Routing.



Schematic of HDI, sensor arrays, readout chips and blade.

300

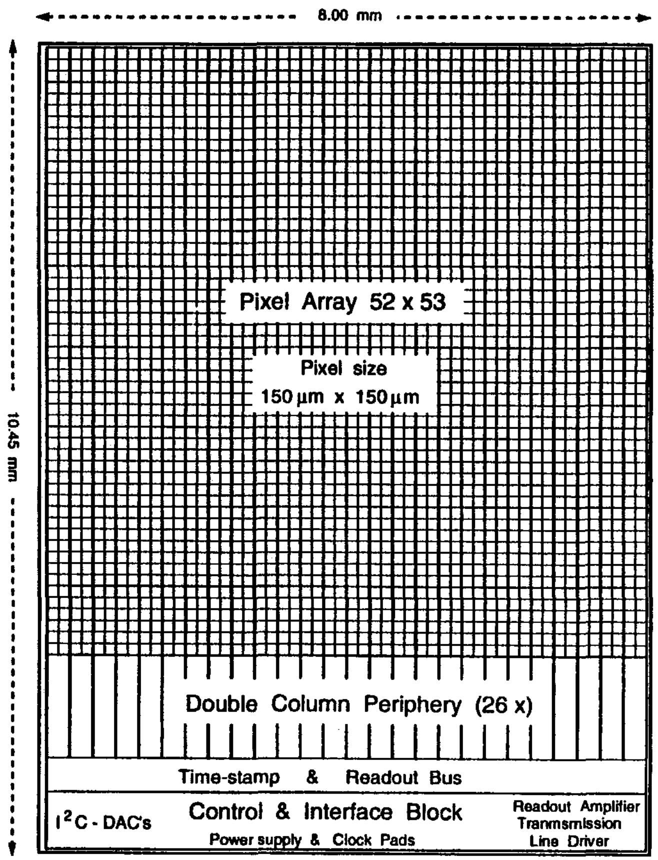


Figure 17: Conceptual layout of pixel readout chip

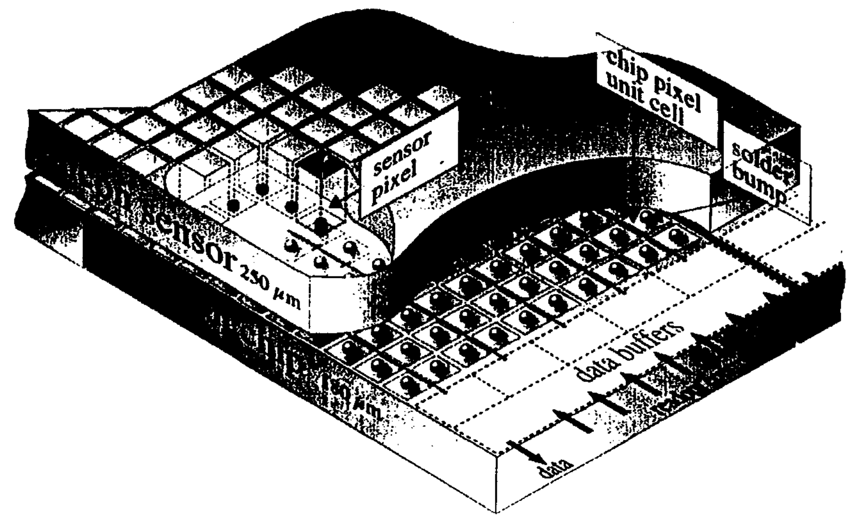


Figure 1: Schematic view of a pixel detector element.

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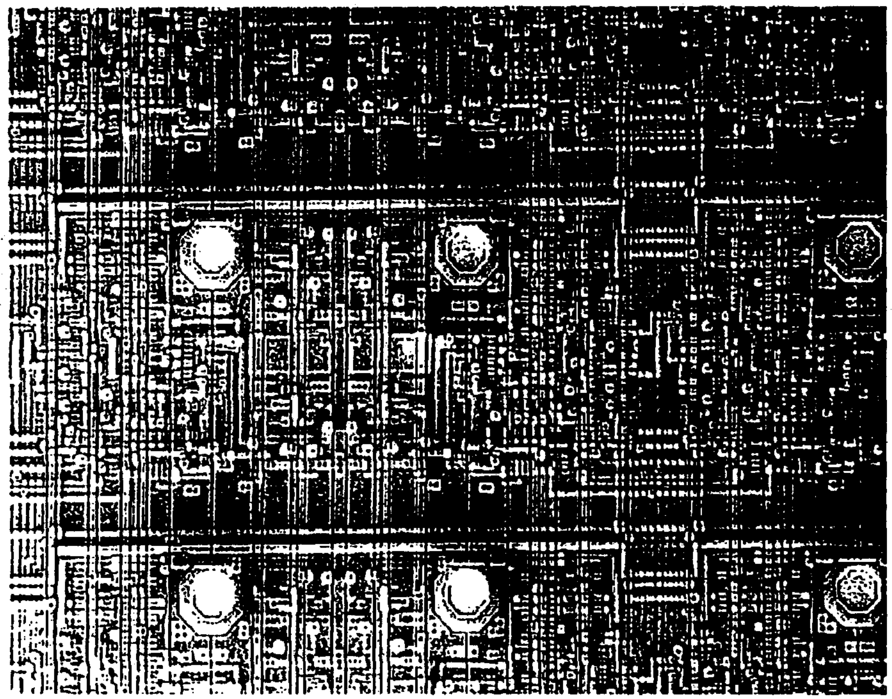

Figure 13: SEM scan of pixel unit cells on the DM_PSI30 chip (DMILL).

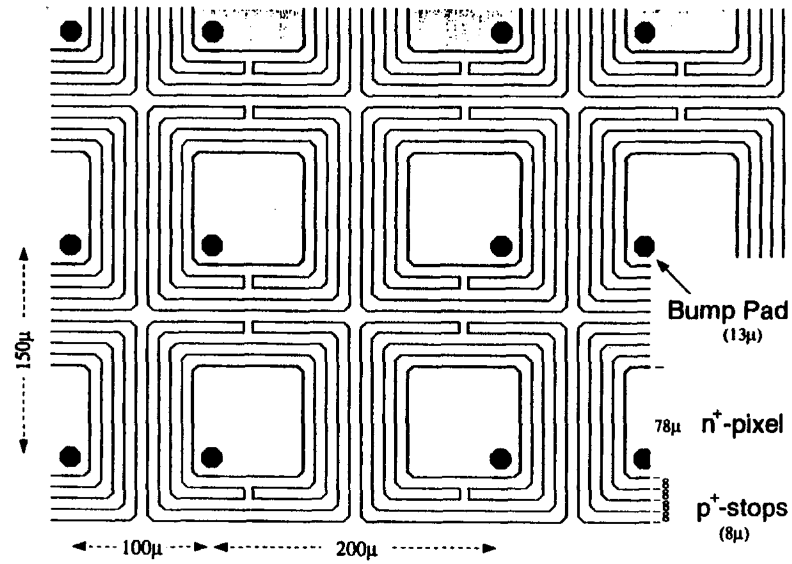

Figure 9: Layout of 150 μ $m \times 150$ μ m pixel sensor. The double p-stop rings around each n-pixel are floating and allow a high resistive path to neighbours.

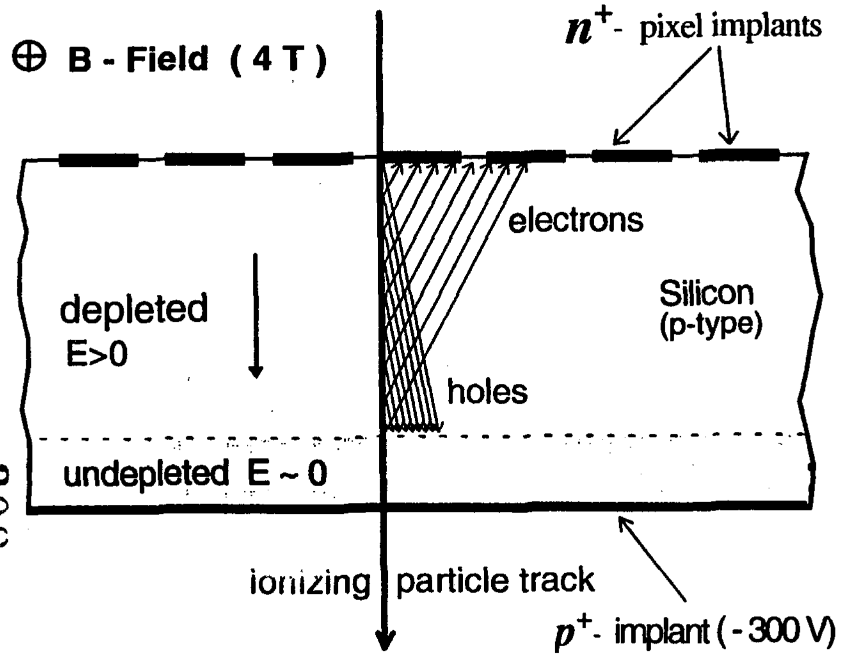

Figure 2: Charge sharing induced by Lorentz drift. After type inversion the detector depletes from the n-pixel side. With increasing radiation dose the detector cannot be fully depleted and the charge sharing effect is reduced.

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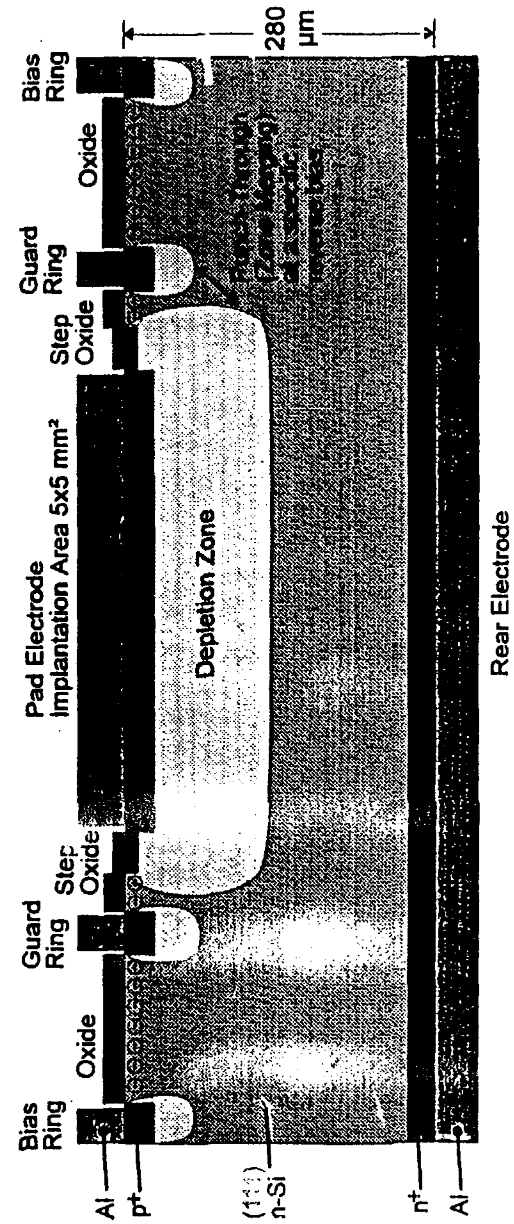
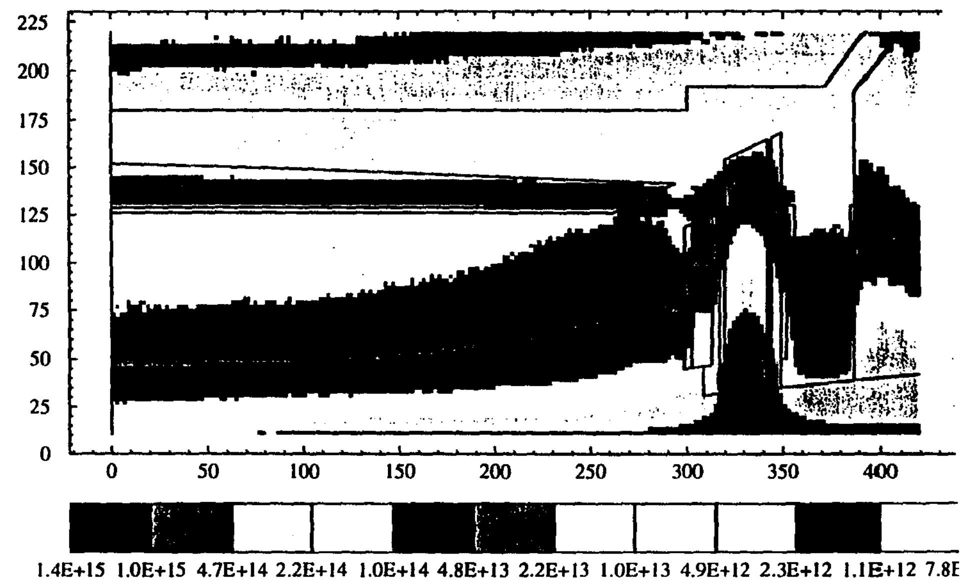
Testing Devices



Goals for CMS Sensor Array R&D

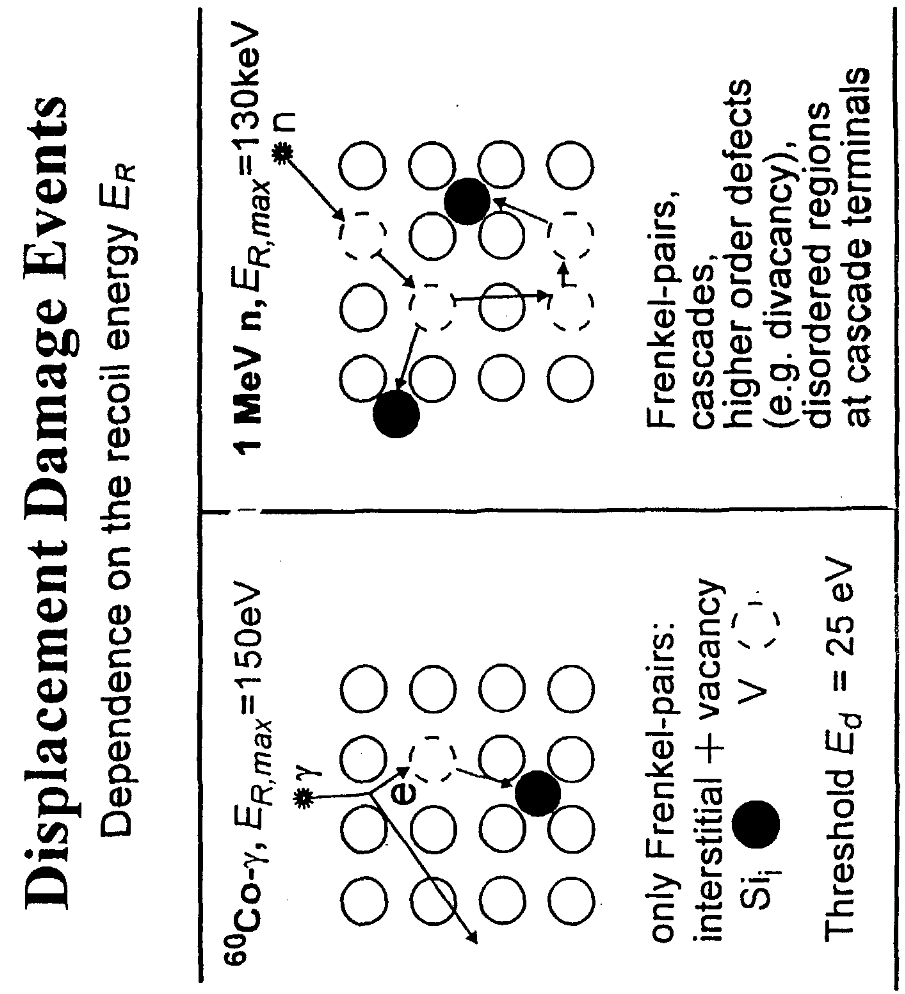
Design pixel sensor arrays for LHC heavy radiation environment
(6 x 10**14 pi/cm**2)

➔300-400V depletion voltage, a new game!
➔ new guard ring designs to sustain high voltage
➔ channel stops



Radiation damage effects

- changes eff. carrier density
- type inversion
- higher depletion voltage
- leakage current
- reduction in signal if partial depletion
- increase in noise
- degradation in spatial resolution
- power consumption
- heat load



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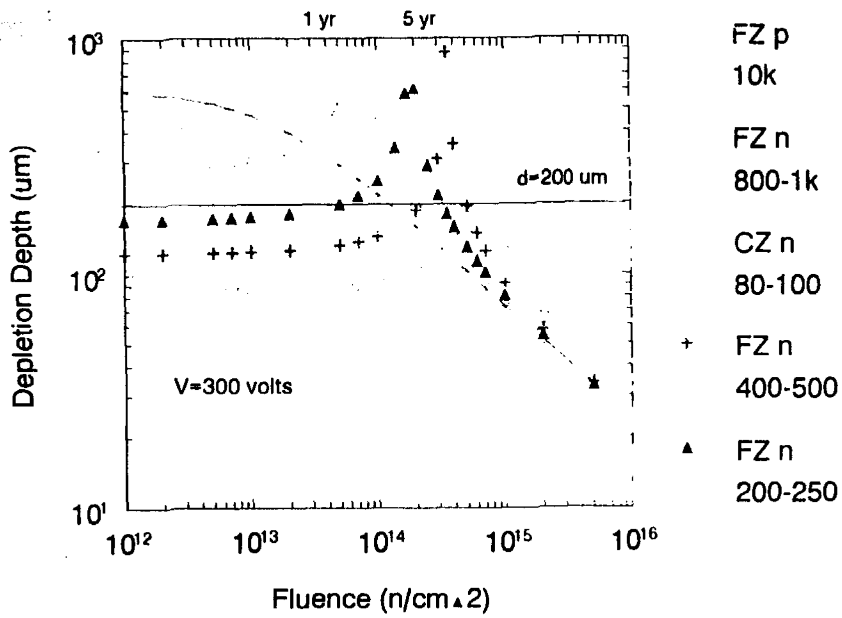
Comparisons among various starting silicon materials

Calculated depeltion depth

Neff=Nd0-Na0-0.07*Fn, Fn=6E13/yr



Comparison among various starting silicon materials

$N_{eff} = N^0_{eff} - 0.07 * \Phi_n$

d=200 µm, V=300 volts, Φ_n =6 x10^{13} n/cm^2/yr *t

Type	ρ(Ω-cm)	N^0_{eff} (cm^{-3})	SCSI Φ_n (n/cm^2)	Initial depletion status	Final depletion status	Appropriate configuration	Process Difficulty (1-10)
FZ n	4-6 k	1x10^{12}	1.4x10^{13}	Full t≤2.5 yr	Partial t≥2.5 yr	$n^+/n/p^+$	10 (double side)
FZ p	10-15 k	-1 x10^{12}	N/A	Full t≤2 yr	Partial t≥2 yr	$n^+/p/p^+$	7 (single side)
CZ (hi [O]) n	80-100	5x10^{13}	>7x10^{14}	Partial t≤9.7 yr	Full t≥9.7 yr	$p^+/n/n^+$	4 (single side)
FZ n	800-1k	5x10^{12}	7x10^{13}	Full t≤3.4 yr	Partial t≥3.4 yr	$n^+/n/p^+$	10 (double side)
FZ n	400-500	1x10^{13}	3.6x10^{14}	Partial t≤0.15yr	Full 0.15≤t≤4.6 yr	$n^+/n/p^+$	10 (double side)
FZ n	200-250	2x10^{13}	1.9x10^{14}	Partial t≤2.5 yr	Full 2.5≤t≤7.0 yr	$p^+/n/n^+$	4 (single side)

Development Strategy

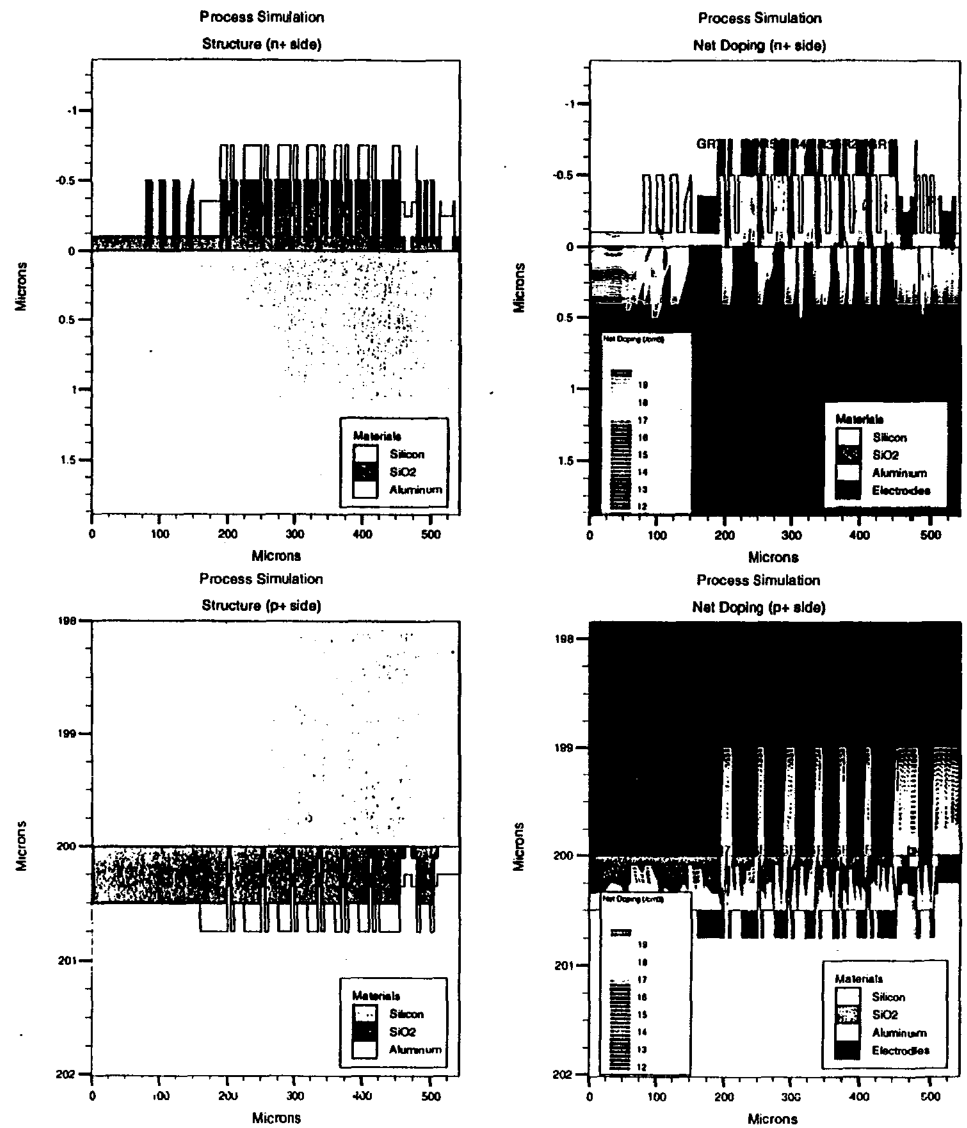
- Rad-hard GuardRing design (collaborate with BNL)
- Rad-hard pixel arrays (BNL, Pisa, PSI)
- Prototype sensors (collaborate with PSI, Pisa)
- Preseries/production
- Acceptance tests

Rad-Hard Guard Rings

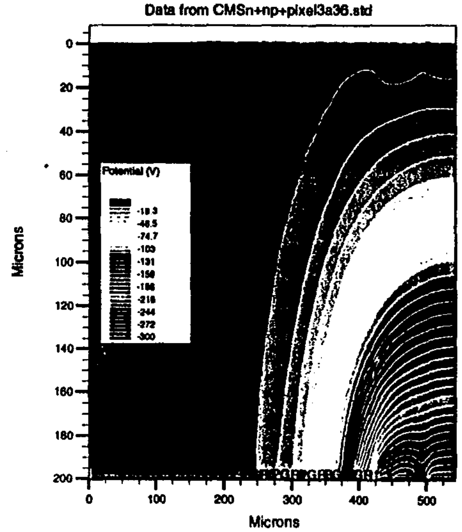
- Collaborate with BNL (Li)
- simple structures
- Silvaco simulation package
- design at JHU
- variation:
  number and shape of GRs
  field plates
- process at BNL JHU students
- radiation with n beam
- measure characteristics
- understand the process
- faster turn around
- silicon thickness and R

1997 Submission

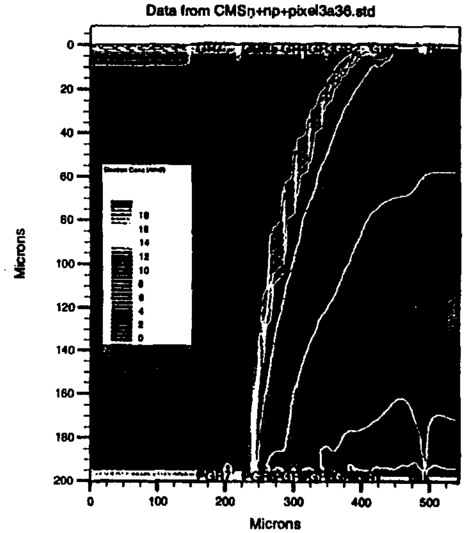
Feb-Mar: Simulation at JHU
Apr: Design work at JHU for Multi-guard rings, test structures,
single pixels, pixel arrays, and fan-out arrays.
May 1: designs to Photronics.
May 15: wafers arrived at BNL.
May 19: masks arrived at BNL.
May 22: fabrication began at BNL.
Jun 3: Lehman Review I.
Jul 31: first wafers processed.
Aug: first batch of wafers processed.
Sep: diced and tests.
Oct: neutron irradiation at UMass Lowell.
wafers processed with deeper implants
Oct-Dec: Tests.



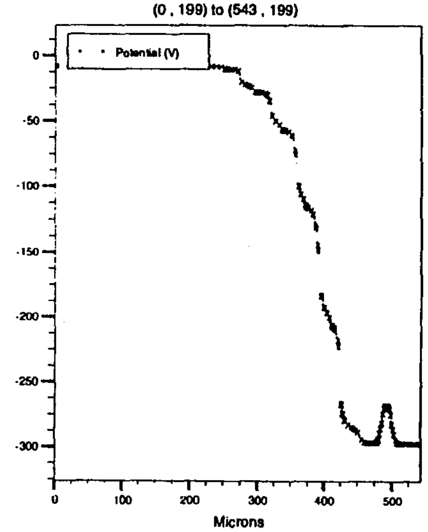
N-type, Neff=5e12/cm **3, ph(n)=0, Larger SCSI fluence
Data from CMSn+np+pixel3a36.std



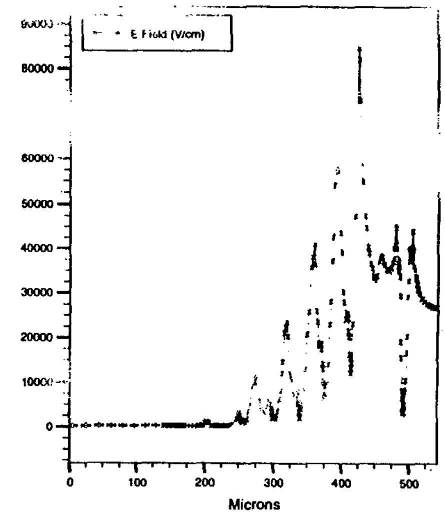
N-type, Neff=5e12/cm **3, ph(n)=0, Larger SCSI fluence
Data from CMSn+np+pixel3a36.std



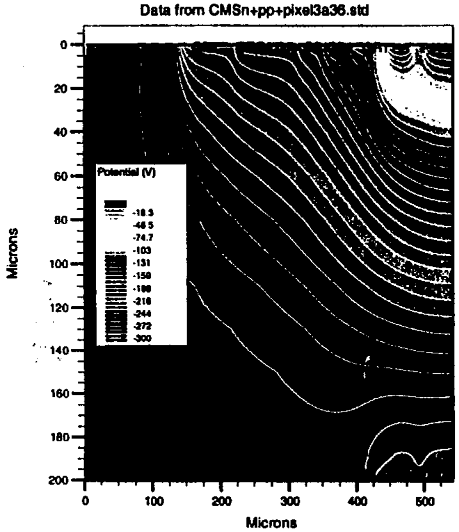
Section 1 from CMSn+np+pixel3a36.std
(0 , 199) to (543 , 199)



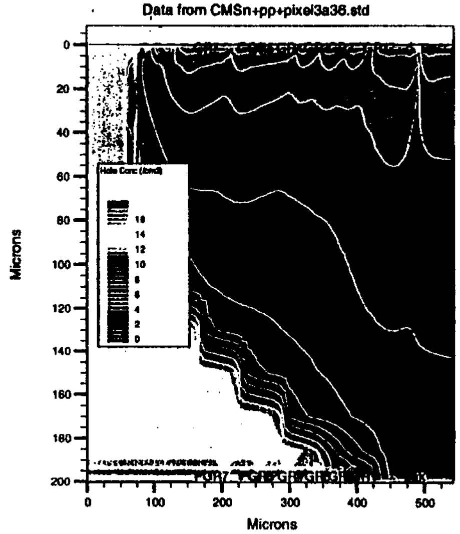
Section 1 from CMSn+np+pixel3a36.std
. 198) to (543 , 198)



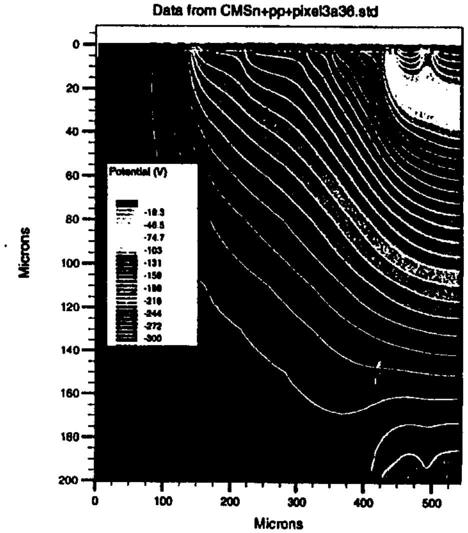
P-type, Neff=-5e12/cm **3, ph(n)=5.7e13 n/cm*2
Data from CMSn+pp+pixel3a36.std



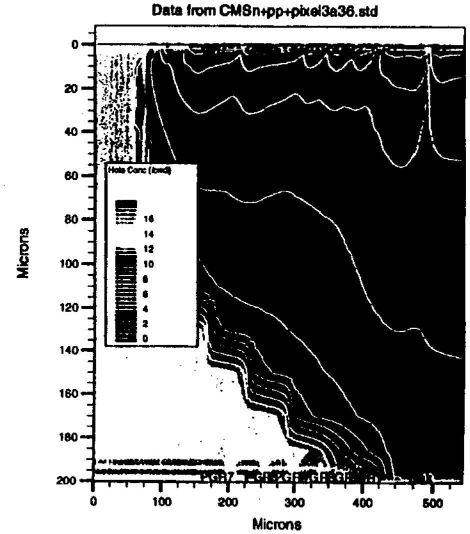
P-type, Neff=-5e12/cm **3, ph(n)=5.7e13 n/cm*2
Data from CMSn+pp+pixel3a36.std



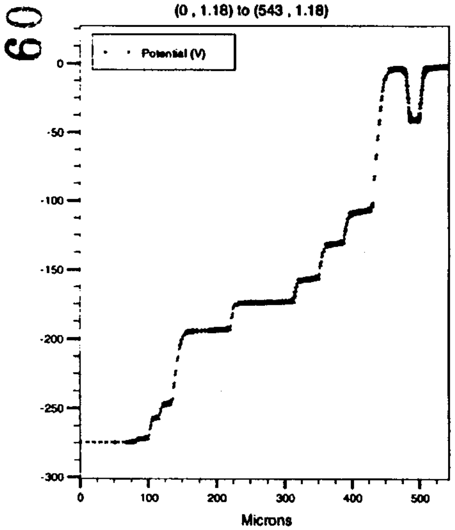
P-type, Neff=-5e12/cm **3, ph(n)=1.4e14 n/cm**2
Data from CMSn+pp+pixel3a36.std



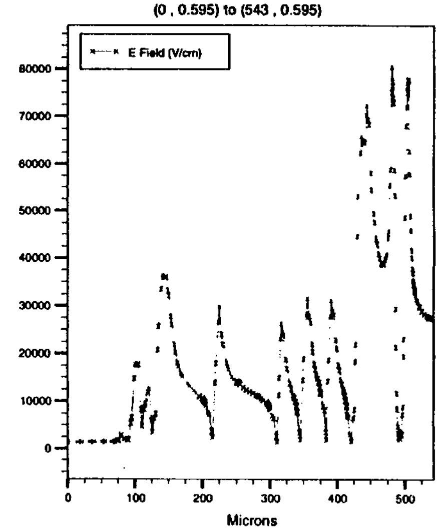
P-type, Neff=-5e12/cm **3, ph(n)=1.4e14 n/cm**2
Data from CMSn+pp+pixel3a36.std



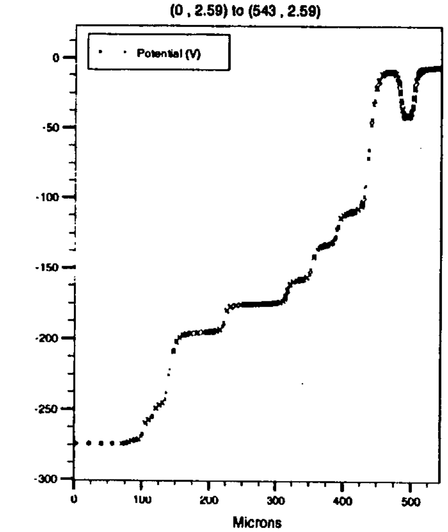
Section 1 from CMSn+pp+pixel3a36.std
(0 , 1.18) to (543 , 1.18)



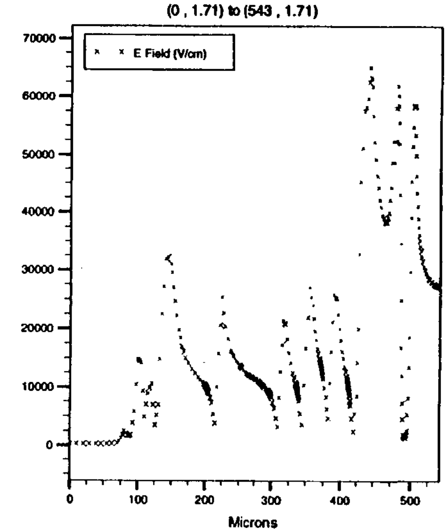
Section 1 from CMSn+pp+pixel3a36.std
(0 , 0.595) to (543 , 0.595)

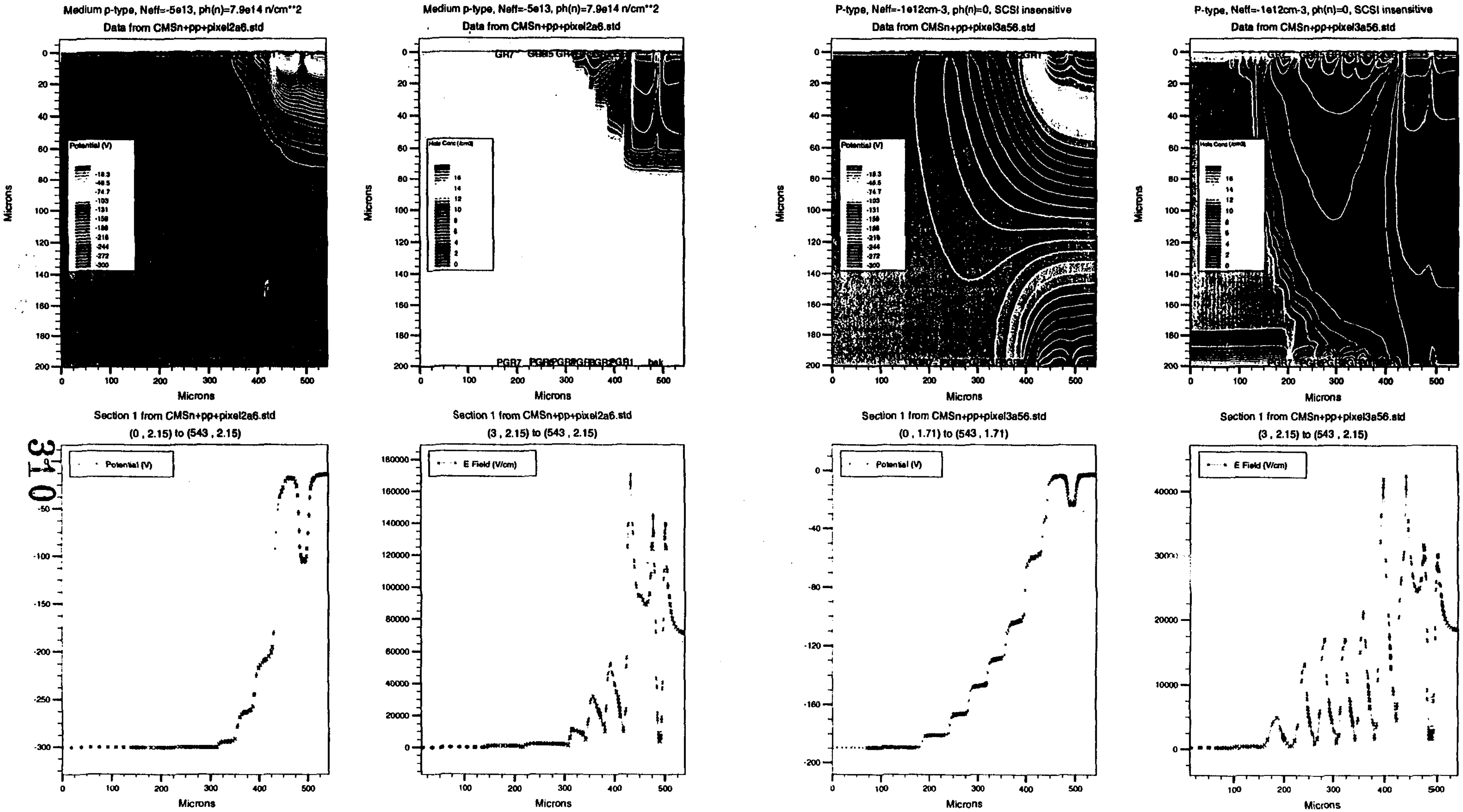


Section 1 from CMSn+pp+pixel3a36.std
(0 , 2.59) to (543 , 2.59)

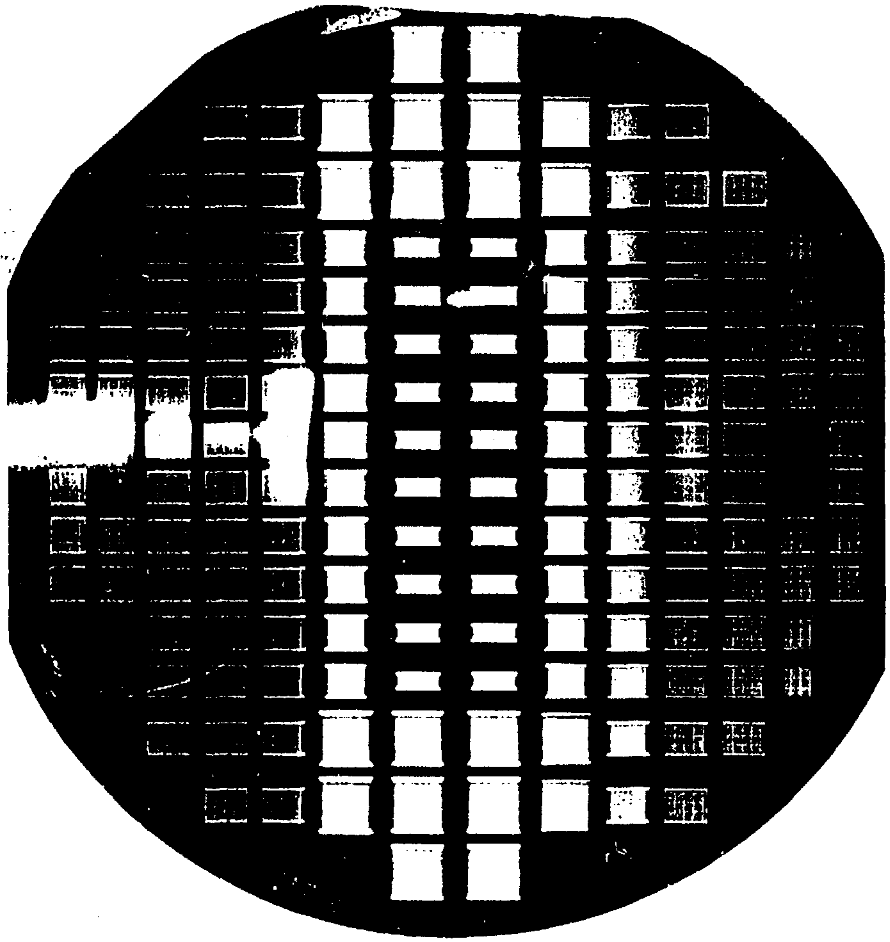


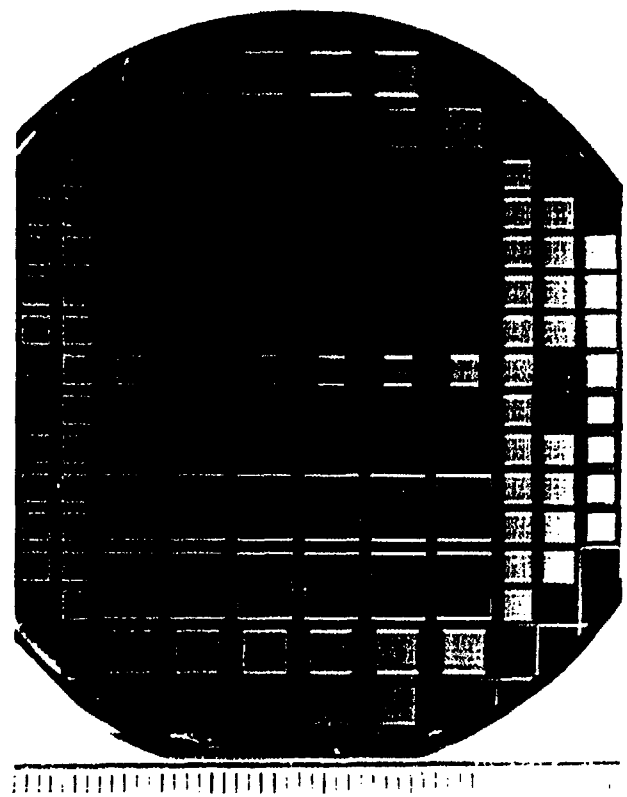
Section 1 from CMSn+pp+pixel3a36.std
(0 , 1.71) to (543 , 1.71)




Medium p-type, Neff=-5e13, ph(n)=7.9e14 n/cm**2
Data from CMSn+pp+pixel2a6.std
Potential (V)
Microns
Medium p-type, Neff=-5e13, ph(n)=7.9e14 n/cm**2
Data from CMSn+pp+pixel2a6.std
Hole Conc (/cm3)
Microns
P-type, Neff=-1e12cm-3, ph(n)=0, SCSI insensitive
Data from CMSn+pp+pixel3a56.std
Potential (V)
Microns
P-type, Neff=-1e12cm-3, ph(n)=0, SCSI insensitive
Data from CMSn+pp+pixel3a56.std
Hole Conc (/cm3)
Microns
Section 1 from CMSn+pp+pixel2a6.std
(0 , 2.15) to (543 , 2.15)
Potential (V)
Microns
Section 1 from CMSn+pp+pixel2a6.std
(3 , 2.15) to (543 , 2.15)
E Field (V/cm)
Microns
Section 1 from CMSn+pp+pixel3a56.std
(0 , 1.71) to (543 , 1.71)
Potential (V)
Microns
Section 1 from CMSn+pp+pixel3a56.std
(3 , 2.15) to (543 , 2.15)
E Field (V/cm)
Microns

Wafer Designed for FNAL





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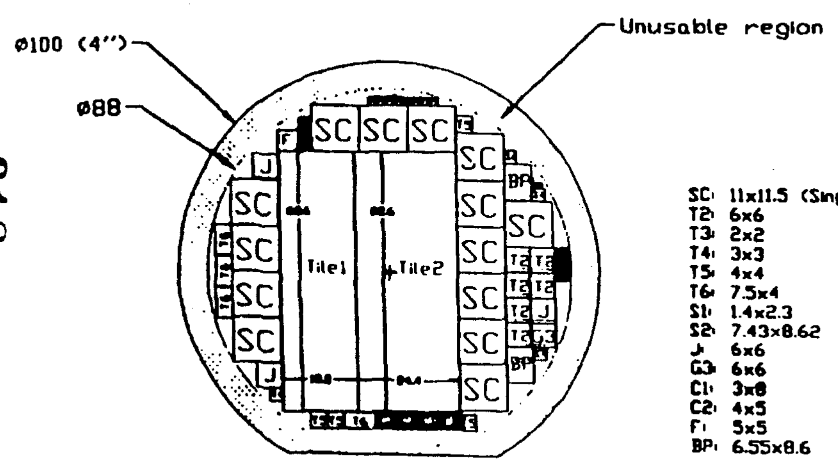
CMS Sensor submission with Atlas (July 1997)

Figure 1 CMS Sensor Submission with Atlas July 97.



SC: 11x11.5 (Single Chip)
T2: 6x6
T3: 2x2
T4: 3x3
T5: 4x4
T6: 7.5x4
S1: 1.4x2.3
S2: 7.43x8.62
J: 6x6
G3: 6x6
C1: 3x8
C2: 4x5
F: 5x5
BP: 6.55x8.6

Grant Gorfine, UNM
Mar 17, 1997
Dimensions: mm
File: wafers
Comments: Cut line assumed to be [illegible] micron wide.

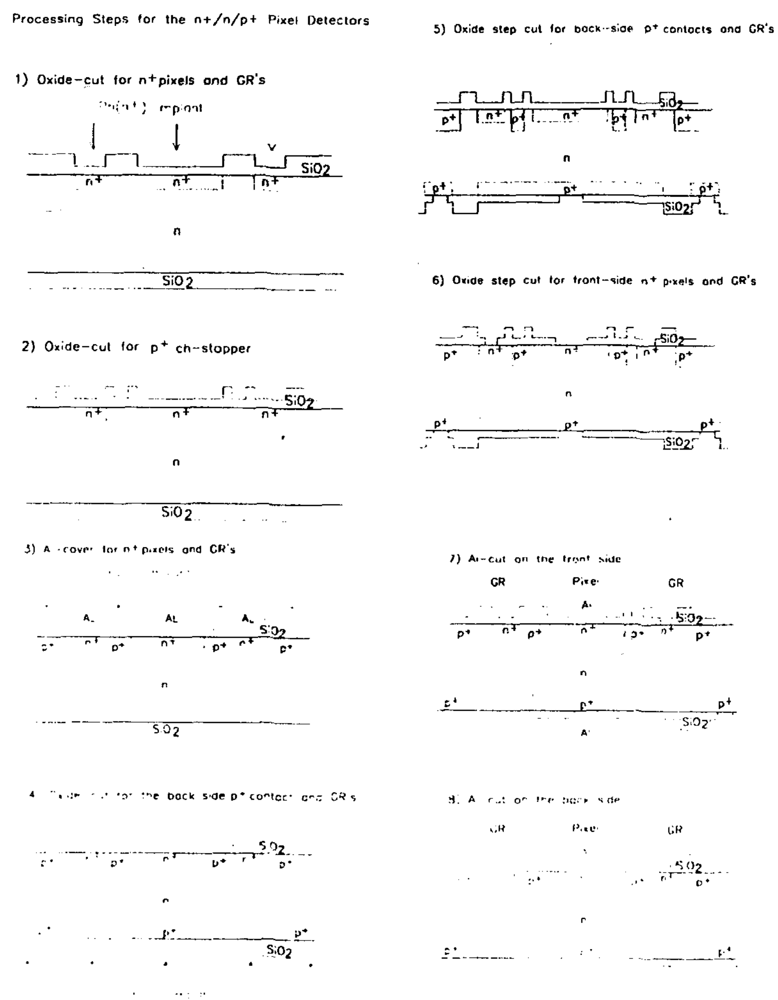


Fig. 2. Processing steps for n+/n/p+ pixel detectors.

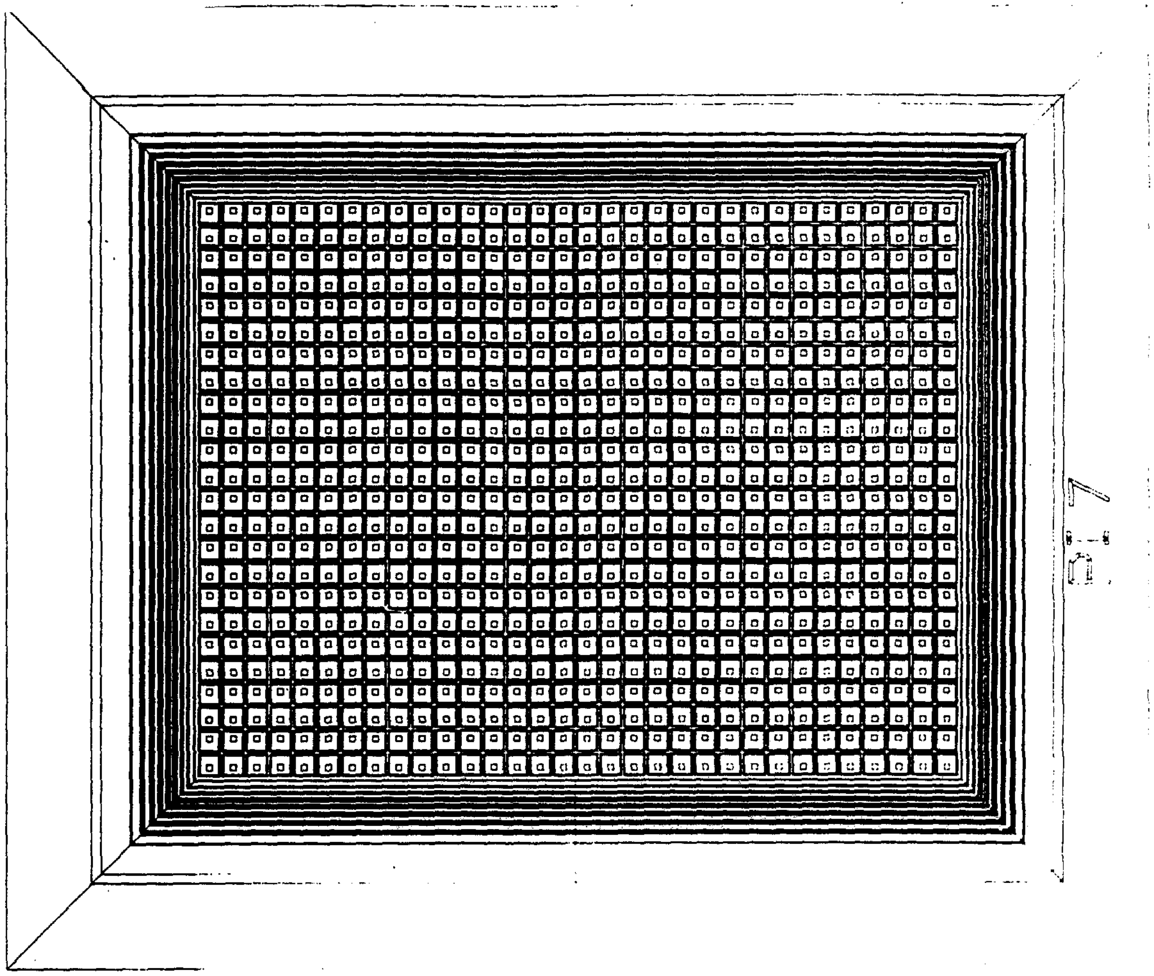
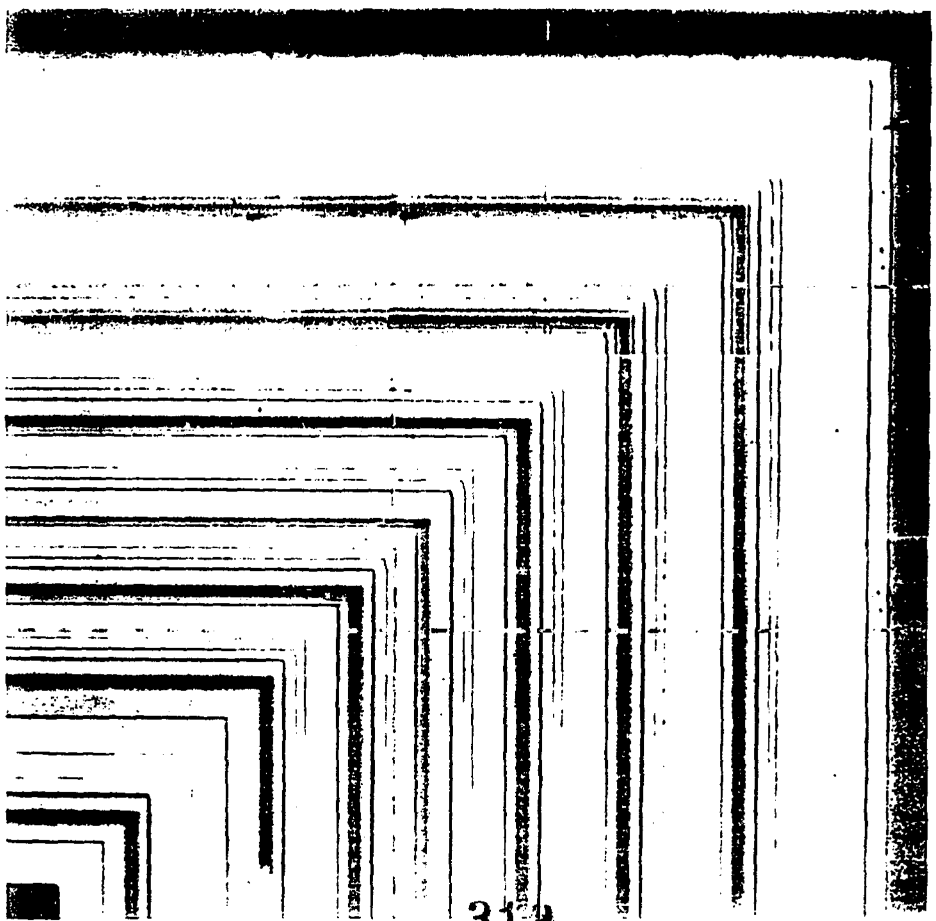
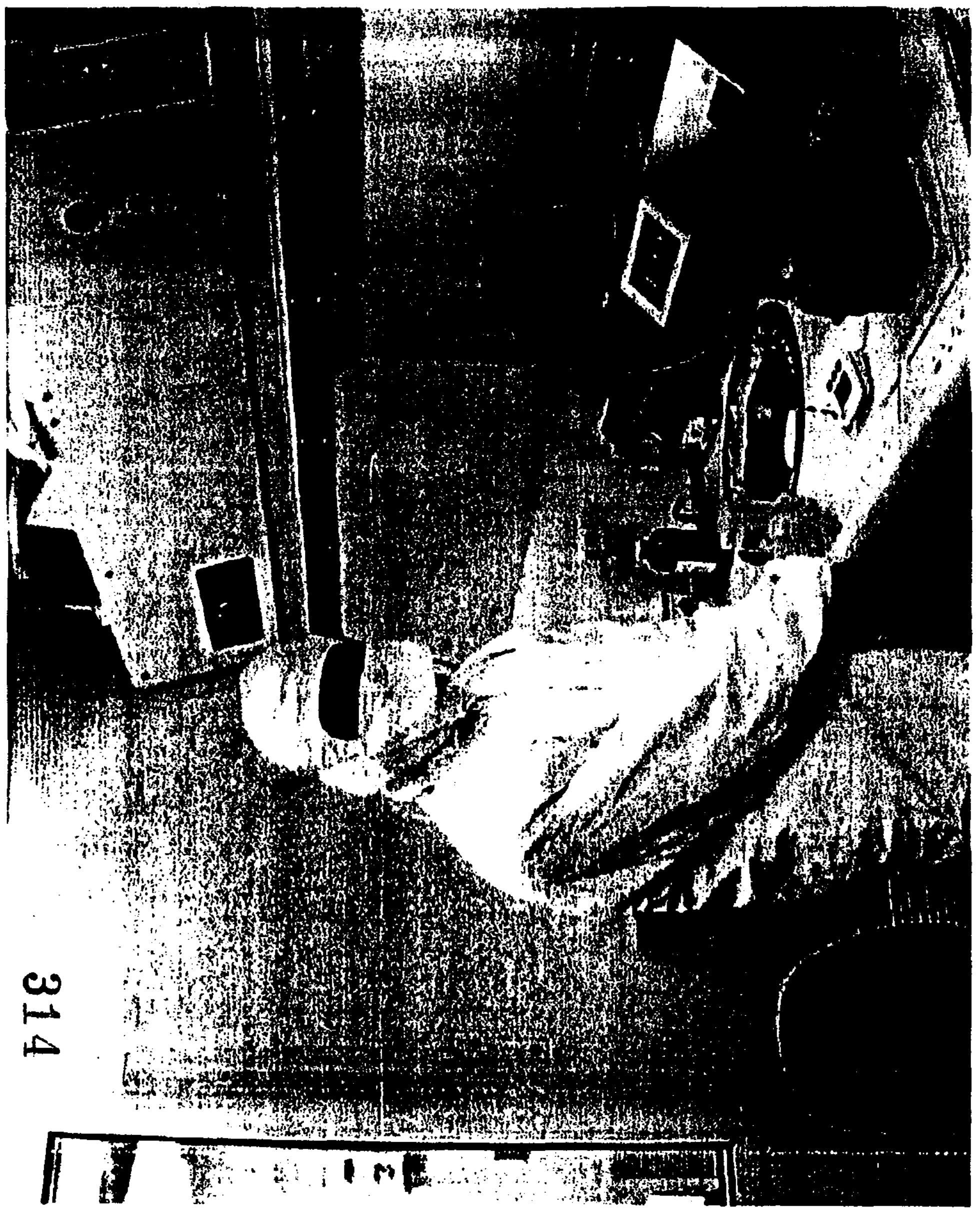


Fig. 7





Wafers Fabricated

Wafer No. 740, 741, 742, 743, 745
Fab. Date: 6/26/97 (25 keV B)
Thickness: 200-250 μ
Resistivity: 2K Ω-cm
Configuration: n+/n/p+

Wafer No. 754, 755, 764, 765
Fab. Date: 10/97 (40keV B)
Thickness: 200-250 μ
Resistivity: 2K Ω-cm
Configuration: n+/n/p+(754-755)
p+/n/n+(764, 765)

Wafer No. 726, 727, 728, 729, 730, 731
Fab. Date: 3/98 (reprocessed from 5/97)
Thickness: 200-250 μ
Resistivity: 2K Ω-cm
Configuration: n+/n/p+

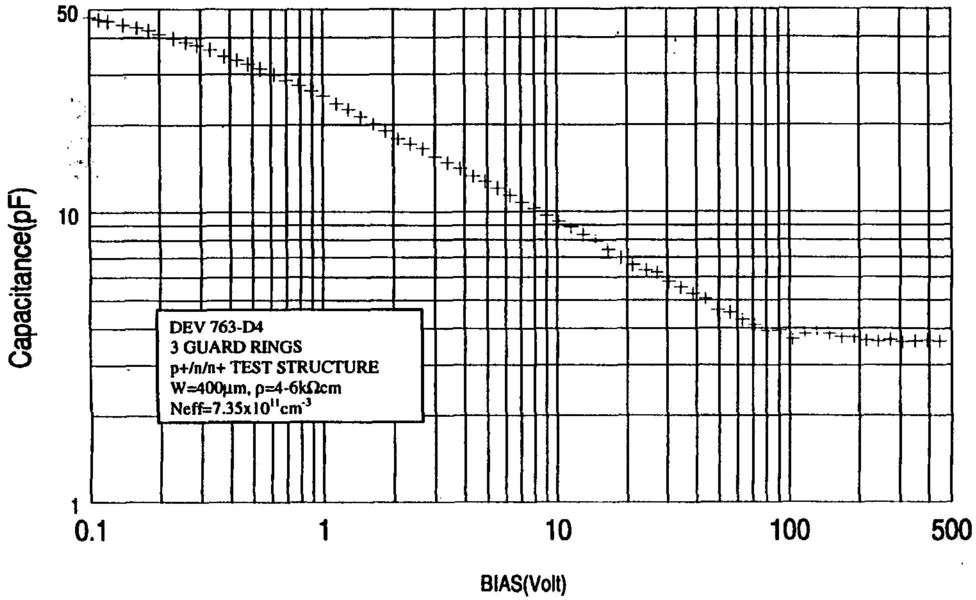


Fig.4b. C-V Characteristic with all guard rings floating [1]. The bulk full depletion is about 90V.

[1] Sheet file: c:\msoffice\winword\poster\fig2.doc

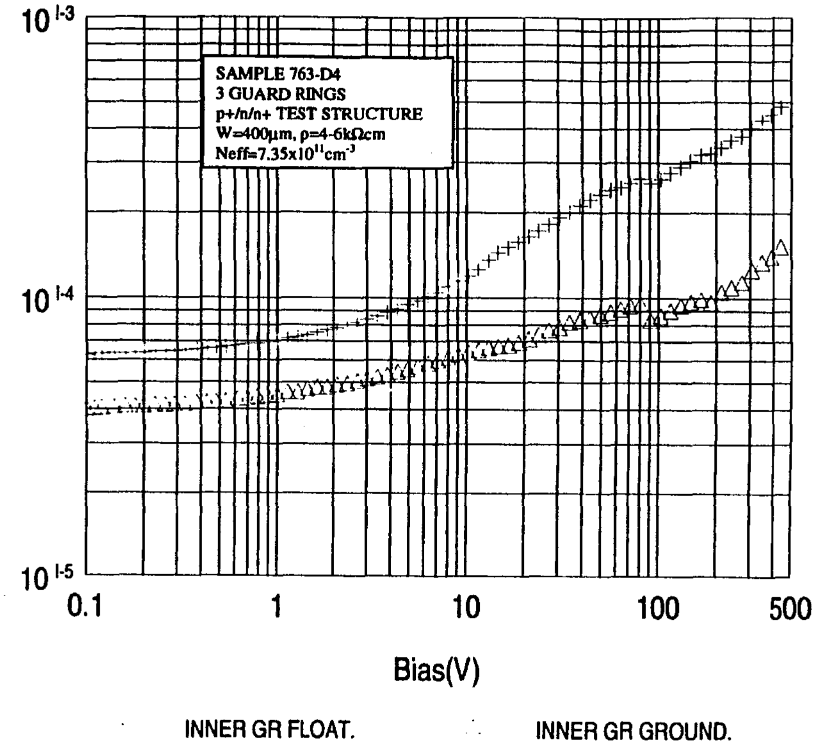
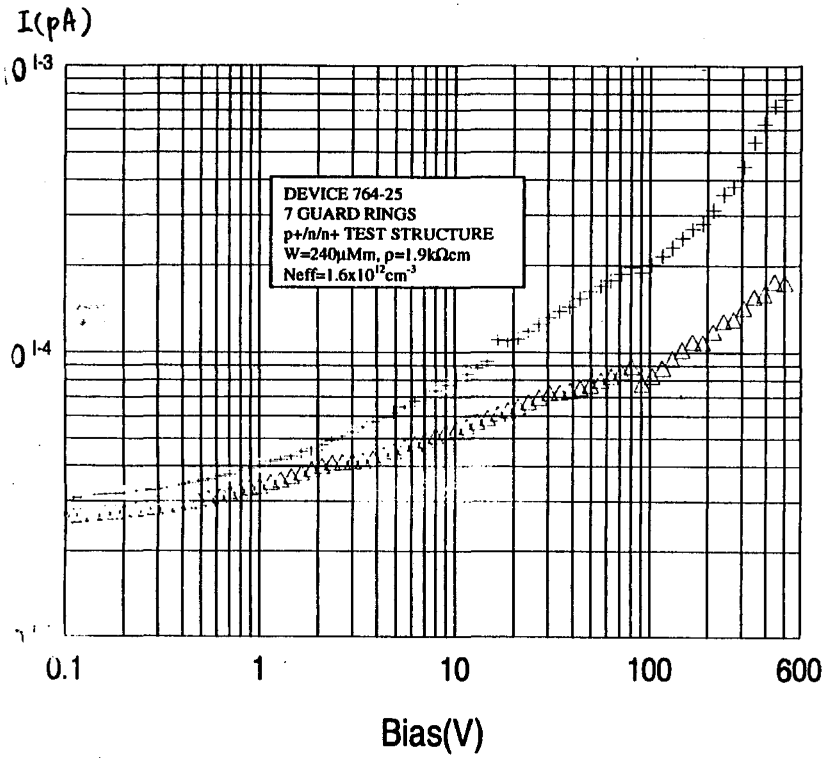
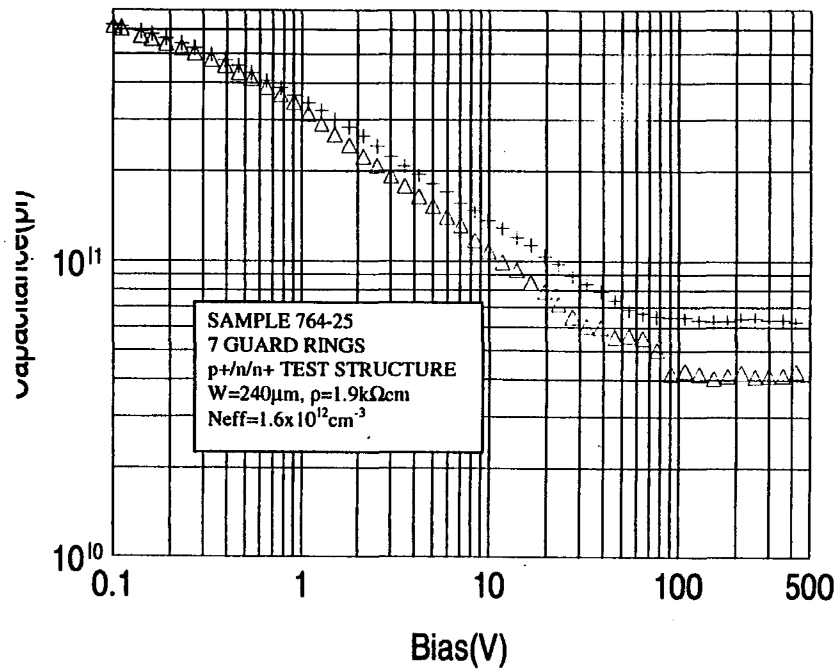


Fig.4a. I-V Characteristics with inner guard ring floating or grounded[1]. No breakdown is observed up to 500V.

[1] Sheet file:c:\msoffice\winword\poster\fig4.doc



INNER GR FLOAT.   INNER GR GROUND.



INNER GR FLO   INNER GR GRO

Fig.5a. I-V Characteristics with inner guard ring floating or grounded[1]. No breakdown is observed up to 500V.

Fig.5b. C-V characteristics with inner guard ring floating or grounded[1]. The bulk full depletion is about 70V.

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[1] Sheet file: c:\msoffice\winword\poster\fig7.doc

[1] Sheet file:c:\msoffice\winword\poster\fig5.doc

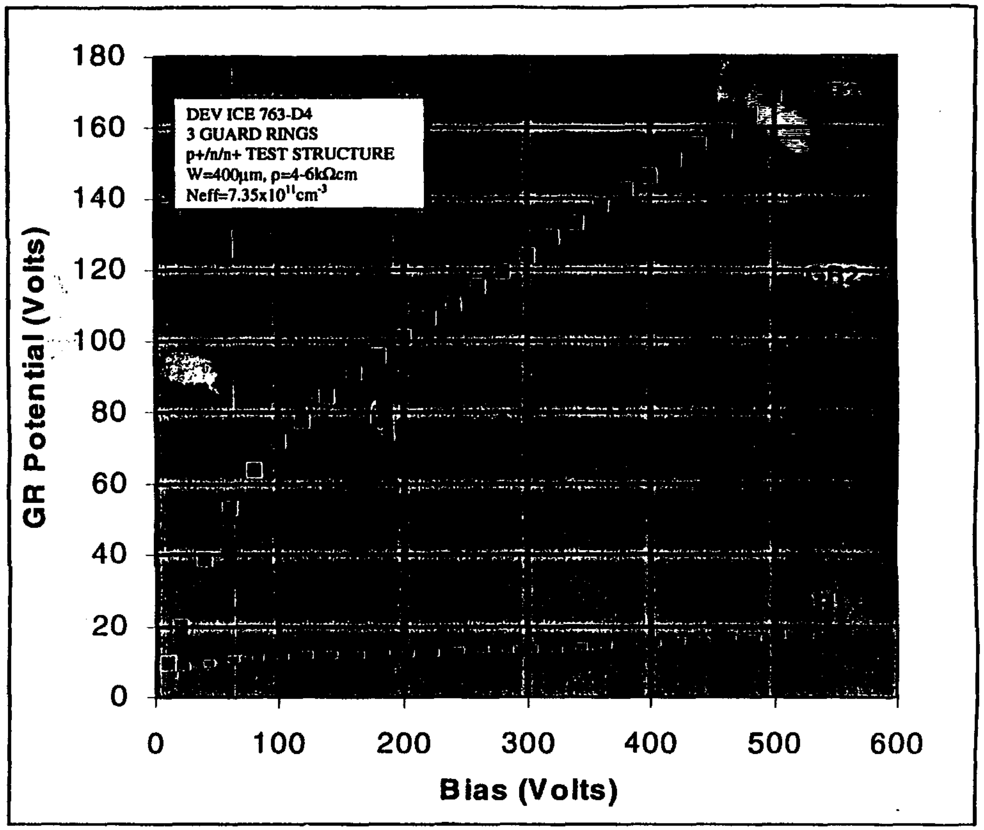

Fig.4c. Guard rings potential versus voltage bias[1]. Label GR1 corresponds to the inner guard ring, GR3 to the outer one.

[1] Sheet file:c:\msoffice\winword\poster\fig3.doc
Figure: imported from Excel; data in proper floppy disk.

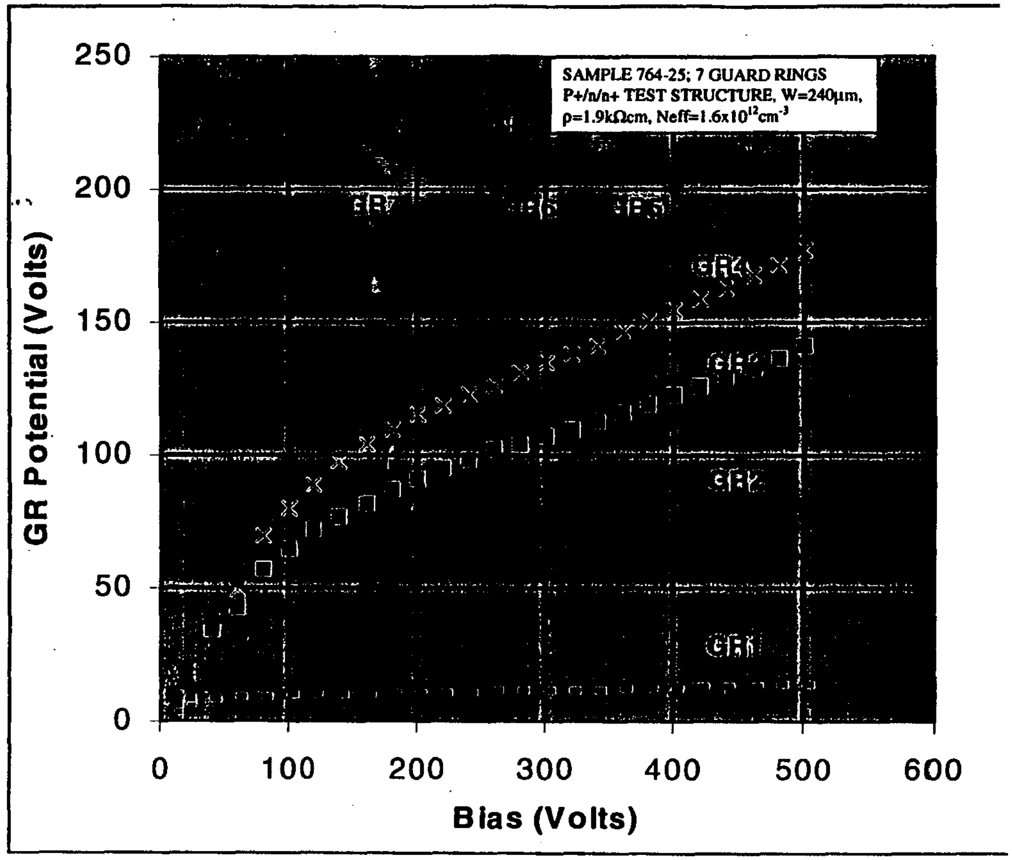

Fig.5c. Guard rings potential versus applied bias[1]. Label GR1 refers to inner guard ring, GR7 to the outer one.

[1] Sheet file: c:\msoffice\winword\poster\fig6.doc

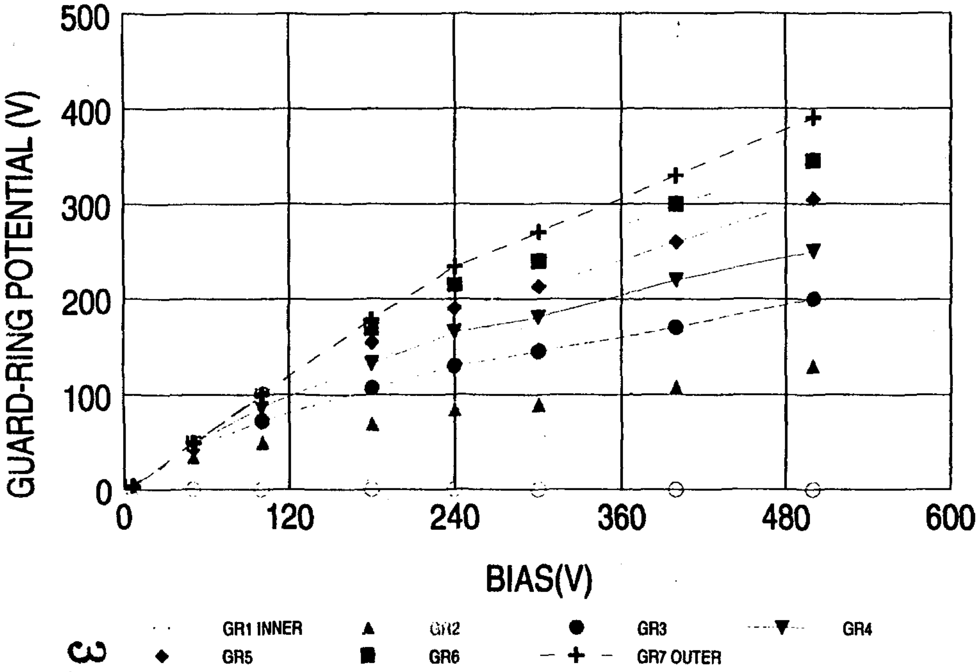

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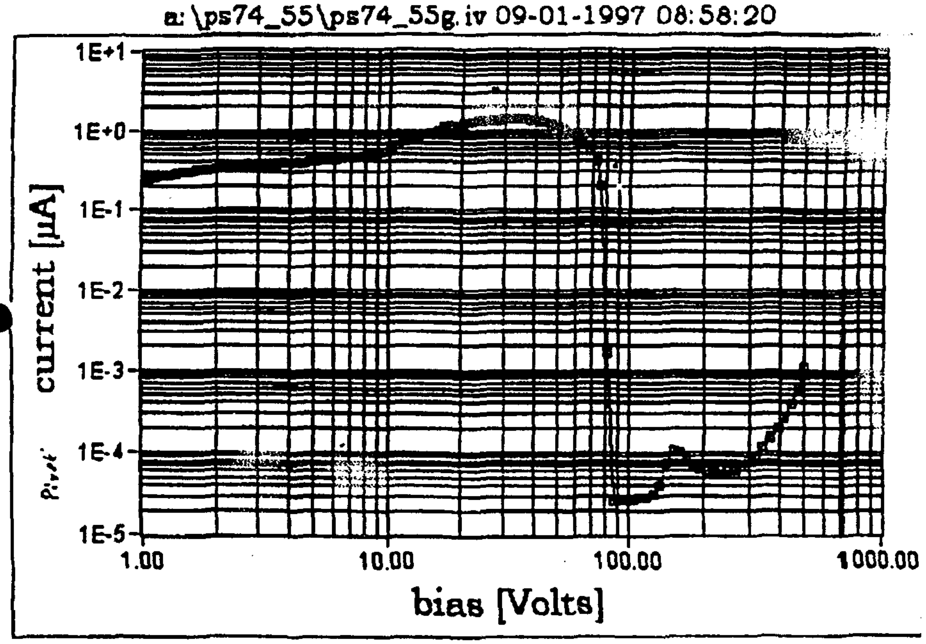
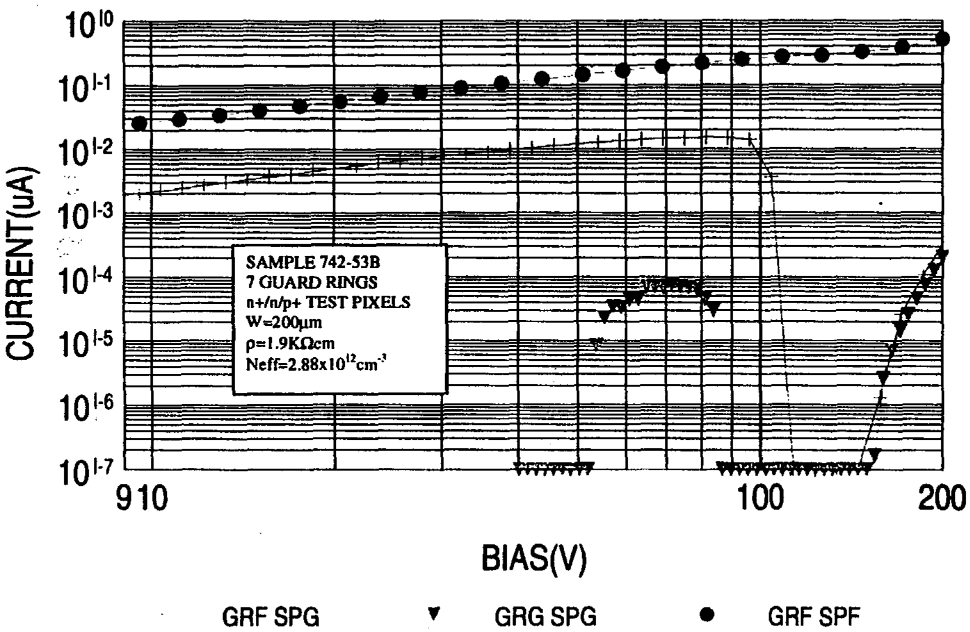
Fig.6. Expected guard-ring potential versus bias characteristic obtained, by numerical simulations, for sample 764-25 (a 7 guard-rings, p+/n/n+ test structure)[1]. Inner guard ring is set at zero potential.

Leakage Current of a Single Pixel vs. Bias Voltage from 1 to 500 V.



Sheet file:c:/msoffice/winword/poster/fig13.doc



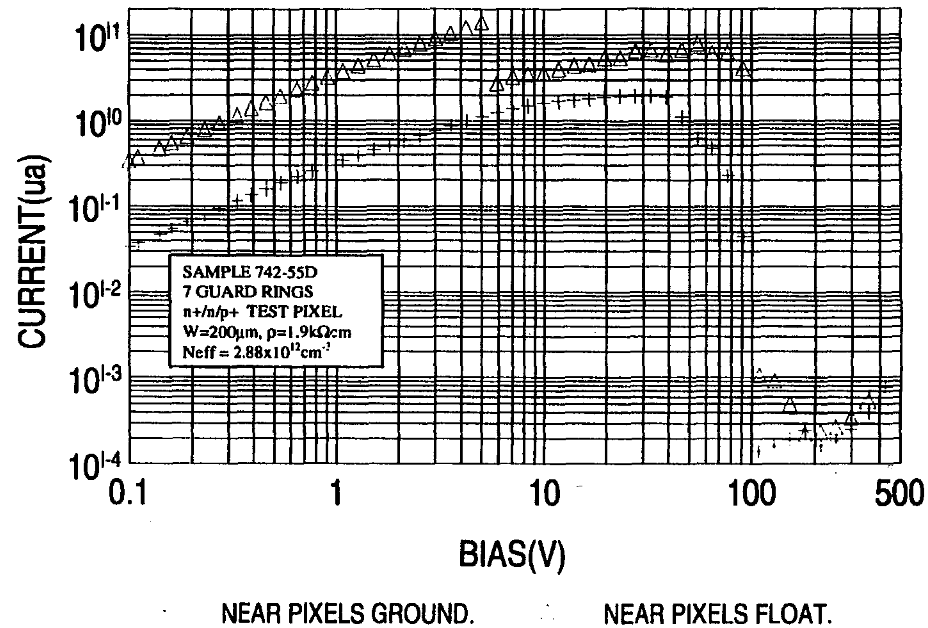


Fig.3a. Several I-V characteristic of the pixel 742-53b, obtained with different set up[1]. GRF(G) means "guard ring floating (grounded)", while SPF(G) means "surrounding eight pixels floating (grounded)".

Fig. 3b. I-V Characteristic of pixel 742-55D [1] device with inner guard ring grounded. Pinch off occur at full depletion.

[1] Sheet file: c:\msoffice\winword\poster\fig11.doc

[1] Sheet file: c:\msoffice\winword\poster\fig9.doc

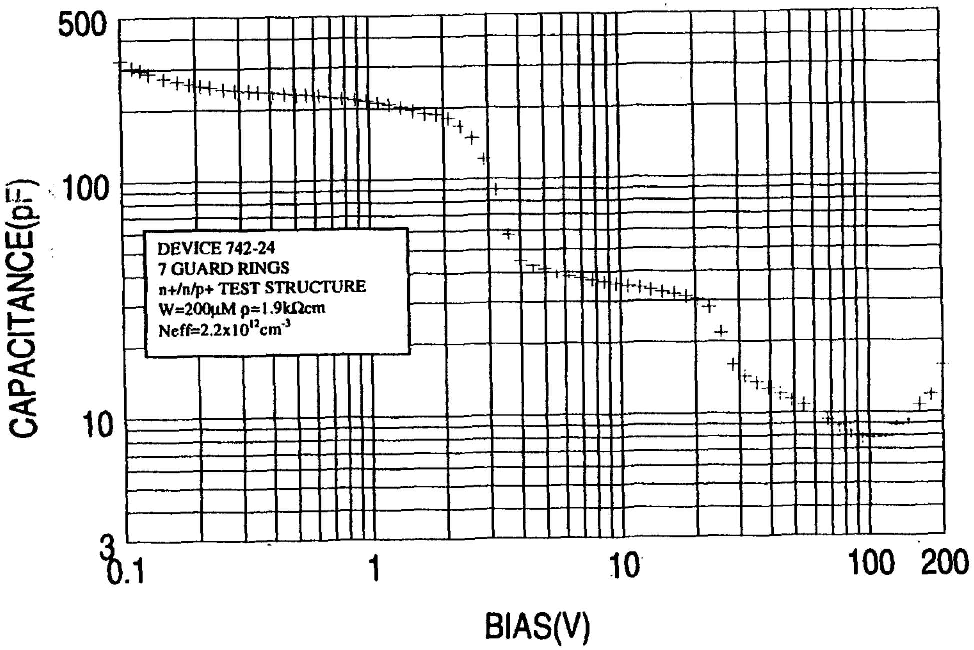
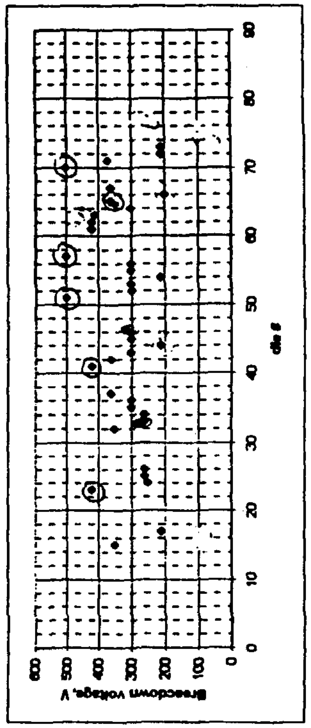


Fig.3c. C-V Characteristic of test structure with all guard rings floating. Flat band voltage is about 3V. Depletion occur at 90V.

Sheet1

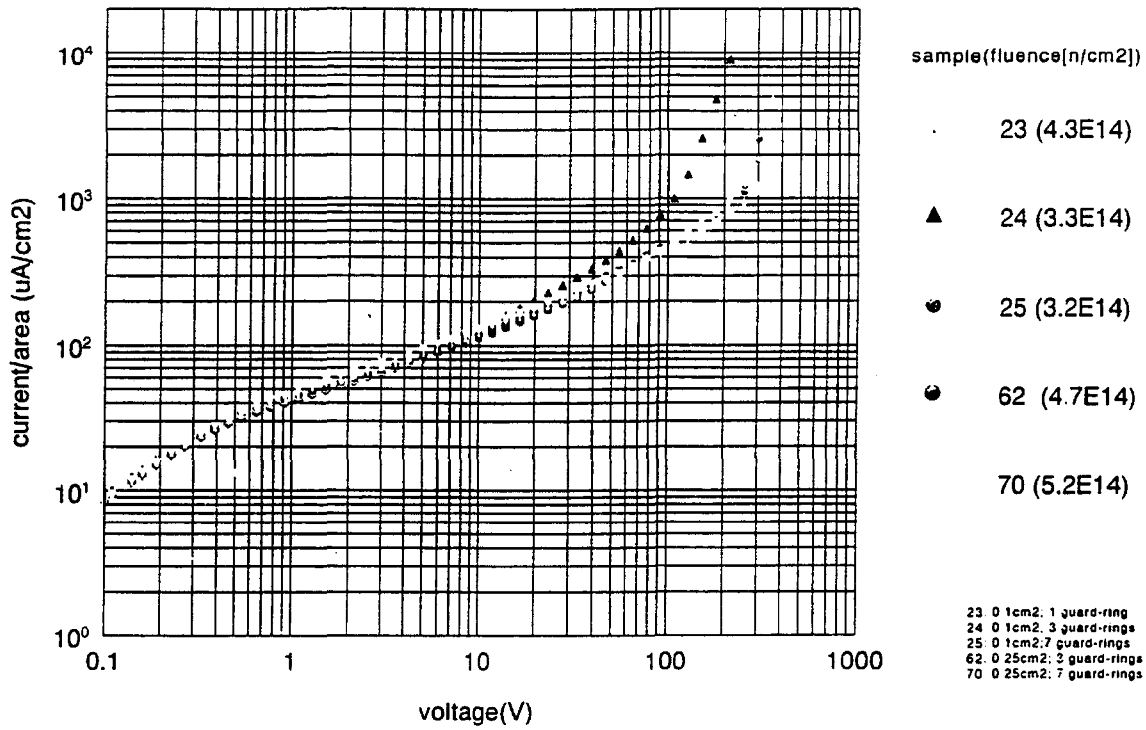
Evaluation test of p-i-n array wafer # 742 (after laser cut)

Array # on wafer	Saturated current (nA)	Bias at Ir=1uA (V)	Breakdown voltage (V)
15	400	50	350
16	no	30	90
17	100	70	210
23	no	40	420
24	no	40	250
25	no	20	260
28	1000	10	260
32	30	140	350
33	250	90	260
34	25	60	260
35	no	170	300
36	50	190	300
37	no	30	360
41	15	65	420
42	1.5	55	360
43	20	130	300
44	no	[illegible]	210
45	100	140	300
46	30	160	300
51	300	220	500
52	1000	14	300
53	no	220	300
54	10	60	210
55	no	[illegible]	300
56	no	[illegible]	300
57	100	[illegible]	500
61	20	[illegible]	420
62	20	[illegible]	420
63	no	[illegible]	410
64	no	[illegible]	300
65	no	100	360
66	no	200	200
67	400	160	360
70	4	200	500
71	20	95	370
72	no	26	210
73	no	90	210
74	1	62	90
75	no	37	160
76	4	37	100
77	80	130	250

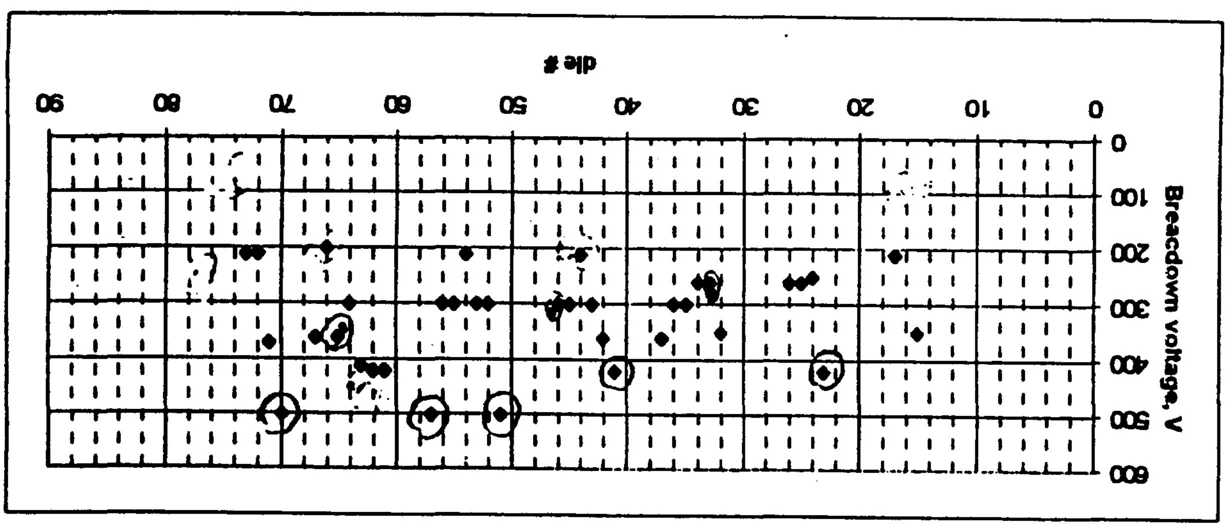


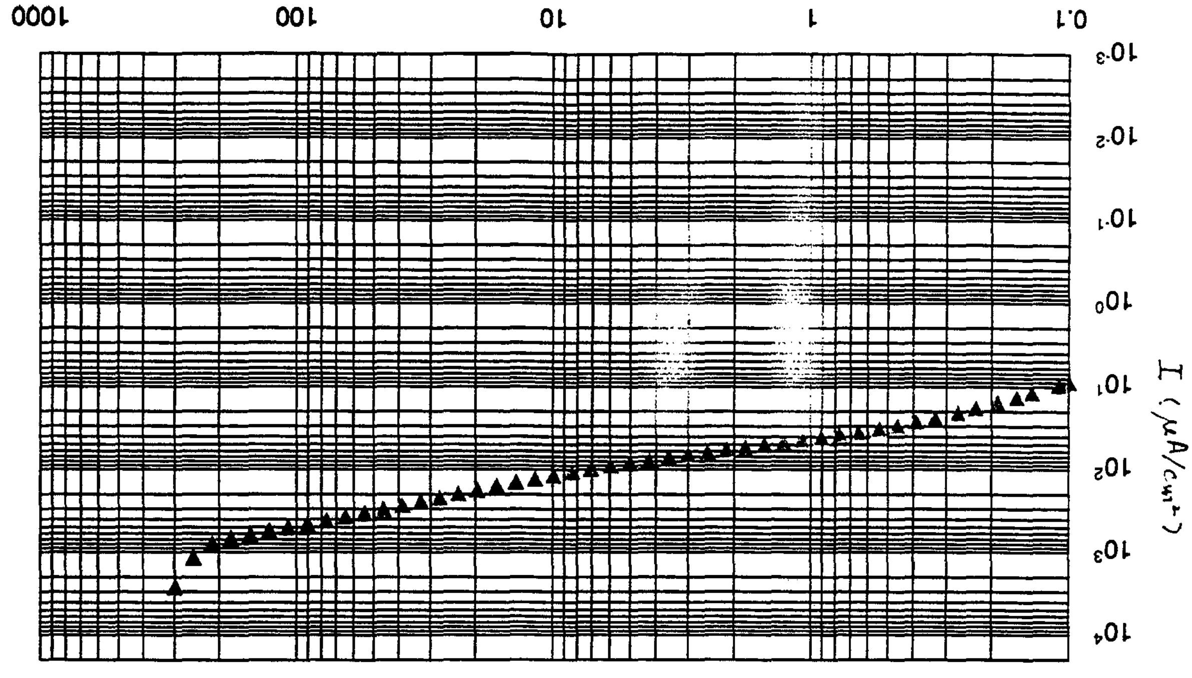
WAFER 742- n+/n/p+ TEST STRUCTURES

W=200um; r=1.6K(ohm)cm



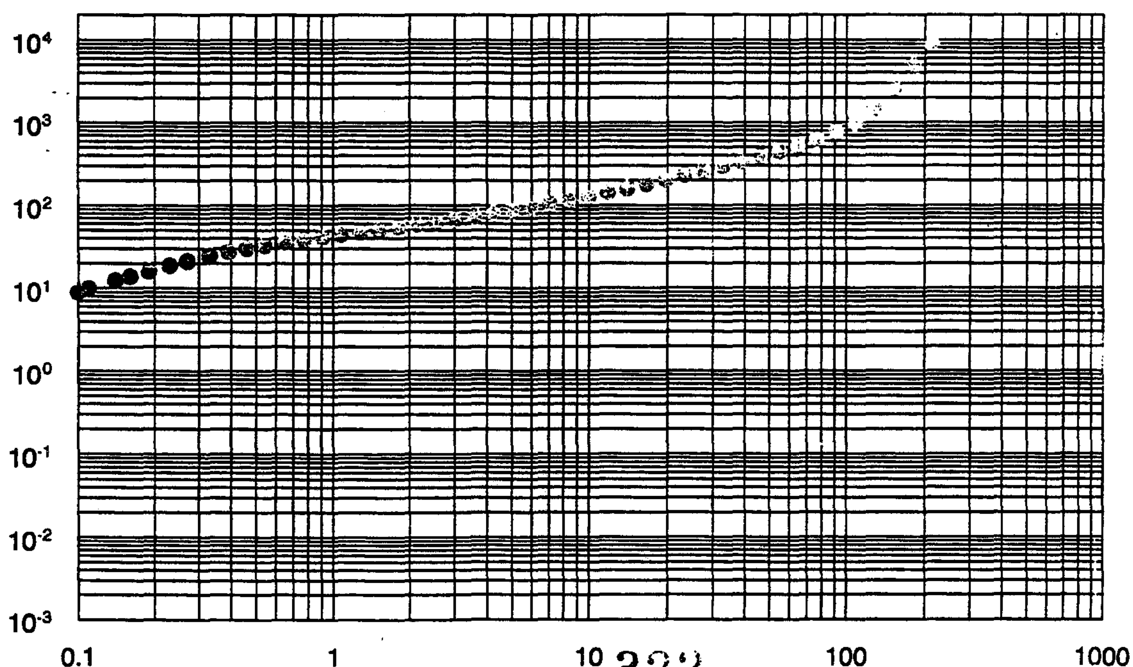
file 742irriv.tc

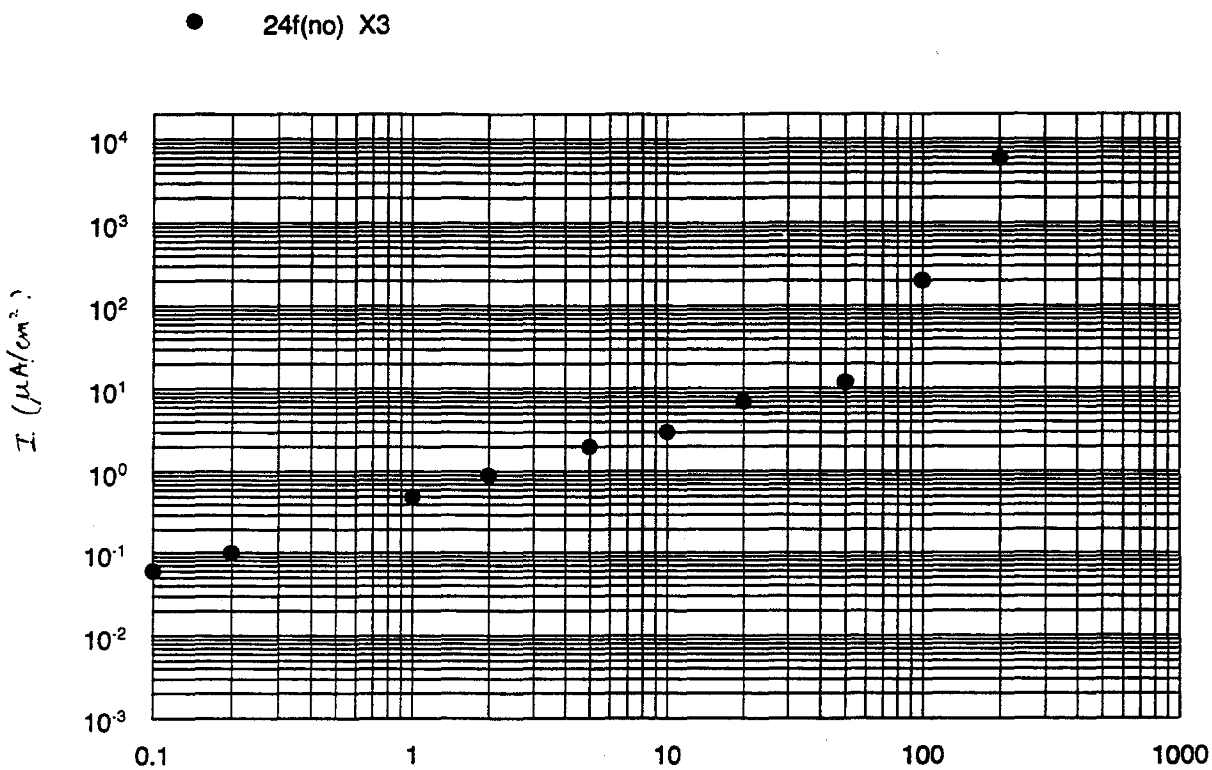




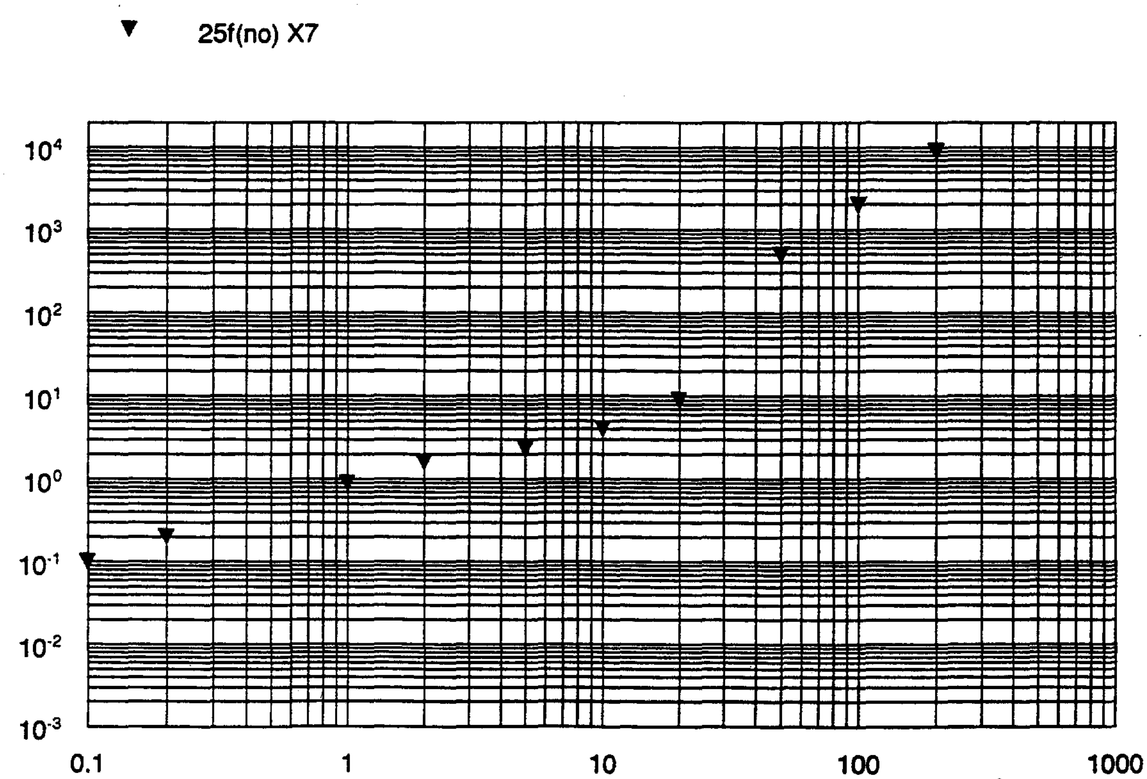
▲ 25(3.2E14) X7

● 24(3.3E14) X3





C:\DOWNLOAD\PROJECT\A2.TC



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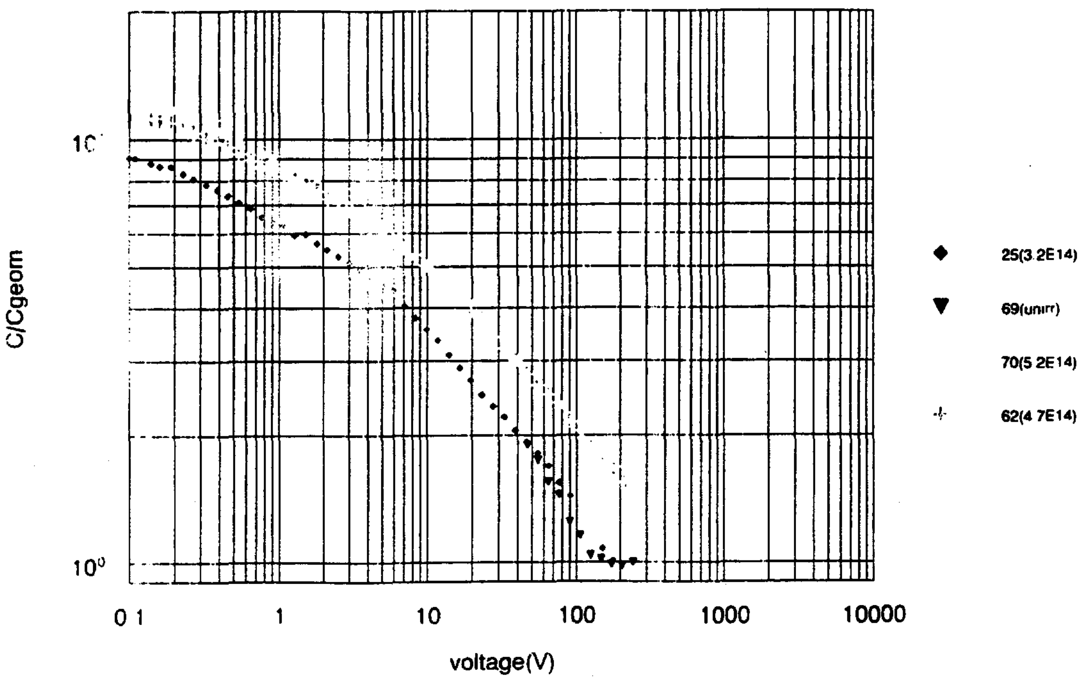
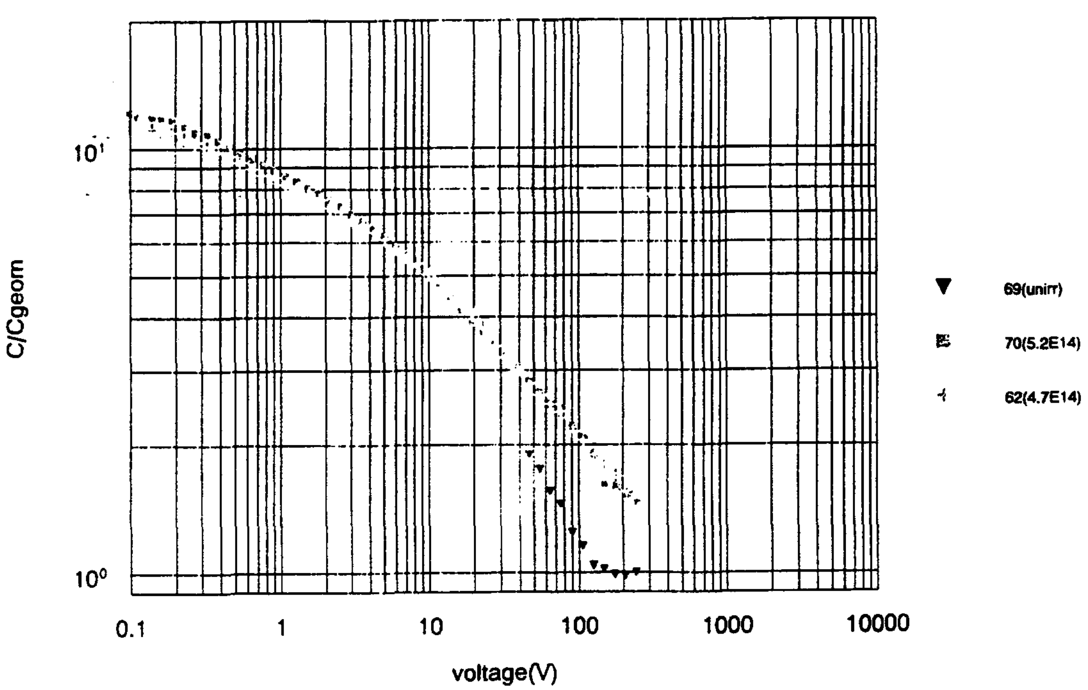
WAFER 742- TEST STRUCTURES

file 742cv.tc



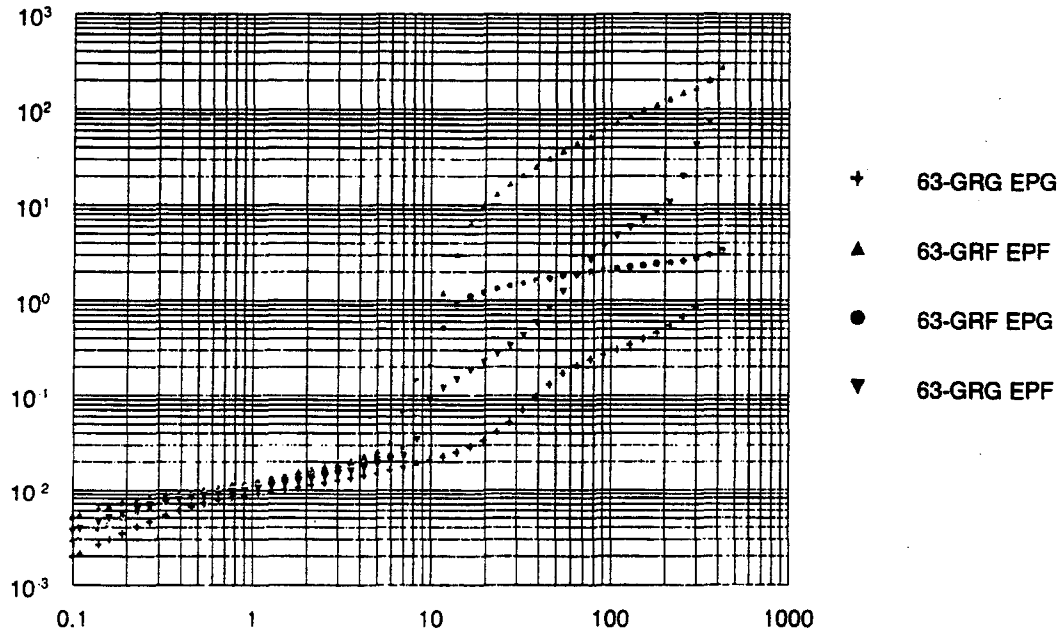
WAFER 742- TEST STRUCTURES

file 742cv.tc



SAMPLE 742-63;n+/n/p+ single pixel

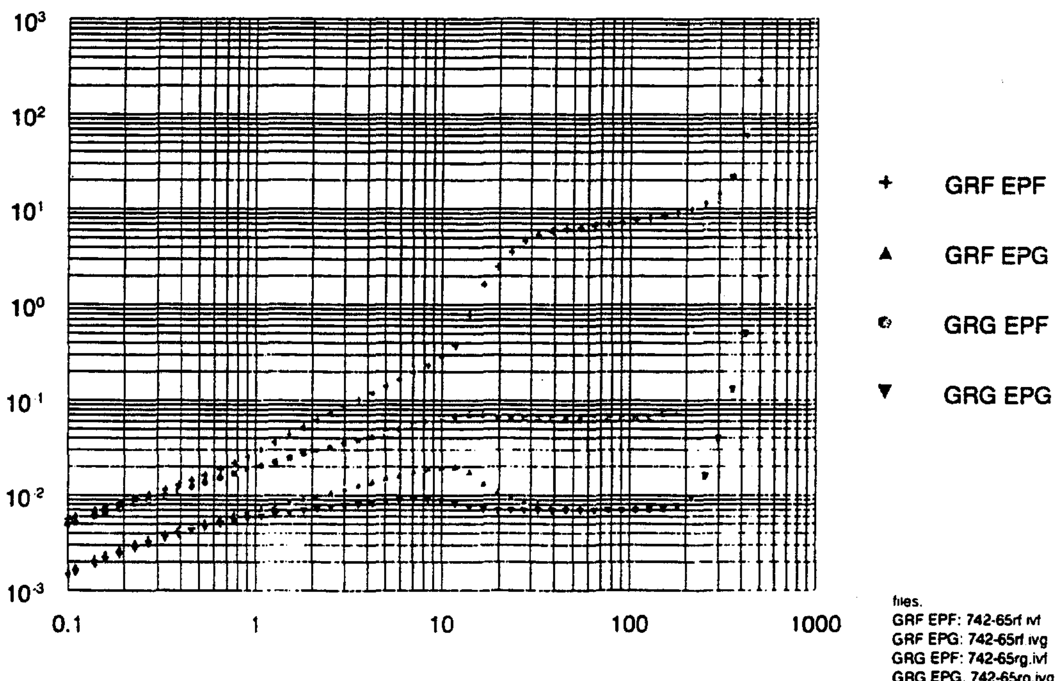
W=200um; r=1.9Kohm*cm



file 74263iv.tc

SAMPLE 742-65;n+/n/p+ single pixel

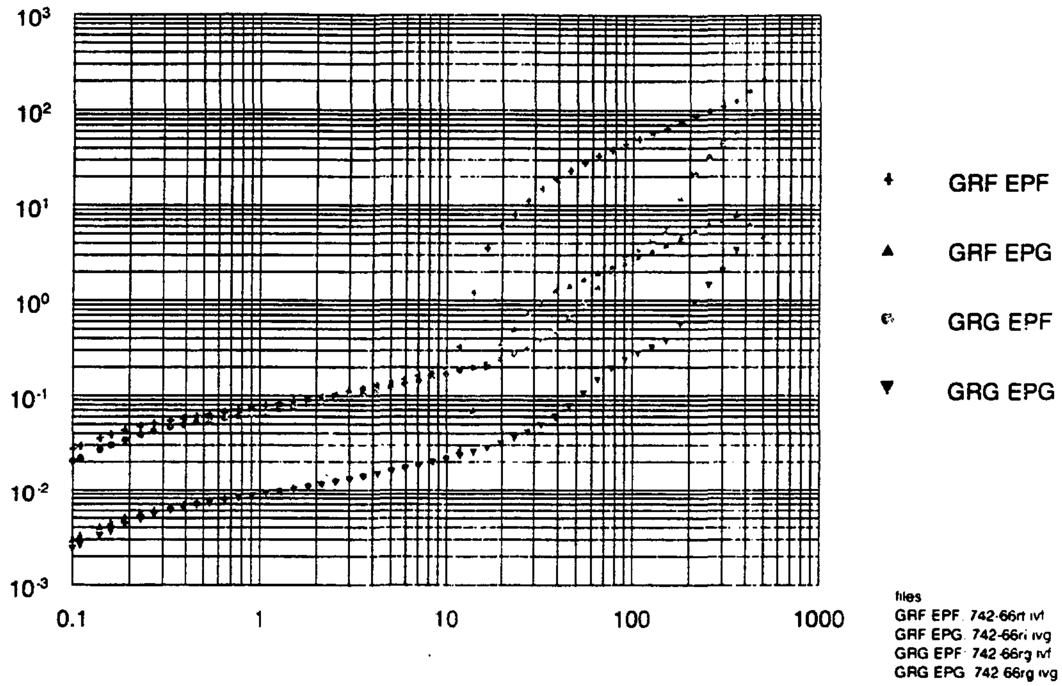
W=200um;r=1.9Kohm*cm;fluence=1.4e14n/cm2



file 74265iv.tc

SAMPLE 742-66;n+/n/p+ single pixel

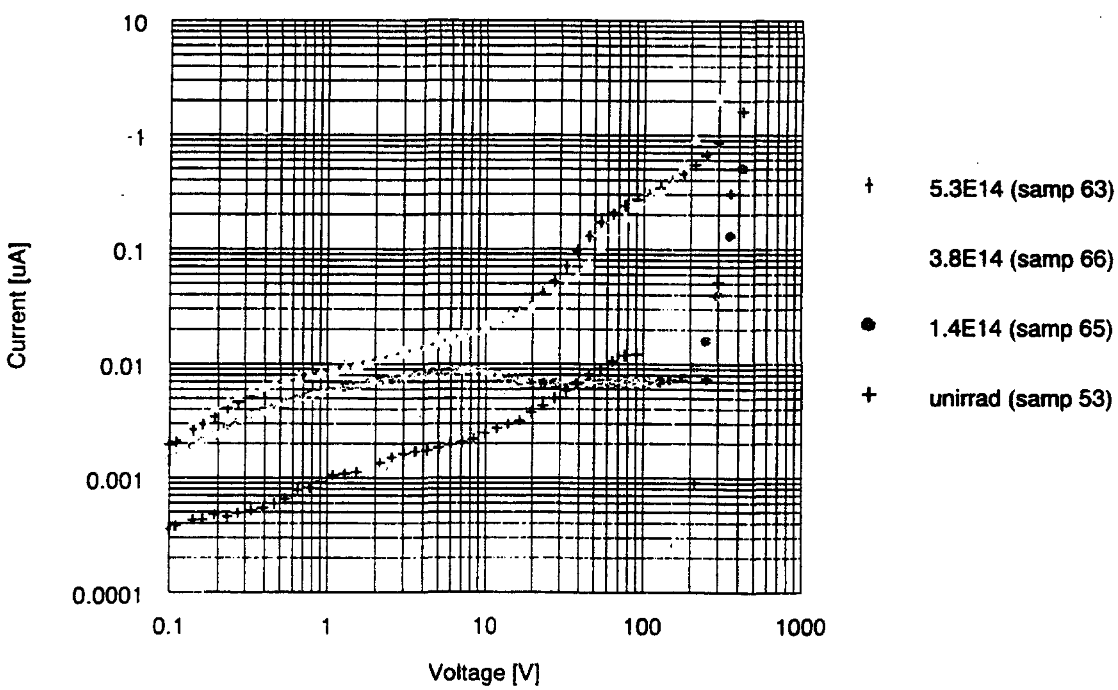
W=200um;r=1.9Kohm*cm;fluence=3.8e14n/cm2



file 74266iv.tc

Wafer 742- n+/n/p+ single pixels

r = 1.9 kOhm cm (all guard rings grounde



Progress in 1997

We have learned the following,

* 200-250 micron wafers have been processed ,
* medium resistivity is more radiation hardened than standard high resistivity,
* 5-7guardrings can operate to 300V without BD, even after radiation.
* number of guardrings changes breakdown voltage, but not leakage current,
* radiation raises leakage current, but not breakdown voltage,
* comparison with p+nn+ with identical designs, suggests BD due to p-stops
* more than 7 guardrings does not help, probably due to the same reason

Improvement for1998

- low resistivity wafers(500 Ohm-cm)
- refined field plates.
- concentrate on 5-9 GRs
- details at corners, and spacing,
- improvement in processing:
- double-side protection during processing,
  new inspection stage and light,
  improved clean-room and water system,
  improved field plates,
- new power supply to 1 kV for characterization.

Summary

Results in 1998 identified a design of guard rings being able to operate to 300V without breakdown, before and after irradiation, with tolerable leakage current.

Facilities have been improved, and factors have been identified to improve designs to produce sensors with breakdown above 500V while keeping leakage current low.

Prototype & Production

- begin with 24x32 arrays
- then 53 x 52 arrays
- 5 different sizes:
  ~0.9 x1.7 cm to
  ~1.7 x 4.1 cm
- one 4"-wafer for each blade
- pre-series
- production
- testing

1998-99 Plan

Mar: wafers processed with revised field plates
Mar 12: Initial FY98 funds allocated.
Mar 18: worked out FY98 plan with BNL.
May 20: Lehman Review II.
May-June: simulation and design
    design 24x32 125x125μ pixel arrays
July: masks produced, processing starts at BNL
Sep: processing complete.
Oct-Nov: dicing and testing,
    prepare FY99 prototype work w/ vendors.

1999
Complete work for multi-guardring R&D
Design 52x53 150x150μ pixel arrays
Submit designs to commercial foundry as soon as FY99 funds is allocated.
Tests sensor arrays.
Prepare for sensor prototype work.

2000 Apr 01: GR and pixel arrays R&D done
    prototype begins

2001 Aug 01: Preseries ordered.
    Dec 01: Testing preseries.

2002 Apr: Production wafers ordered.
    Sep: production wafers delivery begins, lasts for 12 mo.
    Oct: sensor acceptance tests begins, lasts for 12 mo.
    Nov: pipeline delivery of sensors to FNAL for assembly begins installation of sensors to blades begin at FNAL, for 12 mo.

2003 Oct: delivery of tested sensors to FNAL complete.

Pixel '98 Workshop
Fermilab, 05/08/98

Breakdown characterization of $n^+/p/p^+$ multiguarded diodes

G. Bolla*, D. Bortoletto.
Department of physics, Purdue University,
1396 Physics Bldg. West Lafayette 47907 IN, USA.
email: bolla@fnal.gov

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G.P. Grim, R.L. Lander, and D.E. Pellett.
Dept. of Physics, University of California, Davis,
Davis, CA 95161, USA.

[redacted] National Laboratory

Zheng Li.
Brookhaven National Laboratory,
PO Box 5000, Upton, NY 11973-5000, USA.

Abstract

Single sided, multiguarded, $n^+/p/p^+$ PIN diodes have been processed at BNL with high resistivity silicon. Various designs, from one to eleven guardrings, with alternating p-stops have been characterized at Purdue University to evaluate the $n^+/p/p^+$ technology as a candidate single side substitute to the usual double sided $p^+/n/n^+$ or $n^+/n/p^+$ devices. Exposure to 67 *Mev* p^+, integrated fluence of 3.2 10^{14} p^+/cm^2 has been performed at the UC Davis Crocker Nuclear Laboratory and the response to irradiation is compared with the preirradiation performances.

p-type versus n-type substrate

- At high fluences:

$$\mathrm{Vdep} \propto |\mathrm{Neff}| \propto \Phi$$

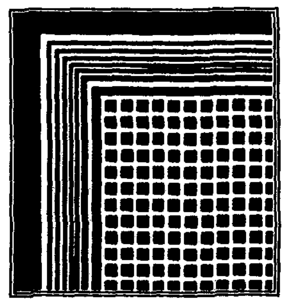
- No type inversion ↑

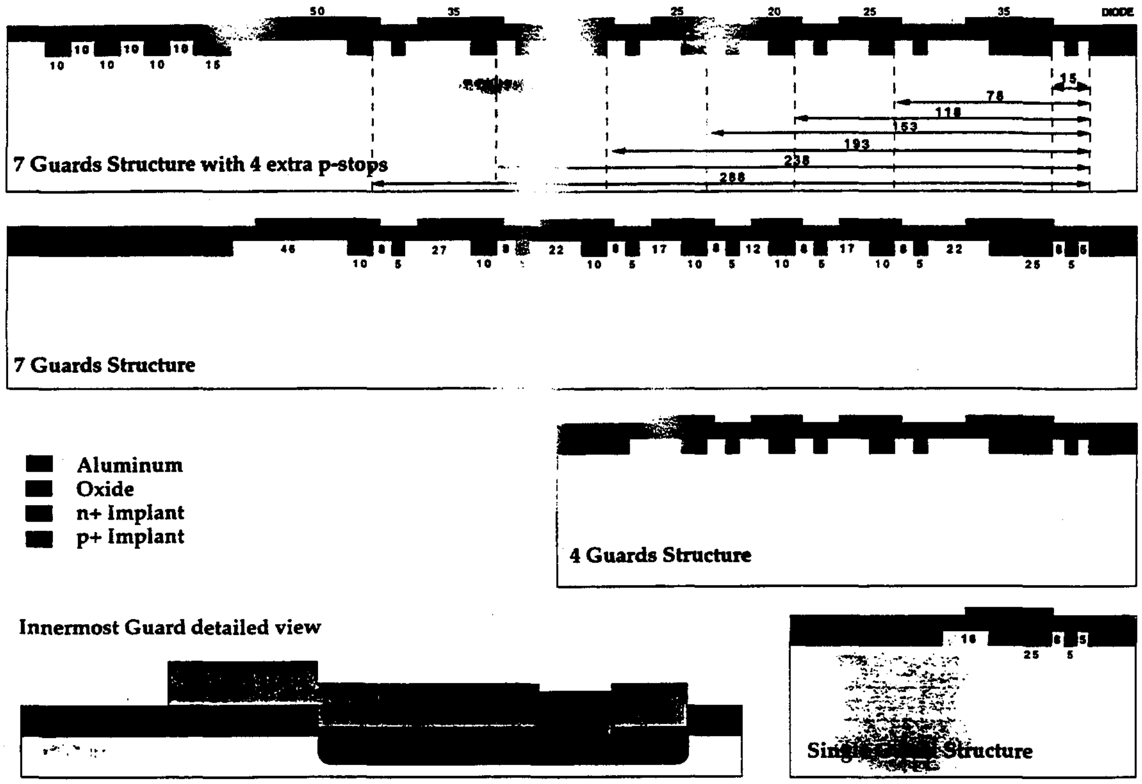
- Can be single sided ↑

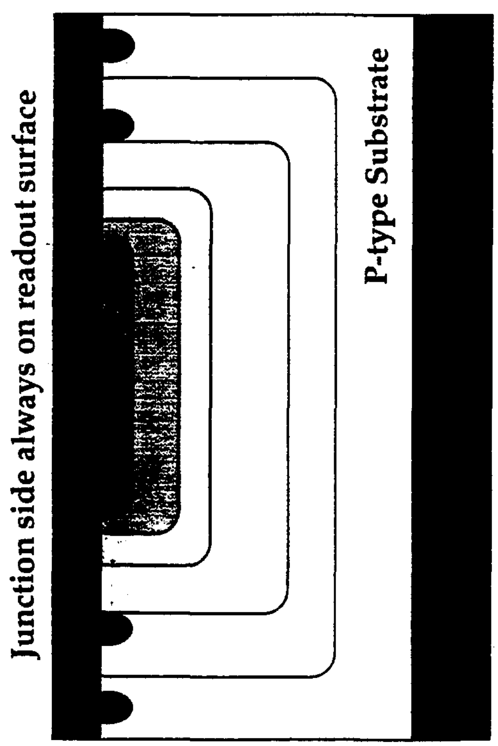
Cheaper

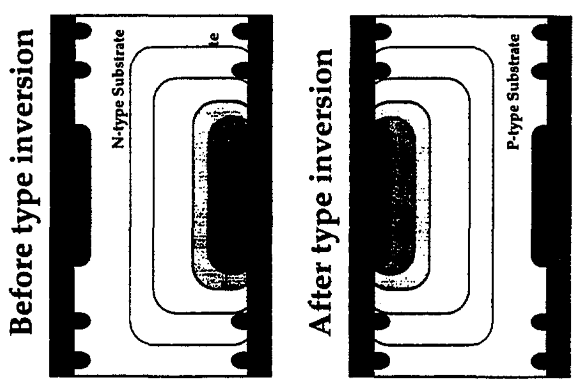
- Availability of starting material ↓

Four different Multiguarded Diodes have been designed and fabricated at BNL. Tested before and after dicing they have been irradiated up to an integrated fluence of 3.2 10^{14} p+/cm^2 with 67 MeV protons and retested.




DIODE
7 Guards Structure with 4 extra p-stops
7 Guards Structure
Aluminum
Oxide
n+ Implant
p+ Implant
4 Guards Structure
Innermost Guard detailed view


Junction side always on readout surface
P-type Substrate


Before type inversion
N-type Substrate
After type inversion
P-type Substrate

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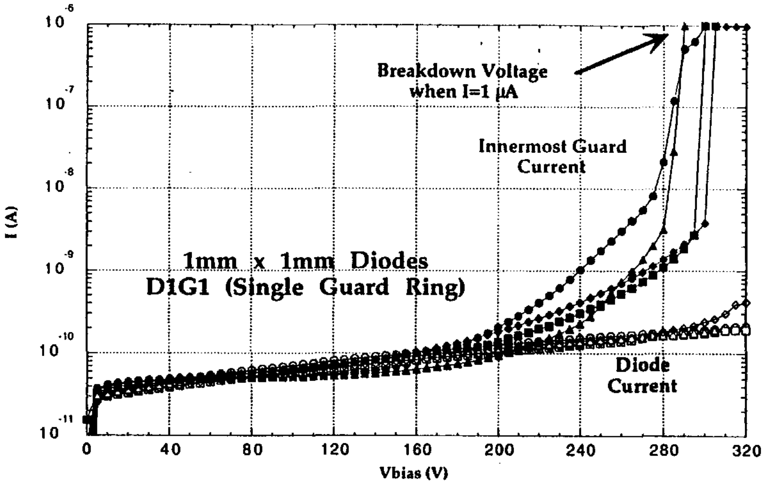

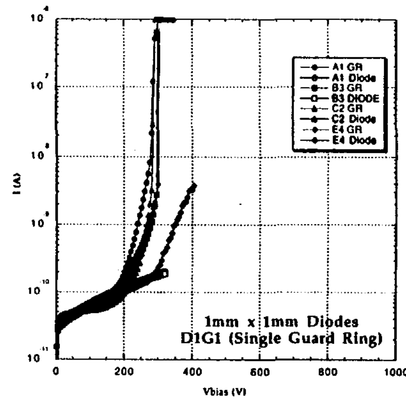

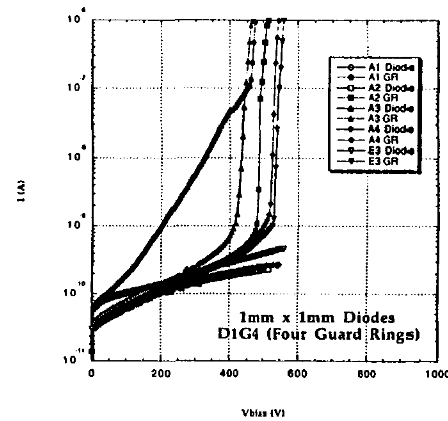

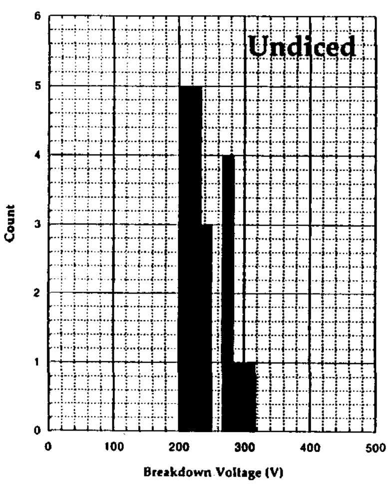

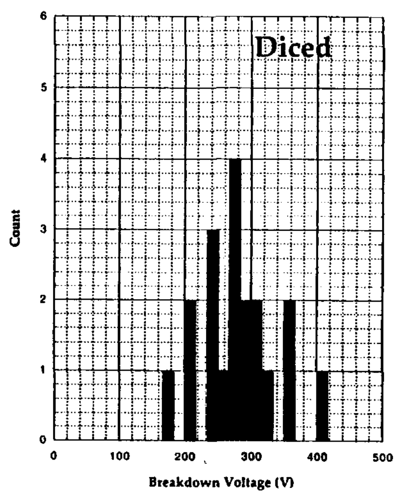

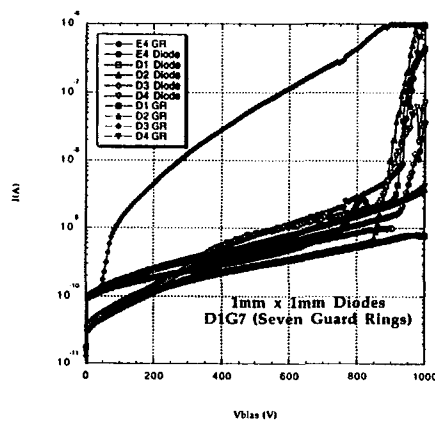

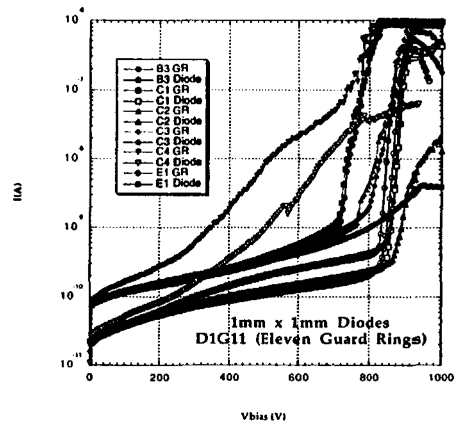

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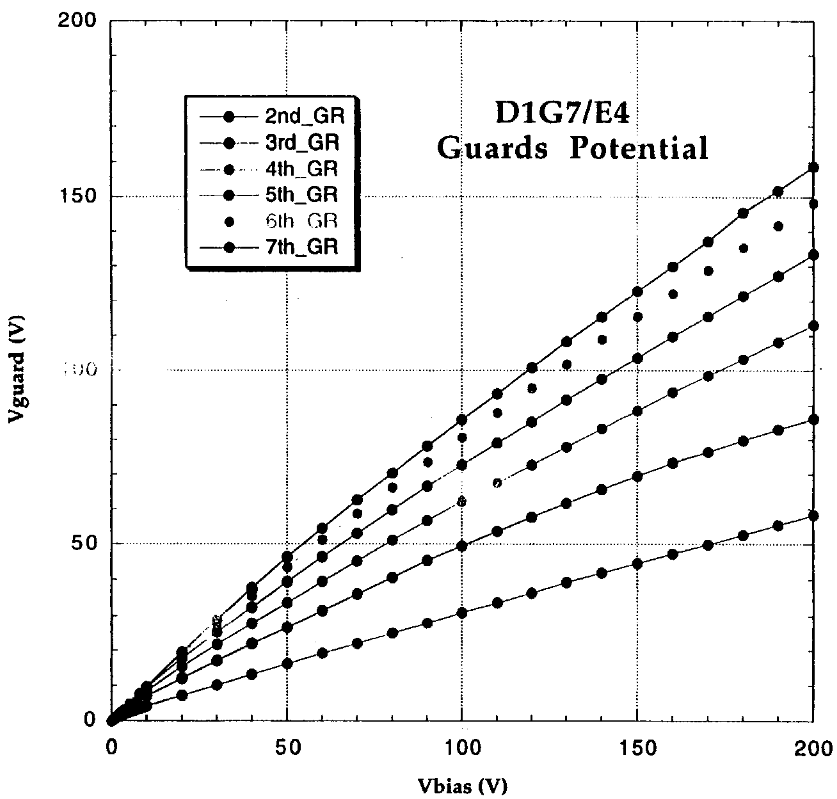

Irradiate at UCD Cyclotron

- 62.5 MeV proton kinetic energy
  - Well instrumented radiation damage test beam set up by UCD and Naval Research Laboratory
  - Fluence monitored to 10% accuracy using SEM calibrated by Faraday cup
  - Profile approx. uniform over 7 cm dia.
    - Beam profile well-measured by several techniques
  - Dose rate was 2.3 Krad (Si)/s
  - Total Dose was 27 Mrad (Si), ~2 × effective dose at CMS pixels
- **Surface charge effects**
  - Scale like ionization dE/dx
  - approx. 6x minI
- **Bulk damage effects** (should not be important here ...)
  - Scale like non-ionizing energy loss (NIEL)
  - approx. 2x minI proton
- **Irradiate under bias**
  - Vds = Vgs = 1 V (nmos)
  - Vds = Vgs = -1 V (pmos)
  - done in argon atmosphere

"Improved" process

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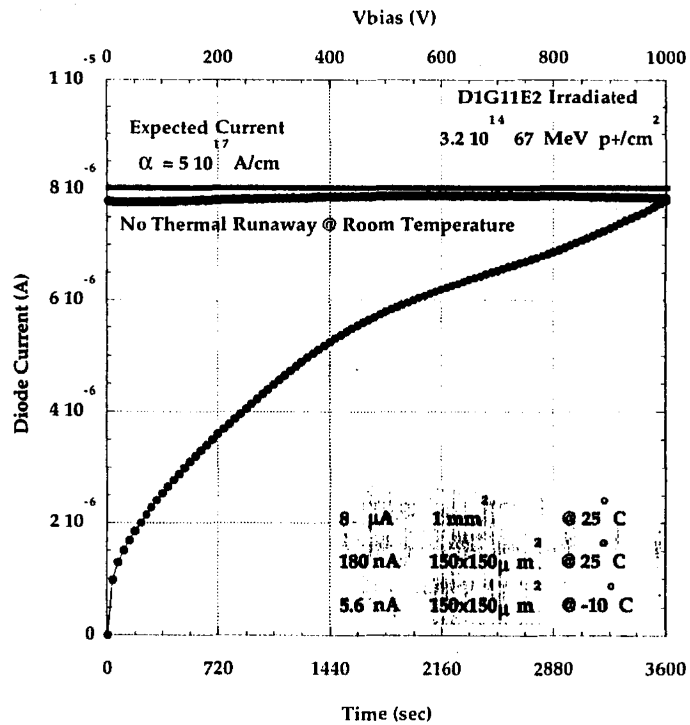
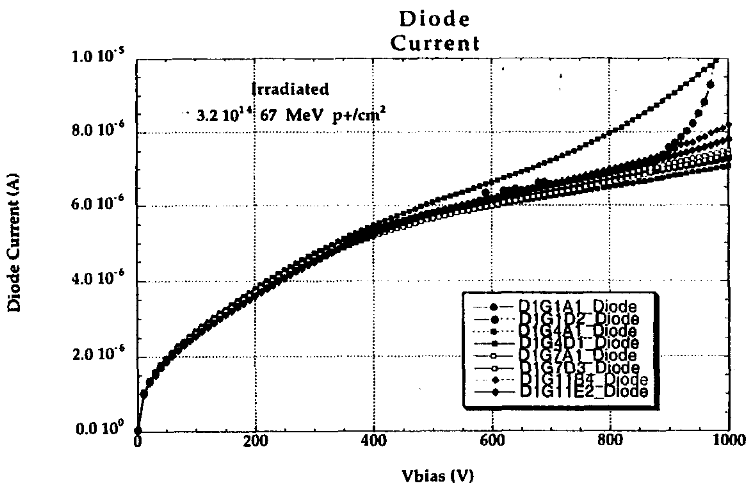
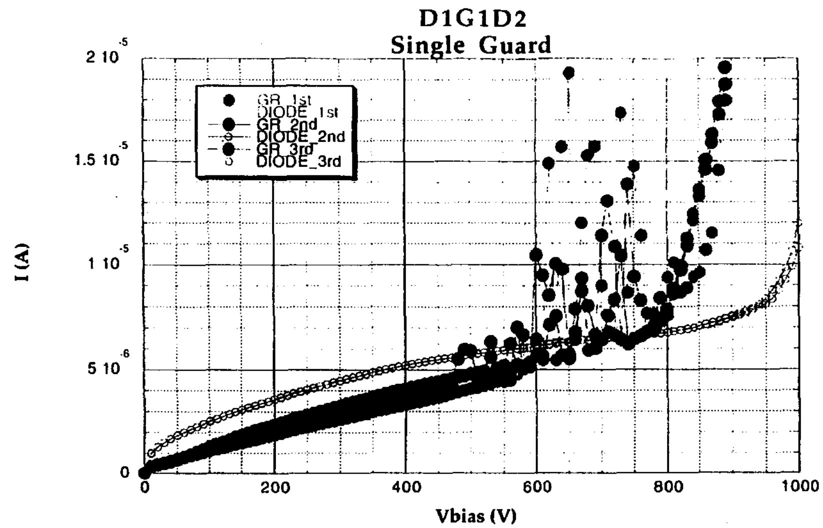
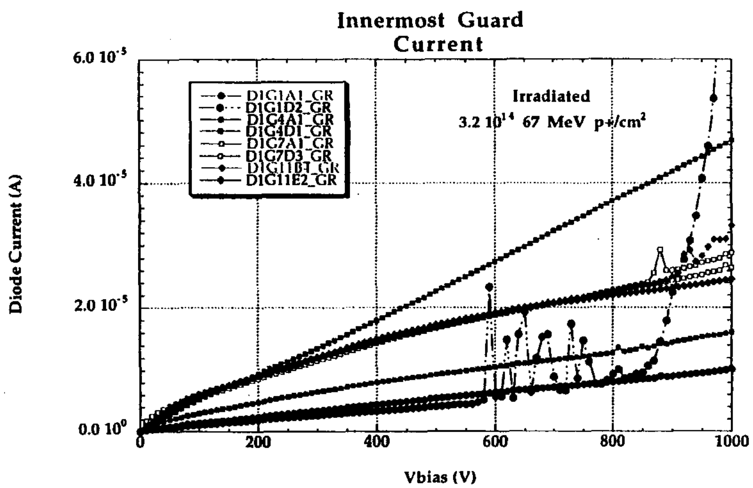
Storage

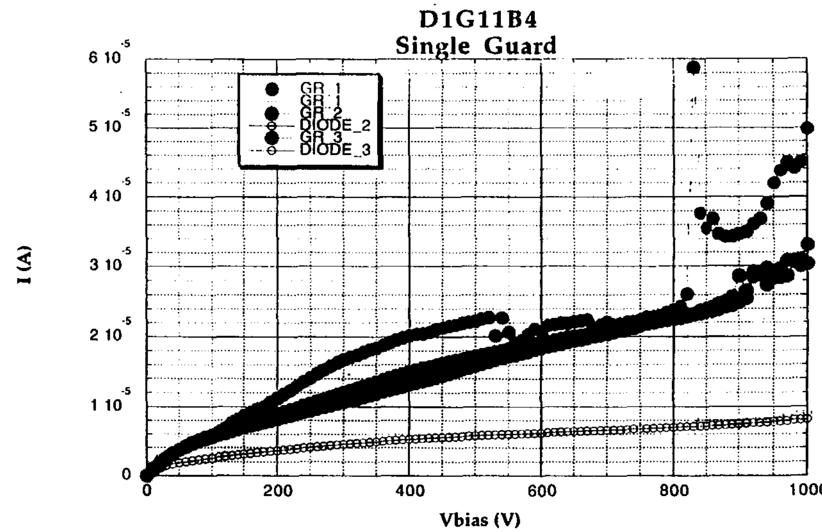
- Pre-radiation, storage at room temperature
- During radiation, 3 hrs at room temperature
- Post radiation, storage at -20C for approximately 11 days
- After 11 days at -20C, the diodes spent ~60 hours at ~3C
- This was followed by ~80 hours @ -20C
- May 1st: Shipped to Purdue Fed-Ex taped to a Blue-Ice Pack ?
- Storage @ -5C.
- 2 hours @ room temperature for probing
- 1 day @ room temperature (Silver Epoxy to cure)

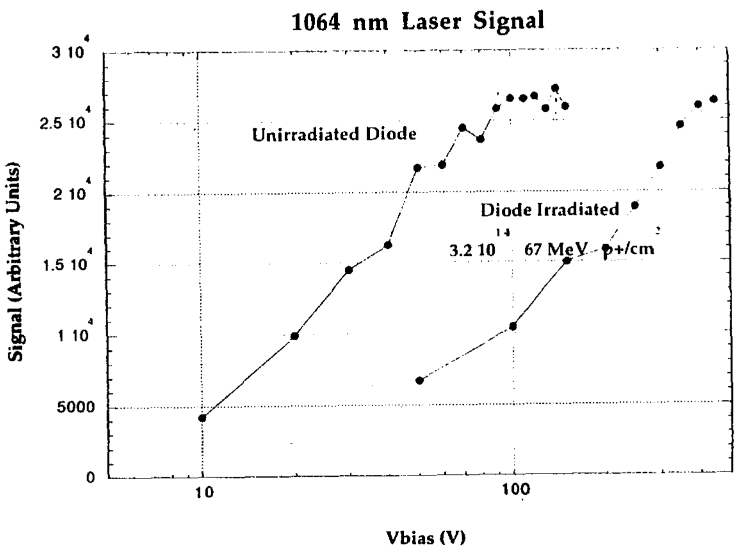


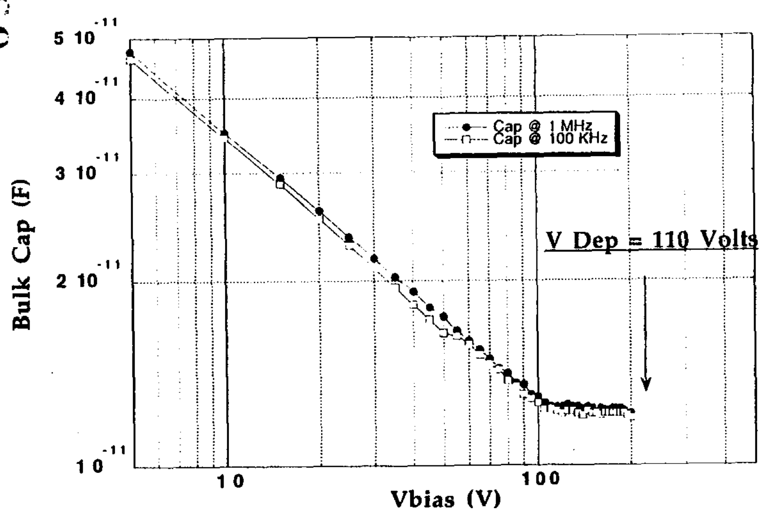

Diode
Current
Irradiated
3.2 10^14 67 MeV p+/cm^2
Diode Current (A)
1.0 10^-5
8.0 10^-6
6.0 10^-6
4.0 10^-6
2.0 10^-6
0.0 10^0
0
200
400
600
800
1000
Vbias (V)
D1G1A1_Diode
D1G1D2_Diode
D1G4A1_Diode
D1G4D1_Diode
D1G7A1_Diode
D1G7D3_Diode
D1G11B4_Diode
D1G11E2_Diode


D1G1D2
Single Guard
I (A)
2 10^-5
1.5 10^-5
1 10^-5
5 10^-6
0
0
200
400
600
800
1000
Vbias (V)
GR_1st
DIODE_1st
GR_2nd
DIODE_2nd
GR_3rd
DIODE_3rd


Innermost Guard
Current
Irradiated
3.2 10^14 67 MeV p+/cm^2
Diode Current (A)
6.0 10^-5
4.0 10^-5
2.0 10^-5
0.0 10^0
0
200
400
600
800
1000
Vbias (V)
D1G1A1_GR
D1G1D2_GR
D1G4A1_GR
D1G4D1_GR
D1G7A1_GR
D1G7D3_GR
D1G11B4_GR
D1G11E2_GR


D1G11B4
Single Guard
I (A)
6 10^-5
5 10^-5
4 10^-5
3 10^-5
2 10^-5
1 10^-5
0
0
200
400
600
800
1000
Vbias (V)
GR_1
GR_1
GR_2
DIODE_2
GR_3
DIODE_3





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Future

- Annealing effects
- Gamma Irradiation
- More statistic
- Larger devices
- Bumpbonded pixels Arrays

Conclusions

- <u>Multiguard Structure that works!</u>
- <u>Radiation hardeness inside LHC requirements</u>

Recent Results of Radiation Hardness Studies on CVD Diamond Detectors

W. Adam[1], C. Bauer[2], E. Berdermann[3], P. Bergonzo[4], F. Bogani[5], E. Borchi[6], A. Brambilla[4], M. Bruzzi[6], C. Colledani[7], J. Conway[8], W. Dabrowski[9], P. Delpierre[10], A. Deneuville[11], W. Dulinski[7], B. van Eijk[12], A. Fallou[10], F. Fizzotti[13], F. Foulon[4], M. Friedl[1], K.K. Gan[14], E. Gheeraert[11], E. Grigoriev[9], G. Hallewell[10], R. Hall-Wilton[15], S. Han[14], F. Hartjes[12], J. Hrubec[1], D. Husson[7], H. Kagan[14], D. Kania[14], J. Kaplon[9], C. Karl[16], R. Kass[14], K.T. Knöpfle[2], M. Krammer[1], A. Logiudice[13], R. Lu[13], P.F. Manfredi[17], C. Manfredotti[13], R.D. Marshall[4], D. Meier[9], M. Mishina[18], F. LeNormand[7], A. Oh[16], L.S. Pan[14], V.G. Palmieri[19], H. Pernegger[1], M. Pernicka[1], A. Peitz[8], S. Pirollo[6], P. Polesello[13], K. Pretzl[19], V. Re[17], J.L. Riester[7], S. Roe[9], D. Roff[15], A. Rudge[9], S. Schnetzer[8], S. Sciortino[6], V. Speziali[17], H. Stelzer[3], J. Steuerer[16], R. Stone[8,22], R.J. Tapper[15], R. Tesarek[8], G.B. Thomson[8], M. Trawick[14], W. Trischuk[20], R. Turchetta[7], E. Vittone[13], A. Wagner[16], A.M. Walsh[8], R. Wedenig[9], P. Weilhammer[9], W. Zeuner[16], H. Ziock[21], M. Zoeller[14]

The RD42 Collaboration

[1] Institut für Hochenergiephysik der Österr. Akademie d. Wissenschaften, A-1050 Vienna, Austria
[2] MPI für Kernphysik, D-69029 Heidelberg, Germany
[3] GSI, Darmstadt, Germany
[4] LETI (CEA-Technologies Avancees) DEIN/SPE - CEA Saclay, 91191 Gif-Sur-Yvette, France
[5] LENS, Florence, Italy
[6] University of Florence, Florence, Italy
[7] LEPSI, CRN, Strasbourg 67037, France
[8] Rutgers University, Piscataway, NJ 08855, U.S.A.
[9] CERN, CH-1211, Geneva 23, Switzerland
[10] CPPM, Marseille 13288, France
[11] LEPES, Grenoble, France
[12] NIKHEF, Amsterdam, Netherlands
[13] Univerity of Torino, Italy
[14] The Ohio State University, Columbus, OH 43210, U.S.A.
[15] Bristol University, Bristol BS8 1TL, U.K.
[16] DESY, Hamburg, Germany
[17] Universita di Pavia, Dipartimento di Elettronica, 27100 Pavia, Italy
[18] FNAL, Batavia, U.S.A.
[19] Lab. für Hochenergiephysik, 3012 Bern, Switzerland
[20] University of Toronto, Toronto, ON M5S 1A7, Canada
[21] Los Alamos National Laboratory, Research Division, Los Alamos, NM 87545, U.S.A.

Abstract

The inherent properties of diamond are well suited for use in tracking detectors, especially in the high rate and high radiation environments of future colliders such as the LHC. To survive in this environment, detectors must be radiation hard. In order to demonstrate the radiation hardness of CVD diamond, we exposed samples to large fluences of 300 MeV pions, 500 MeV and 24 GeV/c protons, and 1 MeV neutrons. The signal response to minimum ionizing particles is measured before and after irradiation. Results show that CVD diamond is an extremely radiation hard material and well suited for use in regions of highest radiation at the LHC.

[22]Presented Pixel 98 Talk

1 Overview of CVD Diamond Detectors

Tracking detectors in future high energy experiments will be exposed to increasingly higher levels of radiation. The potential damage to both the sensors and electronics caused by expected levels of radiation is in many cases exceeding current detector technology. A search for new sensor material which might be inherently radiation hard has yielded two candidates: gallium arsenide and chemical vapor deposited (CVD) diamond. We report here results from recent pion, neutron and proton irradiation studies on CVD diamond detectors.

Chemical vapor deposited (CVD) diamond is a polycrystalline, high band gap material. It tends to grow in a columnar structure where the grain size increases from the substrate (nucleation) side to the growth side. The charge collection efficiency is related to the grain size: it is close to zero near the substrate side and grows linearly to the growth-side surface[2]. To improve the average bulk charge collection efficiency, material from the substrate side can be polished away.

Table 1 lists some properties of CVD diamond in comparison to silicon. The most distinctive feature of diamond is its large band gap, 5.5 eV. This large band gap along with the associated large cohesive energy are responsible for much of the radiation hardness of diamond. The large band gap also makes diamond an excellent electrical insulator. As a result, a large electric field can be applied without producing significant leakage current. Thus, there is no need for a reverse biased *pn*-junction and the diamond detector functions much like a "solid-state" ionization chamber.

Although diamond appears ideal in many characteristics, it does have one limitation: its large band gap, which determines many of its outstanding properties, also makes the signal size about half that of silicon for an equivalent thickness in radiation lengths. On average, 3600 electron-hole pairs are created per 100 μm of diamond traversed by a minimum ionizing particle. The quality of current CVD diamond material does not allow the above limit of signal size to be achieved due, most likely, to imperfections in the the crystal lattices that cause the produced charge to become trapped before it is fully collected. Compensating for this loss of signal is diamond's lower dielectric constant and negligible leakage current: both of which tend to reduce frontend noise.

Prototype detectors using CVD diamond have been constructed. An electromagnetic calorimeter prototype using CVD diamond as the active sensor material has been built and tested in 1993[7]. Microstrip tracking detectors have also been constructed and tested by RD42[8]. Testing of a prototype pixel detector by RD42 is detailed elsewhere in these proceedings.

2 Characterization of Diamond Detectors

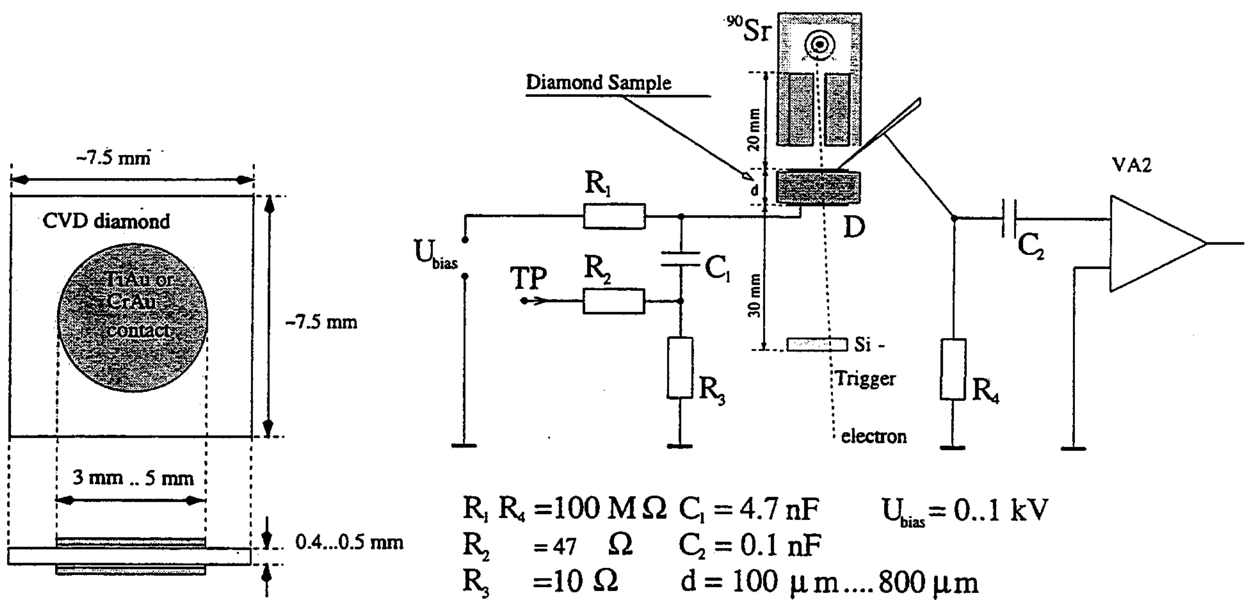
A simple and reliable method to characterize the charge collection efficiency of diamond detectors before and after each irradiation is needed to determine whether or not significant damage has occurred. Figure 1 shows such a system. As shown, a ^{90}Sr beta source

Property	Diamond	Silicon
Band Gap [eV]	5.5	1.12
Breakdown field [V/cm]	10^7	3×10^5
Resistivity [Ω-cm]	$> 10^{11}$	2.3×10^5
Intrinsic Carrier Density [cm^{-3}]	$< 10^3$	1.5×10^{10}
Electron Mobility [$cm^2V^{-1}s^{-1}$]	1800	1350
Hole Mobility [$cm^2V^{-1}s^{-1}$]	1200	480
Saturation Velocity [μm/ns]	220	82
Thermal Conductivity [W m^{-1} K^{-1}]	1000-2000	150
Dielectric Constant	5.6	11.9
Cohesive Energy [eV/atom]	7.37	4.63
Neutron Transmutation Cross Section [mb]	3.2	80
Energy to create e-h pair [eV]	13	3.6
Mass Density [gm/cm^3]	3.5	2.33
Ave Number of e-h Pairs Created/100 μm [e]	3600	7300

Table 1: Comparison of Properties of Diamond and Silicon[1]

is normally incident onto one diamond surface and a silicon diode trigger is placed on the opposite surface. With proper collimation most triggers result, on average, in a beta electron depositing approximately minimum ionizing energy through the bulk of the diamond. With electrodes placed on both surfaces and with a voltage (typically 1V/μm) applied, the electron-hole pairs produced move in opposite directions in response to the applied electric field. A signal can thus be measured using a charge-integrating amplifier.

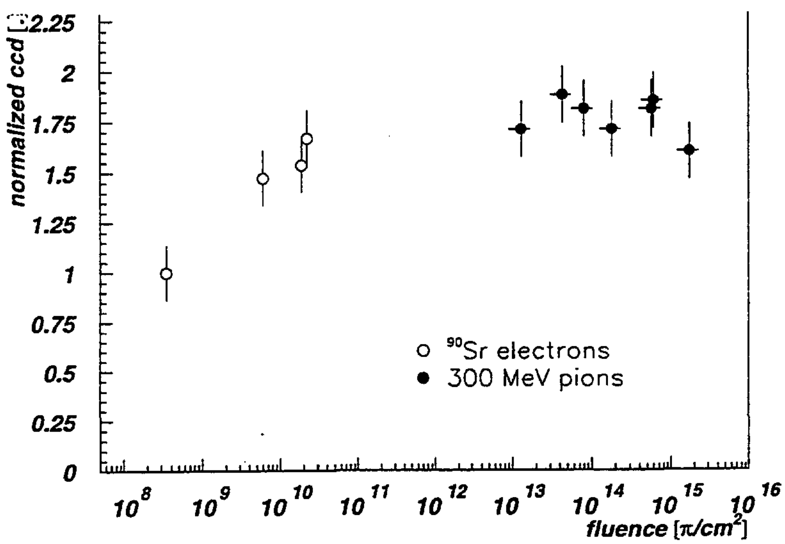
Figure: 1 ^{90}Sr Measurement System



3 Pion Irradiation Study

In 1994 and 1995, diamond detectors were irradiated with 300 MeV pions at PSI, in Villingen, Switzerland. A total fluence of 1.8 x $10^{15}\pi/\text{cm}^2$ was obtained over this period. The diamonds were kept at room temperature before, during and after irradiation. Figure 2 shows the results of the irradiation by comparing charge collection before and after irradiation using the ^{90}Sr characterization setup described above.

Figure 2: Pion Irradiation of CVD Diamond



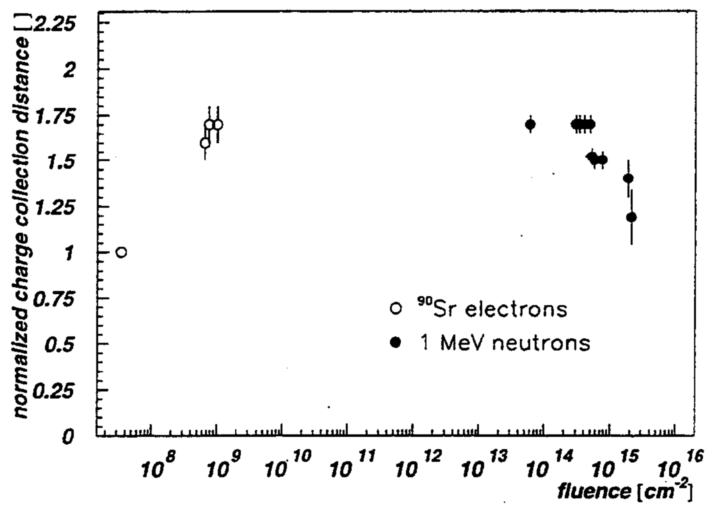
The diamond detectors studied have varying charge collection efficiencies, but are all shown normalized to 1, measured at the lowest fluence using ^{90}Sr. The four lowest fluence points are all taken using ^{90}Sr, prior to pion irradiation, and illustrate the "pumping" or increase in charge collection efficiency of diamond detectors with modest levels of ionizing irradiation. This pumping effect can be explained by the eventual filling or neutrallization of traps in the bulk diamond by the ionization from irradiation. Once a trap is filled it can no longer trap or impede the progress of the charge carriers as they move to the electrodes, thus increasing the effective collected charge. These traps stay neutrallized for extremely long periods of time (months) if the diamond are kept light-tight.

The points labled "300 MeV Pions" are mesurements performed using ^{90}Sr but "pumped" by the pion irradation to the given fluence. There is no significant degradation of the charge collection up to 1.8 x $10^{15}\pi/cm^2$.

4 Neutron Irradiation Study

Neutron irradiation studies have been carried out at the ISIS neutron spallation source at RAL, Chilton, UK. The source had two energy maxima: one below 10KeV and one of interest at 1 MeV. The study completed in 1996 achieved a fluence of 1.9 x $10^{15}n/\text{cm}^2$. All samples were biased at 100V to sample the beam induced current during irradiation and maintained at room temperature before, during and after irradiation.

Figure 3: Neutron Irradiation of CVD Diamond

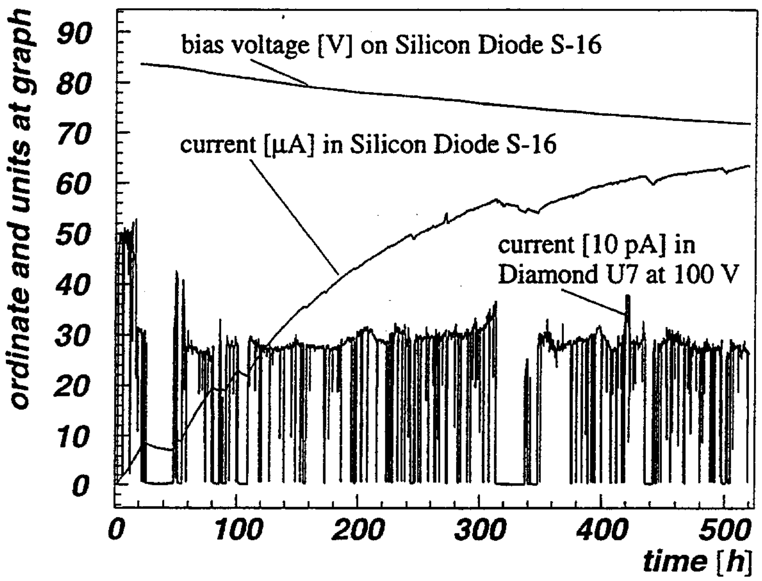


As shown in Figure 3 above, starting a little less than 10^{14} and up to 5 x $10^{15}n/\text{cm}^2$, the relative charge collection "pump-up" value agrees well with that for ^{90}Sr low fluence measurements. This pump-up is most likely due to a photon component in the beam. At 1.9 x 10^{15} n/cm^2 there is a 15% decrease in charge collection.

Figure 4 below shows the beam induced currents measured thougout the irradiation period. The current for diamond detector labeled U7 shows good correlation to the beam current structure (not shown), with clear periods of beam off at 20-50 hours and at 315-340 hours as well as many brief segments of beam instability.

For comparision, a silicon diode of comparable area was also irradiated and its current measured. As can be seen in Figure 4, the silicon diode current is two orders of magnitude higher than for the diamond detector and shows an increase in current throughout the irradiaton period. During the extended periods when the beam was off, the current decreases slightly (evidence of annealing) but does not return to the pre-irradiated value.

Figure 4: Neutron Beam Induced Current



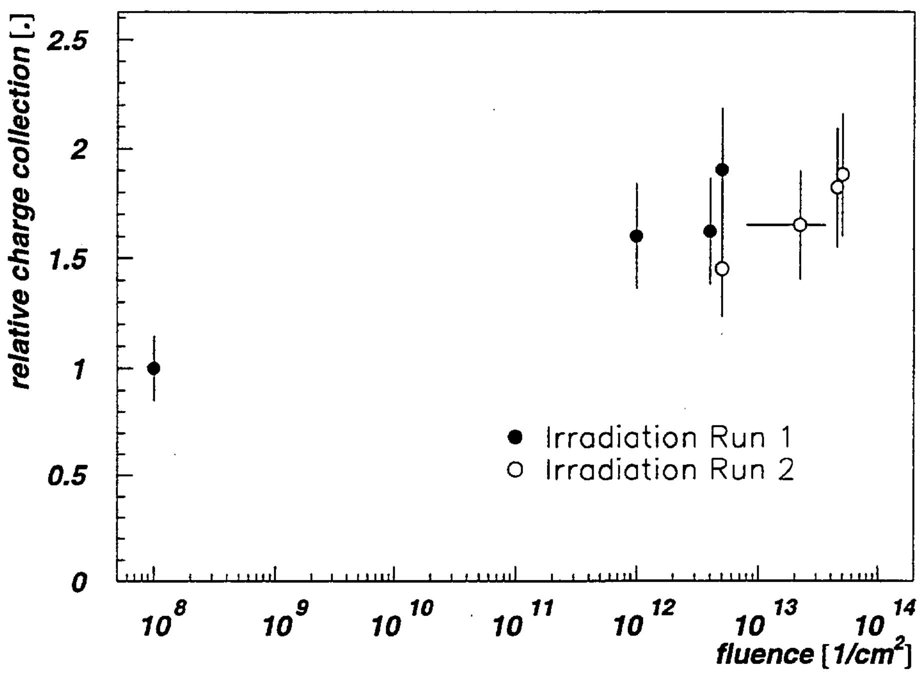
5 Proton Irradiation Studies

5.1 Triumf irradiation

A proton irradiaton study at Triumf was performed in 1994 and 1995. A fluence of 8 x $10^{13} p/cm^2$ was achieved using protons of 500 MeV kenetic energy with a flux of 8 x $10^8 p/cm^2/s$.

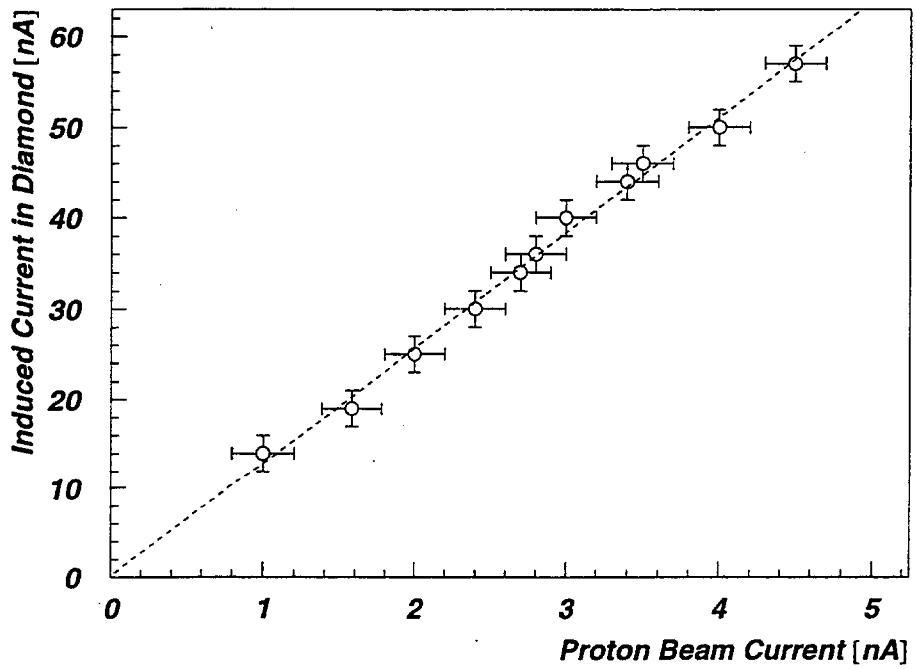
Figure 5 shows the charge collection efficiency of diamond detectors, again normalized to 1 at the lowest, unpumped ^{90}Sr fluence. A typical pump-up factor of 1.5 to 1.7 is evident for the measurments made after the high fluence irradiations with protons. Hence there is no apparent decrease in the charge collection efficiency up to the maximum fluence.

Figure 5: Triumf Proton Irradiation of CVD Diamond



The Triumf proton beam was continuous and the flux could be controlled between zero and 8 x $10^8 p/cm^2/s$. The flux was measured with an ionization chamber whose current was propostional to the flux. Figure 6 shows the beam induced current in one of the diamond detectors as a function of current in the ionization chamber. The linear response of the diamond current to the proton flux suggests that the charge collection efficiency of diamond is unchanged up to 8 x $10^8 p/cm^2/s$, which is equivalent to a 5 nA proton beam current and demonstrates the high rate capability of CVD diamond detectors.

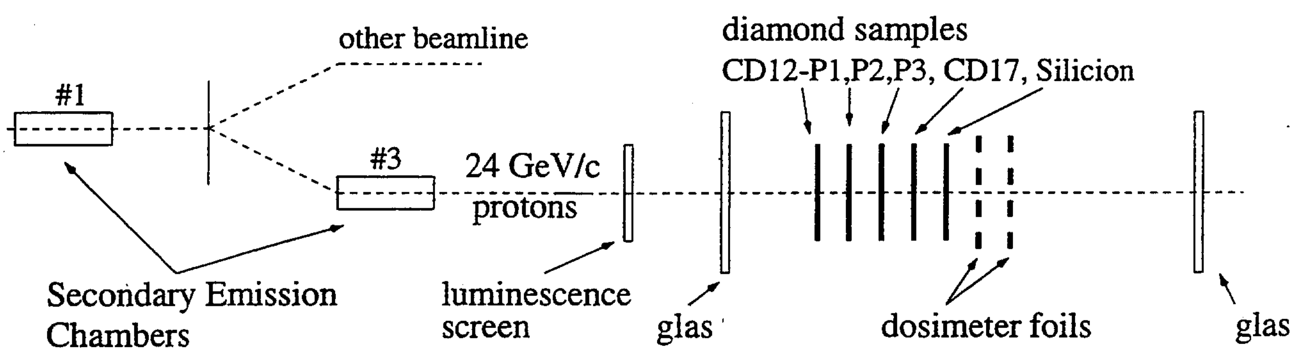
Figure 6: Triumf Beam Induced Current



5.2 CERN PS irradiation

In June of 1997, there was a 2 week irradiation at the PS at CERN in beamline T7. The beamline setup is shown below in Figure 7. A fluence of 5 x $10^{15} p/cm^2$ was achieved with an average flux of 2.9 x $10^{10} p/cm^2$/spill. A spill lasted 0.3 seconds, with two or three spill extractions in a 14 second accelerator cycle. The proton momemtum was 24.2 GeV/c.

Figure 7: CERN PS Beamline Setup



The proton flux was measured by two secondary emmission chambers. Proton fluence was determined by an aluminum foil activation method. The amount of ^{24}Na generated in the aluminum foil is proportional to the total fluence and can be determined by gamma spectroscopy. Figure 8 relates the integrated flux given by the two secondary emmission chambers to the Al foil dosimetry mesurements.

Figure 8: CERN PS Proton Fluence

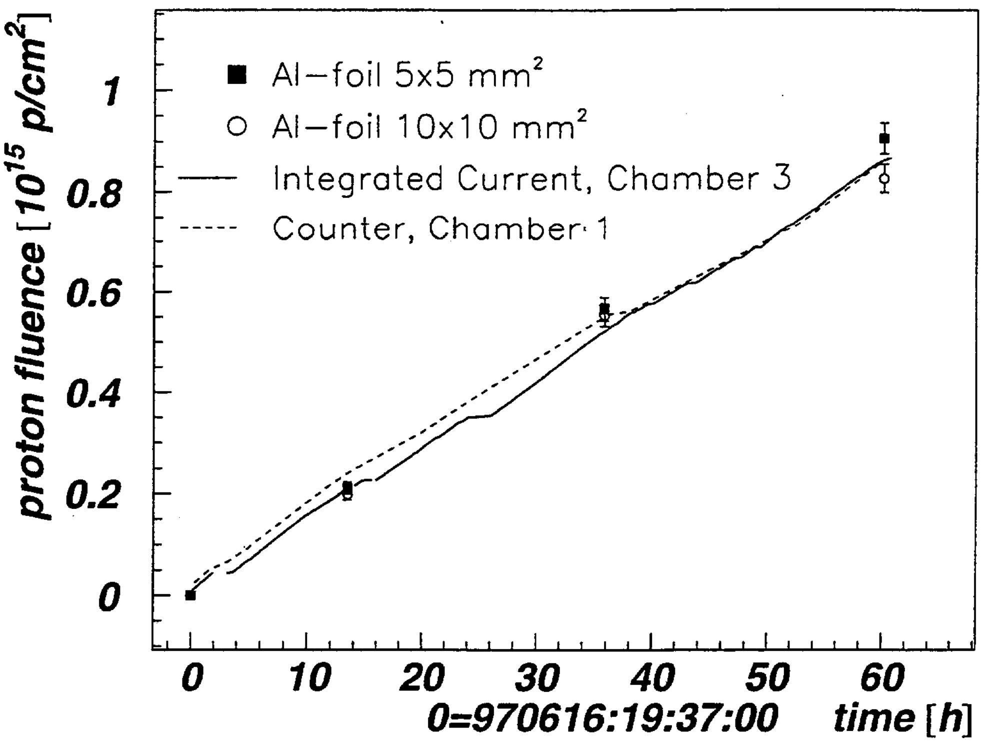


Figure 9 shows the fluence received by each sample. Note that after 70 hours the number of spill extractions per accelerator cycle increased from 2 to 3.

Figure 10 shows the pumped charge distribution before irradiation, after 0.9 x $10^{15} p/cm^2$ and after 5 x $10^{15} p/cm^2$ for the sample that reached the highest proton fluence. The mean and most probable charge are slightly higher after the dose of 0.9 x $10^{15} p/cm^2$ compared to before proton irradiation. This is likely due to incomplete pumping during the ^{90}Sr measurment. The charge measurement after the highest fluence show a 20% decrease in most probable and a 40% decrease in mean due to fewer events with high charge in the Landau tail.

Figure 9: CERN PS Proton Fluence on CVD Diamond

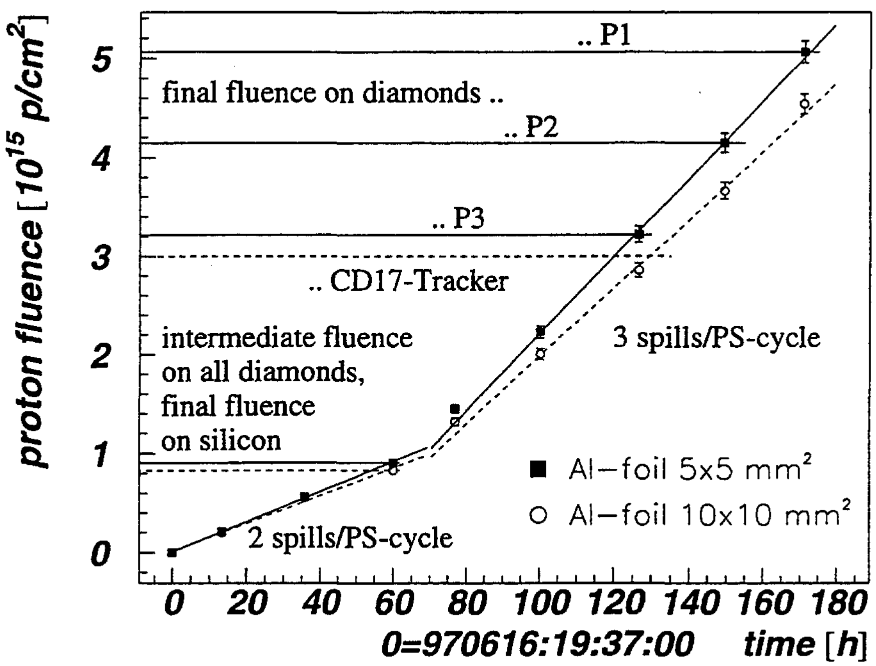


Figure 10: Diamond Collected Charge Histogram, Before and After p Irradiation

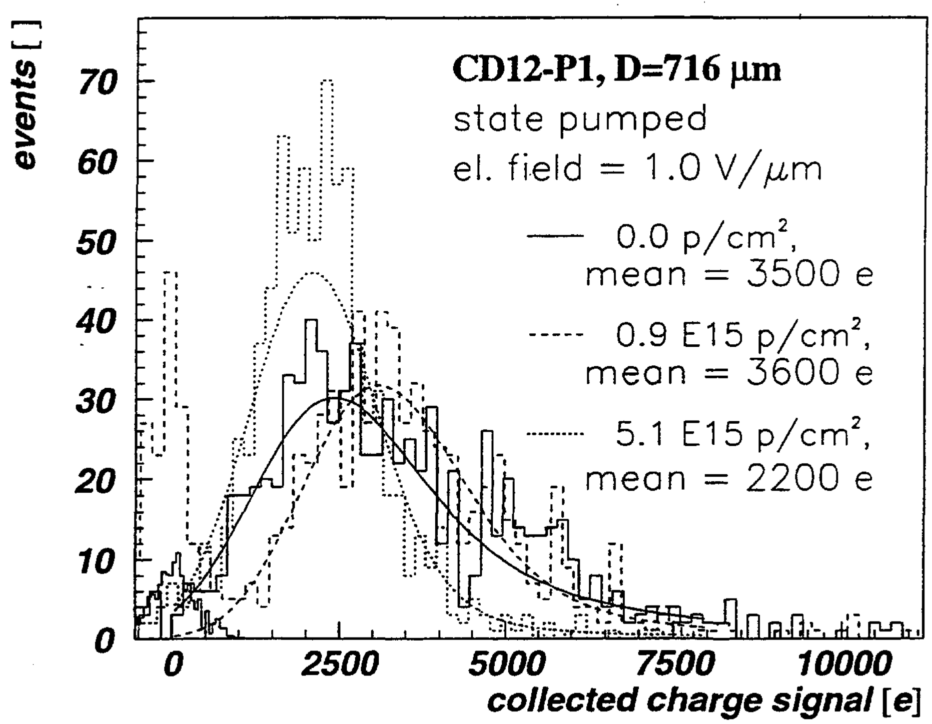
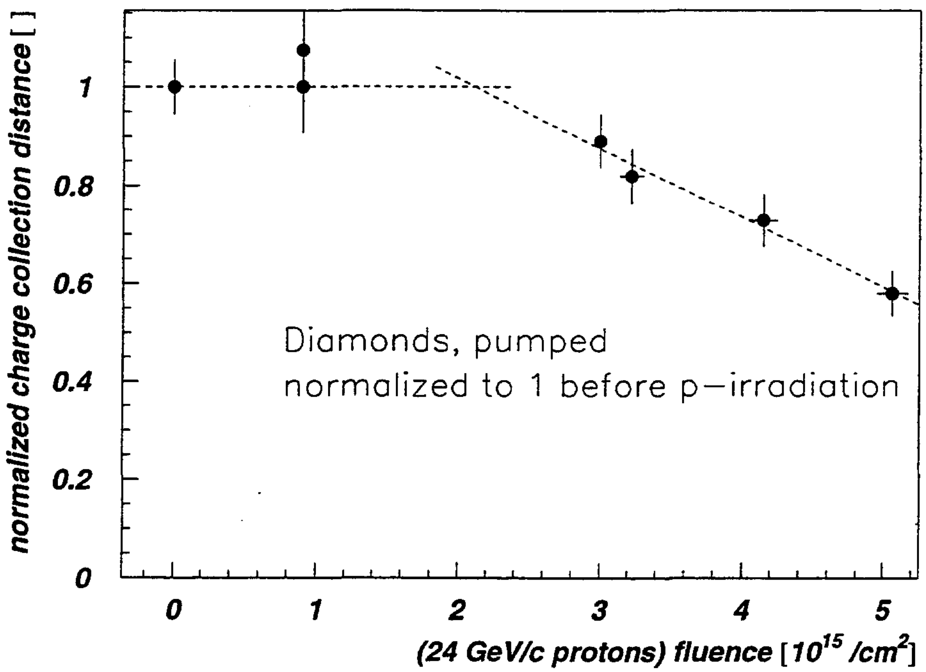


Figure 11 shows relative charge collection (normalized to the unirradiated pumped value) as a function of fluence for all samples. Up to 0.9 x $10^{15} p/cm^2$ there is no decrease in pumped charge collection. The data from 3 to 5 x $10^{15} p/cm^2$ suggests a linear decrease in charge collection reaching a net 40% decrease at 5 x $10^{15} p/cm^2$.

Figure 11: Charge Collection of Proton Irradiated Diamonds



6 Summary and Future Work

CVD diamond detectors have been shown to handle high beam flux without any degradation of charge collection. Furthermore, the dark current of the diamond detectors is unchanged when measured before and after irradiations, and is typically a few pA.

The results of the above irradiations are summarized in Table 2. For comparison, the expected dose at a radial distance of 7.5 cm from the beam line for one year of LHC running at design luminosity is also given. These results indicate that diamond detectors will survive the radiation exposures expected for LHC pixel detectors for at least ten years of LHC running.

There are new data from recent irradiations (1997) using pions and neutrons which are currently under analysis. The data are taken with higher quality CVD diamond and extend the reach in fluence. It is clearly important to continue these studies with the highest grade diamond material available.

	1 LHC Year [10] $r = 7.5$ cm	Dose Required to Damage Diamond
Neutrons	5×10^{13} cm^{-2}	2×10^{15} cm^{-2}
Charged Hadrons	2×10^{14} cm^{-2}	$> 2 \times 10^{15}$ cm^{-2} π
		$> 2 \times 10^{15}$ cm^{-2} p

Table 2: Summary of diamond irradiations.

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Evidence for charge collection efficiency recovery in heavily irradiated silicon detectors operated at cryogenic temperatures

Vittorio Palmieri, Kurt Borer, Stefan Janos

Laboratorium fuer Hochenergiephysik, Universitaet Bern, Sidlerstrasse 5, 3012 Bern, Switzerland

Cinzia Da Viá

Department of Physics and Astronomy, University of Glasgow, Glasgow G128QQ, Scotland

Luca Casagrande

Laboratório de Instrumentação e Física Experimental de Partículas, av. E. Garcia 14, 1000 Lisboa, Portugal

Abstract.

Charge collection efficiency of 300 μm thick silicon detectors, previously irradiated with 2.23 10^{15} n/cm^2, has been measured at 4.2 K, 77 K and 195 K. The recovery measured at a bias voltage of 250 V leads to a most probable signal for minimum ionizing particles of 13000 electrons, preserving its fast characteristics (< 5 ns). Negligible difference is observed between 77 K and 4.2 K operation, while no recovery is measurable at 195 K. The samples were stored at room temperature and cooled only when operated.

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Radiation damage in silicon detectors has been the subject of intensive studies in recent years in view of their use in LHC experiments at CERN. Different approaches have been followed by several groups in order to understand the physics of the radiation-induced damage [1]. The conclusions of these studies suggest to fix the working temperature of the inner silicon trackers of the two largest LHC experiments (ATLAS and CMS) slightly below 0 °C [2]. As long as this temperature is maintained, clusterization of primary lattice displacements is reduced and the lifetime of the detectors prolonged. However low temperature operation only delays bulk type inversion and does not prevent dramatic depletion voltage changes [3]. Moreover, if the radiation fluence approaches 10^{15} $n_{1MeV\,eq}/cm^2$, which is the anticipated irradiation of the innermost trackers after 15 years of LHC operation [4], the detectors become unusable [5].

Electrical characterization of irradiated detectors at cryogenic temperatures has been extensively studied, while Charge Collection Efficiency (CCE) is normally investigated only at room temperature and slightly below 0 °C. In this letter we report minimum ionising particle (mip) CCE of silicon detectors irradiated with 2.23×10^{15} n/cm^2 and afterwards operated at cryogenic temperatures. It will be shown that cryogenic cooling produces relevant recovery of the CCE when compared to operation at room temperature or close to 0 °C where the CCE is practically unmeasurable. It is important to stress that the investigated devices are cooled only during operation and otherwise stored at room temperature.

Moderate cooling is normally applied to irradiated silicon detectors to lower the leakage current and to inhibit "reverse annealing" [6]. At cryogenic temperatures, however, the trapping and de-trapping of carriers in radiation induced levels cause modifications of the detector electrical properties, such as the effective concentration of the ionised charges. This will in turn modify the electrical field distribution and therefore affect the CCE. Radiation-induced defect characterisation, at cryogenic temperatures, by means of Thermally Stimulated Current (TSC) [7] and Transient Current (TC) [8] techniques, has shown that the mobility of the carriers increases significantly leading to much faster output signals, while traps are inactive. In fact, at cryogenic temperatures, the de-trapping rate of electrons and holes is strongly affected by the reduced thermal energy. Trapping of drifting charges becomes the predominant effect, leading to the condition that a consistent fraction of deep-levels are filled and therefore inactive. Similar properties have been observed in the case of diamond detectors, in which the as-grown material already contains very deep traps. In this case, even at room temperature, neutralisation of deep traps is normally achieved by optical or electrical trap filling (*pumping*) [9].

Float Zone (FZ) silicon detectors 300 μm thick, 0.7 x 0.7 cm^2 were irradiated for 30 minutes at TRIGA [10] up to 2.23 x 10^{15} n/cm^2 . Two different types of materials (oxygenated and non-oxygenated), currently under study by the CERN RD48 (ROSE) collaboration, were investigated. Both are n-type $Al/n^+/n/p^+/Al$ implanted diodes. The as-grown resistivities are 1.8 kΩ-cm and 2.7 kΩ-cm for the oxygenated and the non-oxygenated materials respectively. The characterization of similar samples is described in [11].

The CCE measurements were performed at three different temperatures (4.2 K, 77 K and 195 K) immersing a cryogenic insert, described elsewhere [12], in liquid He, liquid N_2 and solid CO_2 respectively. The set of measurements for each detector always started at 4.2 K and was subsequently increased to 77 K and 195 K in two steps. At 4.2 K rather long (~10h) leakage current stabilization was necessary, while at higher temperatures one hour was sufficient. Mips charge distribution was measured at different bias voltages at the three temperatures for each irradiated detector. Non-irradiated detectors from the same wafer were used as reference and measured in exactly the same conditions. The bias voltage was varied from 50 V up to 250 V (the maximum value allowed by our set-up). Mips selection from a ^{106}Ru source was obtained using an additional silicon diode detector behind the test sample to provide a trigger. The trigger signal was amplified by a fast charge amplifier, while the signals from the detector were amplified by a charge amplifier with 2 μs shaping constant (AMPTEK 225, ~6000 e^- FWHM noise) and subsequently sent to a multi-channel analyzer. The large noise was mainly due to the 150 pF capacitance of the coaxial cable from the detector in the cryostat to the amplifier. The fast current signal of the detector was also measured directly with a low noise FET input voltage amplifier (5 ns risetime, 5 μV rms noise) connected to a digital oscilloscope (Tektronix 620B) in averaging mode. The detectors leakage current was continuously measured by a picoammeter (Keithley 697) for different bias voltage settings.

Fig. 1 shows the charge distribution for mips recorded at 77 K for (a) non-irradiated and (b) irradiated, silicon oxygenated diodes at 250 V bias voltage. As expected, we measure a reduction of the collected charge for the irradiated detector. It is worth stressing that the non-irradiated detectors show 100% CCE at full depletion voltage for all temperatures. The mips fast current signal of the irradiated silicon oxygenated diode at 250 V bias voltage is shown in fig. 2. This measurement was limited by the 5 ns risetime of the voltage amplifier. Similar results from the non-oxygenated detectors were obtained in the same experimental conditions. No appreciable changes were observed in either type of detectors when comparing operation at 77 K and 4.2 K.

The CCE (normalized to the corresponding non-irradiated detectors) of the irradiated samples, (a) oxygenated and (b) non-oxygenated, is shown in fig. 3 as a function of the bias voltage. The oxygenated diode, at 250 V bias voltage, shows a CCE of 0.52 ± 0.05 and 0.48 ± 0.05 at 4.2 K and 77 K respectively. Under the same bias conditions, the corresponding values for the non-oxygenated detector are 0.45 ± 0.05 and 0.47 ± 0.05. At 195 K the signals of the irradiated samples were indistinguishable from the pedestal. This is not surprising since, at this temperature, TSC measurements show that most of the radiation induced traps are still active.

Our results demonstrate that cryogenic operation of heavily irradiated silicon detectors leads to a significant recovery of the CCE. No significant difference was found between 77 K and 4.2 K. The measured values are expected to improve once a suitable mechanism of additional trap filling (*pumping*) is applied. Work in this direction is currently in progress. Concerning the read-out, conventional semiconducting electronics operates successfully at 77 K. In the context of high energy physics experiments, for example, interesting results have been achieved for the ATLAS liquid argon calorimeter [13]. In particular, at this temperature, bipolar circuits are expected to survive bulk radiation damage for the reasons discussed in this letter. For operation at 4.2 K it is possible to rely on Nb-based Josephson superconducting circuits which have already been shown to be the ultimate in radiation-hard technology [14]. Although a liquid He cooling system requires some sophistication, a much simpler picture applies for liquid N_2 where cooling pipes, like those proposed for the LHC experiments, could be used in combination with additional thermal insulation.

We conclude that cryogenic temperature operation allowed, for the first time, to obtain a mip signal (most probable dE/dx) of 13000 electrons for a 300 μm thick semiconductor detector irradiated above 10^{15} n/cm^2. This remarkable result was not affected by room temperature storage of the unbiased detectors.

We are grateful to K. Pretzl and U. Moser for suggestions and help in the realization of the experimental set-up. We are indebted with F. Lemeilleur and A. Ruzin for useful discussions and for providing the measured detectors. S. Pirollo, M. Bruzzi and Z. Li are also acknowledged for useful discussions on semiconductor detectors at cryogenic temperatures. K. Smith, S. Paul, E. Borchi, P. Sonderegger and C. Benvenuti are warmly thanked for their constant encouraging support from the early stages of this project. One of the authors (L.C.) acknowledges financial support from the EC (TMR programme) under contract number ERBFMBICT961204. This research was supported by the Schweizer Nationalfonds zur Förderung der wissenschaftlichen Forschung and by the Stiftung zur Förderung der wissenschaftlichen Forschung an der Universität Bern.

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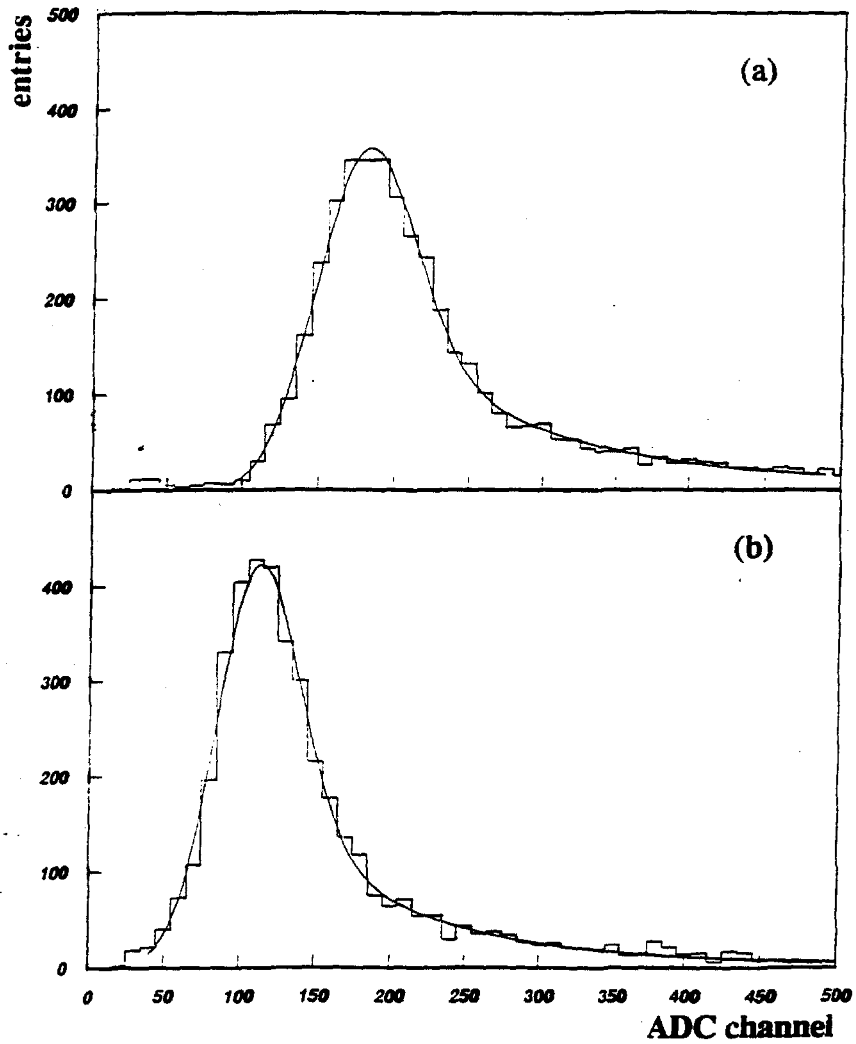
Figure Captions

Figure 1. Charge distributions for mips recorded at 77 K for (a) non-irradiated and (b) irradiated. silicon oxygenated diodes at 250 V bias voltage.

Figure 2. Mips current signal from the irradiated silicon oxygenated diode amplified by a fast low-noise (5 ns rise time, 5 μV rms noise) voltage amplifier and acquired by a digital oscilloscope in averaging mode. The detector bias voltage was 250 V.

Figure 3. CCE for irradiated detectors, (a) oxygenated and (b) non oxygenated, normalized to the corresponding non-irradiated ones, as a function of the applied bias voltage. Error bars include estimated systematic errors. The curves are drawn as guides to-the-eye.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500
400
300
200
100
0
(a)
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300
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0
(b)
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400
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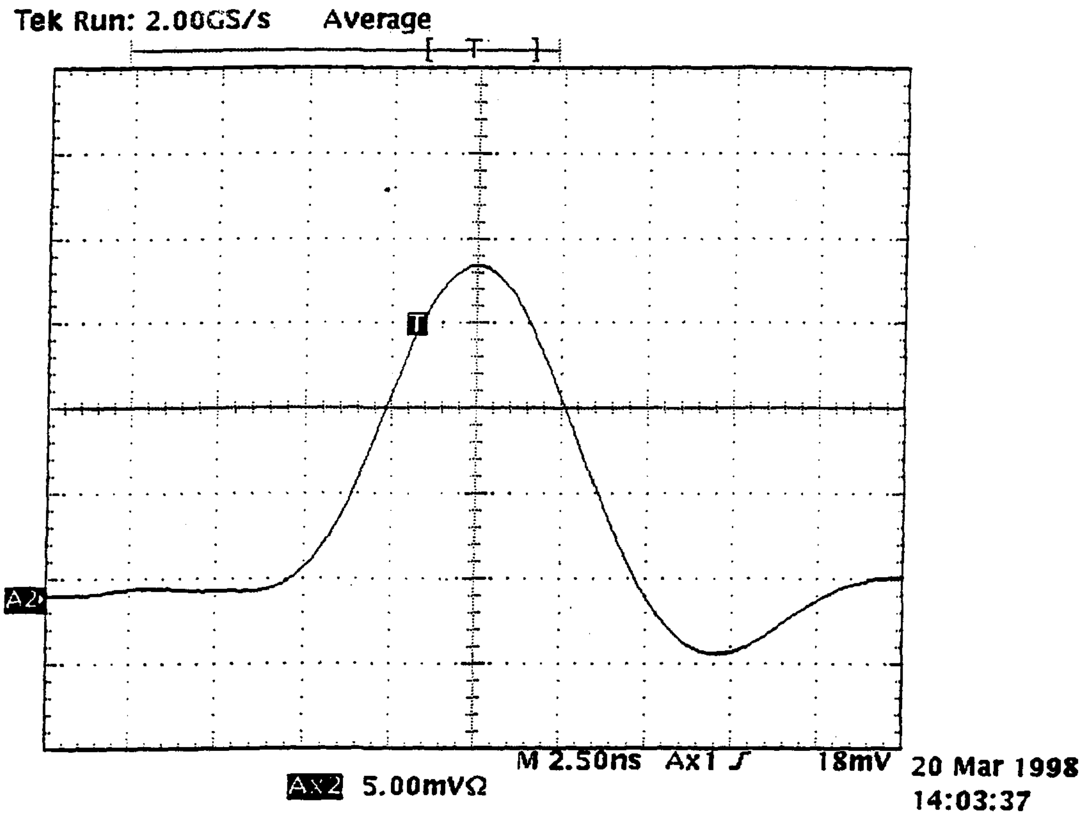
500
ADC channel

Figure 1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A2
M 2.50ns Ax1 ∫ 18mV
Ax2 5.00mVΩ
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14:03:37

Figure 2

360

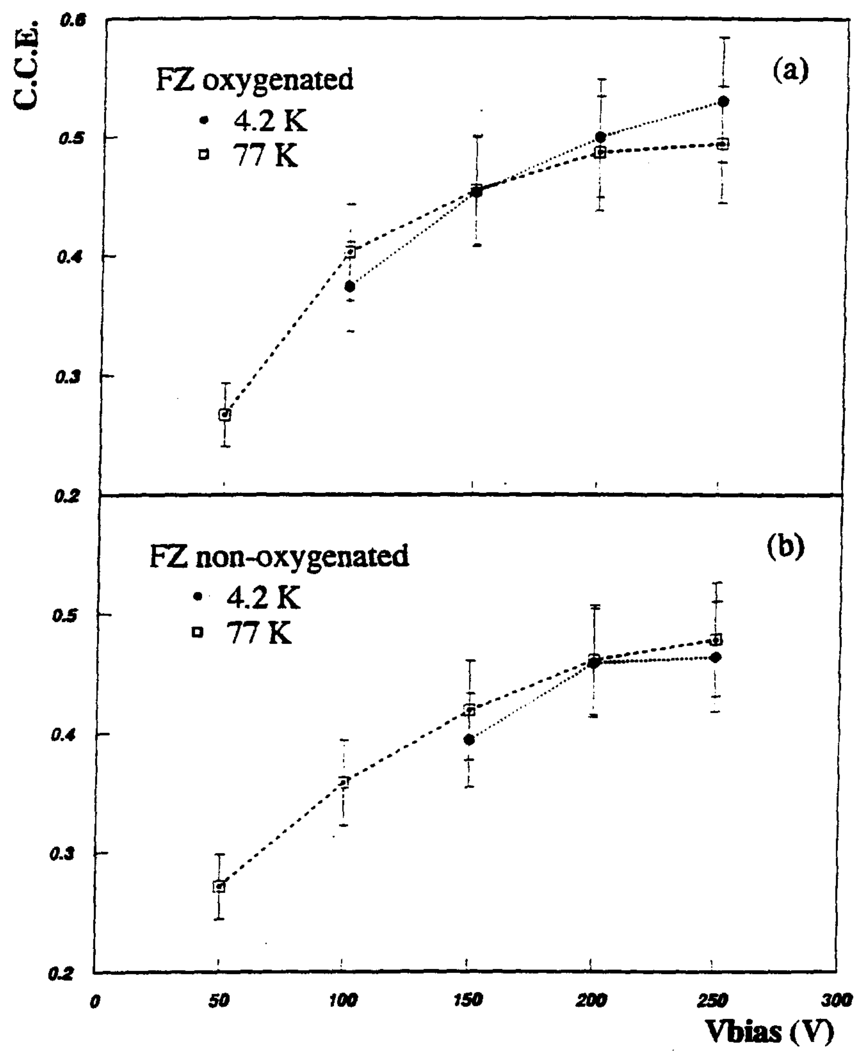

C.C.E.
FZ oxygenated
• 4.2 K
▫ 77 K
(a)
FZ non-oxygenated
• 4.2 K
▫ 77 K
(b)
0.6
0.5
0.4
0.3
0.2
0
50
100
150
200
250
300
Vbias (V)

Figure 3

Bump Bonded Pixel Detectors on CVD Diamond from RD42

W. Adam[1], C. Bauer[2], E. Berdermann[3], P. Bergonzo[4], F. Bogani[5], E. Borchi[6], A. Brambilla[4], M. Bruzzi[6], C. Colledani[7], J. Conway[8], W. Dabrowski[9], P. Delpierre[10], A. Deneuville[11], W. Dulinski[7], B. van Eijk[12], A. Fallou[10], F. Fizzotti[13], F. Foulon[4], M. Friedl[1], K.K. Gan[14], E. Gheeraert[11], E. Grigoriev[9], G. Hallewell[10], R. Hall-Wilton[15], S. Han[14], F. Hartjes[12], J. Hrubec[1], D. Husson[7], H. Kagan[14], D. Kania[14], J. Kaplon[9], C. Karl[16], R. Kass[14], K.T. Knöpfle[2], M. Krammer[1], A. Logiudice[13], R. Lu[13], P.F. Manfredi[17], C. Manfredotti[13], R.D. Marshall[4], D. Meier[9], M. Mishina[18], F. LeNormand[7], A. Oh[16], L.S. Pan[14], V.G. Palmieri[19], H. Pernegger[1], M. Pernicka[1], A. Peitz[8], S. Pirollo[6], P. Polesello[13], K. Pretzl[19], V. Re[17], J.L. Riester[7], S. Roe[9], D. Roff[15], A. Rudge[9], S. Schnetzer[8], S. Sciortino[6], V. Speziali[17], H. Stelzer[3], J. Steuerer[16], R. Stone[8], R.J. Tapper[15], R. Tesarek[8], G.B. Thomson[8], M. Trawick[14], W. Trischuk[20], R. Turchetta[7], E. Vittone[13], A. Wagner[16], A.M. Walsh[8], R. Wedenig[9], P. Weilhammer[9], W. Zeuner[16], H. Ziock[21], M. Zoeller[14]

The RD42 Collaboration

E. Charles, A. Ciocio, K. Dao, K. Einsweiler, D. Fasching, A. Joshi, S. Kleinfelder, O. Milgrome, J. Richardson, P. Sinervo

LBL/Wisconsin Pixel electronics team

[1] *Institut für Hochenergiephysik der Österr. Akademie d. Wissenschaften, A-1050 Vienna, Austria*
[2] *MPI für Kernphysik, D-69029 Heidelberg, Germany*
[3] *GSI, Darmstadt, Germany*
[4] *LETI (CEA-Technologies Avancees) DEIN/SPE - CEA Saclay, 91191 Gif-Sur-Yvette, France*
[5] *LENS, Florence, Italy*
[6] *University of Florence, Florence, Italy*
[7] *LEPSI, CRN, Strasbourg 67037, France*
[8] *Rutgers University, Piscataway, NJ 08855, U.S.A.*
[9] *CERN, CH-1211, Geneva 23, Switzerland*
[10] *CPPM, Marseille 13288, France*
[11] *LEPES, Grenoble, France*
[12] *NIKHEF, Amsterdam, Netherlands*
[13] *University of Torino, Italy*
[14] *The Ohio State University, Columbus, OH 43210, U.S.A.*
[15] *Bristol University, Bristol BS8 1TL, U.K.*
[16] *DESY, Hamburg, Germany*
[17] *Universita di Pavia, Dipartimento di Eletronica, 27100 Pavia, Italy*
[18] *FNAL, Batavia, U.S.A.*
[19] *Lab. für Hochenergiephysik, 3012 Bern, Switzerland*
[20] *University of Toronto, Toronto, ON M5S 1A7, Canada*
[21] *Los Alamos National Laboratory, Research Division, Los Alamos, NM 87545, U.S.A.*

Abstract

Diamond is a nearly ideal material for detecting ionizing radiation. Its outstanding radiation hardness, fast charge collection and low leakage current allow it to be used in high radiation environments. These characteristics make diamond sensors particularly appealing for use in the next generation of pixel detectors planned for experiments at Fermilab and the LHC. Over the last year we have worked with several groups who have developed pixel readout electronics in order to optimise sensor preparation on diamond substrates for bump-bonding. We describe the four different approaches that are being actively pursued and the results of one fully bonded sensor tested in a beam. This device shows good hit efficiency as well as clear spatial correlations to tracks measured in the reference telescope. The position resolution observed is that expected given the detector pitch. Preparations for the next generation of CVD diamond pixel detectors will also be described.

1 Introduction

At present both the ATLAS and CMS detectors at the Large Hadron Collider (LHC) plan to install pixel devices as the innermost layers of their tracking detector. Pixel detectors facilitate pattern recognition and vertexing in locations where the track occupancy on strip detectors would be too high or the bulk damage too great. Substituting CVD diamond sensors for Silicon would solve the radiation damage problem [1] while preserving other features of solid-state tracking such as precision and stability. Each pixel cell will be readout by an individual charge amplifier followed by a fast shaper. The shaped signals will then be evaluated by sparsification logic and eventually delivered to the back end. The pixel detector readout chip must geometrically match the pixel pattern on the detector substrate since a single active cell on the detector substrate will be connected to its readout cell via a bump bond. Bump bonding is a difficult process on the 50 μm scale such as is required for both experiments. Though pixel readout electronics are still in the development phase, tests have been undertaken with existing designs in order to study the bump bonding process including preparation of the contact surface.

2 Sensor Prototypes

The first diamond pixel detector was tested in August 1996 in a particle beam at CERN. This detector was readout via a pixel fanout structure metallized on a glass substrate. The purpose of this test was to investigate the feasibility of pixel geometries on a diamond substrate and the charge collection performance. This device had a mean signal-to-noise ratio of 27:1 and a position resolution consistent with digital resolution for a device with 150×150 μm^2 pitch. Based on the success of this test, we produced pixel sensors to the specifications of ATLAS and CMS. The contact geometry on the diamond surface has been fabricated to match the requirements of the existing readout chips for ATLAS and CMS. Table 1 gives an overview of diamond sensor samples with substrate size and pixel cell size. The metalisation contact and proposed bump bonding material are also listed.

	pixel cell size [μm^2]	diamond substrate size [μm^2]	metallisation [elements]	passivation [yes/no]	bumb bonding metal
CMS/1	100×100	3725×4725	Cr/Au	yes	In
ATLAS/1	50×414.4	3800×5800	Cr/Ni/Au	yes	In
ATLAS/2	50×414.4	3800×5800	Ti/W	no	Sn/Pb
ATLAS/3	50×536	4000×8000	Ti/W	no	In

Table 1: Overview on diamond pixel detectors for pixel chips in CMS and ATLAS, The dimensions of the sensors, their metallisation and passivation layers are listed.

The first bump bonding tests were performed in collaboration with the CMS group. Other devices were bump bonded with the ATLAS group and tested with a source for its charge collection and efficiency. Figure 1 and Figure 2 show the first diamond pixel sensors with a pixel metallization pattern for CMS and ATLAS. An ATLAS/3 pixel detector has been produced and successfully bonded to the pixel readout chip at Boeing. The choice of Ti/W for the readout pads was natural as Ti creates the best ohmic contact with the diamond surface, facilitating the extraction of the signal, while W is an inert over-metal that is commonly used in integrated circuit processing.

Tungsten also resists oxidation a feature necessary as the diamond sensors were prepared in a different location than the final bump-bonding. Silicon sensors previously bonded by Boeing have exhibited less than 10^{-4} failed bonds. A visual inspection of the bump bonds on our diamond device showed a yield of 100%.

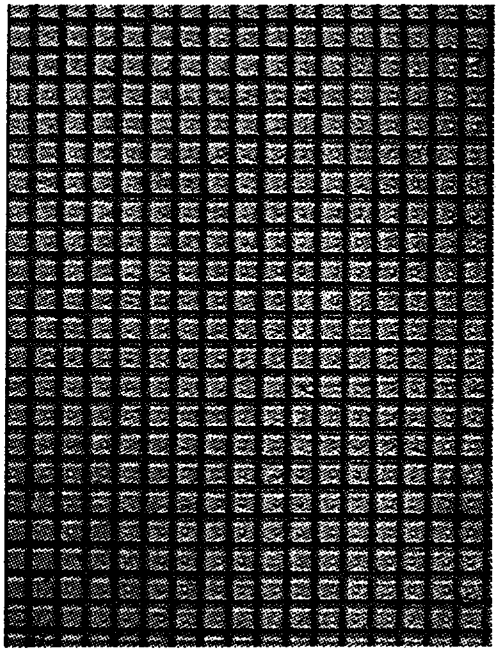


Figure 1: Top view of a CMS diamond pixel sensor showing the overall pixel pattern. The pixel metallization is Cr/Au for this device. The pixels are covered with a passivation layer. The passivation has a hole offset from the pixel center for the Indium bond.

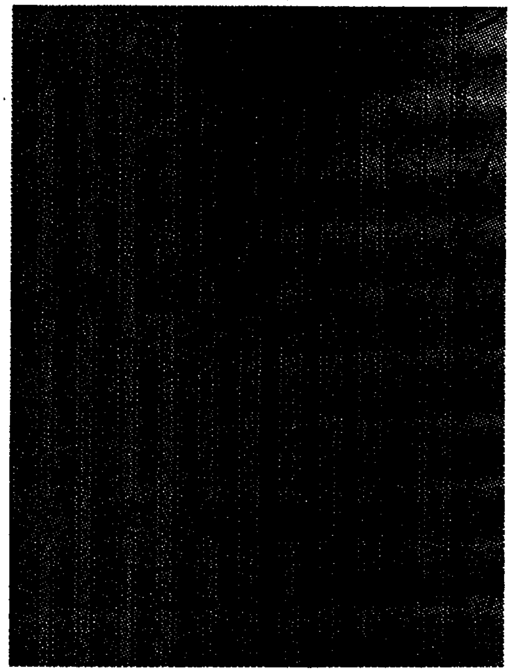


Figure 2: Corner view of the ATLAS/3 pixel sensor showing the overall pixel pattern. The metallization is Ti/W. The pixels are not covered with a passivation layer.

3 Source Test Results

The first test of the ATLAS/3 pixel tracker was performed using a ^{107}Ru source at CERN in late 1997. The relatively low electron end point energy of 3.54 MeV meant that it was not possible to include a silicon reference plane between the pixel prototype and the trigger. Thus no external spatial information was available from this initial test. The source was mounted 5 cm from the surface of the pixel detector. A 7×7 mm^2 scintillator trigger counter was mounted 3 cm behind the pixel detector. In order to quantify the trigger acceptance and efficiency a silicon pixel detector (readout with the same readout chip) was tested in parallel. We took about 15,000 triggers in the silicon test run. We observed 5,100 hits in the silicon pixel detector which roughly corresponds to the 35% geometric acceptance expected from the active area of the pixel detector (17.3 mm^2) relative to the area of the trigger counter (49 mm^2).

The signal size of a diamond detector can be increased by about a factor of 1.6 by exposing the diamond to < 1 krad of ionizing radiation. In this first test, we decided not to pump up the diamond pixel since the readout chip was not implemented in a radiation-hard technology and could have been damaged. Furthermore, since the readout chip might be damaged by over voltage, we did not operate the diamond pixel detector at full voltage. The net result was that the signal from the diamond was about a factor of two lower than had been observed in previous tests of this device. Also, during this test the threshold of the readout chip was about a factor of two higher than the minimum value. However a run of 39,000 triggers yielded hits in 75 % of the pixels. Given the reduced signal and high sparsification threshold only about 2 hits per pixel were seen. Thus Poisson fluctuations can account for the absence of hits in a further 15 % of the pixels. This result was sufficiently encouraging to re-mount the tracker in the testbeam described in the next section.

4 Testbeam Results

The ATLAS/3 pixel tracker was tested in a 50 GeV pion beam at CERN in April of 1998. The standard RD42 silicon reference telescope [2] was used to provide four x and y measurements of the track, each with 2 μm precision. The resulting track extrapolations onto the plane of the diamond were better than 2 μm in each dimension, significantly better than the resolution expected from our pixel tracker. We collected 200 k tracks at normal incidence to the diamond surface and have studied the pixel hit distribution, charge deposition and spatial correlations between the pixel tracker and the external reference telescope.

4.1 Bonding Efficiency

Figure 3a) shows the number of hits found per pixel during this test. The size of the boxes is proportional to the number of tracks above threshold in each pixel cell. Further study of the charge distribution in columns 4 and 6 indicates that many of these hits resulted from false triggers. We exclude these columns from further study. In addition there is an apparent reduction in the number of hits seen on the "right" half of the tracker when compared to the "left" half. This effect is still under study. It may indicate a variation in the readout threshold across the chip or a non-uniformity in the efficiency of the external (scintillator) trigger system.

The most striking feature of fig. 3a) is that charged particle hits have been recorded in almost all of the pixel cells. This is further evidence that a high bump-bonding yield has been achieved. Figure 3b) shows a projection of the number of hits seen in each pixel. In the top plot we see that there are 26 pixels that failed to record a single hit. In the lower plot we restrict our attention to the four columns on the "left" side of the tracker. There only 6 of the 256 pixels failed to record a hit. From the lower plot it is clear that there is very little chance that many of these six were a fluctuation, as there is only one additional pixel which saw only a single hit. From this data we conclude that at least 98% (250/256) of the channels were successfully bonded and capable of recording hits. A similar conclusion can be drawn from the top distribution. There a background subtraction, based on the number of cells with only a few hits recorded, of about 15 channels is estimated. This leaves 11 channels (26-15) that appear truly lacking hits leading us, again, to conclude that 98 % (501/512) of the channels are bonded.

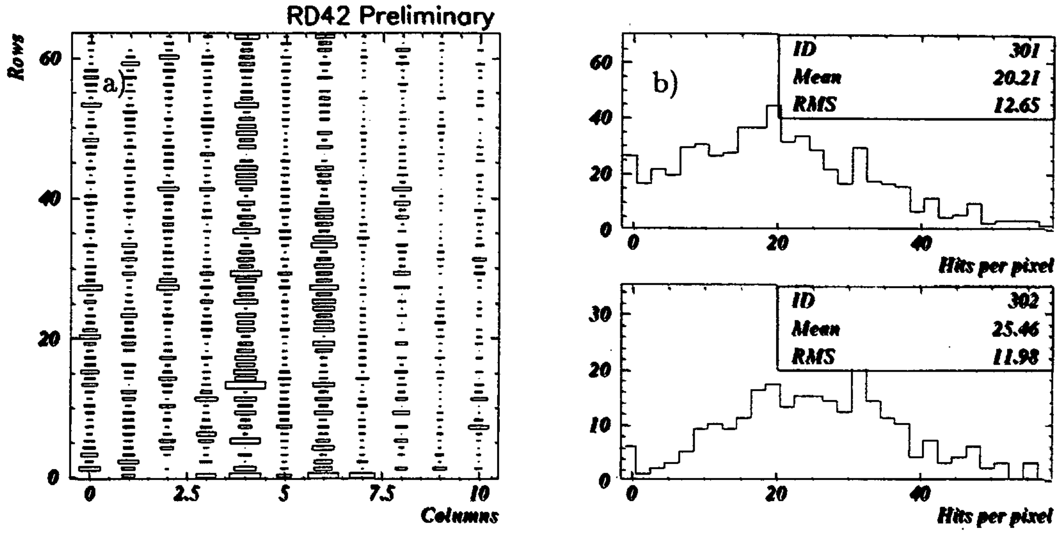


Figure 3:
a) The number of hits per pixel seen in April 1998 testbeam run. b) The distribution of number of hits per pixel cell. The top plot shows the distribution over the whole tracker (512 cells) while the bottom plot shows the number of hits per cell only on the "left" side of the detector where a significantly higher number of hits per cell have been recorded.

4.2 Charge Distribution

Of the 200 k testbeam tracks recorded the trigger acceptance calculation predicts 66 k of them should have passed through the diamond tracker. Excluding the two noisy columns we should have seen 49 k hits. Figure 4a) shows the time-over-threshold (charge) distribution for all the tracks recorded in this run. We see only 12 k hits. We attribute this 25% efficiency to a combination of reduced charge in the un-pumped diamond as well as a sparsification threshold of about 4000 electrons. In this testbeam we were able to operate the diamond sensor at full bias voltage (550 V for the 550 μm thick detector) but were still hesitant to expose the tracker to sufficient ionising radiation to fully pump the detector. While we were able to lower the threshold slightly, compared to the source test performed earlier, we still had a threshold that was almost a factor of two higher than optimal.

One of the features of using diamond as a sensor material is that it can be recycled. In this case, the diamond material that we are now using as a pixel tracker was previously tested as a strip tracker. As such we have data on the charge distribution we expect from the pixel detector. Figure 4b) summarises our understanding of the situation. The solid gray histogram is the single-strip charge observed in this diamond material when it was a strip tracker with 50 μm pitch. This charge corresponds to a 200 μm collection distance, consistent with that seen in source characterisations of this material. The single strip charge is all that is relevant to our pixel tracker

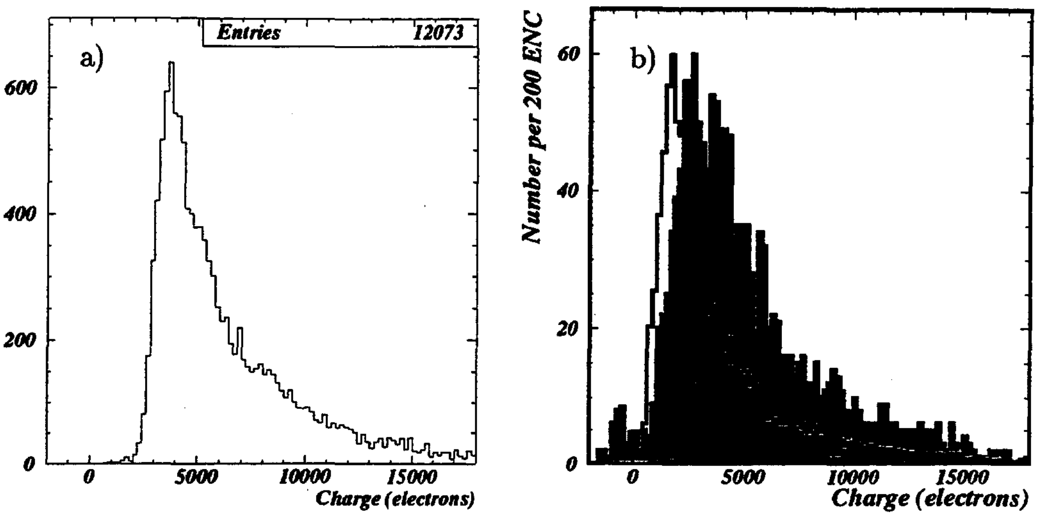


Figure 4:
a) Distribution of time over threshold (charge) measurements for triggered pixels in April 1998 testbeam. b) Comparison of the charge observed in the pixel tracker (dark grey) in the April 1998 testbeam with that seen in the same diamond when it was instrumented as a strip tracker in May 1997 (light gray histogram). The open histogram is a prediction, based on the observed (light gray) charge and the fact that the diamond was not pumped in the 1998 test, for the charge we should expect to see in the pixel tracker. From the turn-on of the charge seen in the pixel tracker (dark grey) we conclude that the pixel electronics was operating with a 4000 e^- threshold.

as we expect, and see, no significant sharing of cluster charge between neighbouring pixels. This data was taken with the tracker fully pumped (exposed to about 10 kRad of ionising radiation). Extensive study of this effect lead us to conclude that trackers not prepared in this way produce 40 % less charge. Thus, the open histogram is the single strip data scaled down by 40 %. Overlaid (in black) is the actual charge observed in the pixel detector. We conclude that the high threshold (4000 e) with which we were operating explains the missing hits.

In future tests we plan to pump the detector up (returning to the charge distribution shown in gray in fig. 4b). If we can also lower the threshold to 2000 e then we would expect this pixel tracker to achieve an efficiency of 80 %. To move much beyond this will require a slightly lower threshold and/or higher quality diamond. We expect that in the next 12 months we will have both.

4.3 Spatial Resolution

The correlation between reference telescope track positions and the position of hits recorded in the pixel tracker is shown in figs. 5a) and 5b). Only 20 % of the total sample has been tracked at this stage. A clear correlation between the two measurements is seen. At very low "Pixel x position" we see a degradation in the position resolution consistent with known defects in the patterning, near one edge of the diamond sensor.

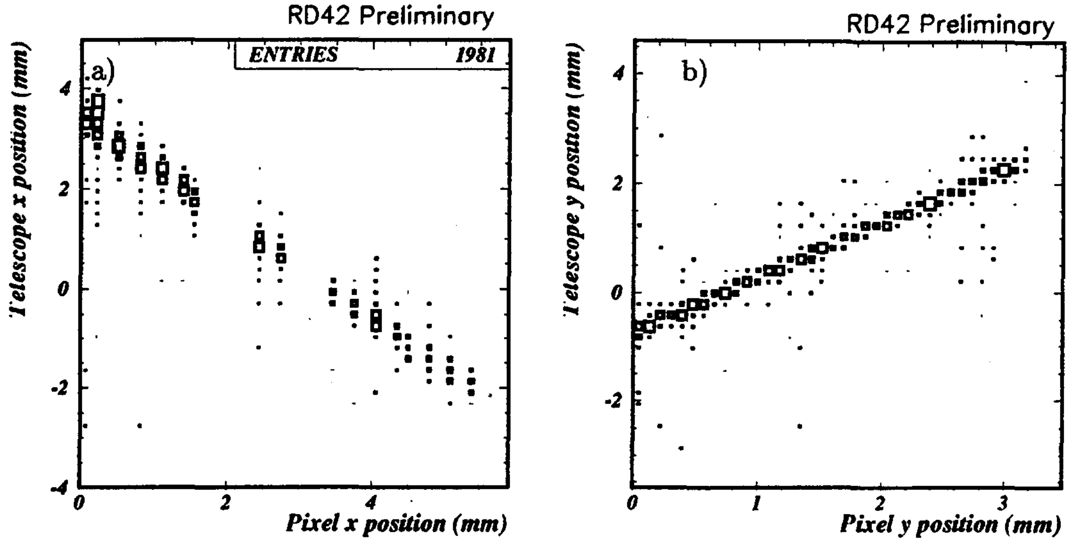


Figure 5:
The spatial correlation between the pixel detector hits and the reference telescope tracks in a) the x (long pixel) view and b) the y (short pixel) view.

Projections of these two plots along the diagonal yield the results shown in figs. 6a) and 6b). The resolution along the direction of the large pixel dimension (536 μm in length) is, as expected, a top-hat distribution with a full width at half maximum of about 500 μm. In the direction measured by the small pixel dimension we see a position resolution, 14.8 μm, consistent with the strip pitch divided by the square root of twelve. In both cases there are minimal tails beyond the main peak indicating that very few of the hits recorded by the pixel tracker are unrelated to the charged tracks measured in the telescope. The beam intensities recorded in our telescope are such that fewer than 1 % of the triggers contain more than one charged track thus the potential for confusion in the reconstruction of the reference telescope, while minimal, is not completely negligible. However, it should be clear that the vast majority (over 99 %) of the hits that trigger the pixel readout chip result from the passage of charged particles also reconstructed in the reference telescope.

5 Conclusions

The RD42 collaboration has undertaken an aggressive effort to produce working diamond pixel prototypes. This is a natural progression of the work that has been undertaken by the collaboration up to now. As diamond is a sufficiently radiation hard material to survive, for the lifetime of the LHC, at small radii, it is now natural that diamond be adapted to the readout geometries best suited to these detection regions.

Work with one prototype tracker system (the ATLAS/3) has yielded a fully functional proto-

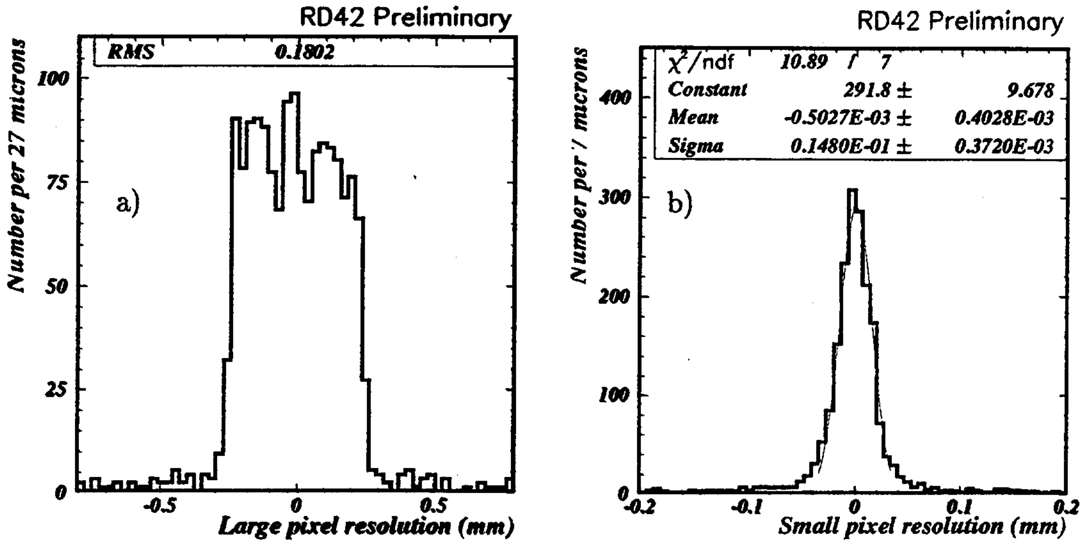


Figure 6:
The position resolution of the pixel detector prototype in a) the x (long pixel) view and b) the y (short pixel) view.

type that has proven high bump-bonding yields are possible. Testbeam studies of this diamond sample have served to further emphasize that the material currently available, though promising, is not entirely adequate to produce fully functional pixel detector systems. However, with modest improvements in detector material quality and the reduction of readout thresholds – similar to those that will be needed to readout thinned silicon sensors – the goal of producing a CVD diamond based pixel tracker system appears to be achievable in the near future.

References

[1] W. Adam *et al.*, RD42 renewal (1997), LHCC-97/3.

[2] F. Borchelt *et al.*, Nucl. Instrum. and Meth. **A354**, (1991), 506.

3D--A New Solid-State Detector Architecture

Progress Report -- May 1998

Christopher Kenney and Sherwood Parker
U. of Hawaii

Julie Segal* and Christopher Storment
Stanford University

A. Introduction

Until now, planar technology, in which all fabricated elements are on or within a few microns of the surface, has been the only technology used for the fabrication of integrated circuits as well as for silicon strip and pixel detectors [1].

The coming generation of high intensity machines such as the Large Hadron Collider (LHC) will place severe demands on both speed and radiation hardness of the inner tracking detectors. The speed of both strip and pixel detectors is adequate, but only marginally so, since typical pulse rise times of 5-10 ns are a significant fraction of the 25 ns beam crossing interval, and typical pulse lengths of 30-40 ns are longer.

There will, however, be nothing marginal about their response to radiation at the LHC [2] or HERA-B [3] at DESY. Without some change, they will not survive the damage to the bulk silicon. The radiation induced increase in the p-type dopant density and the corresponding increase in depletion voltage, will cause voltage breakdown long before the desired duration of the experiment.

While the Atlas and CMS groups are working on possible solutions to this problem, the only known one at this time consists of keeping the detector cooled to below 0° C before the radiation damage becomes too severe. This prevents the reverse annealing which causes a further large increase in effective dopant density. In addition, it will probably be necessary to use either thinner than normal, or partially depleted detectors. If cooling is lost for more than a few days per year, part or all of the silicon inner layers may be lost.

B. 3D--A possible solution

3D is a proposed technology in which + and - electrodes penetrate from the surface through most or all of the detector bulk. The maximum drift and depletion distances are then set by the electrode spacings rather than the detector thickness. Both depletion voltages and collection times can then be kept small. Simulations of 3D detector designs indicate the initial depletion voltages will be in the range of 1-2 volts, and remain under 10 volts for the lifetime of the experiment. Peak fields, located where the depletion region borders the highly doped electrodes, are an order-of-magnitude below breakdown levels, and <u>decrease</u> under radiation as a larger fraction of the voltage appears across the increasingly highly doped bulk.

The predicted behavior of such detectors are given in "3D--A proposed new architecture for solid-state radiation detectors" in [4]. Here we will only show a sample three-dimensional view (Fig. 1), typical electric fields before and after radiation (Fig. 2), depletion voltage comparisons between a 3D detector and a planar diode with simple 2D electrodes (which will deplete at lower voltages than normal strip detectors--Fig. 3), typical pulses expected on the electrodes of a 3D detector (Fig. 4), and a comparison with pulses on a strip detector (Fig. 5) [5].

C. The first attempts

During our initial tests, we learned of earlier attempts, in the period 1975 - 1982, to develop 3D electrodes for detectors and chip-to-chip connectors for computers [6] using thermomigration to fabricate aluminum doped p type columns in an n type silicon substrate.

In this process, a silicon wafer has a temperature gradient imposed, with the entire wafer maintained above the lowest melting point of an aluminum-silicon mixture. Aluminum, placed on the low temperature surface, diffuses into the silicon, reducing the melting point and forming a molten zone. Aluminum then diffuses from the cooler, high concentration region to the warmer, low concentration region, extending the molten zone there, and causing freezing at the cooler end which now has less aluminum. This process thus produces a column of dissolved aluminum in the silicon.

A paper by T. Anthony and H. Cline of General Electric [7] described an array of deep diodes formed by thermomigration. Among other applications, x-ray detection was mentioned. Fig. 6, reproduced from their paper shows square columns with a 0.5 mm pitch on the top and the distorted columns as they emerge on the bottom of a 3 mm thick silicon wafer. Since electrodes of only one type were mentioned and made, the field between them must have had a long vertical component to either face, and charge made in that region, a long collection distance. No mention was made of ever actually using the device as a detector, and no data were shown.

Another paper was published by G. Alcorn et al. of NASA in the 1982 International Electron Devices Meeting [8]. Their detector used a column in the center of a box-like cell. Both were formed from p-type aluminum doped silicon. Their electric fields would also have been primarily vertical, with the same long collection distances. During thermomigration their columns were sometimes deflected by crystal imperfections. The p box - n substrate - p column also formed a pnp transistor which led to high leakage currents. Actual use as a radiation detector was mentioned, but no data was shown.

A final paper, by T. Anthony [9], showed how diodes can be formed by diffusion from holes formed by laser drilling. Again, only one type of electrode was made, and no actual use as a radiation detector was mentioned.

A patent by Alcorn mentioned n doped columns from laser driven holes with the thermomigrated p-type boxes. No papers were ever published showing either fabricated devices or results from beam tests or experiments.

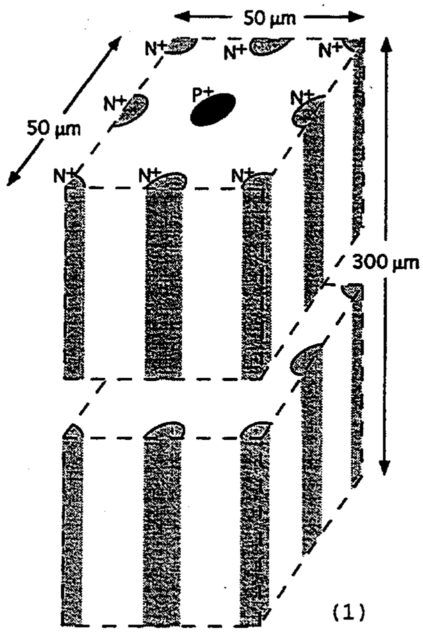


Fig. 1. Three-dimensional view of a typical cell.

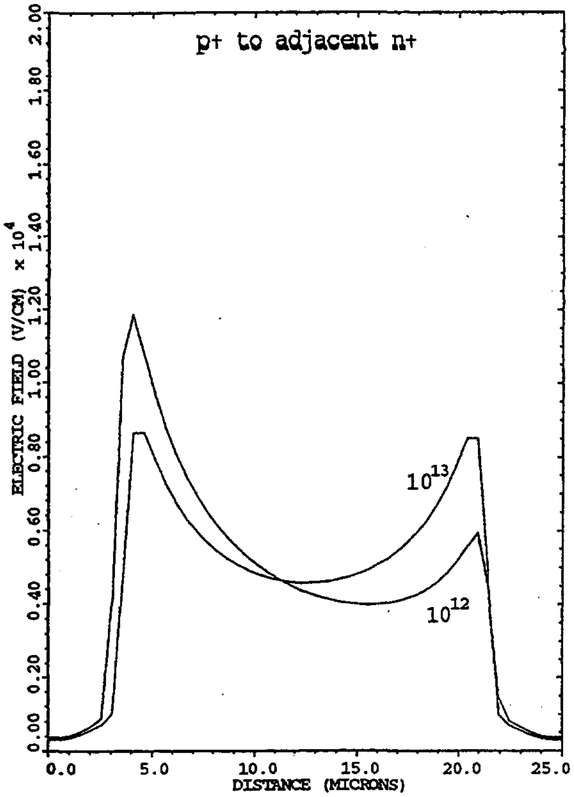


Fig. 2. Comparison of electric field magnitudes for the quarter cell of Fig. 1. 10 V applied voltage, along the line from the p^+- to the adjacent n^+-electrode for substrate dopings of 10^{12}/cc and 10^{13}/cc. With higher substrate dopant levels, as can occur with radiation damage, the peak fields, located where the depletion volume meets the electrodes, actually decrease due to the increase in voltage dropped across the lightly doped (compared to the electrodes) substrate. The small, but non-zero values of the electric fields at the ends of the plot (corresponding to the electrode centers) are due to approximations in the finite-element calculations.

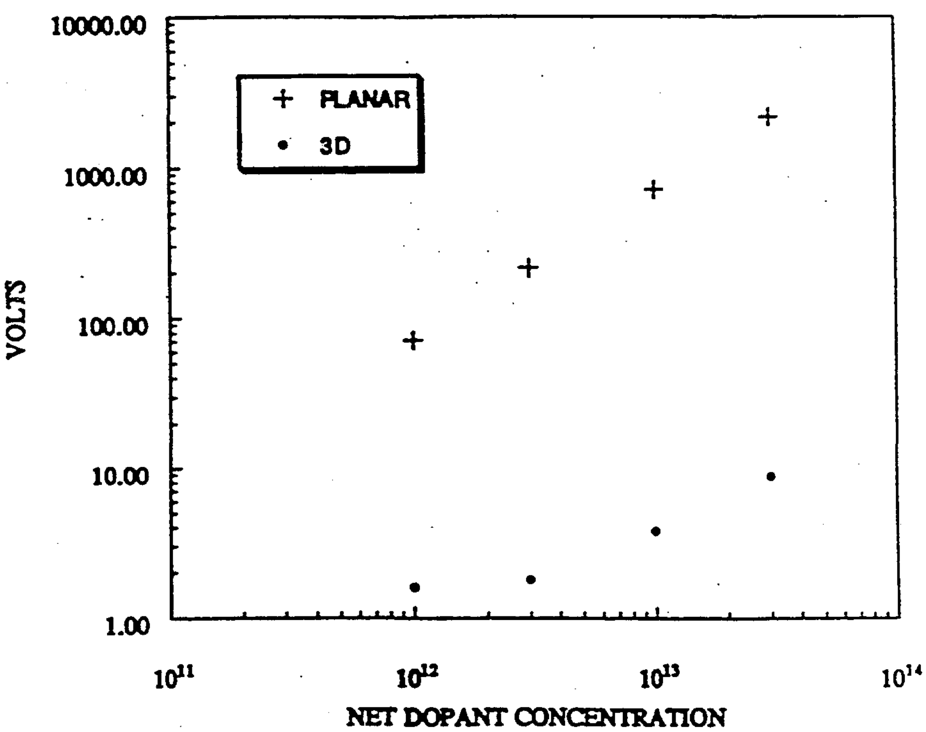


Fig. 3. Depletion voltage for a planar diode on 300 μm thick silicon, and a 3D detector with 50 μm pitch electrodes.

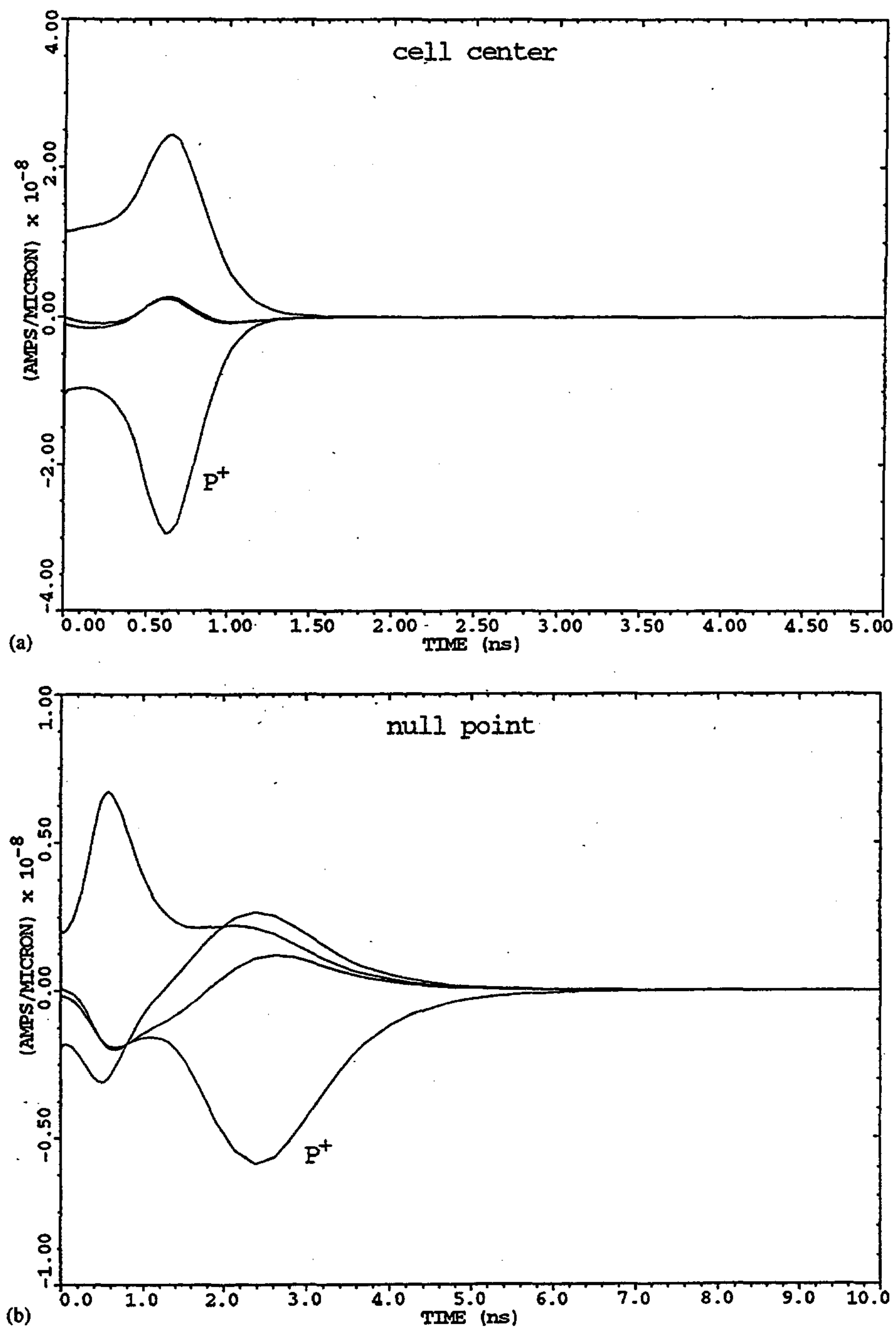


Fig. 4. Current pulses on the electrodes from a track parallel to the electrodes, (a) through the cell center, and (b) through the null point between two n^+ electrodes. The fields are those of Figure 2c, 10^{12} per cc, 10V. Effects of induced pulses from moving charges and diffusion are included, but not Landau fluctuations.

Nuclear Instruments and Methods in Physics Research A310 (1991) 189–191
North-Holland

Electrostatic simulations for the design of silicon strip detectors and front-end electronics

R. Sonnenblick, N. Cartiglia, B. Hubbard, J. Leslie, H.F.-W. Sadrozinski and T. Schalk
Santa Cruz Institute for Particle Physics, University of California, Santa Cruz, CA 95064, USA

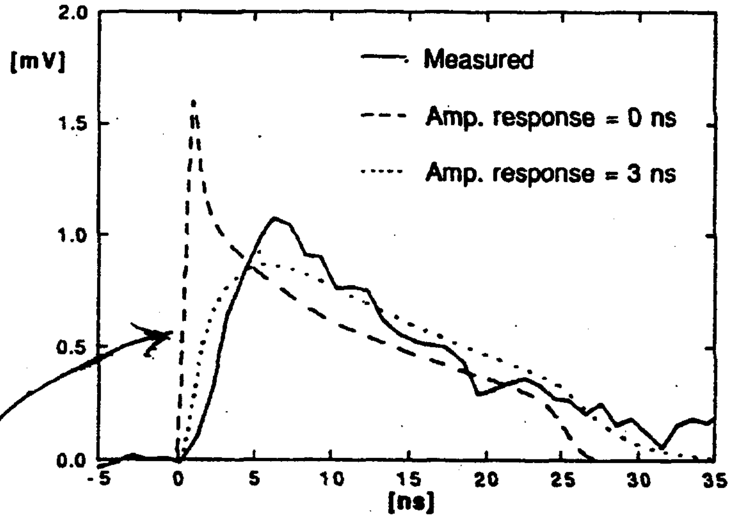


Fig. 3. Pulse shape at the junction side from a minimum ionizing particle. The three curves are the simulated current (with initial diffusion), the simulated current convoluted with the preamplifier response, and a typical observed pulse, respectively.

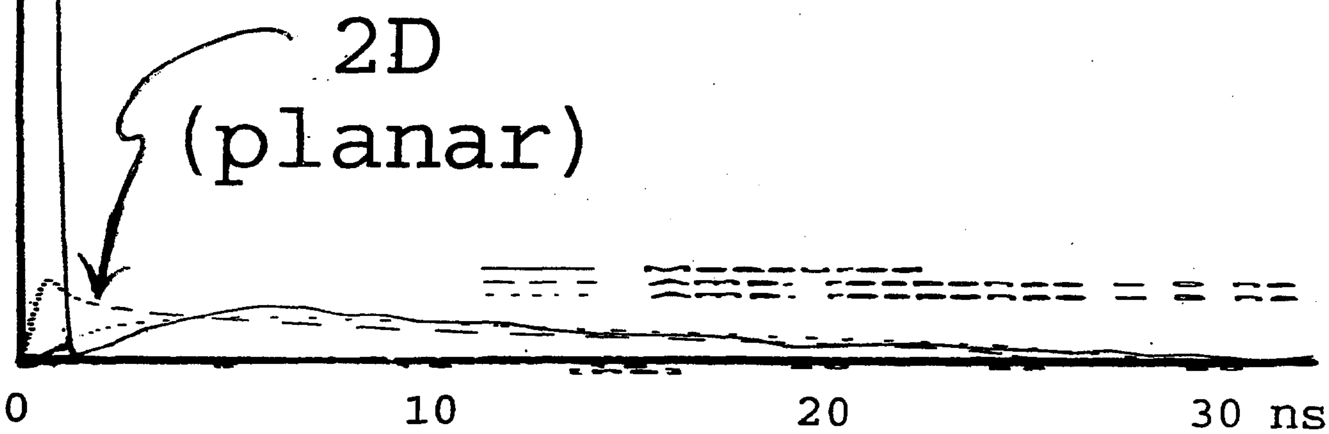
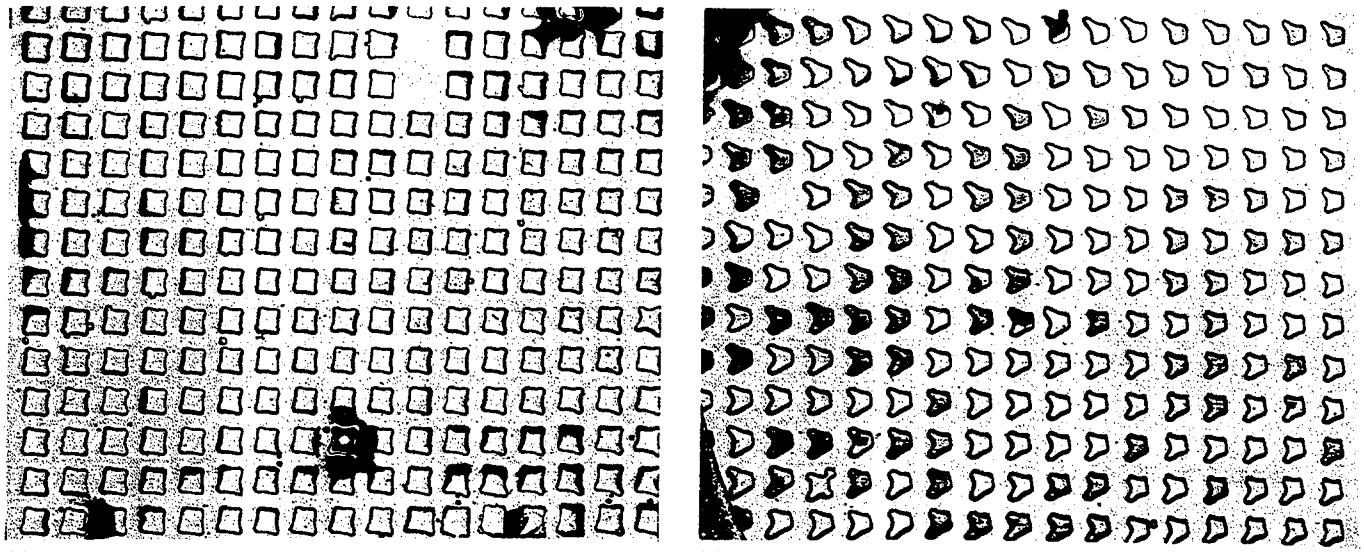


Fig. 5. Calculated pulses on a 3D p^+ electrode (from Fig. 4a) and on a standard 2D, planar electrode strip detector normalized to the same total area. The 2D arrows point to the 0 ns amplifier response curve, which has been xeroxed with the horizontal scale magnified to give the same time axis, and the vertical scale reduced so the area is the same as that of the 3D curve.



(a) (b)

FIG. 6. Cross sections of the p-type array in the n-type silicon cooler. (a) The cooler side of the wafer where the droplets were introduced (15×); (b) the hot side of the wafer where the droplets exited after thermomigration (15×). A slight off-axis thermal gradient used to preserve the registry of the array (Ref. 62) has modified the shape of the droplet trails.

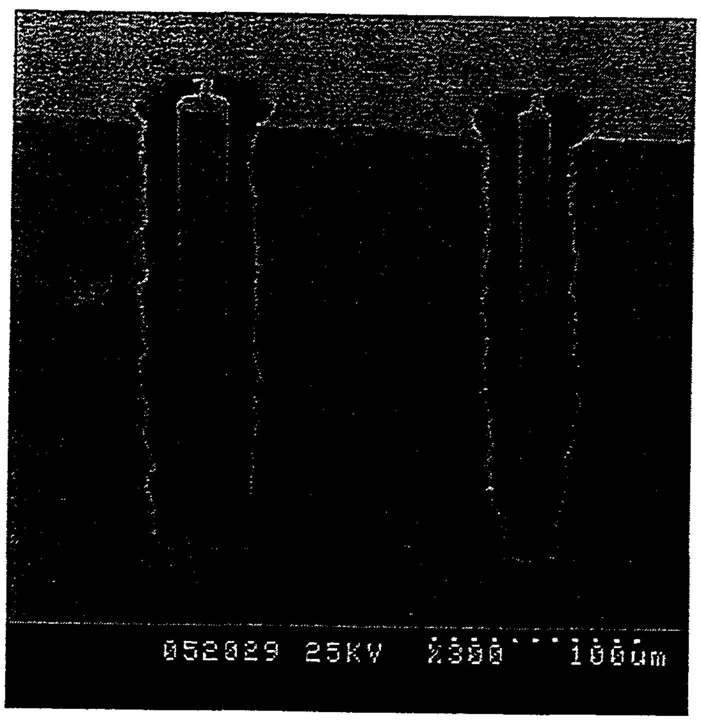


Fig. 7. Scanning electron microscope view of etched, poly-coated, 290 micron-high test structures. The scale at the lower right only applies to horizontal dimensions. Vertical ones are compressed by a factor of about 0.7.

D. The key fabrication tool

In the silicon industry, other than the now standard use of vertically oriented storage capacitors in RAM memories, only tentative steps have been taken since then in the development of 3D structures for integrated circuits [10]. However, intensive development work is underway in the use of VLSI techniques for the fabrication of 3D micro-mechanical structures. Many of these will be not only mechanical parts, but also sensors and actuators, and may also include integrated electronics [11].

Key to much of this work is a plasma etcher made by Surface Technology Systems (STS) [12] that can make vertical cuts at the high rate (for the VLSI world) of over 1 micron/minute. It uses an inductive coil to create the plasma, and a 13.56 MHz phase locked bias voltage to accelerate the ions toward the wafer. A fluorine based chemistry is used for etching. The operating conditions are cycled so etching alternates with the deposition of a protective coating on the sidewalls. STS has installed a machine at the Integrated Circuits Lab at Stanford University.

The method we plan to use to make 3D electrodes, is to etch holes, fill them with doped polysilicon, and diffuse the dopant out into the surrounding single-crystal silicon where the diode junctions will be formed. In an alternate method, the silicon surfaces would be doped first, then followed by poly filling.

E. Initial tests--etching the holes

Since the STS etcher was new, the first task was to characterize it. To do this--to measure its capabilities and determine the proper settings--we first etched arrays of holes and trenches of varying sizes. Optical microscopes with through-the-lens light systems have convergence angles that are far too large to illuminate most of the sides, let alone the bottom of the holes, and a depth of field that is far too small. Scanning electron microscopes have an adequate depth of field, but still have illumination and angle-of-view problems.

Sawing through the etched wafer (and some of the holes) provided the needed side views. Chipping along the hole edges produced several-micron irregularities which did not seriously degrade the diameter measurements. They did, however, leave some uncertainties in our knowledge of the smoothness of the hole walls. The test structures shown in Fig. 7, where cylindrical pillars are centered in 290 micron deep holes and connected to the wall by thin webs, solved that problem, since some saw cuts completely missed the pillars, which can be seen to have smooth, vertical side walls. After etching, but before sawing, the structures shown were coated with a 2 micron thick layer of poly.

Fig. 8 (top) shows the top, and Fig 8 (middle) the bottom, of the right column of Fig. 7. Both have radii of 7.9 microns. The lip at the top protrudes an additional 0.44 microns, while the radius halfway down (not shown) is 1.2 microns less, due, we believe, to thinning of the underlying silicon. Fig. 8 (bottom) shows the bottom of a similar column without the poly. The

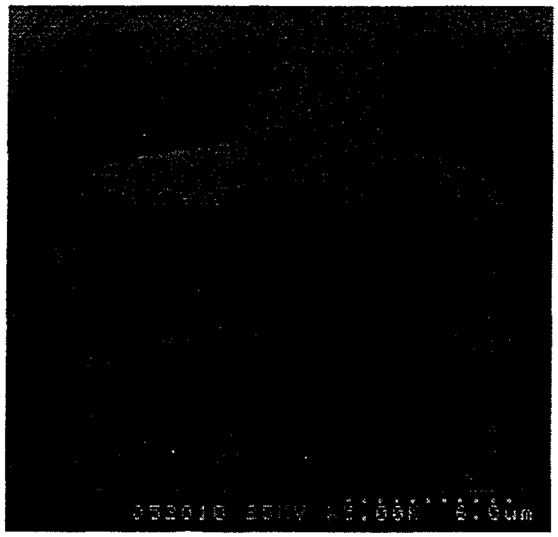


Fig. 8a

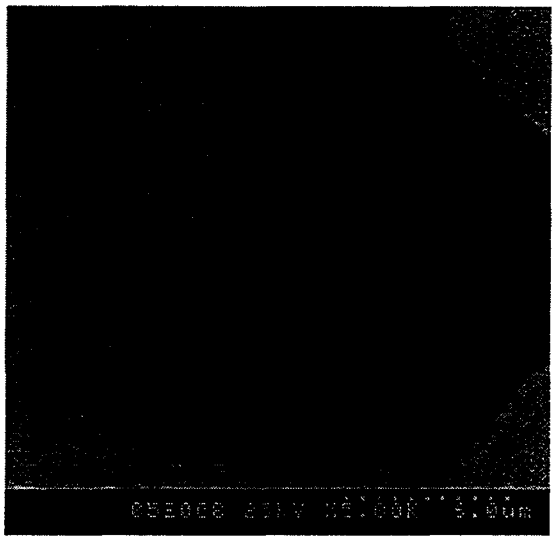


Fig. 8b

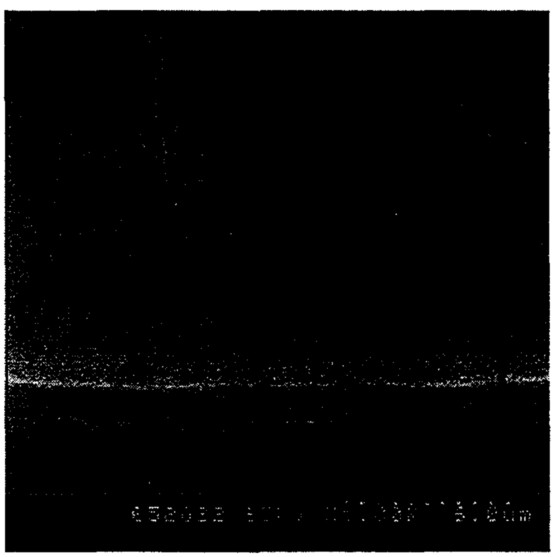


Fig. 8c

Fig. 8. High-magnification views of the (a) top, (b) bottom of the same column, and (c) of a similar column without the poly coating.

poly not only makes a highly conformal coating, but also a smoother one.

Fig. 9 shows saw cuts through typical holes. Fig. 10a, using data from those and many similar views, shows the depth reached as a function of etch time for four as-drawn (lithographic) diameters. Larger diameter holes etch more rapidly, as is particularly evident from Figs. 9a and 9c, since the reaction products must diffuse out of the holes. There is also an increase in diameter, shown in Fig. 10b, due to imperfect sidewall protection. This is the main reason the current depth-to-diameter ratio is limited to 11.5, as shown in Fig. 10c.

F. Initial tests--filling the holes

The holes are filled with poly to keep photoresist, which must be removed before high temperature steps, from being trapped there. That part of the fill for which the diffusion time out is shorter than the minority carrier lifetime, can also be sensitive to ionizing radiation. There are several ways to dope and fill the holes:

(a) They could be doped first and then filled using low-pressure chemical vapor deposition (LPCVD). Gaseous doping methods available at Stanford all form an oxide layer on the exposed silicon surface which could block charge collection from the electrodes. In addition, the poly deposition rate is reduced by the presence of mobile phosphorus atoms on the surface.

(b) They could be partially filled with poly, doped, filled with more poly, and annealed to drive in the dopant. Although there is evidence in the literature that dopants diffuse rapidly through polysilicon, the rate depends on the exact conditions of the poly deposition. With no oxide layer, signal charge could be collected from some or all of the poly electrode.

A series of test wafers was fabricated and sent to Solecon Laboratory for surface resistivity profile (SRP) analysis [13]. The SRP analyses, shown in Fig. 11a and 11b, demonstrate that LPCVD poly growth is not affected by the presence of an underlying glass, heavily doped with either boron or phosphorus. Rapid diffusion of both boron and phosphorus through poly and into the single-crystal bulk using our operating conditions has been confirmed by the SRP results shown in Fig. 11c and 11d.

G. The first fabrication run -- structures

The mask set being used in our first 3D fabrication run contains designs for 34 variations of 3D detectors and 6 sets of test structures. They include:

1. strip and pixel detectors with varying pitch, electrode diameter, guard-ring arrangement, and electrode pattern. Some pixel detectors have individual cells read out via wire-bond pads.

2. ATLAS pixels with bump-bond pads that fit the standard ATLAS cell dimensions, with 2 or 3 n-type electrodes per cell with spacings of 100 or 67 microns and the same number of p-type electrodes with the same pitch. These geometries should reduce the voltage required to fully

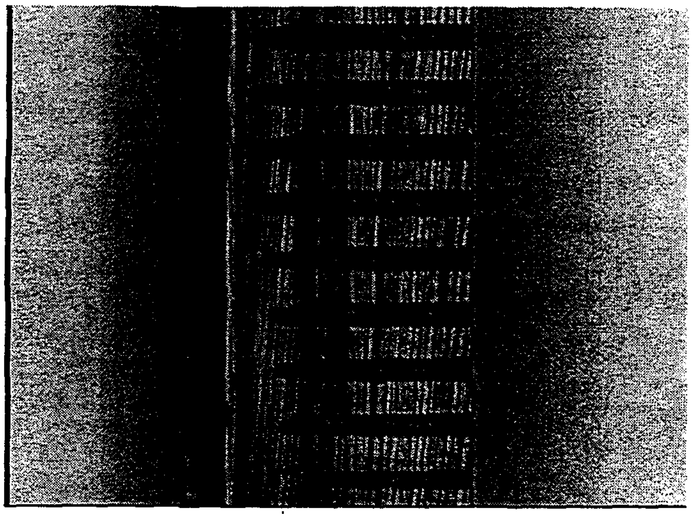


Fig. 9a

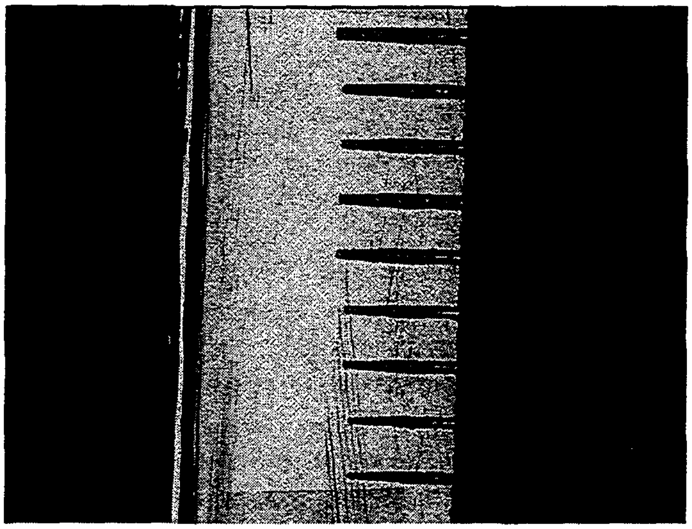


Fig. 9b

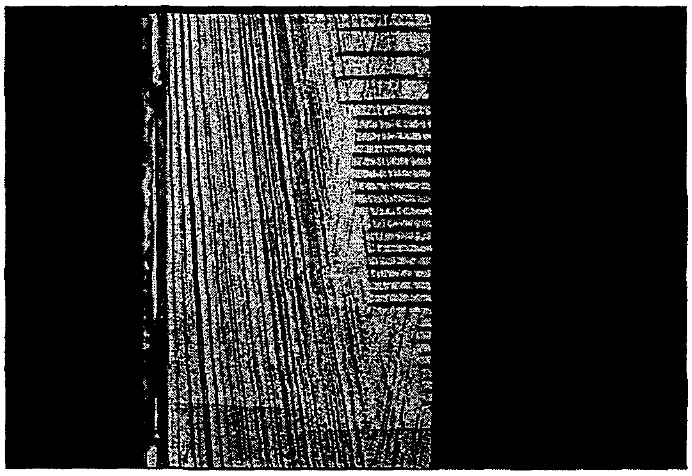


Fig. 9c

Fig. 9. A view of part of a set of etched holes, showing the increased depth reached by holes of larger diameters. The wafer was 540 microns thick and the etch time was 5 hours. The photo-mask hole diameters in Fig. 9a, from top to bottom are: 4 holes @ 30 microns, 4 @ 25 microns, and 1 @ 20 microns.

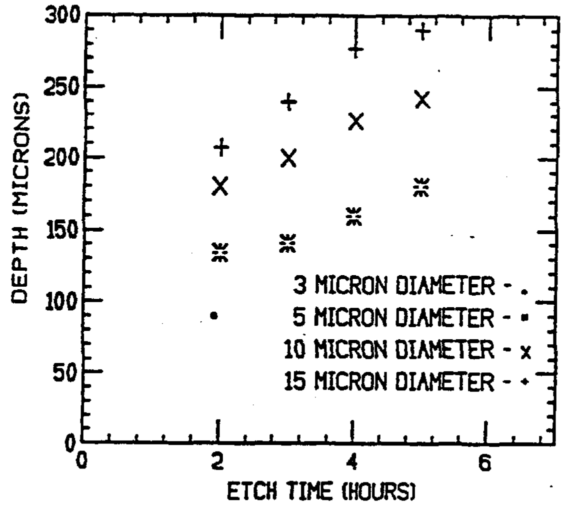


Fig. 10a

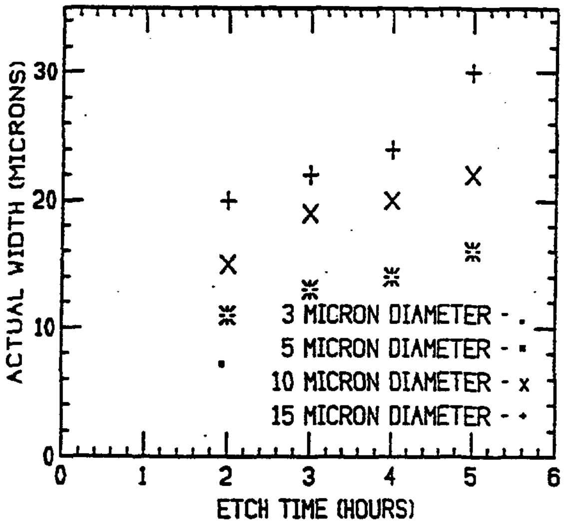


Fig. 10b

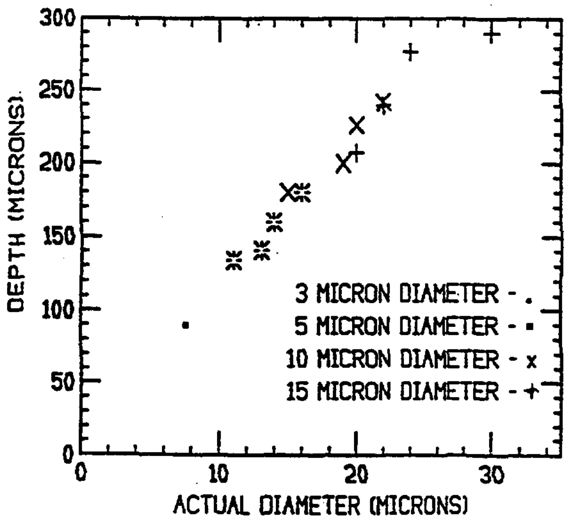


Fig. 10c

Fig. 10. Plots of (a) hole depths as a function of etching time, (b) actual hole diameters as a function of etching time, and (c) depth as a function of actual diameter for various hole diameters on the lithographic mask.

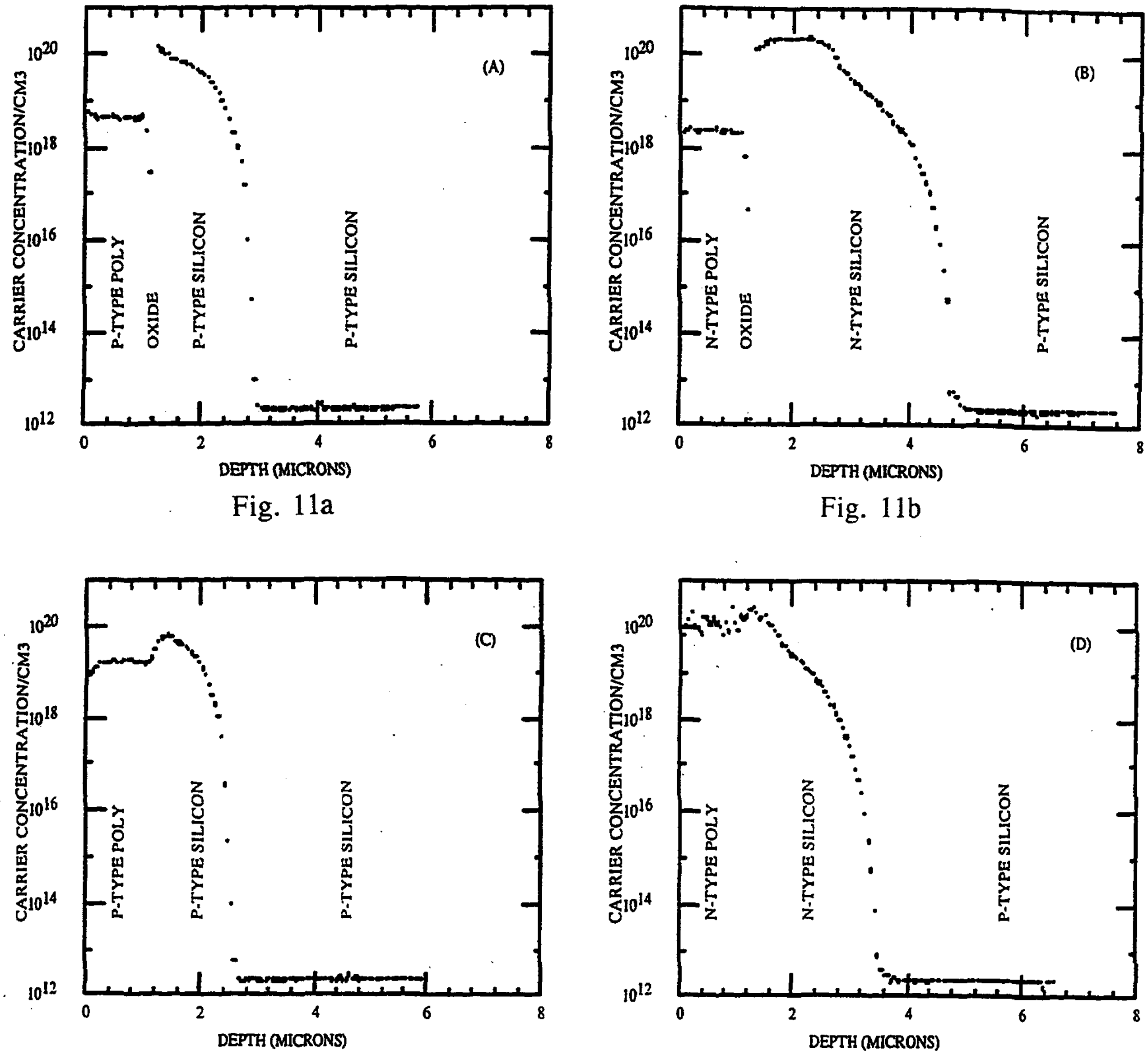


Fig. 11a

(B): N-TYPE POLY, OXIDE, N-TYPE SILICON, P-TYPE SILICON

Fig. 11b

(C): P-TYPE POLY, P-TYPE SILICON, P-TYPE SILICON

Fig. 11c

(D): N-TYPE POLY, N-TYPE SILICON, P-TYPE SILICON

Fig. 11d

Fig. 11. Surface resistivity profiles showing the net dopant concentration versus depth for high-resistivity wafers which have: (a) boron doping, then 1.2 microns of poly deposited, (b) phosphorus doping, then 1.2 microns of poly deposited, (c) 1.2 microns of poly deposited, then doping with boron, (d) 1.2 microns of poly deposited, then doping with phosphorus. As a final step all wafers were given a thin capping oxide and annealed for 3 hours at 1000° C.

deplete the detectors after bulk radiation damage by factors of about 8 and 15.

3. centimeter-long strip detectors using the same geometry as an ATLAS sensor, but with the individual 3D pixel cells tied together to form strips which can be read out via standard silicon strip readout electronics.

4. a small pixel array, using the ATLAS sensor geometry, which has each cell connected to a bonding pad, allowing the detector to be tested using aluminum-wire bonding to standard front-end electronics.

5. detectors in which the drift time within a cell is measured.

6. sets of parallel trenches and concentric cylinders to measure capacitance and current versus voltage, providing information on the leakage currents, depletion voltages, device capacitances, and the effects of radiation damage.

7. detectors with all electrodes of each polarity tied together, providing similar information for specific detector types.

8. structures to determine the conductivity of the electrodes, the resistivity of the aluminum and diffusion layers and of the contacts between them.

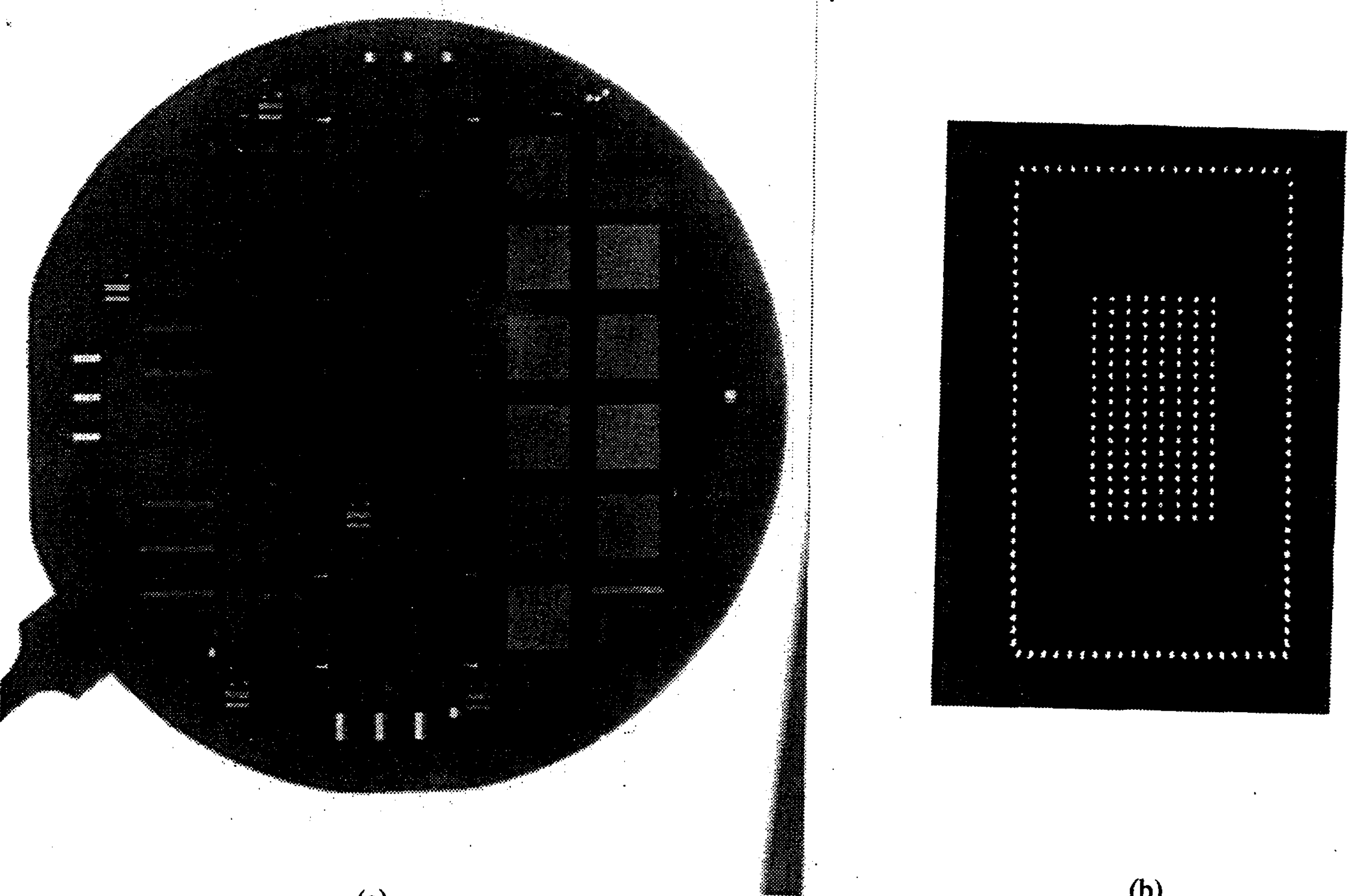
H. Initial fabrication run -- process steps

An overview of the steps for the first group of wafers in fabrication was given in [4]. Fig. 12a shows a wafer, held up to a ceiling light, after the first set of deep holes had been etched. The different levels of brightness correspond to the density of holes. Fig. 12b shows a magnified view of a single structure.

The smaller than expected depth-to-diameter ratio found in the initial etching meant a thicker layer of poly fill was required, and a defect in the deposition tube flowmeter resulted in a 17 (rather than 12) micron thick layer. This poly also covers the entire wafer prior to its removal in step 4, and caused a number of wafers in the original batch to break, particularly in the transition from a 120° C to a 20° C solution, which does not normally cause breakage in uncoated wafers. A magnified view of such a broken surface in Fig. 13 shows the poly filling the hole.

While processing on this run continues, a second batch has also been started using the steps given in Table 1. In this run, the holes will be only partially filled, using a thinner layer of poly, and the second, n-doped set of holes will be etched from the other side of the wafer.

Ultimately, we expect that current work on improvements in the etching parameters and the planned use of thinner wafers will result in smaller diameter holes that can be etched and filled from the same side. There are also milling machines using a directed beam of ions which should etch holes with higher aspect ratios, but the Integrated Circuits Lab does not now have one.



(a) (b)

Fig. 12. Photographs showing light passing through a wafer with the p-electrodes etched completely through: (a) a whole wafer and (b) part of a single structure. (The shadow at lower left is the tweezers holding the wafer; at lower right the edge of the ceiling light fixture.)

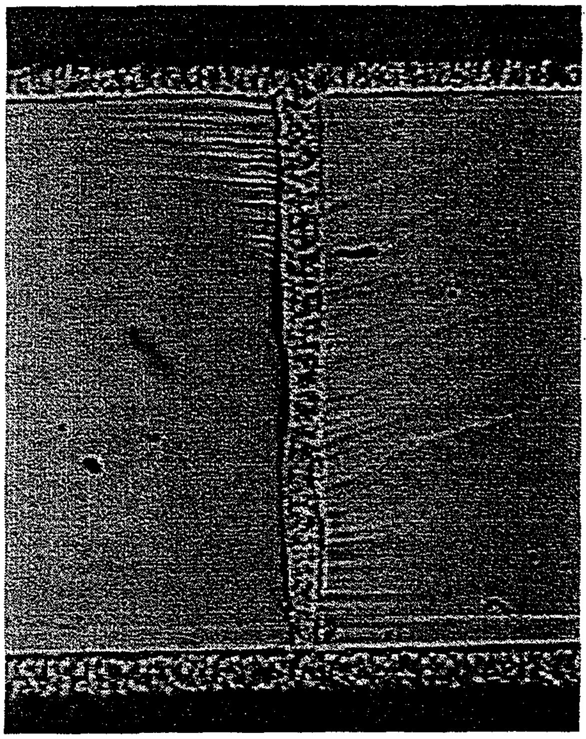


Fig. 13. Cross section of an electrode which has had 0.6 microns of poly deposited on its inner surface, had this surface heavily doped with boron, and then had the remaining hole filled with poly via LPCVD. The poly coat is visible on both the top and bottom surfaces as well as throughout the electrode. Some of the variation in the 23-micron-diameter electrode's profile is caused by the breakage plane not being parallel to the electrode's vertical axis.

Table 1:

STEP	MASK	PURPOSE	PARAMETERS
1	MASK1	MARKS TO ALIGN WAFERS WITH MASKS 2 THROUGH 6	1.2 MICRON THICK RESIST
2		ETCH ALIGNMENT MARKS	SILICON PLASMA ETCH, SF_6 / C_2ClF_5
3		INITIAL CLEANING OXIDE	GROW 0.4 MICRON WET OXIDE
4		ETCH TO REMOVE OXIDE	USE BUFFERED HYDROFLOURIC ACID
5		FIELD OXIDATION TO PROTECT AND PASSIVATE SILICON AND AS ETCH STOP	GROW 1.0 MICRONS OF OXIDE IN STEAM AT 1000 C FOR 5 HOURS
6	MASK2	N CONTACTS	PLASMA ETCH THROUGH OXIDE
7	MASK3	N-ELECTRODES	7.0 MICRON THICK RESIST
8		DEEP ETCH	HIGH-ASPECT-RATIO ETCH USING STS
9		DEPOSIT POLY GETTER LAYER	SiH_4 SOURCE AT 620 C, 0.46 Torr (2000A)
10		PHOSPHORUS DOPING	$POCl_3$ SOURCE, 30 MINUTES AT 950 C
11		DRIVE IN PHOSPORUS	30 MINUTES AT 1000 C
12		REMOVE POLYSILICON FROM TOP AND BOTTOM SURFACES	PLASMA ETCH
13		CAPPING/MASKING OXIDE	GROW 0.2 MICRON WET OXIDE
14	MASK4	P-ELECTRODES	7.0 MICRON THICK RESIST (BACKSIDE)
15		DEEP ETCH (BACKSIDE)	HIGH-ASPECT-RATIO ETCH USING STS
16		DEPOSIT POLY GETTER LAYER	SiH_4 SOURCE AT 620 C, 0.46 Torr
17		BORON DOPING	BBr_3 SOURCE, 30 MINUTES AT 955 C
18		DRIVE IN BORON AND PHOSPORUS	30 MINUTES AT 1000 C
19		REMOVE POLYSILICON FROM TOP SURFACE	PLASMA ETCH
20	MASK5	P CONTACTS	7 MICRON RESIST, LONG LOW TEMPERATURE BAKE TO SPAN HOLES, FOLLOWED BY PLASMA ETCH OF OXIDE
21		IMPLANT TO CONNECT P-ELECTRODE TO METAL	BORON, 20 KeV, 2E15/cm2
22		ETCH TO UNCOVER N CONTACTS	USE BUFFERED HYDROFLOURIC ACID TO REMOIVE STEP 13 OXIDE
23	MASK6	METAL DEPOSITION	DEPOSIT AND ETCH ALUMINUM

Table 1: Outline of 3D process steps.

We conclude with a few comments on some other possible applications of 3D technology.

I. Signal-to-noise ratio

The fast intrinsic pulse times, τ_{det}, can, with the proper circuitry, produce high signal-to-noise ratios, as the signal current is proportional to the detector speed. To make use of this increased current, the frequency response of the filtering must be extended. This increases the noise also, but only as the square root of the frequency spread. For example, the number of traversals per second, n, of a Gaussian noise current I_n with a positive slope past a threshold level I_t is given by [14]:

$$n = \left[\frac{\int_0^\infty \nu^2\, p(\nu)\, d\nu}{\int_0^\infty p(\nu)\, d\nu} \right]^{1/2} \exp\left(- I_t^2 / 2 < I_n^2 >\right)$$

For a filter, $p(\nu)$, that is flat from ν_l to ν_h, and with (typically) $\nu_h >> \nu_l$, we have:

$$n = [(\nu_h^3 - \nu_l^3) / 3(\nu_h - \nu_l)]^{1/2} \exp(- I_t^2 / 2 < I_n^2 >) \approx (\nu_h / \surd 3) \exp(- I_t^2 / 2 < I_n^2 >)$$

I_t can be set equal to a fraction a_1 of $< I_{det} >$.

$$I_t^2 = a_1^2 < I_{det} >^2 = a_1^2 < q/\tau_{det} >^2 = a_2\, \nu_{det}^2$$

Here q is the total charge and the a_i are constants that are independent, to first order, of ν. White noise currents in electronics capable of matching detector speeds will have $\nu_h \approx \nu_{det}$ and

$$< I_n^2 > = a_3\, \Delta\nu = a_3 (\nu_h - \nu_l) \approx a_3\, \nu_h \approx a_4\, \nu_{det}$$ (For a resistor, a_3 would equal 4KT/R.)

The threshold level squared can be increased in proportion to the detector speed squared, giving a near-exponential drop in noise counts that is proportional to the detector speed.

$$n = (\nu_{det} / \surd 3) \exp(- a_2\, \nu_{det}^2 / 2\, a_4\, \nu_{det}) = (\nu_{det} / \surd 3) \exp(- a_5\, \nu_{det})$$

A simple integrator, of course, will not benefit from this speed. The circuit must respond only to rapid changes in voltage on an integrating capacitor, or to high instantaneous currents in a resistive circuit.

J. Other materials

There are a number of other materials where the short collection distances and potential speed of 3D technology may prove useful. Two examples are GaAs and diamond detectors.

The HERA report quoted in the introduction, after discussing radiation damage problems, goes on to say: "Recognizing the potential of diamond detectors, members of the VDS groups have joined the R&D efforts of the RD42 diamond tracker group."[3]. Diamond detectors produce about half as many electron-hole pairs per radiation length as silicon. They have continued to improve through the years, with a 1/e collection efficiency distance that started from zero in 1991, and now is somewhat larger than 200 microns [15].

Given the smaller amount of generated charge, high collection efficiency for all of the 250-300 micron thickness would be desirable -- that is a mean travel distance before capture of perhaps 700 microns using planar technology. 3D technology (using oxygen as well as SF_6 for etching) would already provide high collection efficiency with existing material. Given the very high mobility of electrons in diamond, it would also provide sub-nanosecond pulse rise times.

K. Active Edge Technology

Both pixel and silicon strip detectors made with planar technology must design in dead regions around the edges to allow for edge chipping made during the saw cuts. Also, the electrodes must be kept still further from the edges, so the bulging-out of the depletion region edges stays away from the saw cuts, since the latter are conductive due to their dangling bonds. In addition, the extensive array of guard rings needed to drop the voltage between top and bottom electrodes in a controlled fashion takes space, often more than the depletion region bulge below them. When bulk radiation damage requires high operating voltages, this array uses a significant amount of room.

For example, the current Atlas pixel detector units will loose 15% to 20% of their surface area to these causes [16]. Some proposed imaging systems use silicon strip detectors edge-on to form x-ray images in, for example, mammography [17]. Even in optimized designs ten to twenty percent of photons in the typical mammography spectrum are absorbed in this dead layer.

Cutting out individual detectors with the plasma etcher will eliminate the chip problem for any type of detector. 3D detectors operate at low voltages, and have the same voltage at corresponding points on top and bottom surfaces. Even if guard rings are needed on the surfaces around each electrode, they will not need much area, and the electrodes continuing below the surface will make the silicon volume below them sensitive. This may allow the fabrication of detectors that are fully active right to their edges.

Two types of edges will be studied: doped edges with a coat of doped poly, which can then be held at a definite voltage, and oxide-passivated ones in which the edge potential is set by a combination of fixed charges and by leakage currents.

L. Application of 3D technology to pixel detectors

While monolithic pixel detectors [18] have many advantages, they also have a number of disadvantages:

(a). only pmos electronics could be put in the pixel; nmos had to be along the edges, (b). they are slow; with collection times in the 100 ns region being common along inter-pixel boundaries,

(c). radiation-hard technology, while compatible with pixel fabrication, has not actually been developed for it, and

(d). they employ new technology and so can not be assembled from commercial parts.

Combining 3D and monolithic pixel process steps will permit designs that will eliminate the first two disadvantages and in addition, provide the radiation hard bulk characteristic of 3D devices. The circuit would still have to be hardened, using generally known, but not yet developed steps.

* Current address: Heuristic Physics Laboratories, Inc., 1649 S. Main St. Milpitas, CA 95035

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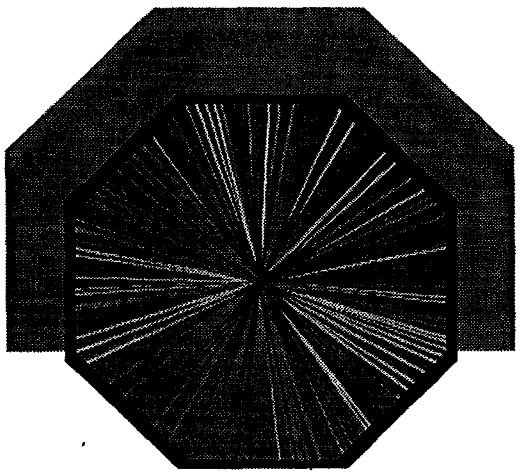
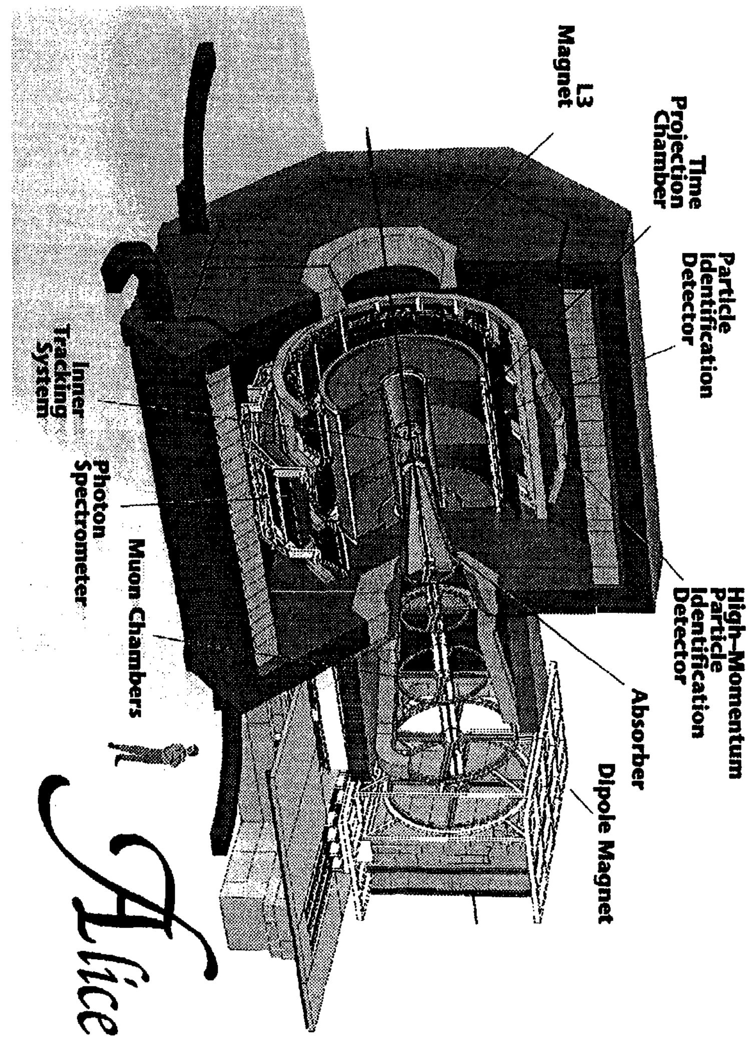
Mechanics and Cooling of the ALICE Inner Tracking System

W. Klempt for the ALICE Collaboration



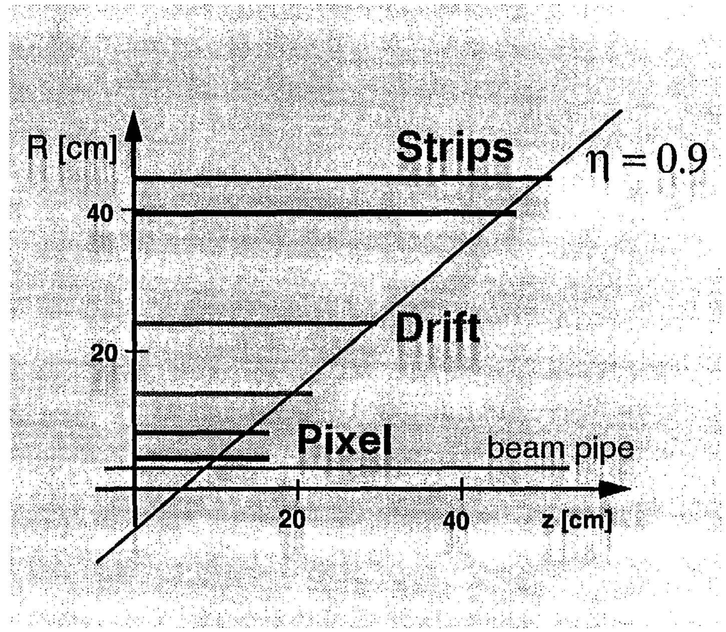
- Layout and Design of the ITS
- Silicon Pixel Detector
- Silicon Drift Detector
- Silicon Strip Detector
- Alignment
- Conclusion



ALICE schedule

- 1997 - 1998
  - R&D, design, prototypes
- July 1998 - June 1999
  - Technical design reports
- 1999 - 2003
  - Production
- 2002
  - L3 dismantling
- 2003
  - Pre-assembly & test in SXL hall
- 2004
  - Installation in P2 experimental area
- 2005
  - 6 month comissioning of detector
  - Ready for pp beam mid 2005

ITS main Parameters



	$\sigma r\phi$ σz μm		No. of Ch. k	Area m^2	Power W	X_0 %
Pixel	15	90	15727	0.26	500 (100)	1.26
Drift	20	30	192	1.26	2000 10[illegible]	(1.13)
Strips	30	860	2620	5.12	1800 1000	1.74

ITS Responsabilities

- **Pixels**

  Bari, Catania, CERN, Padua, Rome, Salerno

- **Drift**

  Catania, Jyväskylä, Ohio, Rez, Turin, Trieste

- **Strips**

  Kharkov, Kiev, Nantes, Strasbourg, Turin, Utrecht-NIKHEF

- **Mechanics, Cooling and Alignment**

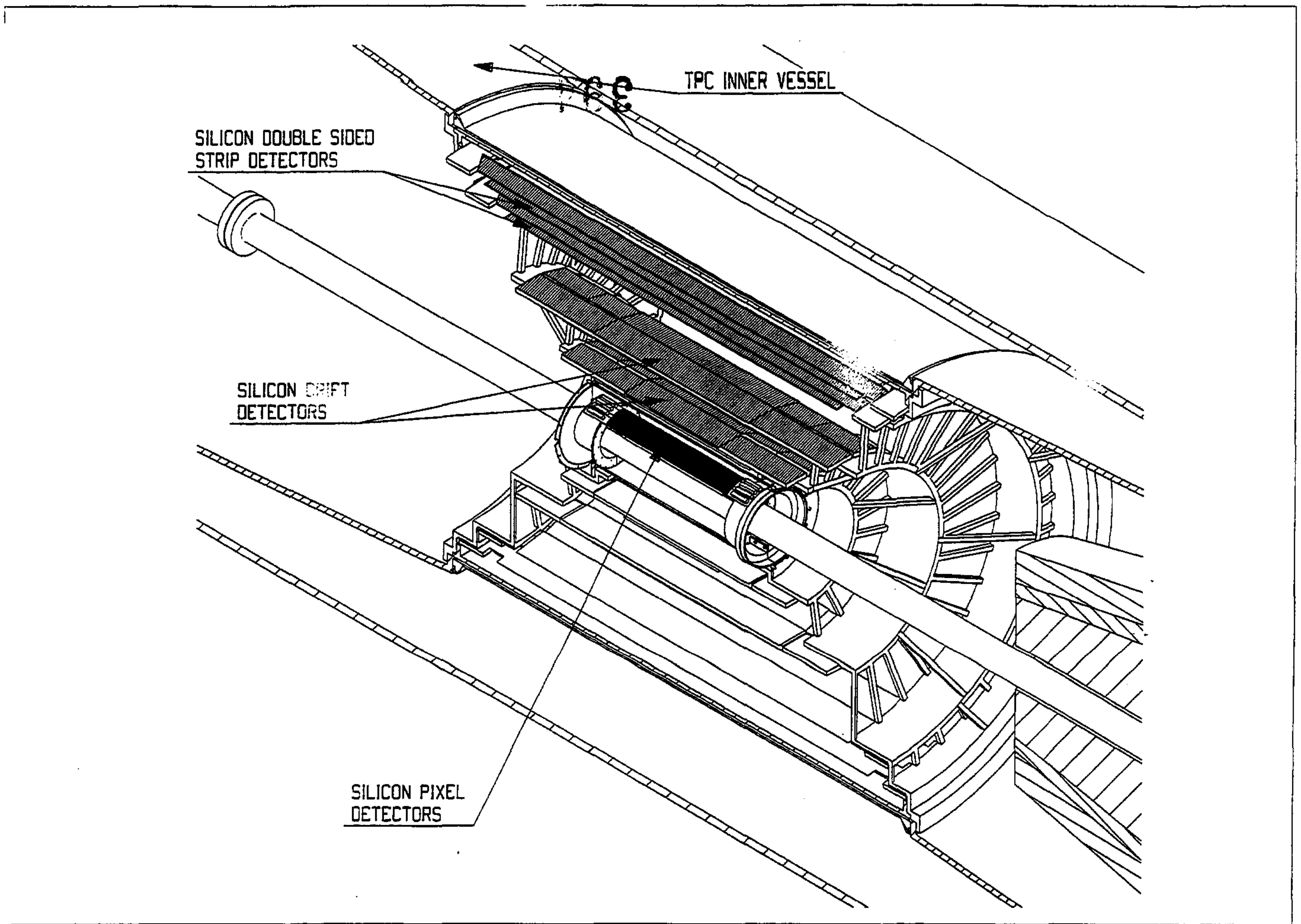
  Jyväskylä, Nantes, Padua, St. Petersburg, Turin, Utrecht-NIKHEF

General Design Concepts

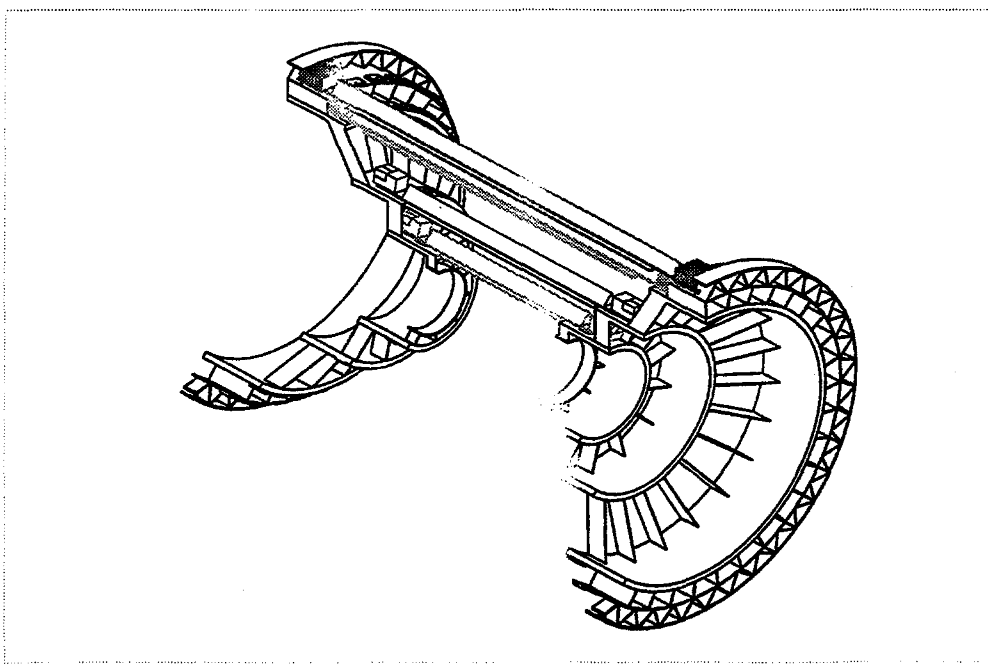
- Material:
  - minimize radiation length
    high Young modulus
    => use unidirectional carbon fibre
  - Optimize thermal and mech. properties
    =>cyanate resin
  - maximise fibre/resin ratio

- Geometry:
  - minimize material for required stiffness
  - reasonable modularity for maintenance

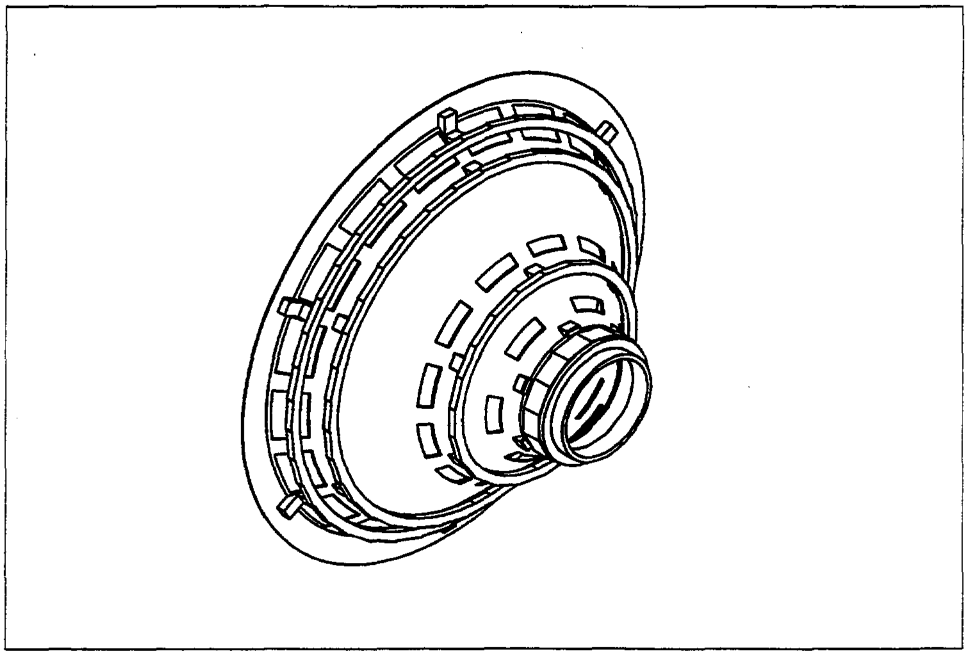
- Operation at Room Temperature:
  - Minimize power consumption in barrel
    => div. of FEE in barrel and end-cap part
  - "leakless" water cooling for Pixel & Strips
  - evaporative C_5F_{12} cooling for Drift

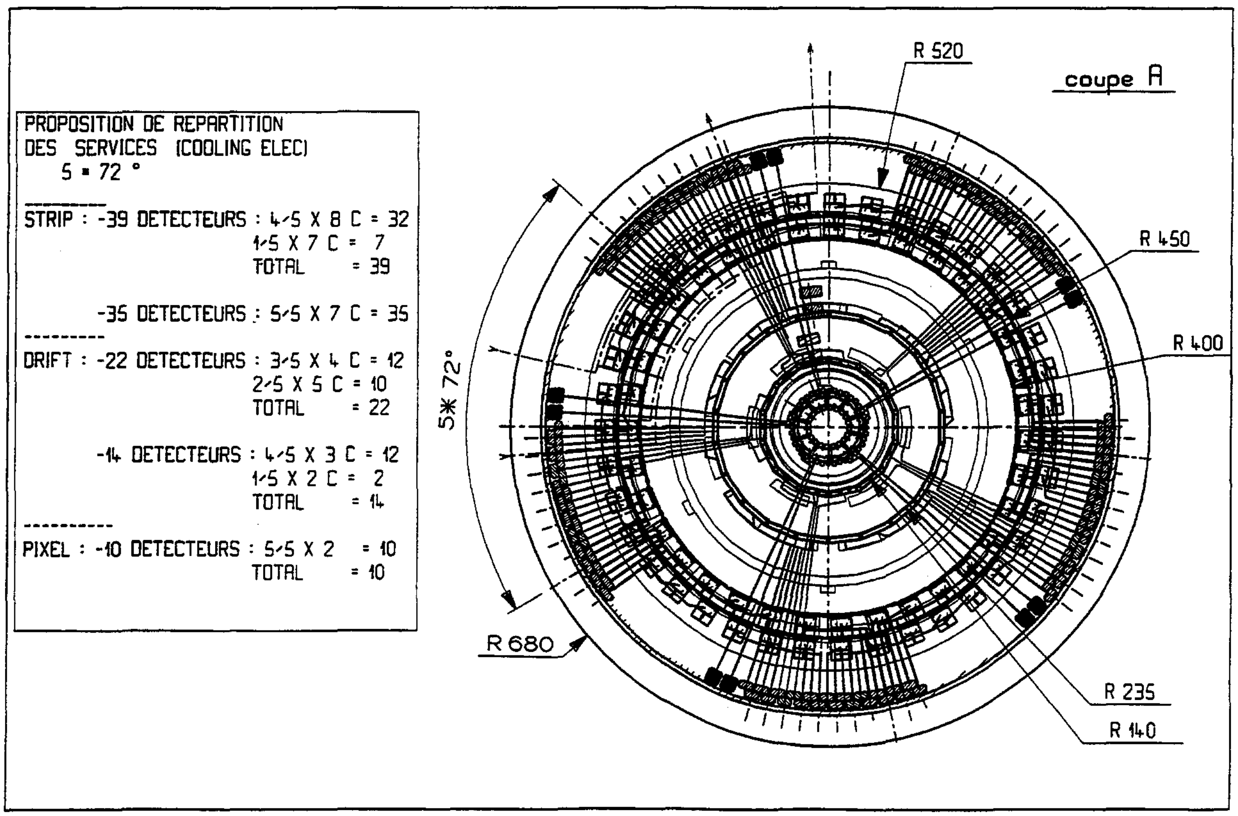


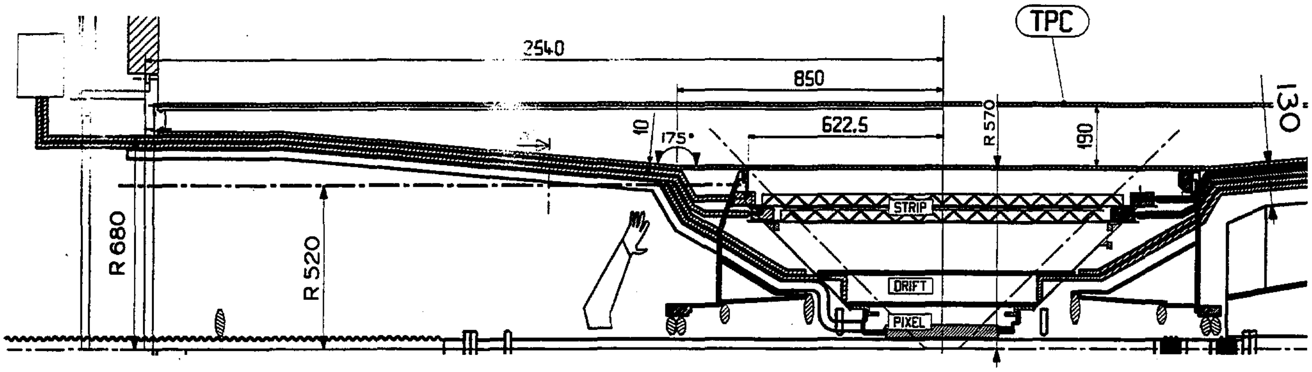
ITS Mechanics



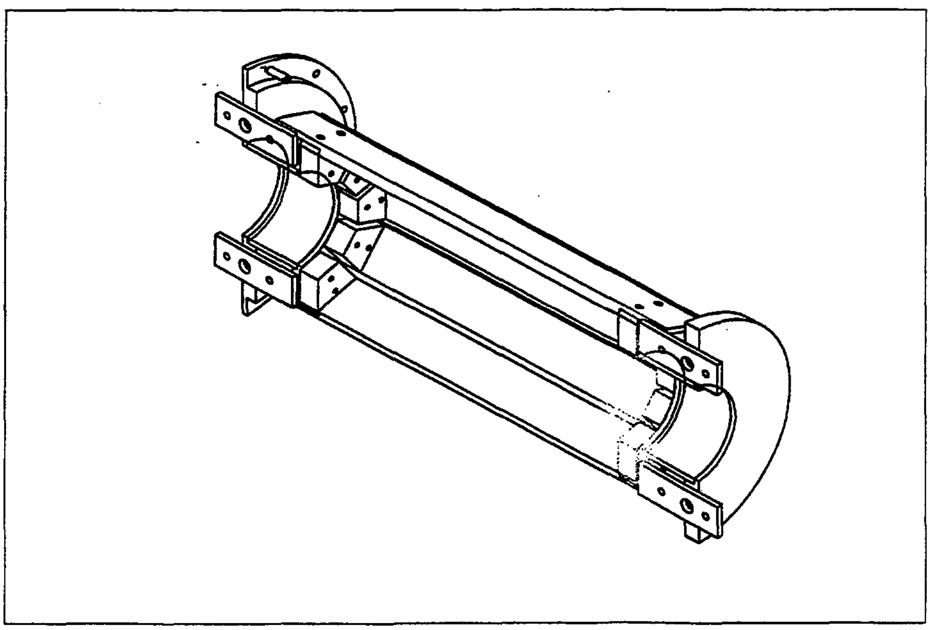
ITS End Flange

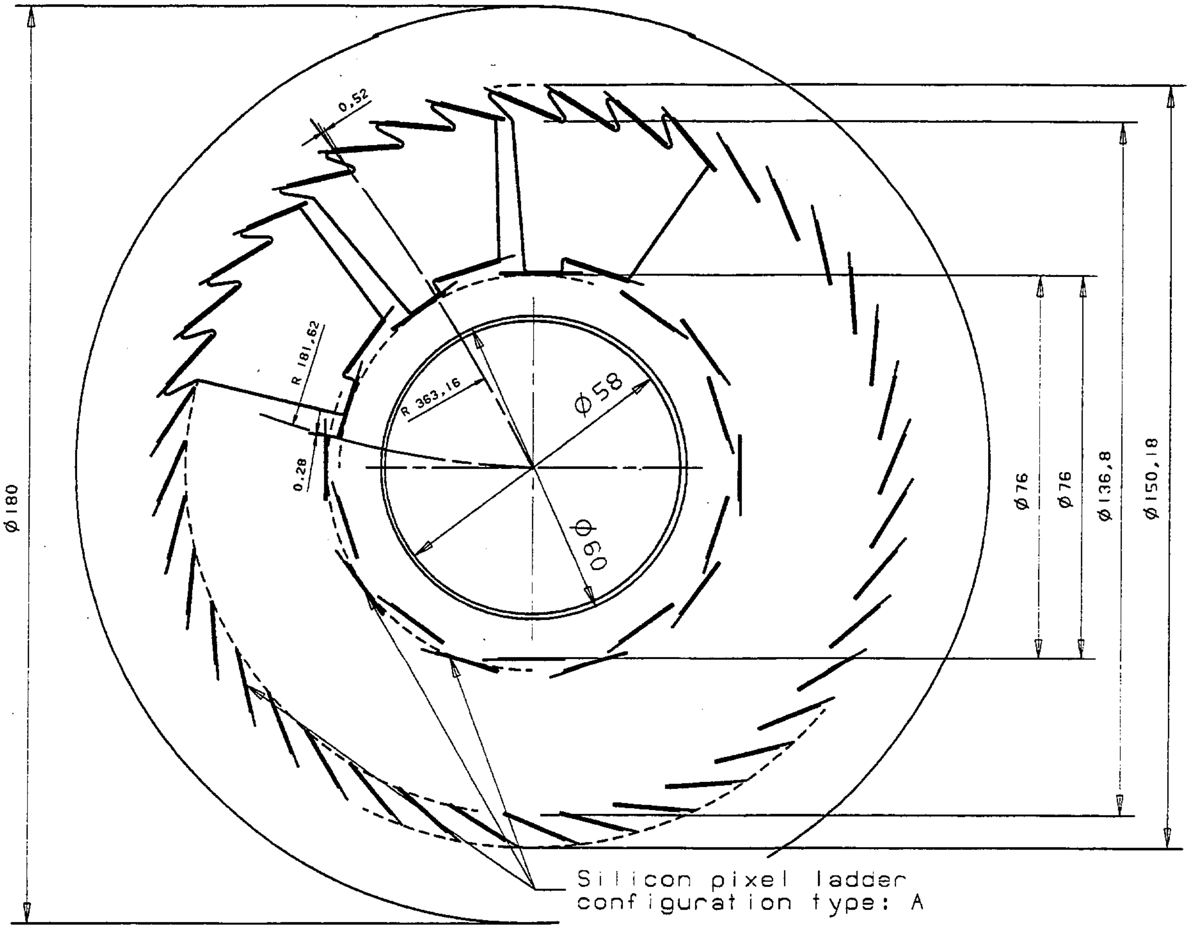


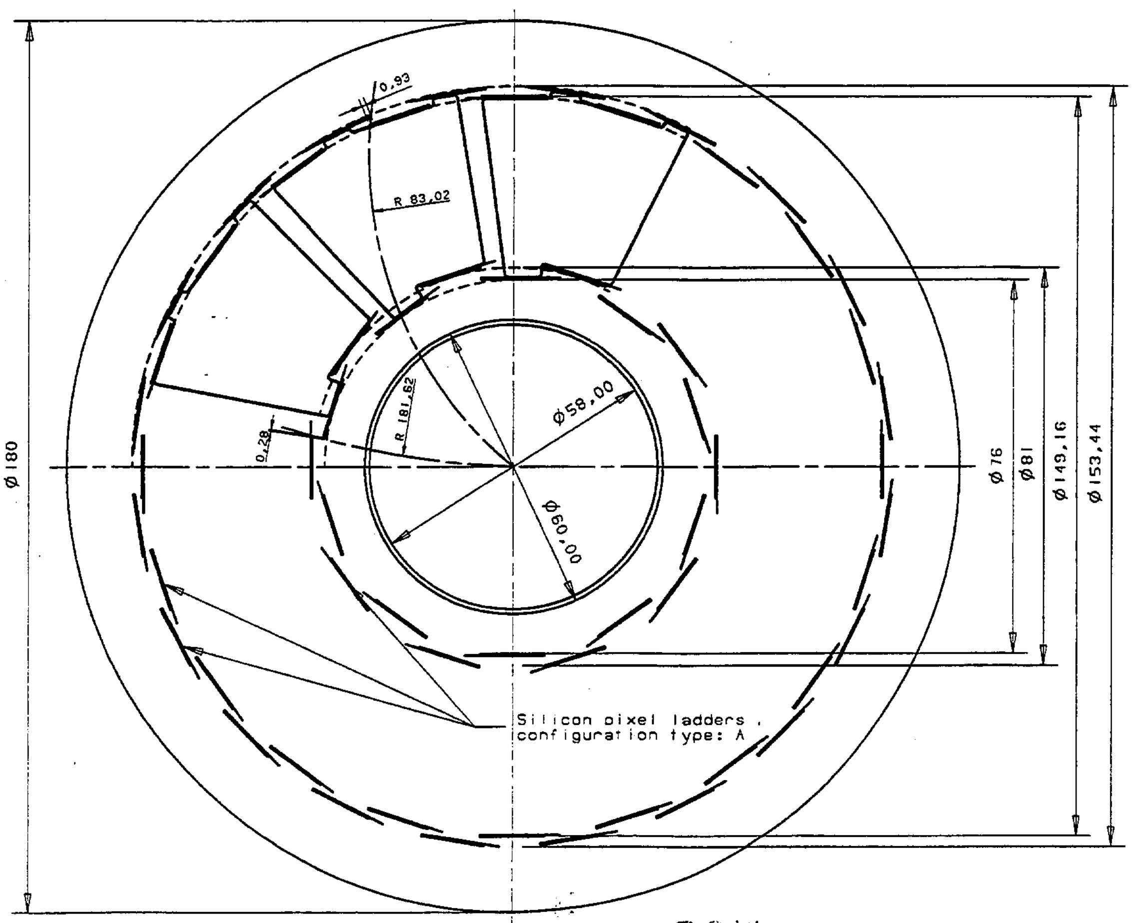




Pixel Mechanics

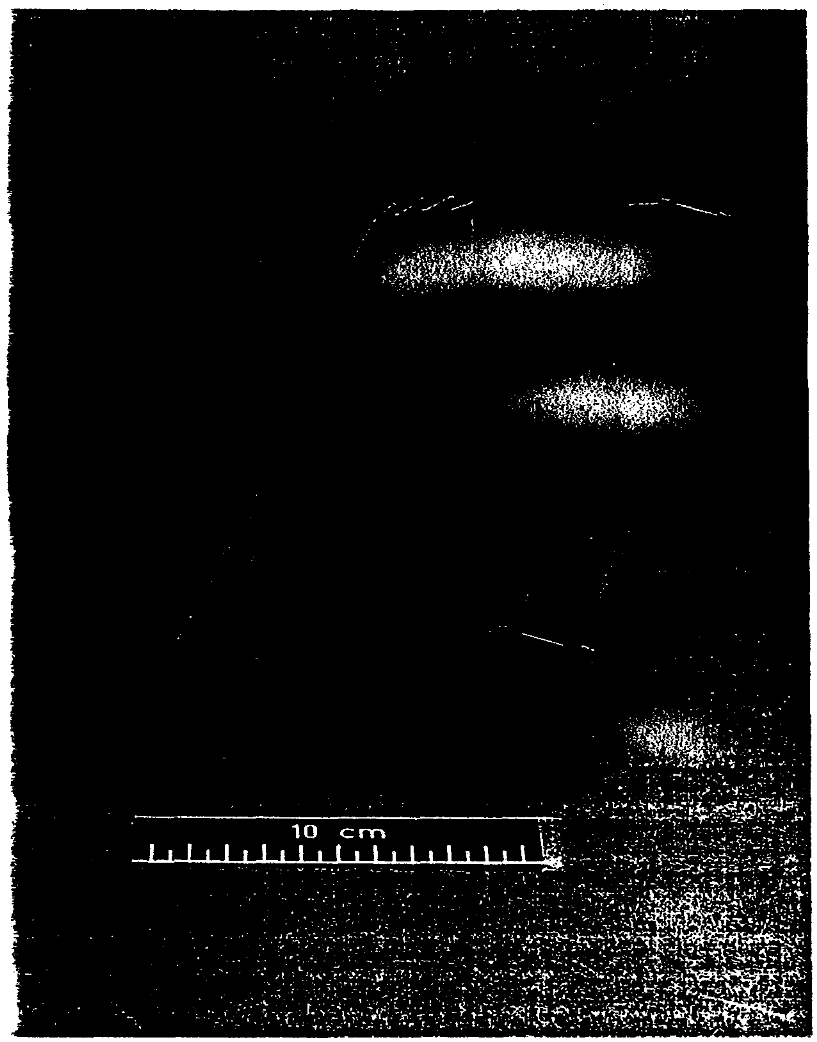



0,52
R 181,62
R 363,16
Ø58
0,28
Ø60
Ø180
Ø76
Ø76
Ø136,8
Ø150,18
Silicon pixel ladder
configuration type: A


0,93
R 83,02
R 181,62
Ø58,00
0,28
Ø60,00
Ø180
Ø76
Ø81
Ø149,16
Ø153,44
Silicon pixel ladders ,
configuration type: A

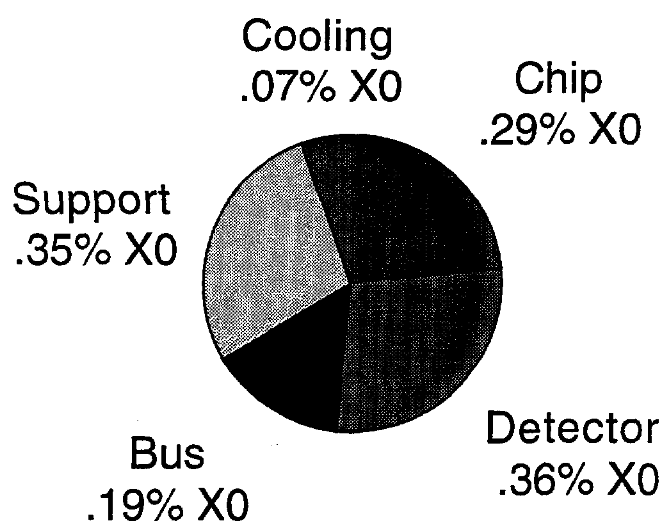
Pixel Ladder Prototype

View of a sector of the pixel ladder structure according to two different ladder disposition:
turbo like ladder disposition;
super posed ladder disposition.

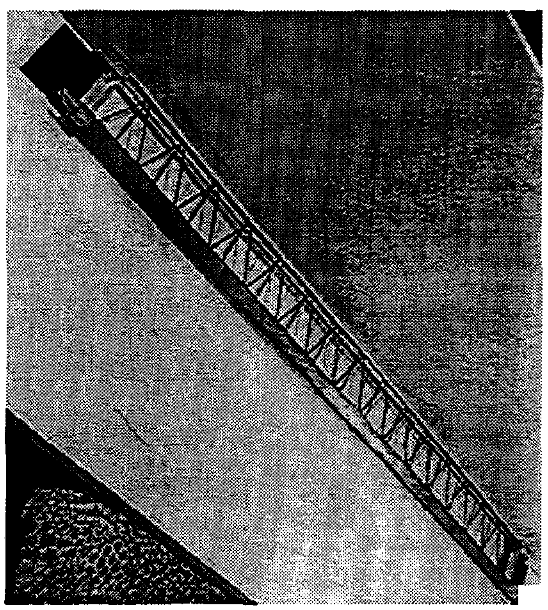


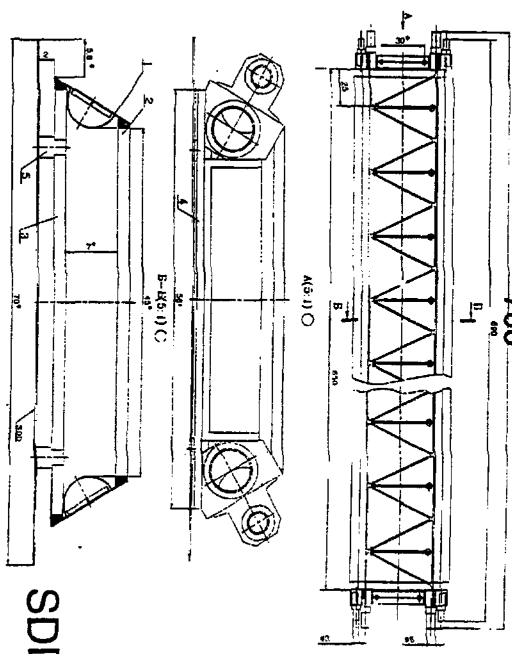
Pixel Material Distribution

Average material seen by a particle traversing both layers = 1.26%X_0



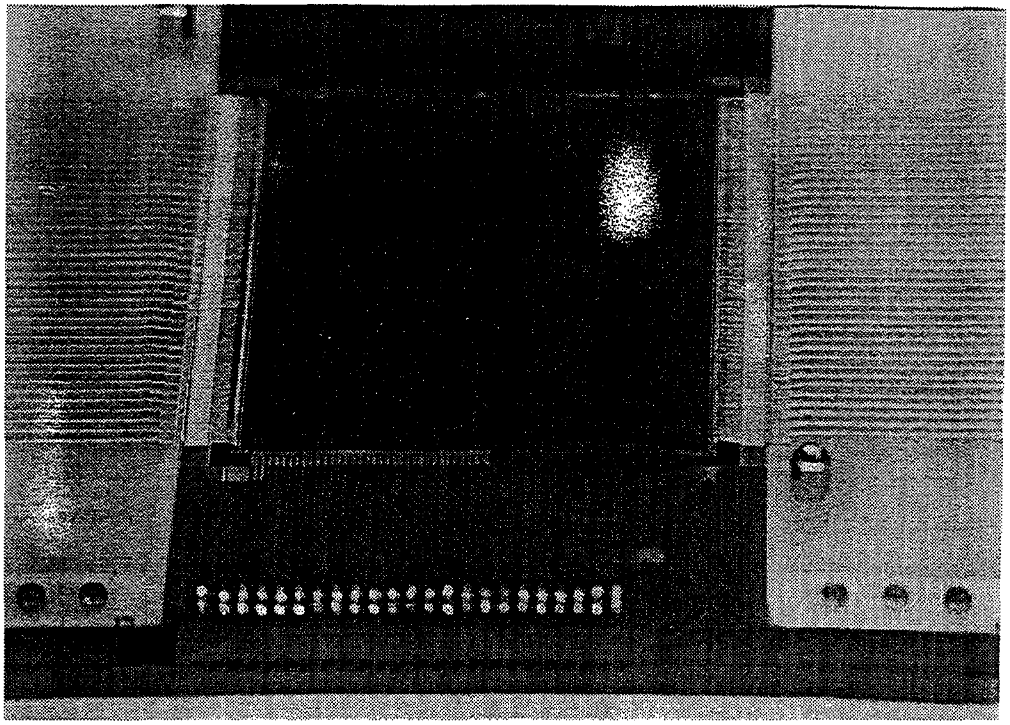
Drift Ladder Design





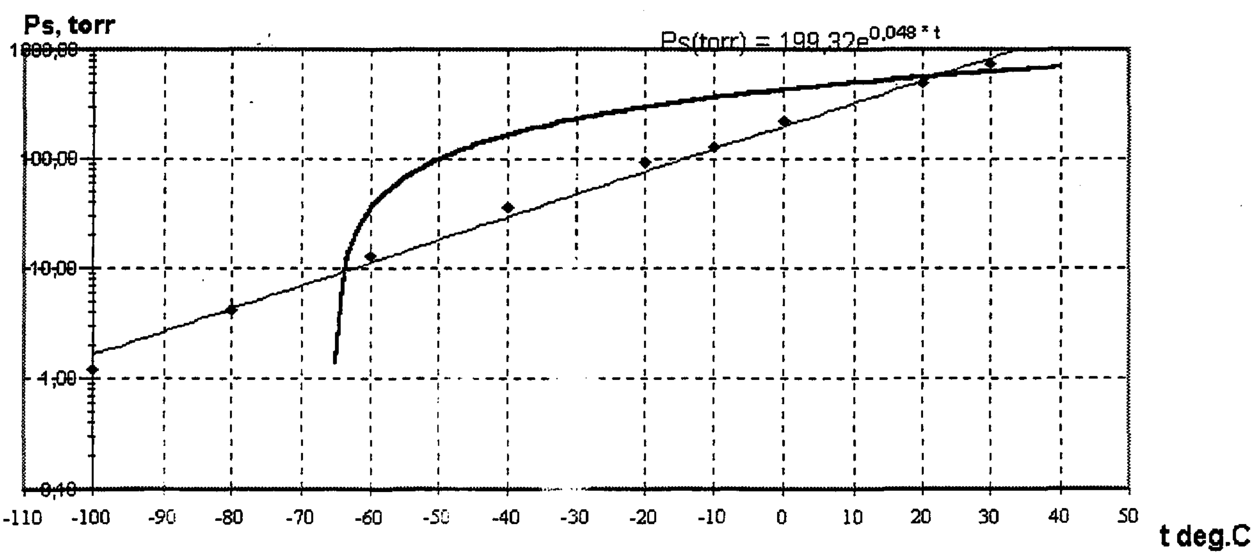
SDD

Silicon Dr[illegible] Detector

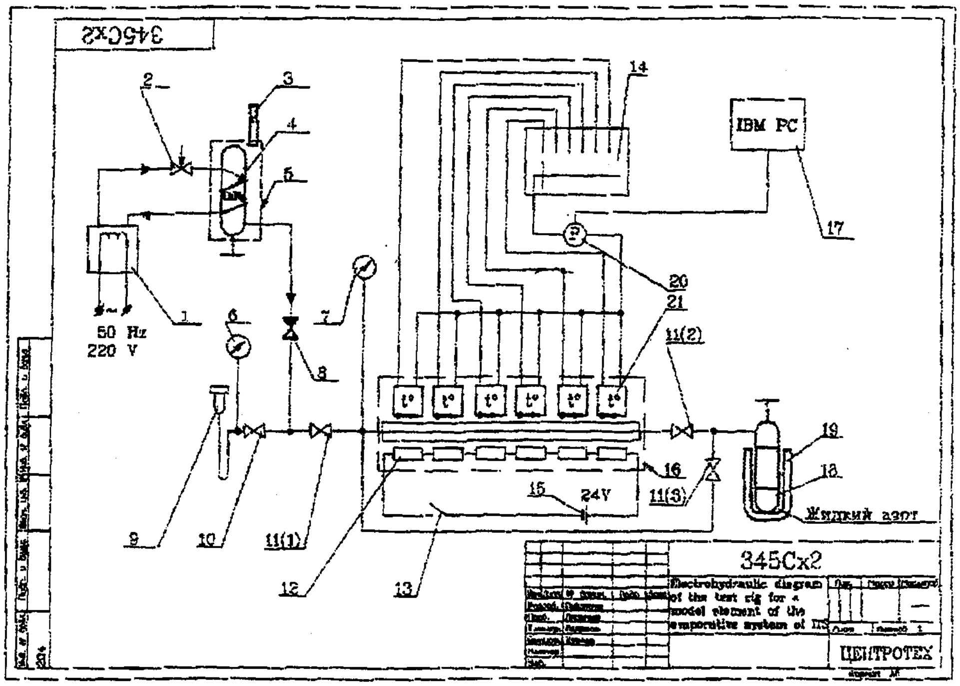


C_5F_{12} Vapour Pressure

Saturated vapor pressure for FC5050 (C5F12) vs. temperature

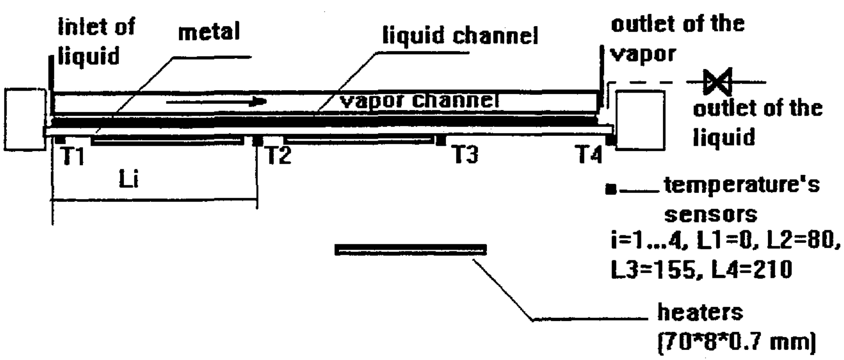


Cooling Test Plant

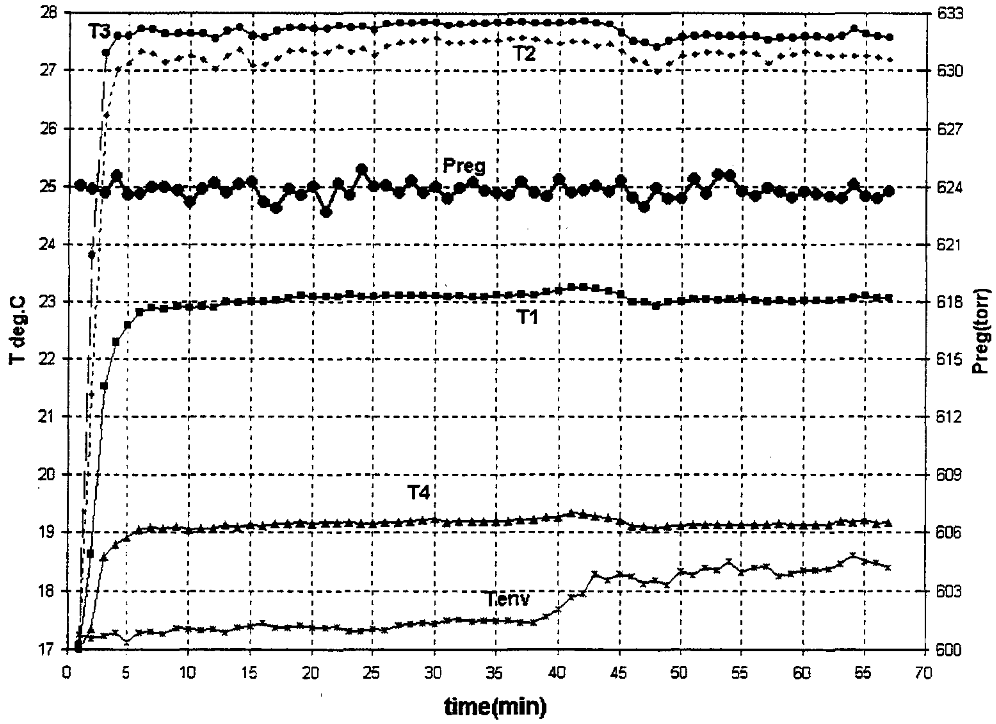


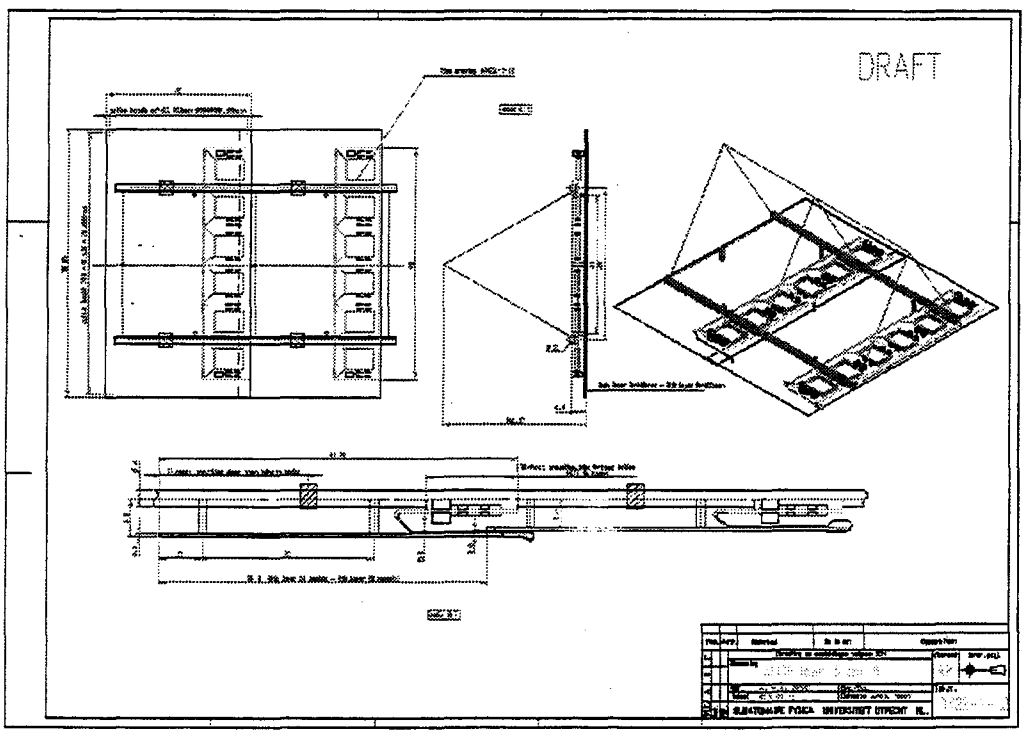
Evaporative Cooling Test Setup

Model of the evaporative cooling artery (ESQ)



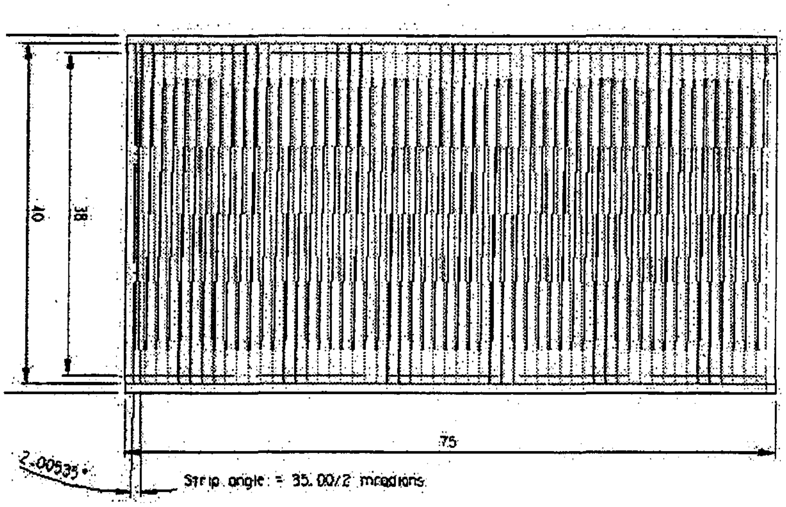
Cooling Test Results

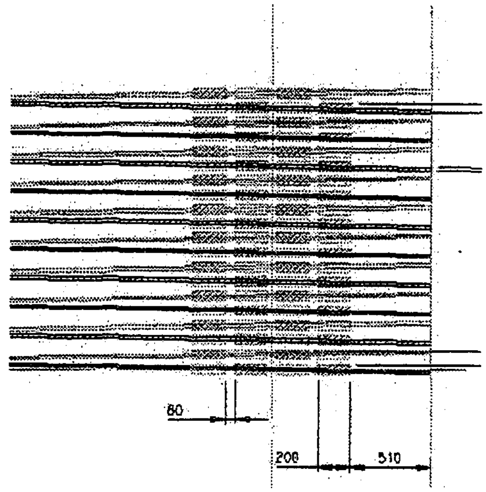




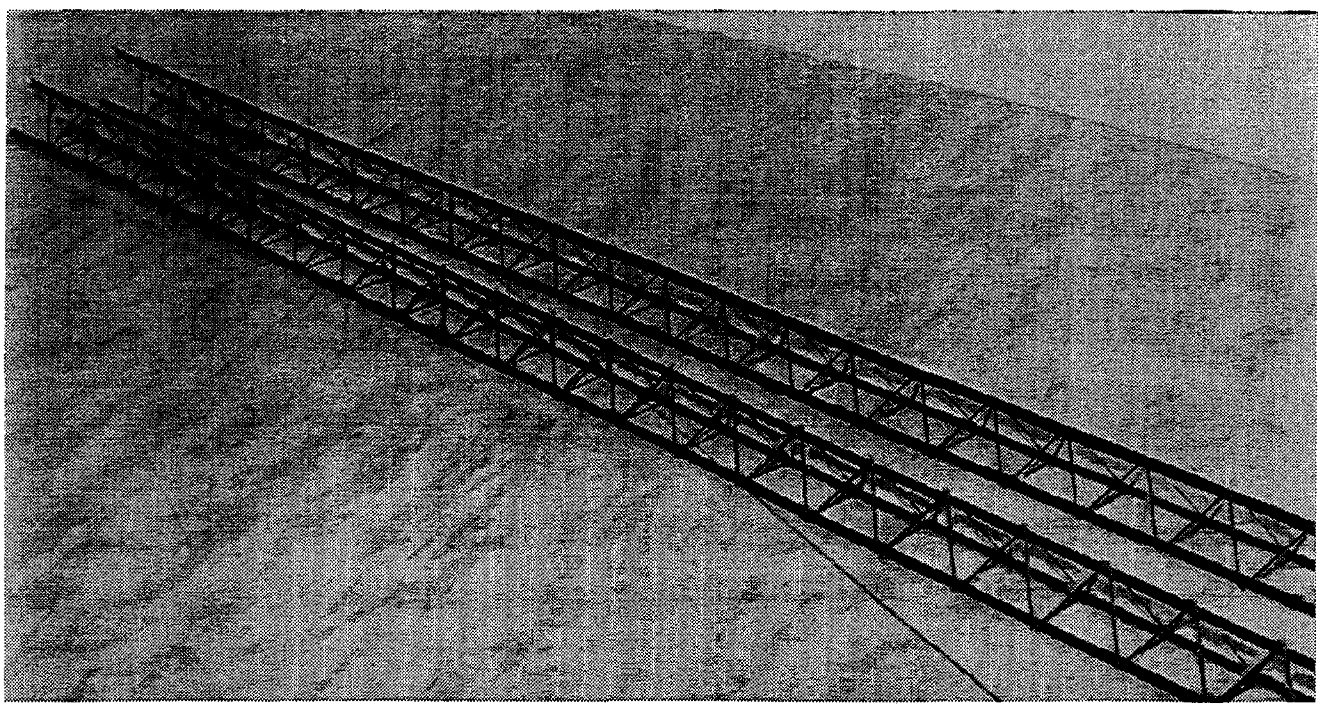
402

Strip Detector



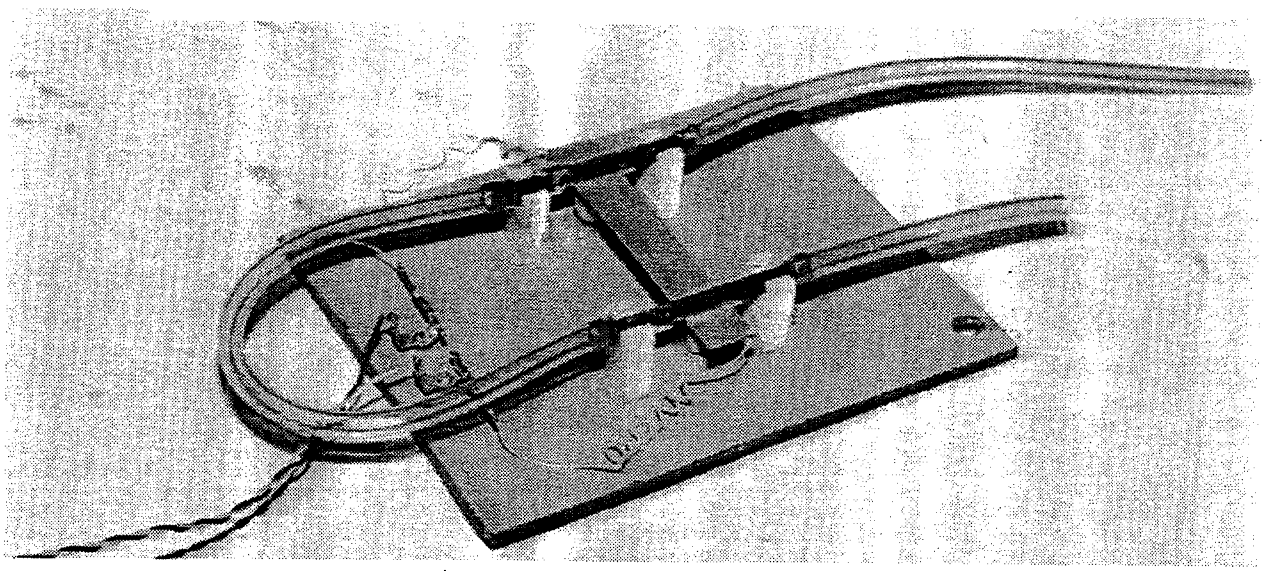


Ladder Prototypes

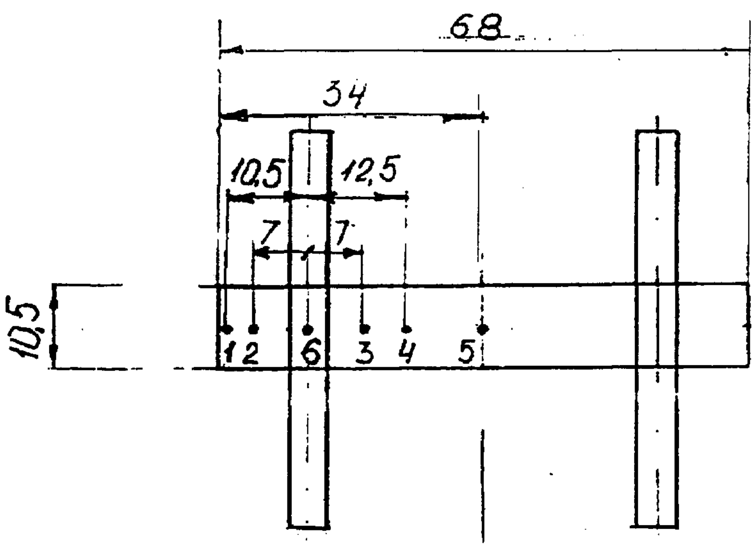


Strip Detector Cooling Test

Use of high thermal conductive carbon fibre

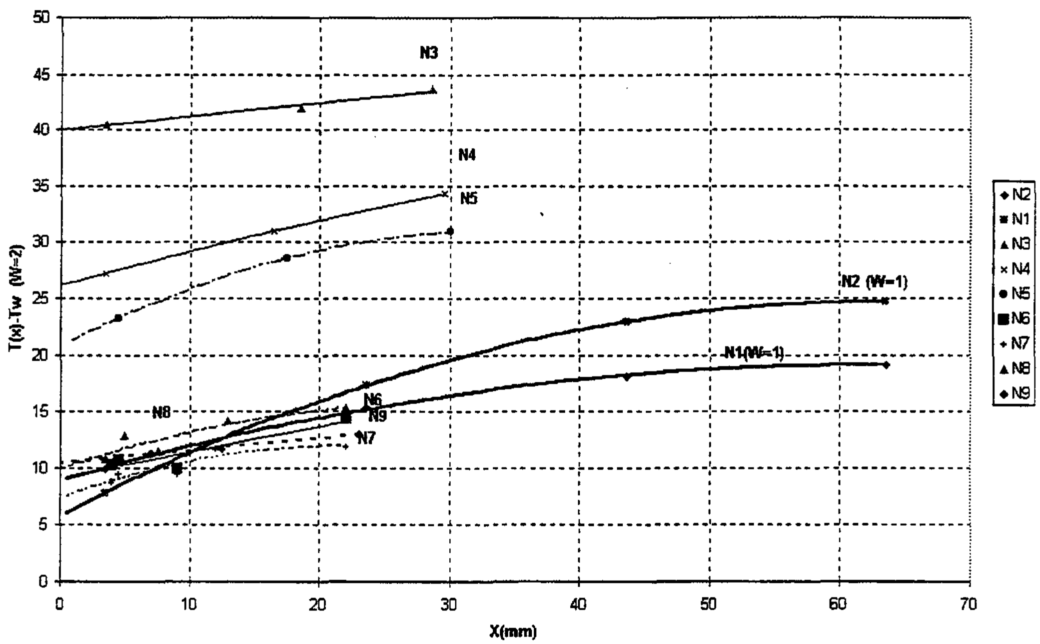


Heat Bridge Test Setup



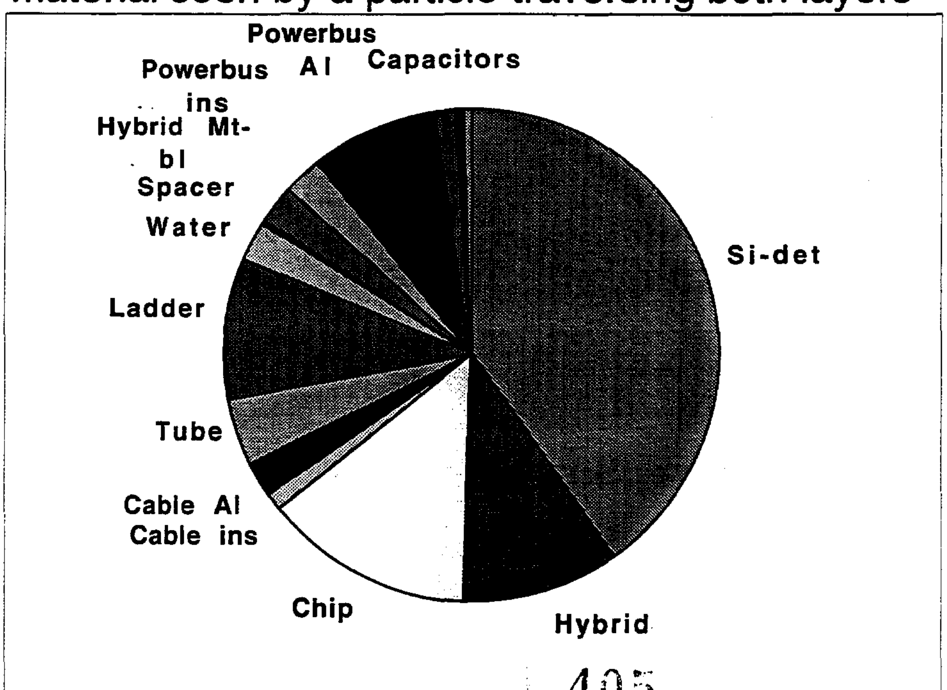
Heat Bridge Cooling Test

The temperatures distribution along the heat bridges variants NN1-9, heat flux 2 watts

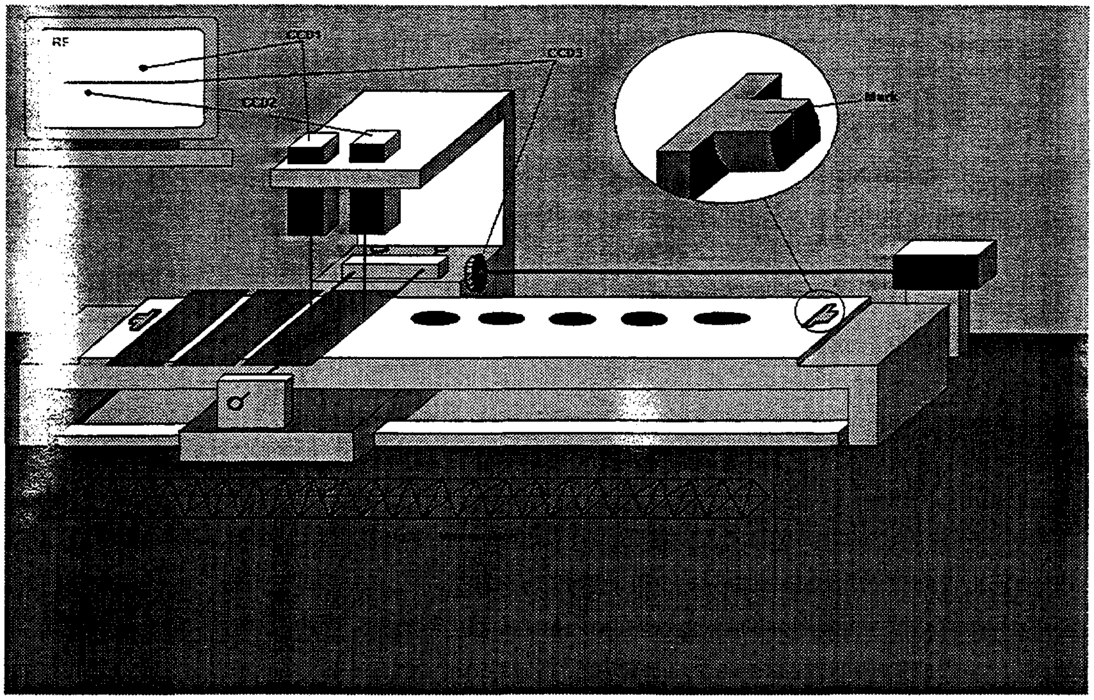


Strip Material Distribution

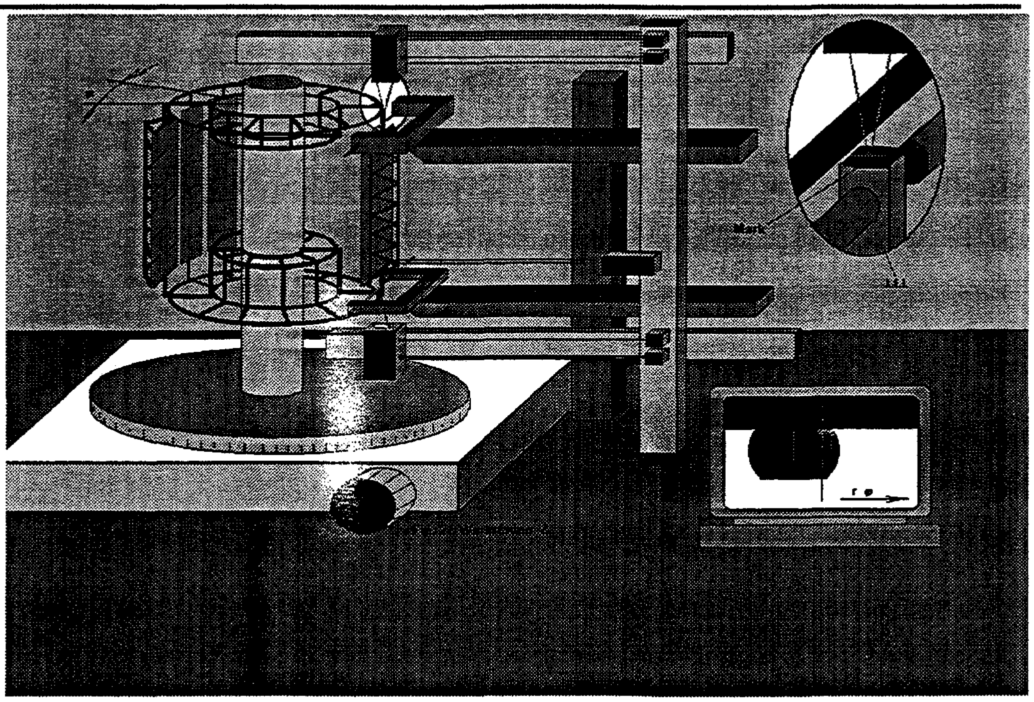
Average material seen by a particle traversing both layers = 1.74%X_0



Strip Ladder Assembly



ITS Assembly



Ladder Alingment

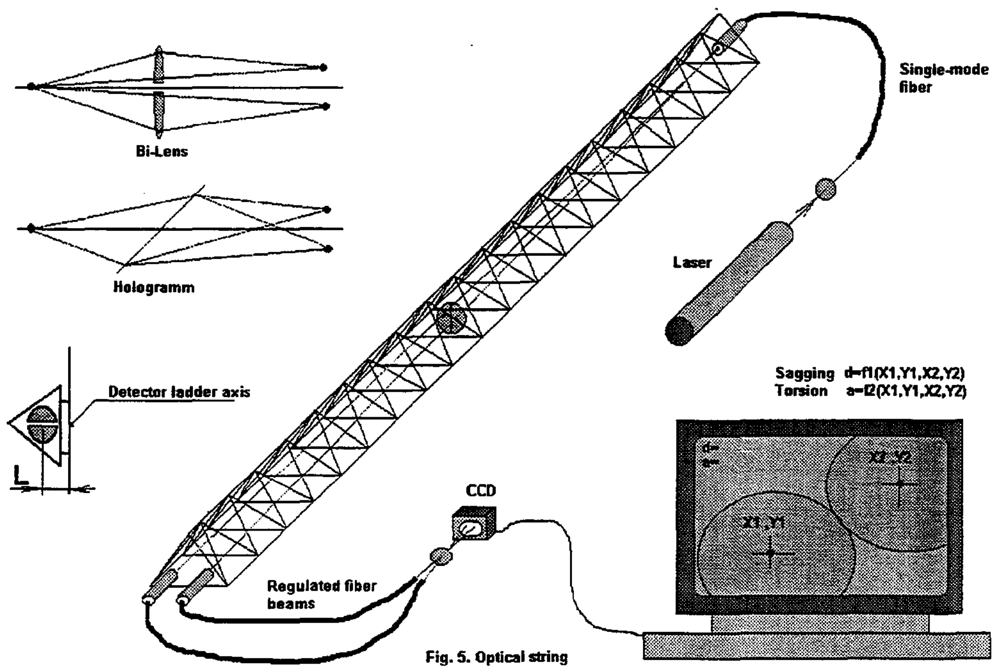
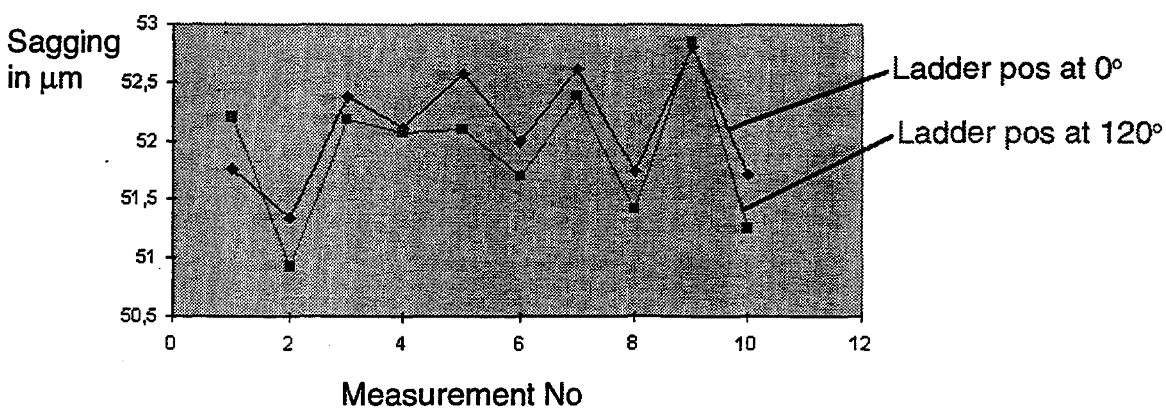
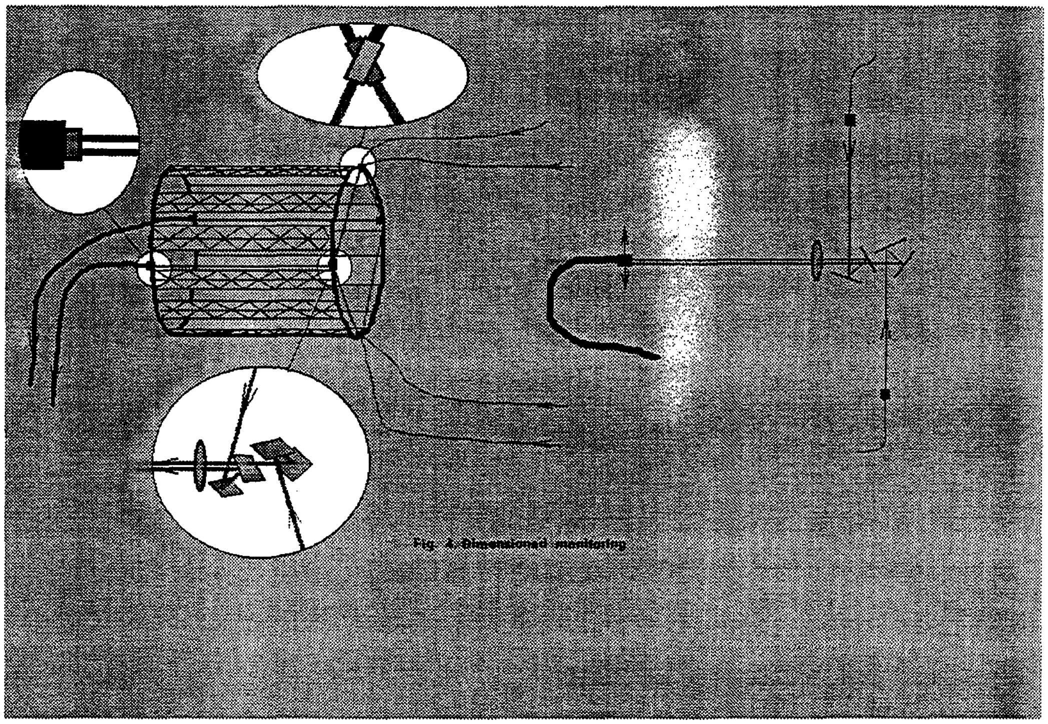


Fig. 5. Optical string

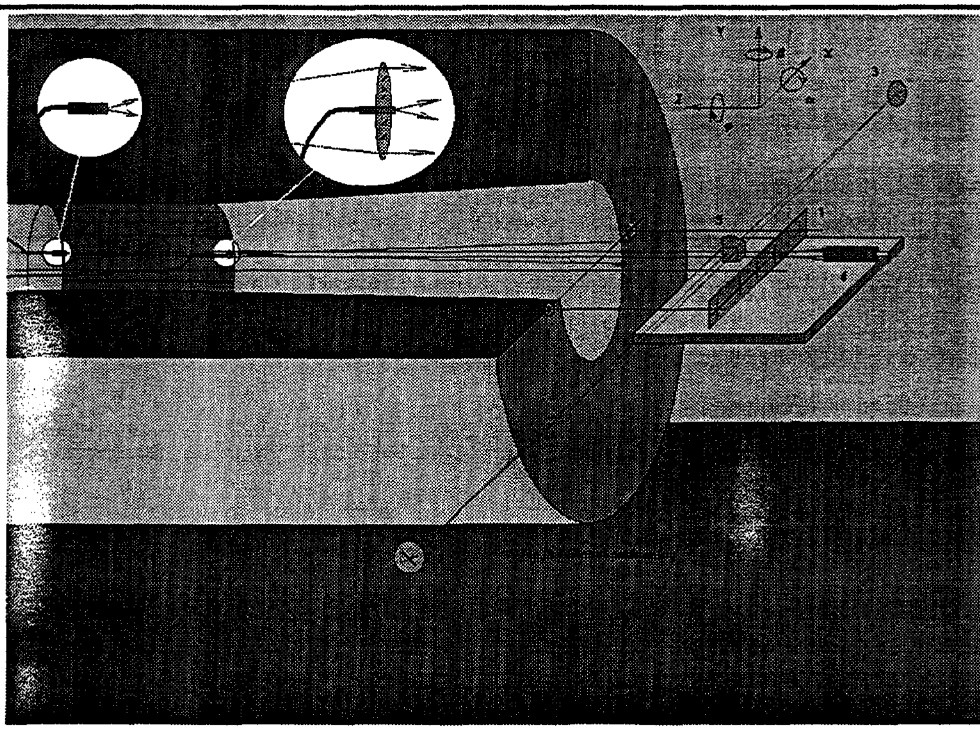
Measurement of Ladder Sagging



ITS Strip Alignment



General ITS Alignment



ATLAS PIXEL DETECTOR COOLING REQUIREMENT

- 2228 PIXEL MODULES, EACH DISSIPATING ~ 5.5 WATTS
  $\Rightarrow$ TOTAL ~ 13 KW
  (NOT INCLUDING ~2KW DISSIPATION IN CABLING WITHIN INNER DETECTOR VOLUME)

- MODULES ARRANGED ON 116 BARREL STAVES + 120 DISK SECTORS
  ~33W DISSIP.
  L~80cm, ~72W DISSIP.

- HEAT DISSIPATION OVER WHOLE OF DETECTOR AREA
  (NOT JUST AT END RINGS, AS IN MOST PRESENT GENERATION VXD'S OPERATING Si STRIPS AT LOW ACCUMULATED DOSES)

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- PIXEL SUBSTRATE TEMPERATURE REQUIRED TO BE LOWER THAN $-6^\circ C$: $\left(-6^\circ C\,^{+0^\circ C}_{-5^\circ C\,MAX}\right)$

  AIM FOR 10 YR OPERATIONAL LIFE FOR BARREL LAYERS AT 10.1 cm AND 13.2 cm RADIUS, + DISKS

  BLAYER (r ~4.3cm) REMOVAL NECESSARY ~ EVERY YEAR @ $10^{34}\ cm^{-2}s^{-1}$

- REQUIREMENT OF LOW X0 AT LOW RADIUS PUSHES US TO REDUCE DETECTOR + ELECTRONICS THICKNESS + SUPPORTS AND SERVICES

LOW MASS COOLING OF SILICON PIXEL AND STRIP DETECTORS BY FLUOROCARBON EVAPORATION.

G. HALLEWELL, CPPM.

R. BUDINSKY[+], G. HALLEWELL[*], G. LENZEN[#], J. THADOME[#], V. VACEK

[*] CPP MARSEILLE
[+] CZECH TECHNICAL UNIVERSITY, PRAGUE
[#] WUPPERTAL UNIVERSITY.

WHAT ARE THEY?

SATURATED (ie $C_nF_{(2n+2)}$) FLUOROCARBONS, MADE BY CHEMICAL SUBSTITUTION OF H BY F IN ANALAGOUS HYDROCARBONS

EXAMPLE: C_4F_{10} – PERFLUOROBUTANE

- CONSIDERABLE BODY OF HV AND MATERIALS COMPATIBILITY EXPERIENCE IN H.E.P. COMMUNITY FROM LARGE RICH | CRID PROGRAMS AT CERN & SLAC
  → C_6F_{14}, C_5F_{12}, C_4F_{10}, C_2F_6

WHY COOL WITH THESE FLUIDS?

(i) NON – CONDUCTIVE
(ii) NON – TOXIC
(iii) NON – FLAMMABLE (C_4F_{10} A HALON REPLACEMENT...)
(iv) NON – OZONE DEPLETING
(v) VERY LOW SOLVENT ACTIVITY
(3M MARKETS UNDER 'FLUORINERT' TM)
(vi) LOW – VISCOSITY (LIQUID PHASE WRT H_2O)
(vii) HIGH EXPECTED RADIATION RESISTANCE (NEEDS STUDIES)

HOWEVER: LIQUID PHASE Cp ONLY ONE QUARTER OF H_2O → EVAP!!

ATLAS COOLING REVIEW RECOMMENDATION 10'97
TO REPLACE AQUEOUS COOLANTS WITH NON-CONDUCTIVE COOLANTS DUE TO RISK OF LEAK DAMAGE
TO DETECTORS ↔ INNER DETECTOR ~ $70M.

CPPM BiPhase Liquid (FC) - Gas(N_2) Cooling System

Fluorocarbon Candidates (1995 3-M data)

Fluorocarbon	PF5030 *	PF5040 *	PF5050 *	PF5060 *	PF5070 *	PF5080 *
Chem. Formula	C_3F_8	C_4F_{10}	C_5F_{12}	C_6F_{14}	C_7F_{16}	C_8F_{18}
Mean Mol. Wt	188	238	288	338	388	438
Bp (1 atm)	-37°C	-2°C	30°C	56°C	80°C	101°C
Dens. (gcm^{-3})	1.35 (20°C)	1.52 (20°C)	1.63 (25°C)	1.68 (25°C)	1.73 (25°C)	1.77 (25°C)
Liquid Viscos (cp)	0.3 (0°C)	0.46 (20°C)	0.45 (25°C)	0.67 (25°C)	0.95 (25°C)	1.4 (25°C)
Surface Tens. (dy.cm^{-1})	4.3 (0°C)	7.4 (20°C)	9.5 (25°C)	12.0 (25°C)	13.0 (25°C)	15 (25°C)
Vapor Press. (@ -10°C: Torr)	2200	550	130	58	12	~ 8
LatHt Vap (J mole^{-1})	15717	22881	25281	29670	30815	40278
Liq Vol Flow (90 W Load) (cm^{3}s^{-1})	~ 0,8	~ 0,6	~ 0,6	~ 0,6	~ 0,6	~ 0,5
Gas Vol Flow (90 W Load) (cm^{3}s^{-1})	~ 50	~ 120	~450	~ 900	~ 3600	~ 4400
Liquid-Gas Expansion Fact @ -10°C	~60	~210	~ 720	~ 1500	~ 6000	~ 8800
Δp max for ΔT = 0.5°C (Torr)	~ 38	~ 11	~ 3,2	~ 1,4	~ 0,4	~ 0,2

Refs: * 3M Speciality Fluids Newsletter Vol1 No. 1, April 1995
3M Speciality Chemicals Div, 3M Center, Building 223-6S-04 St Paul MN 55133-3223
Tel (612) 737-4019 Fax (612) 736-7542

- USE LATENT HEAT OF VAPORISATION (15-25 KJ/mole); WHICH IS MUCH HIGHER THAN LIQUID C_p.

VERY LOW LIQUID FLOW RATES → THIN TUBES → LOW X/X_0
(eg ~ $0.7\ cm^3 s^{-1}$ FOR AN ATLAS PIXEL STAVE)

- SILICON OPERATING TEMPERATURE DEPENDS ON BOILING PRESSURE IN COOLING TUBES
CONTROLLED BY PUMPING SPEED

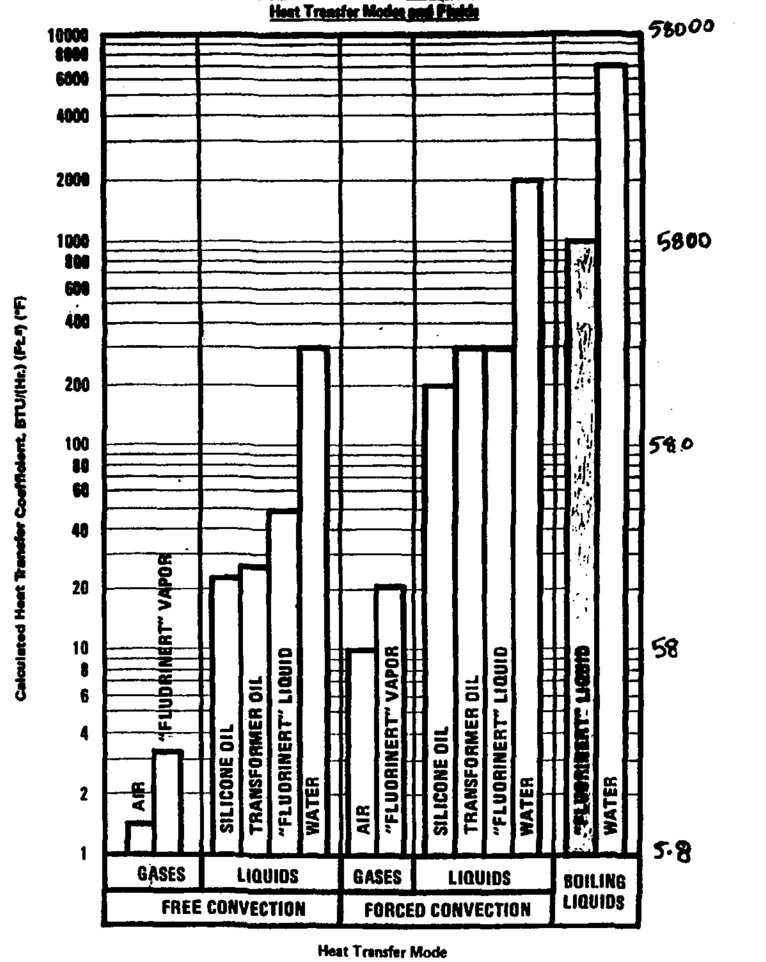
- EXHAUST FLUID IN FORM OF VAPOR → LOW COOLANT X/X_0

USE OF TUBES ALLOWS WIDER CHOICE OF COOLING FLUIDS WITH BOILING PRESSURES DIFFERENT FROM DETECTOR VOLUME AMBIENT 1 BAR ENVIRONMENT.

- VERY HIGH HEAT TRANSFER COEFFICIENT SHOULD EASE THE PROBLEM OF THERMAL IMPEDANCE BETWEEN SILICON AND COOLING TUBE.

FIGURE 11

Typical Heat Transfer Coefficients vs Heat Transfer Modes and Fluids



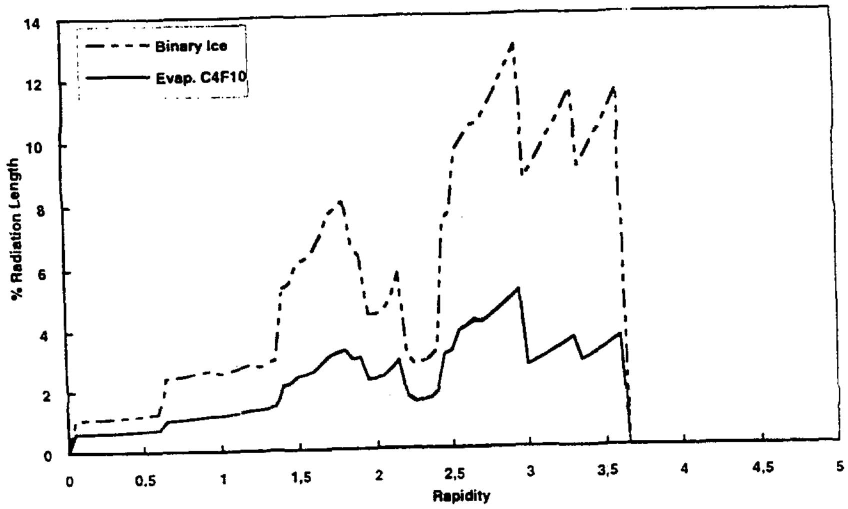


Figure 10-88 Comparison of binary ice and fluorinert cooling assuming the service ro'tings used in Tables 10-15-10-18.(B-layer services routed as listed in Table 10-15, to facilitate layer replacement).

VAPOR PRESSURE CURVES OF RELEVANT FLUOROCARBON REFRIGERANTS

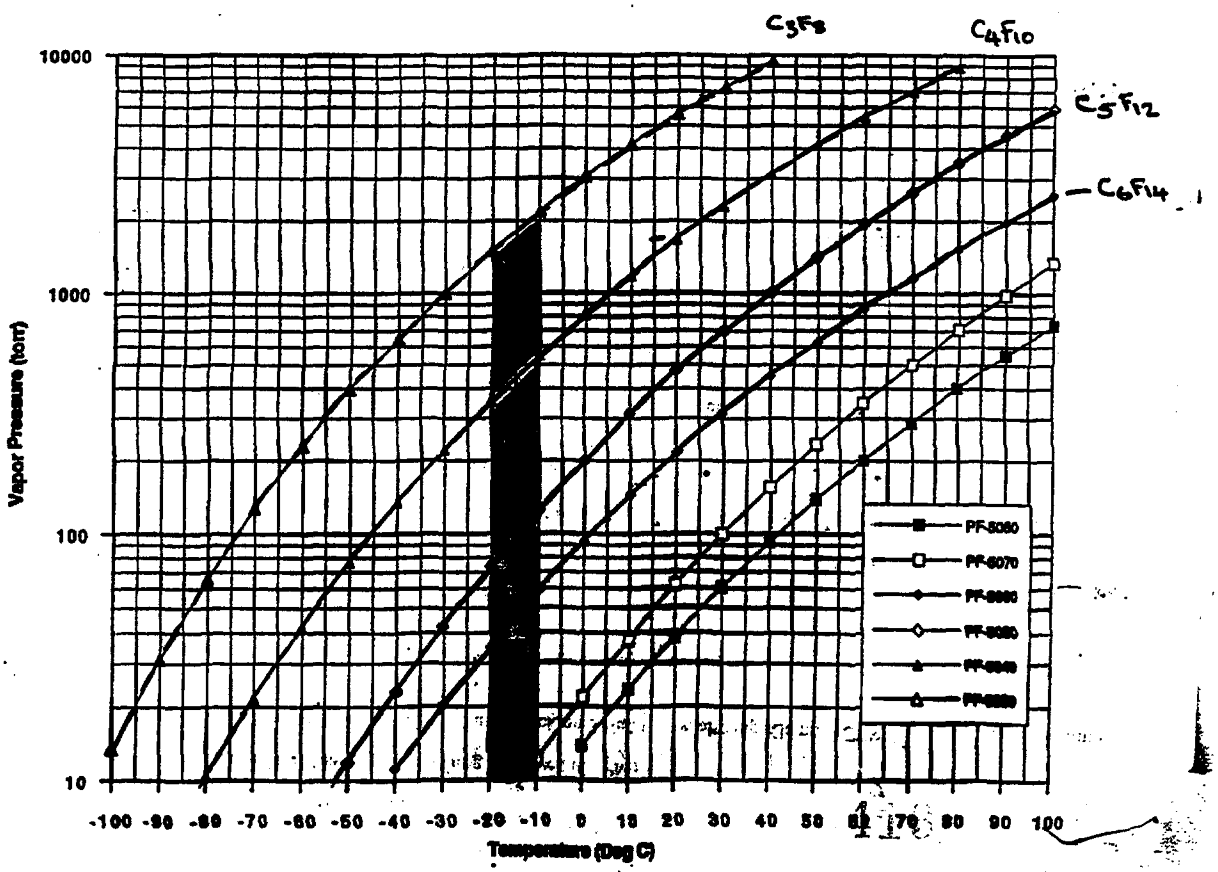
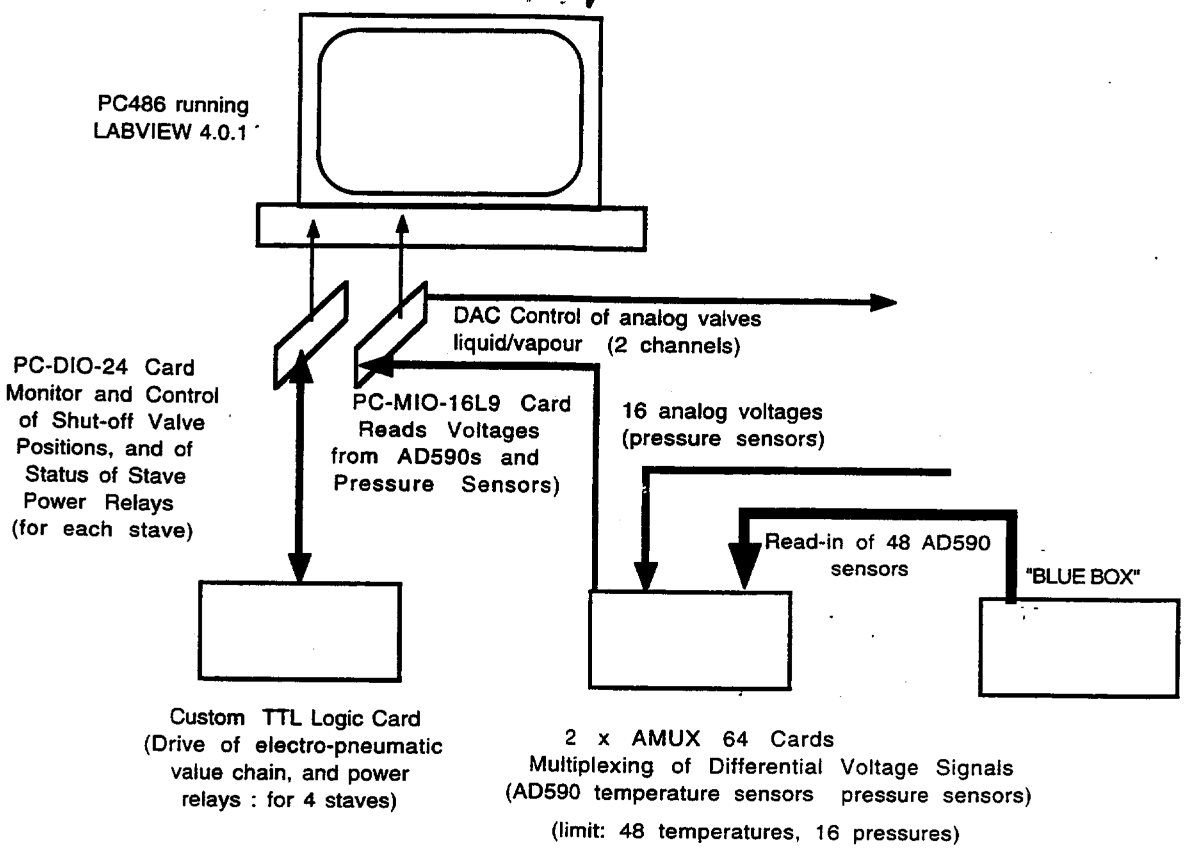
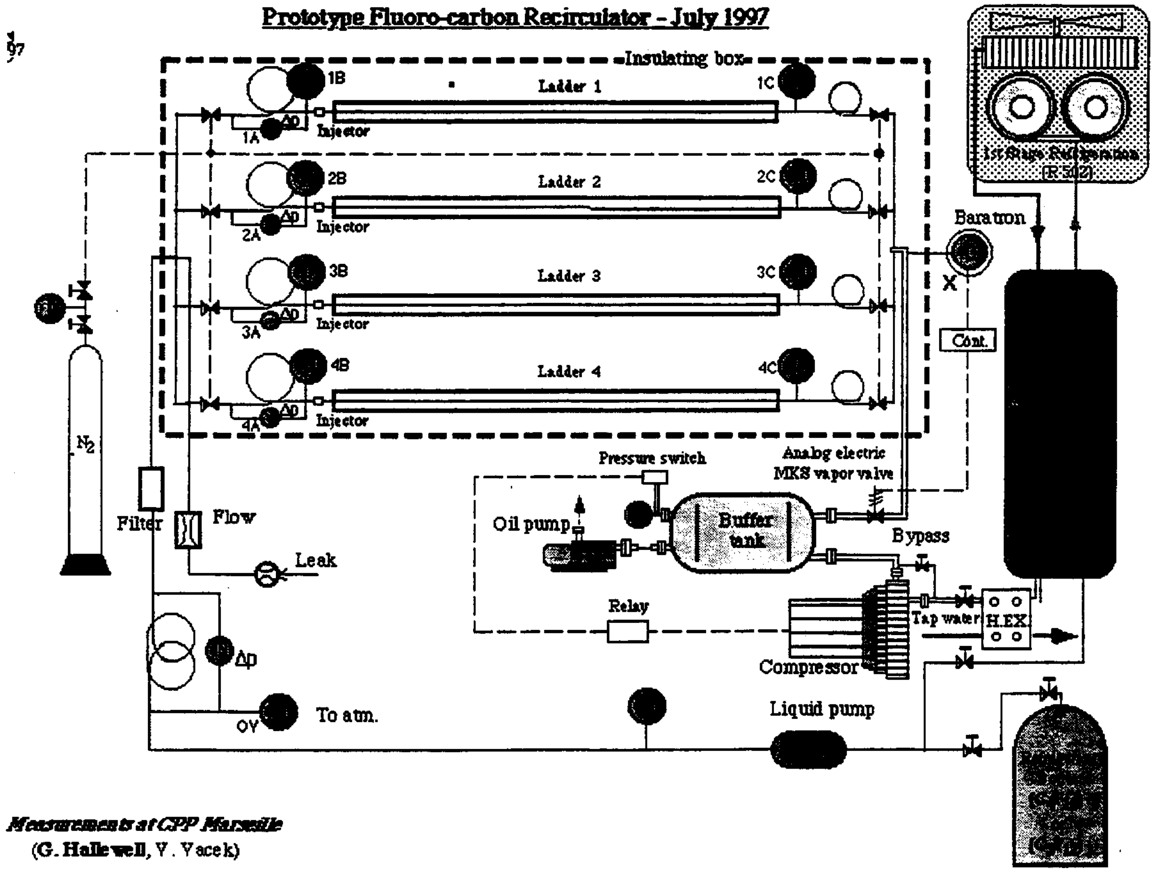


Figure 3-8. Vapor Pressure vs. Temperature for PF-5030 through PF-5080



Prototype Fluoro-carbon Recirculator - July 1997

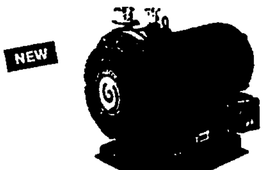


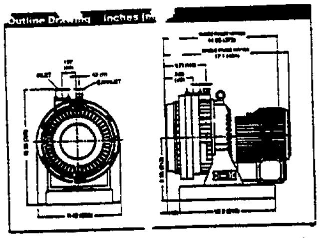
Measurements at CPP Marseille
(G. Hallewell, V. Vacek)

Primary Pumps

Varian 600DS Dry Scroll Pump

NEW





Varian's New 600DS Dry Scroll Pump incorporates a technology that produces clean, cost effective, and reliable vacuum pumping performance. Unlike many other types of dry pumps, the 600DS has both a low ultimate pressure and high pumping speed. With a base pressure in the 10^{-3} Torr range and superior pumping efficiency, it is suitable for applications where oil-sealed mechanical pumps have typically been used.

In the oil-free scroll pump, crescent-shaped pockets are formed and bounded by the meshed scrolls. As the orbiting scroll moves within the fixed scroll, these pockets progressively decrease in volume as they move the pumped gases in the spiral path from inlet to discharge. Sealing is accomplished with PTFE seals against anodized aluminum walls eliminating the need for oil sealing.

Because the scroll pump is intrinsically clean, there is no risk of contaminating your vacuum system. Conventional oil-sealed mechanical pumps require costly accessories (traps and baffles) to achieve only marginal levels of cleanliness. Since no oils are required, the costs of purchasing and disposal of them are eliminated. Few moving parts and carefully chosen materials of construction minimize pump failures, with typical maintenance intervals of twelve to eighteen months. All these factors contribute to low cost of ownership and maximum uptime.

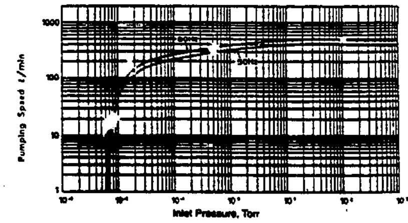
Varian's 600DS Dry Scroll pump is the preferred choice for your clean, high-vacuum requirements.

Features	Benefits
• Scroll Design	• Low ultimate pressure • High speed • Compact size • Quiet, low vibration operation • Two moving parts Long service life
• Oil-Free	• No risk of oil contamination • No expensive traps or filters • No costs of buying and disposing of oil
• Carefully chosen construction materials	• Long life operation • Low maintenance • Low cost of ownership

Common Applications

- Turbo-, Ion-, or Cryo-Pumped Systems
- Load Lock Chambers
- Leak Detection Systems
- Optics
- Research
- Any application where the presence of hydrocarbons is detrimental to your process

Speed Curve



Technical Specifications

Free Air Displacement
60 Hz 600 l/m (21 cfm)
50 Hz 500 l/m (17.5 cfm)

Pumping Speed
60 Hz 500 l/m (17.5 cfm)
50 Hz 420 l/m (15 cfm)

Ultimate Total Pressure
< 10^{-2} Torr (mbar)

Inlet Connection
NW40

Outlet Connection
NW25

Motor Rating
0.8 hp (0.6 kW)

Electrical Supply
1 Phase, 50/60 Hz, 100/115/200/230 V
3 Phase, 50/60 Hz, 200/208/230/380/415 V

Noise Level at 1 meter
60 dBA

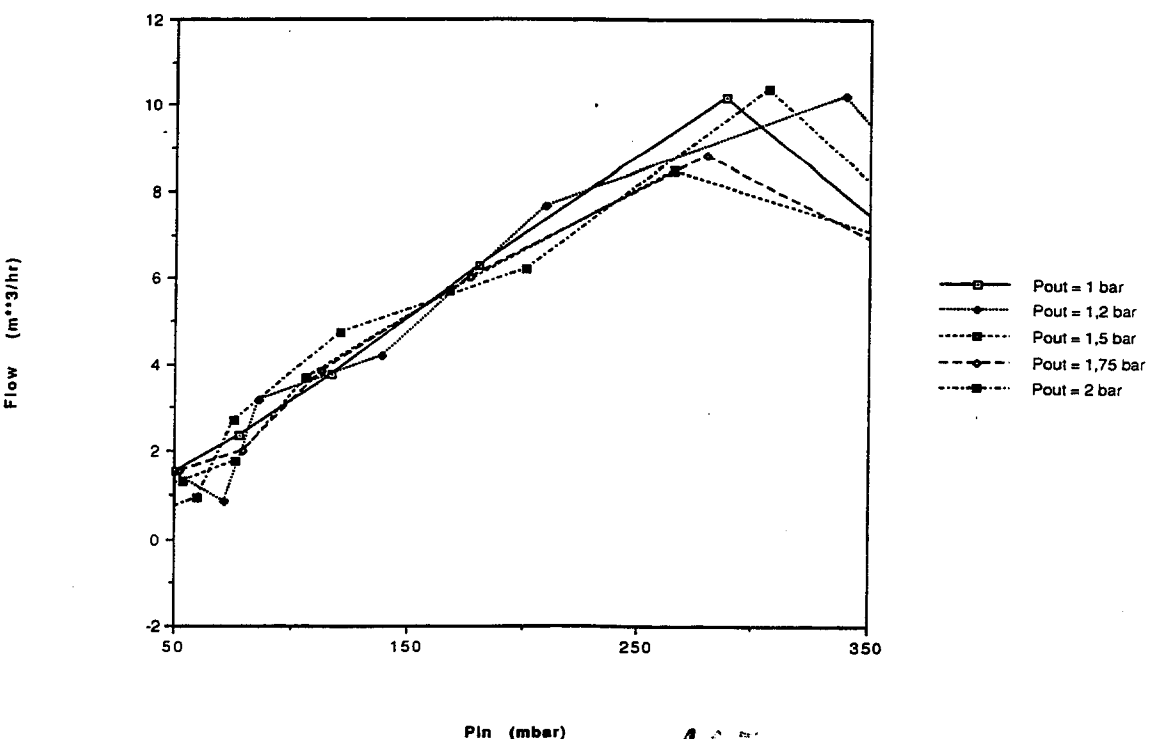
Operating Range
40°F to 105°F (5°C to 40°C)

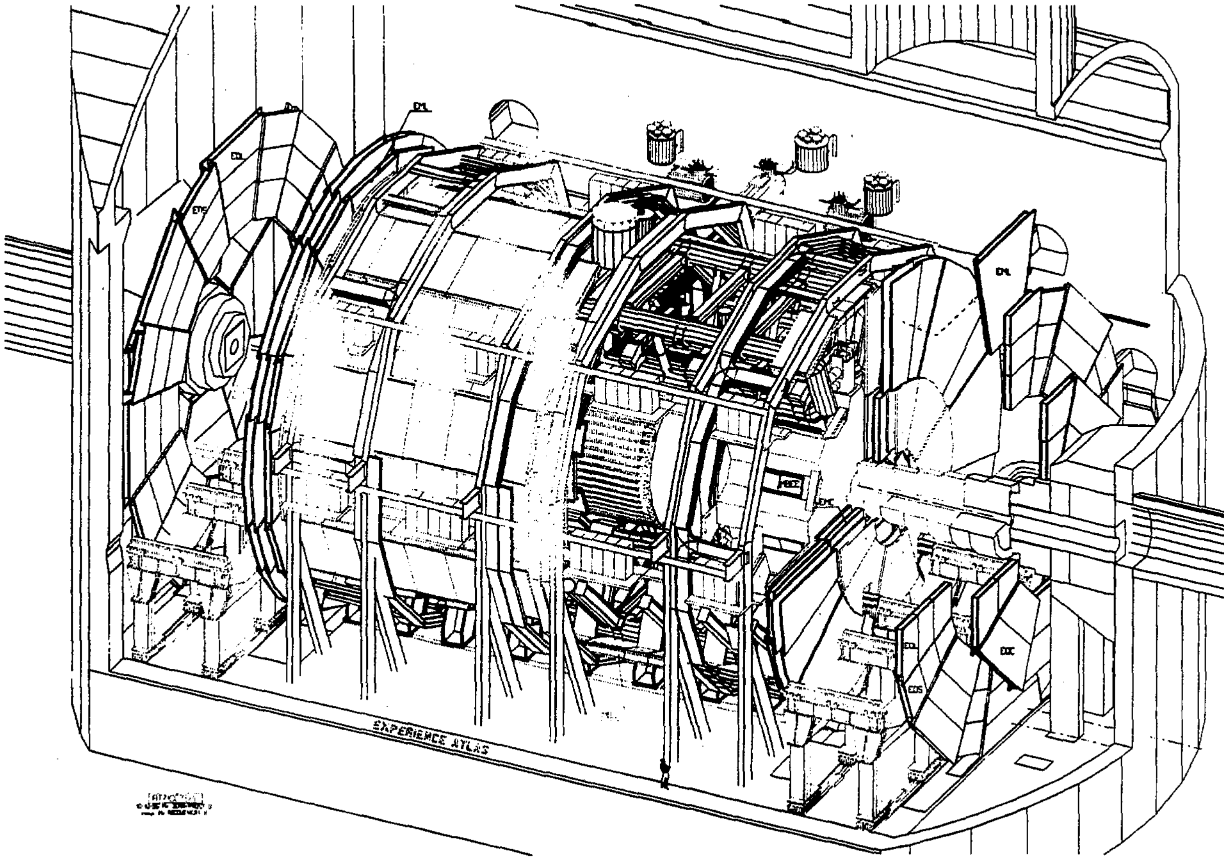
Weight
88 lb (40.0 kg) w/3 phase motor
100 lb (45.0 kg) w/1 phase motor

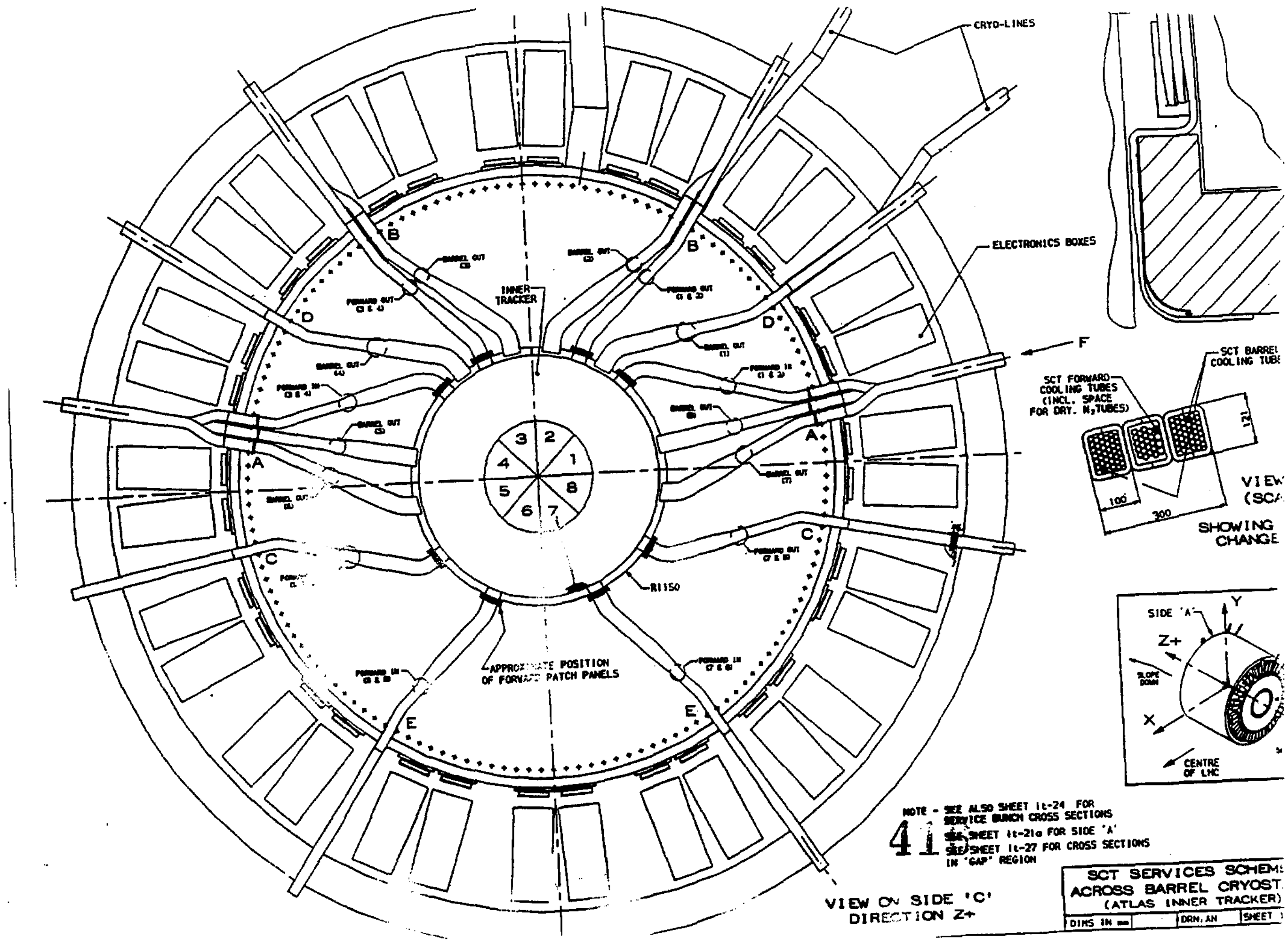
Ordering Information

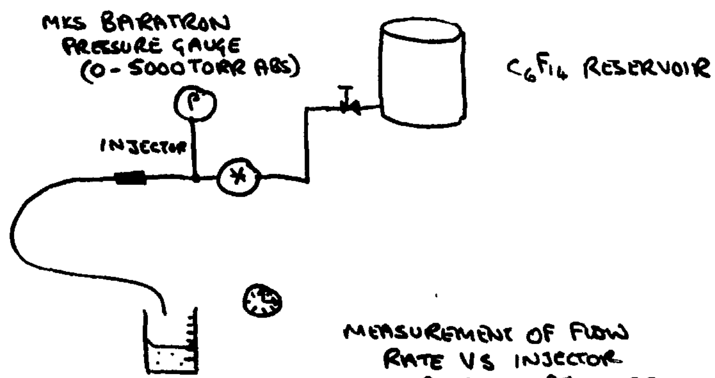
Description	Part Number	S Wei
Model 600DS with base, hour meter, and direct drive motor (1 phase universal)	600DS-1UNIV	1
Model 600DS with base, hour meter, and direct drive motor (3 phase universal)	600DS-3UNIV	
Minor Maintenance Kit	600DS-KMI	
Factory Rebuild Service	600DS-KMA	

Pumping speed of Edwards ESDP30A (C4F10)




EXPERIENCE ATLAS


CRYO-LINES
ELECTRONICS BOXES
INNER TRACKER
BARREL OUT
FORWARD OUT
FORWARD IN
A
B
C
D
E
F
1
2
3
4
5
6
7
8
R1150
APPROXIMATE POSITION OF FORWARD PATCH PANELS
SCT FORWARD COOLING TUBES (INCL. SPACE FOR DRY. N2 TUBES)
SCT BARREL COOLING TUBE
121
100
300
SHOWING
CHANGE
SIDE 'A'
Y
Z+
X
SLOPE DOWN
CENTRE OF LHC
NOTE - SEE ALSO SHEET It-24 FOR SERVICE BUNCH CROSS SECTIONS
SEE SHEET It-21a FOR SIDE 'A'
SEE SHEET It-27 FOR CROSS SECTIONS IN 'GAP' REGION
VIEW ON SIDE 'C'
DIRECTION Z+
SCT SERVICES SCHEM
ACROSS BARREL CRYOST
(ATLAS INNER TRACKER)
DIMS IN mm
DRN. AN
SHEET



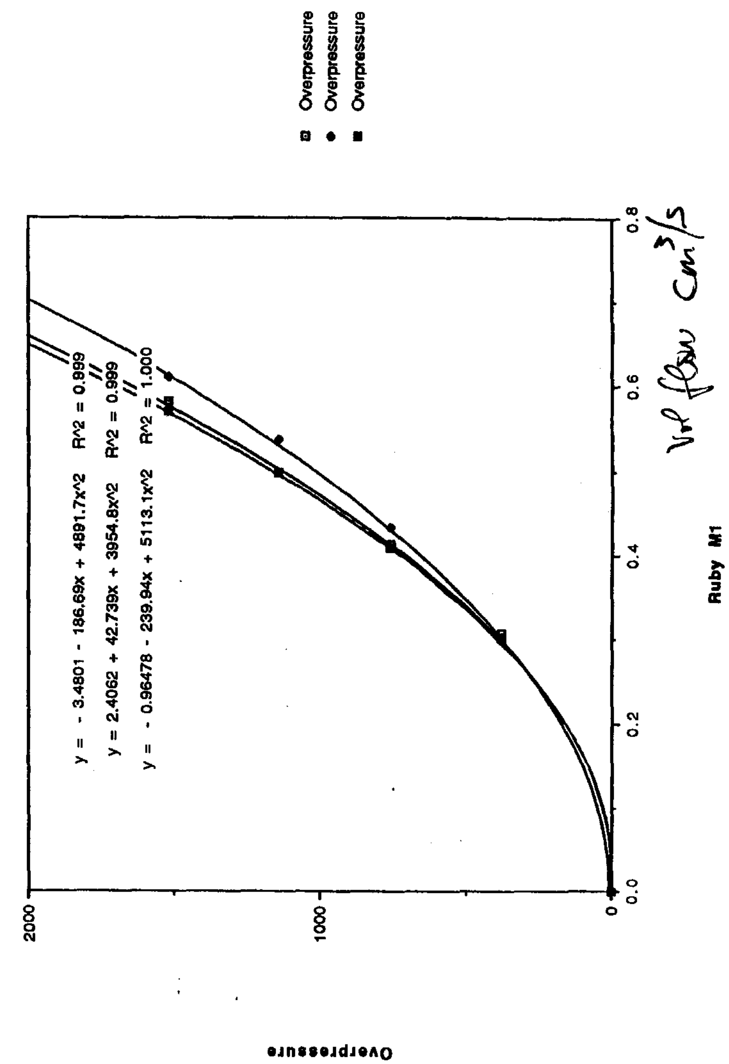
MEASUREMENT OF FLOW RATE VS INJECTOR UPSTREAM PRESSURE

INJECTOR TYPE		FLOW RATE EQUATION	FLOW FOR 2 BAR ABS
"BIG"	#1	$f = -3.2211 + 1.1197 \log P$	0.475 cm^3/sec
"BIG"	#2	$-3.2474 + 1.1212 \log P$	0.475
"BIG"	#3	$-3.1929 + 1.1006 \log P$	0.467
"MID"	#1	$-2.5555 + 0.9002 \log P$	0.416
"MID"	#2	$-3.0069 + 1.0415 \log P$	0.431
"MID"	#3	$-2.5486 + 0.8964 \log P$	0.410
"SMALL"	#1	$-2.0761 + 0.7321 \log P$	0.3406
	#2	$-2.1388 + 0.7486 \log P$	0.3323
	#3	$-1.9766 + 0.7037 \log P$	0.3450

OLD INJECTORS (BY WAY OF COMPARISON)

LADDER 1	(INCLUDES NEEDLE VALVE)	$-4.4167 \cdot 1.1135 \log P$	0.8495
LADDER 2	(INCLUDES NEEDLE VALVE)	$-4.3056 + 1.4862 \log P$	0.6664
LADDER 3		$-3.3644 + 1.1561 \log P$	0.4579

Data from "INJECTOR CAL"

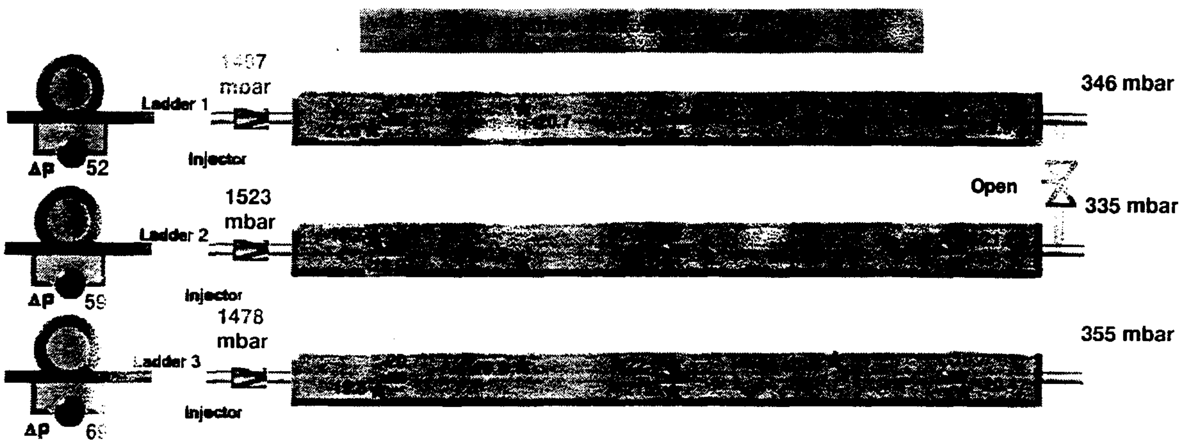


DATE
19/01/...
G123...

Experimental Setup at the CPP Marseille

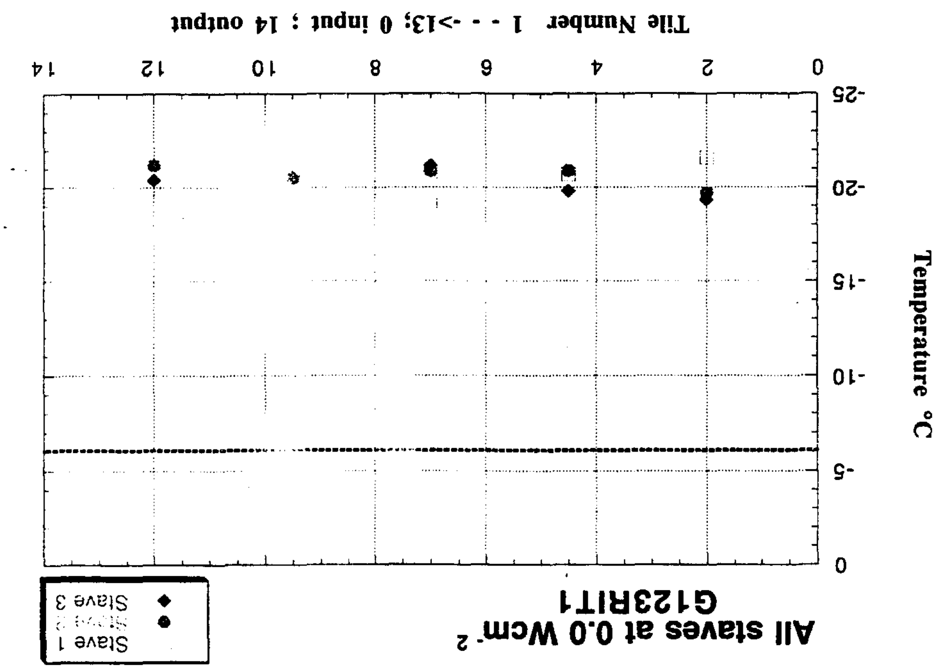
Temperature Distribution Measurements

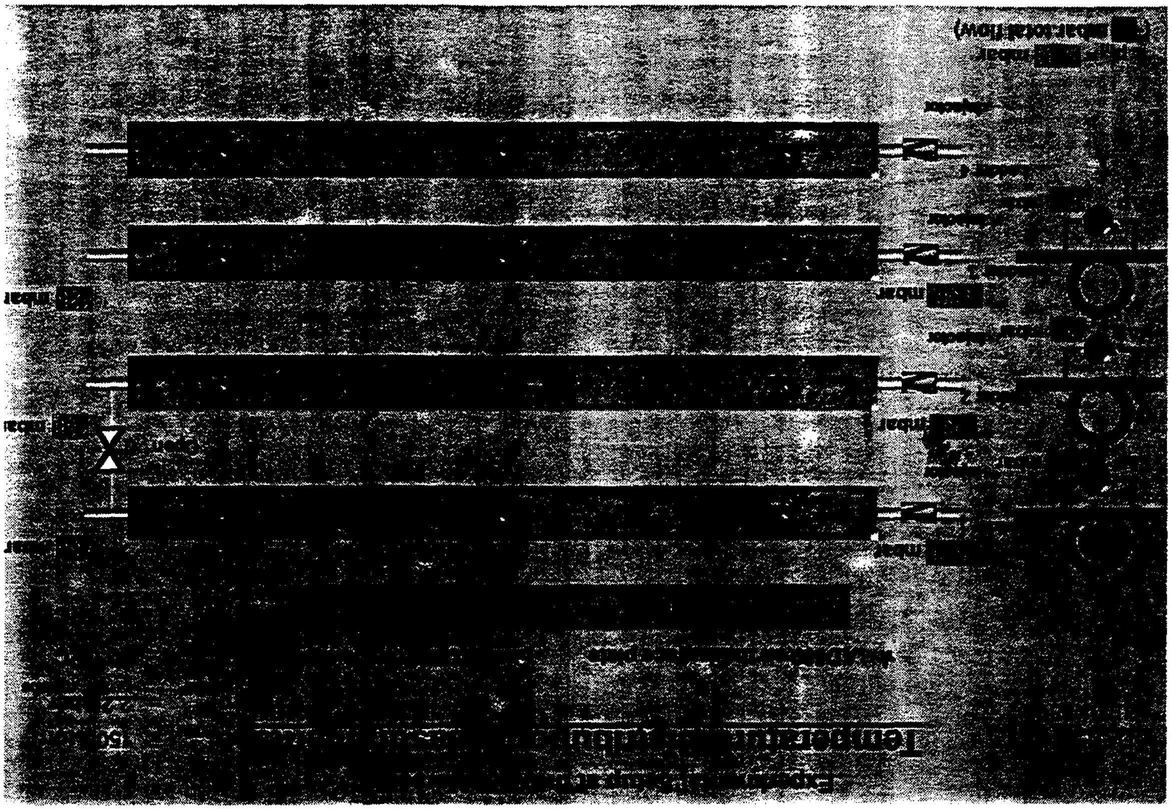
★ AD590 on the surface plate ▬ AD590 on the tube



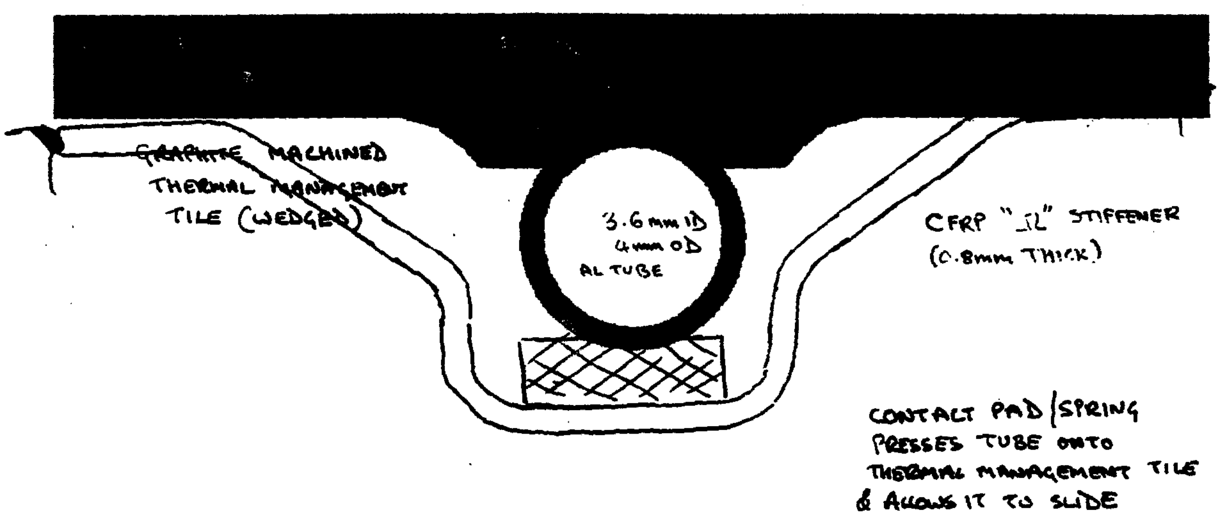
p_{EXHM} = 36 torr
p_{PUMP} = 1.8 bar_{abs}
T_{PUMP} = -4.0 °C
Amb. = 0.9 °C

p_{in} = 1692 mbar
(26 mbar total flow)



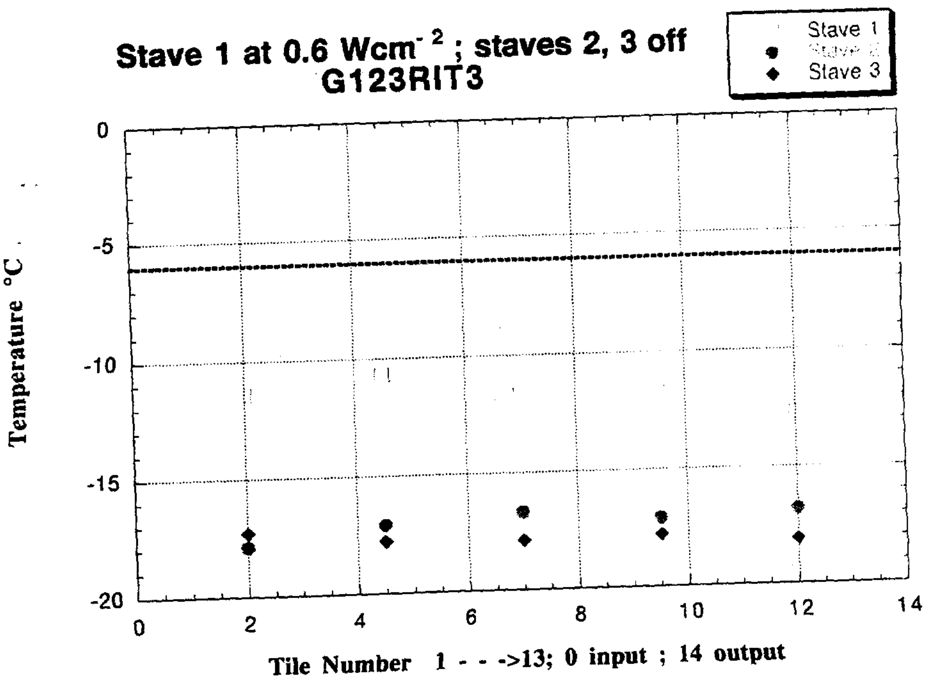


CPPM- WUPPERTAL SLIDING AL TUBE STAVE



FOR T.D.R.

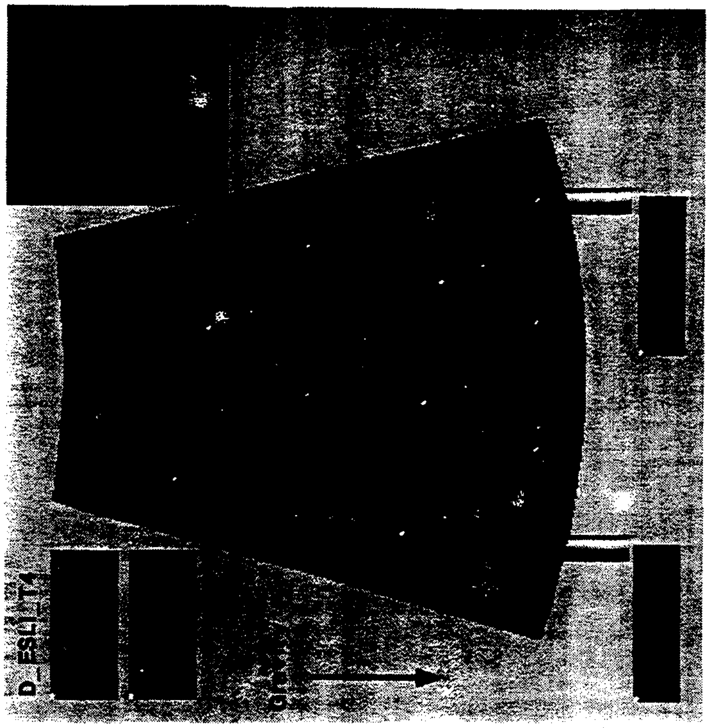
{ FEA DISTORTION STUDIES NECESSARY
THERMAL STUDIES
DISTORTION MEASUREMENTS IN ESPI }



Experimental Setup at the CPP Marseille

Temperature Distribution Measurements

DATE : 19 / 02 / 98

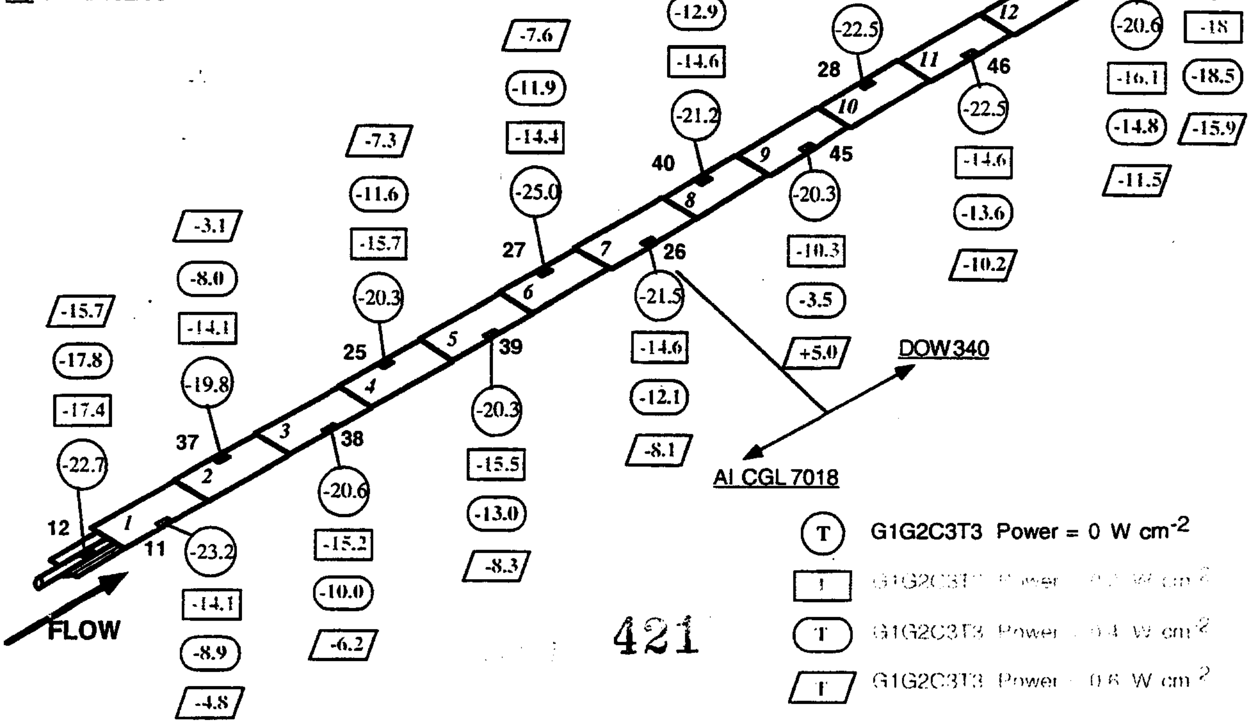


IEW STAVE DESIGN (CPPM+WUPPERTAL) WITH SILICON TILES

emperature distribution measurements at CPPM

HANNEL NUMBER TILE NUMBER

ate : 21/02/98 --> 23/02/98



421

Experimental Setup at the CPP Marseille

Temperature Distribution Measurements

DATE : 19 / 02 / 98

D_ESLI_T4

Gravity

Experimental Setup at the CPP Marseille

Temperature Distribution Measurements

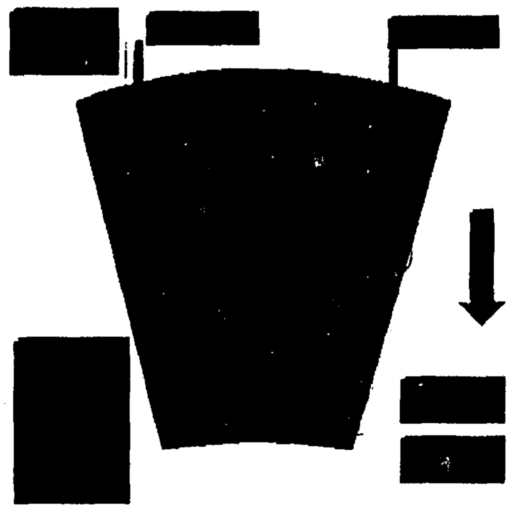
DATE : 19 / 02 / 98

D_ESLI_T3

Gravity

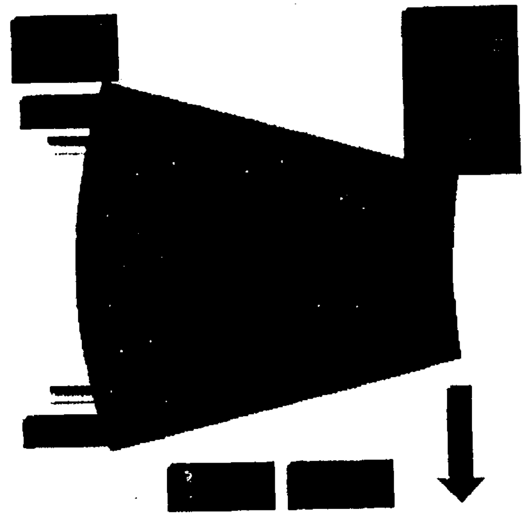
Experimental Setup at the CPP Marseille

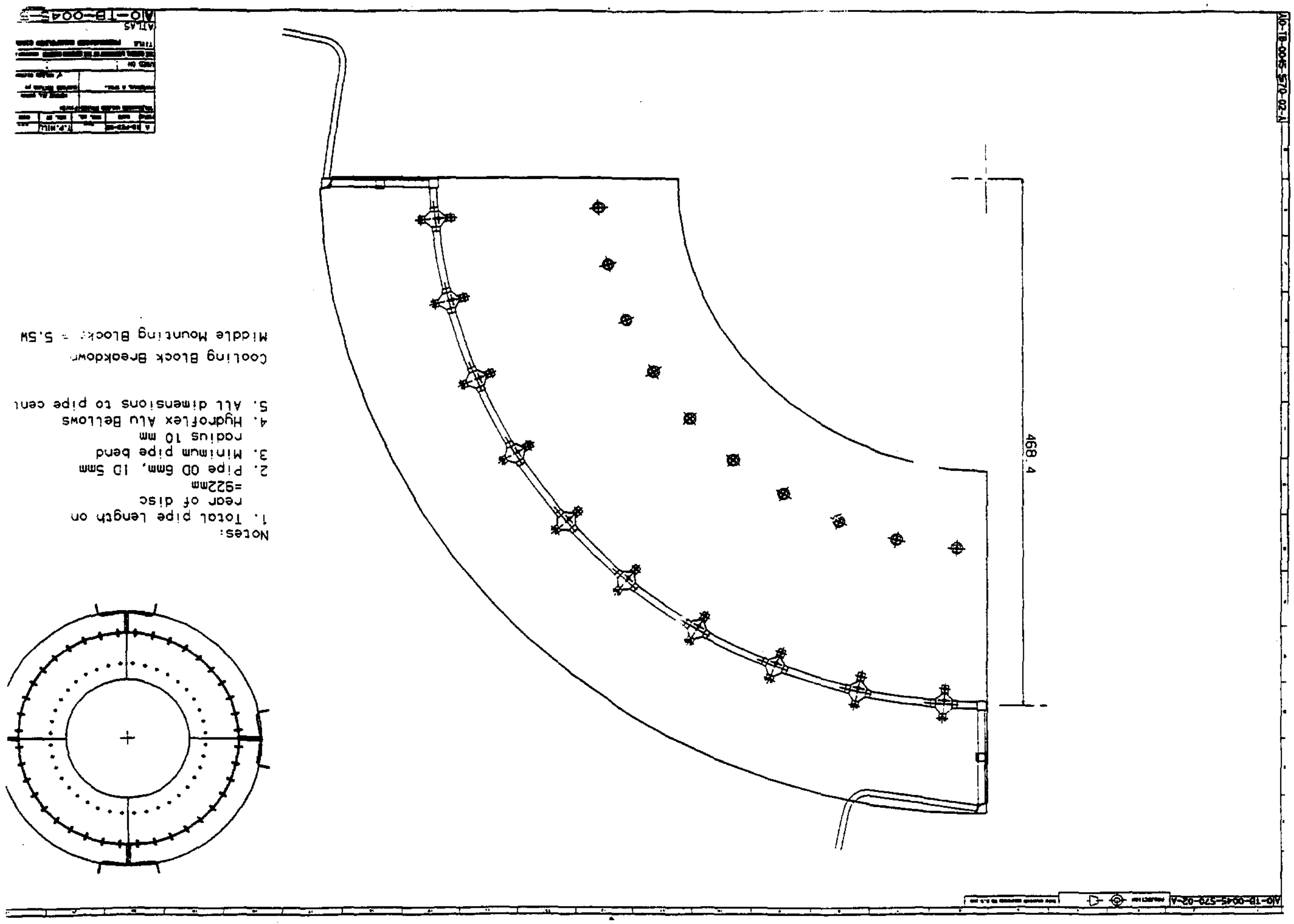
Temperature Distribution Measurements



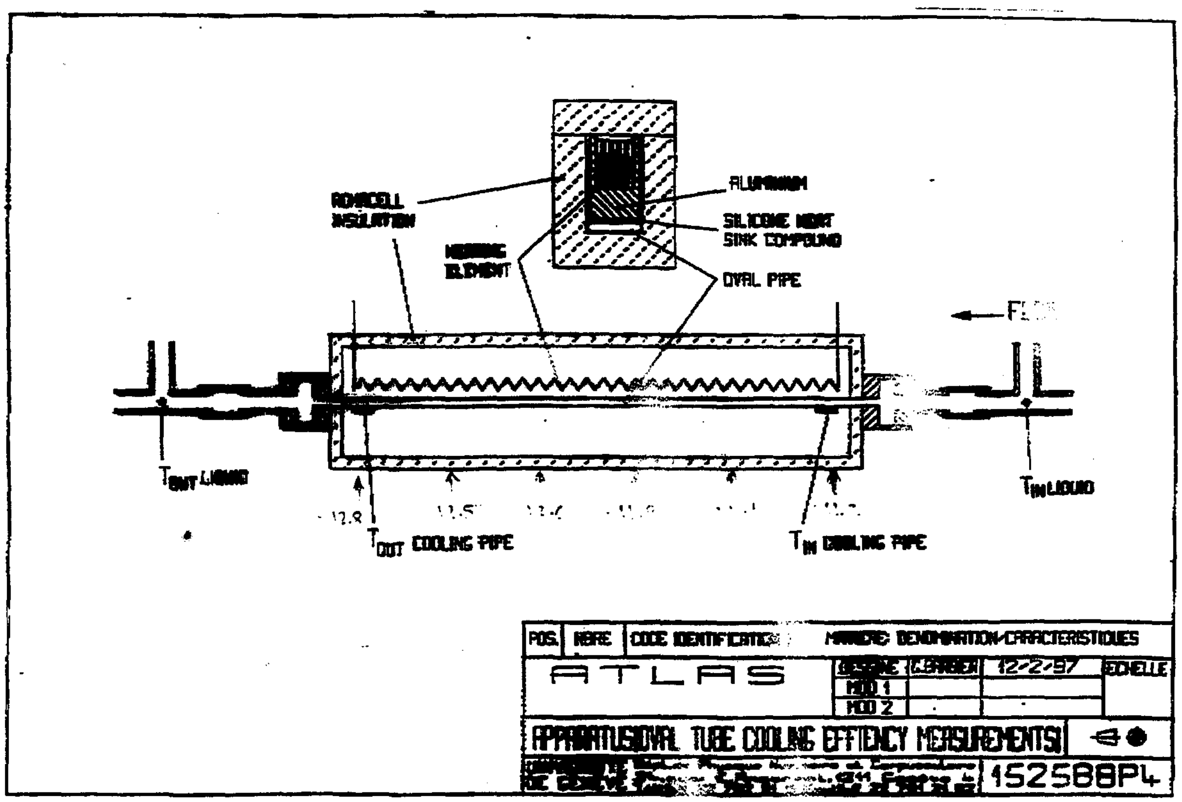
Experimental Setup at the CPP Marseille

Temperature Distribution Measurements

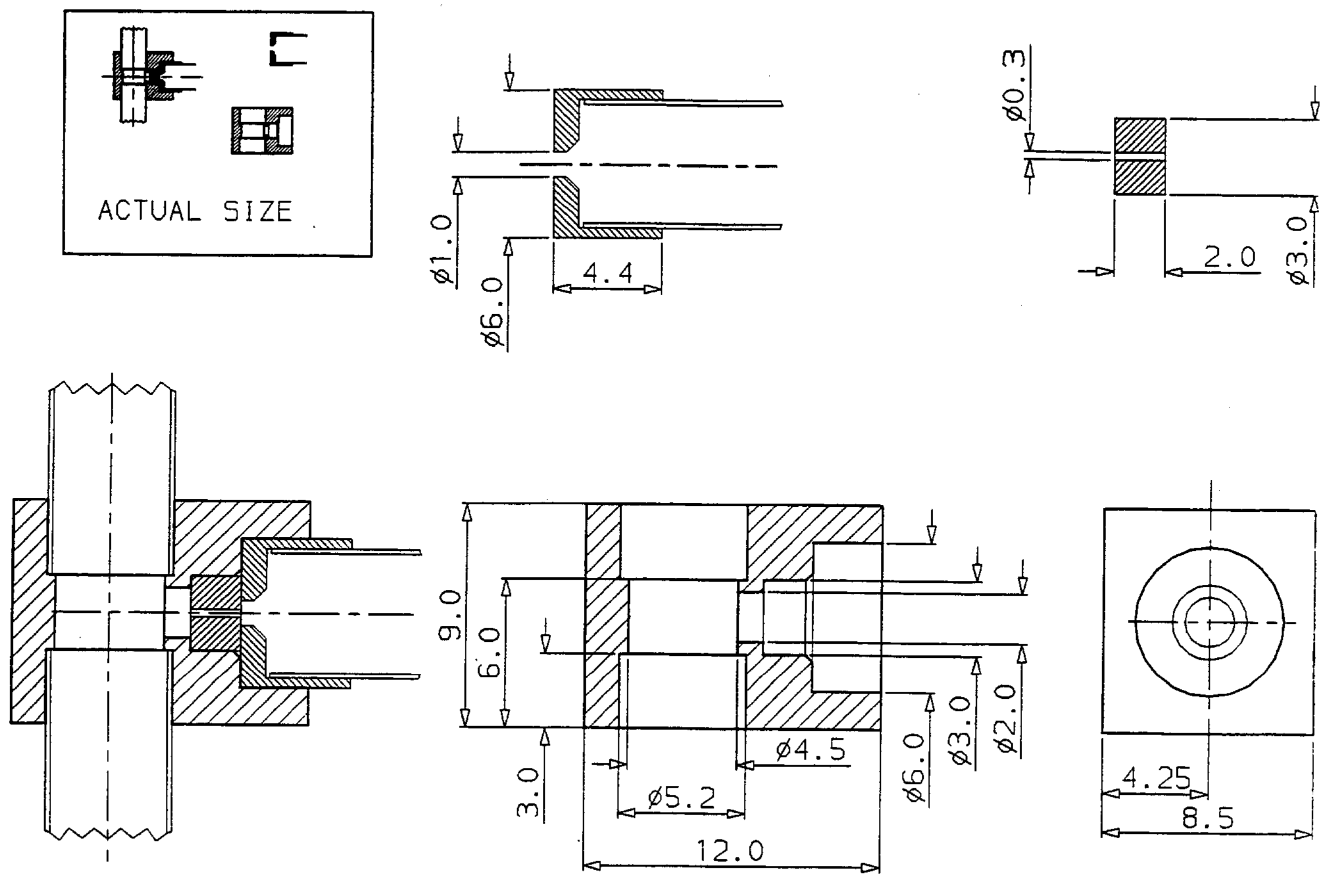




Notes:
1. Total pipe length on rear of disc =922mm
2. Pipe OD 6mm, ID 5mm
3. Minimum pipe bend radius 10 mm
4. Hydroflex Alu Bellows
5. All dimensions to pipe cent
Cooling Block Breakdown
Middle Mounting Block: = 5.5W
468.4
ATLAS

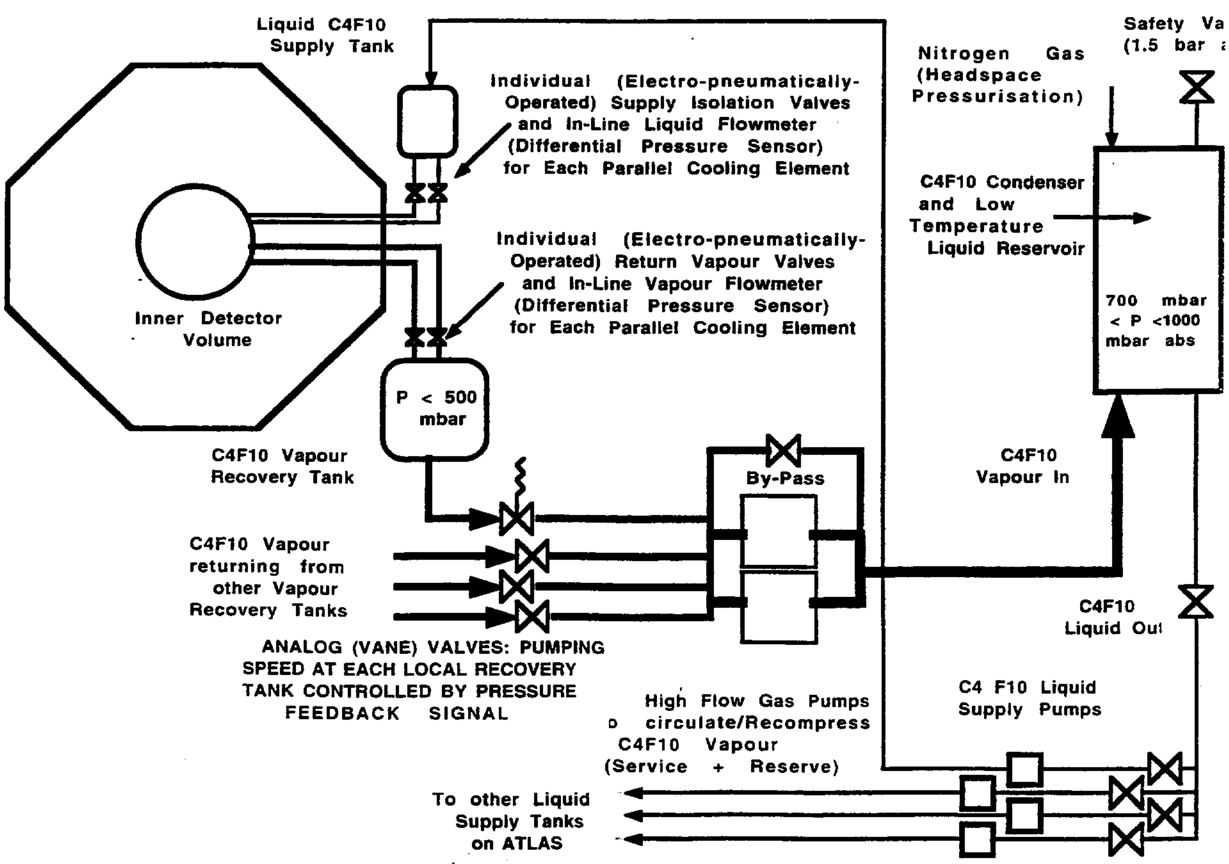


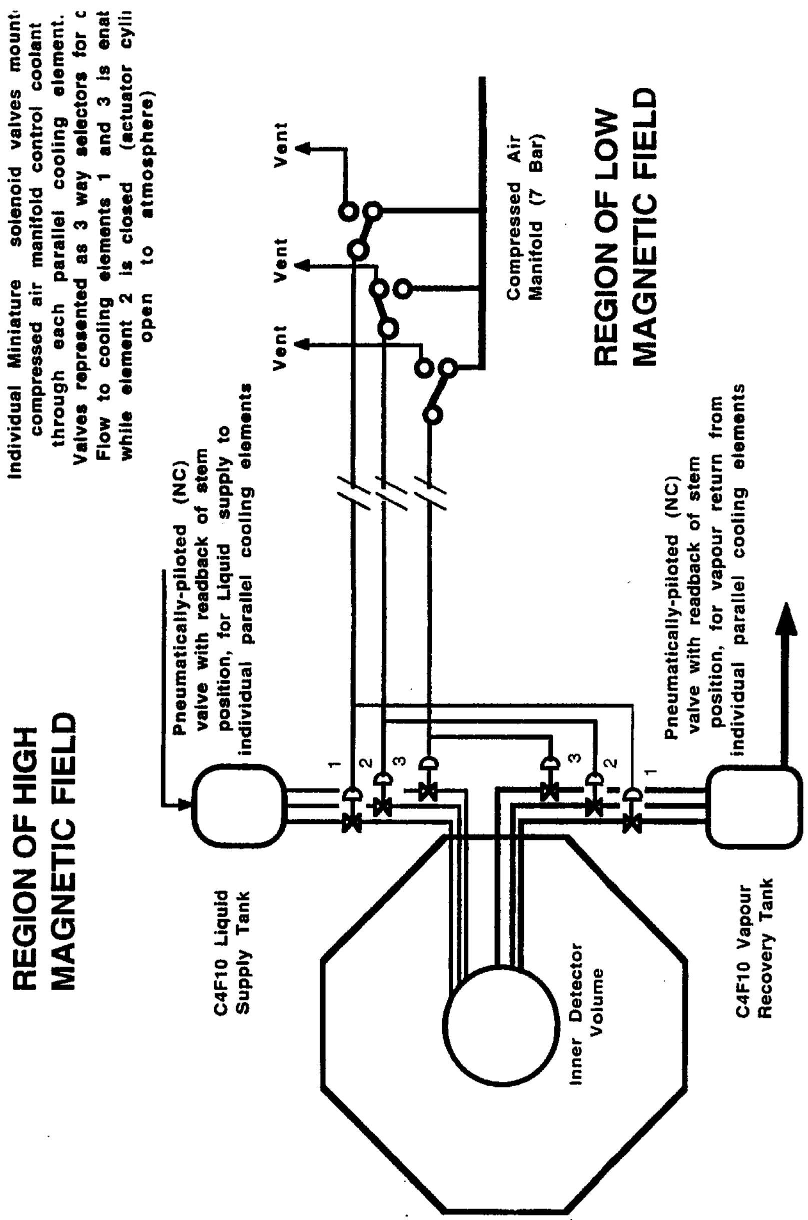
ROHACELL INSULATION
HEATING ELEMENT
ALUMINIUM
SILICONE HEAT SINK COMPOUND
OVAL PIPE
FLOW
T_{OUT} LIQUID
T_{IN} LIQUID
12.8
T_{OUT} COOLING PIPE
T_{IN} COOLING PIPE
POS.
NBRE
CODE IDENTIFICATION
MATIERE DENOMINATION-CARACTERISTIQUES
ATLAS
DESSINE
12-2-97
ECHELLE
MOD 1
MOD 2
APPARATUS(OVAL TUBE COOLING EFFTENCY MEASUREMENTS)
152588PL

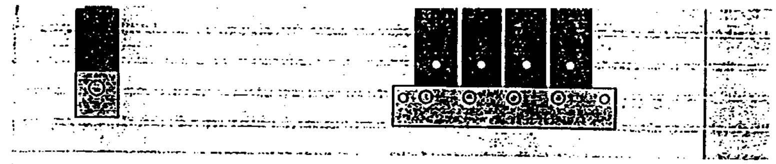


SCALE 5:1

:TUAL SIZE

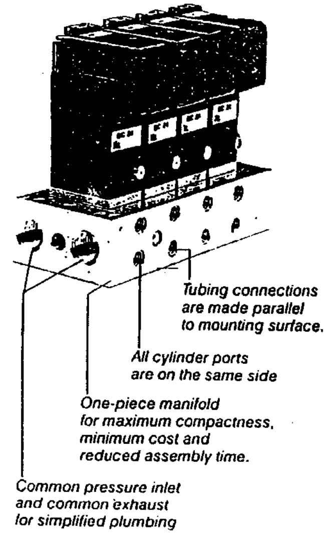


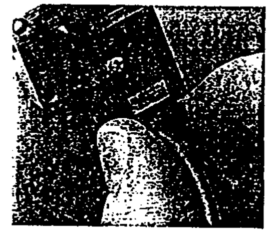




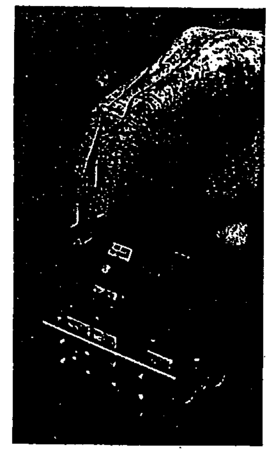
Designed for installation ease!

K Series valves were designed for versatility and ease of installation. These features help make K Series installations quick and economical:





Optional plug-in connector permits prefabricating wiring harness for quick, positive connection. Plug assembly includes indicator light and surge-protection circuitry.



Changing a valve within a manifold grouping is simple.

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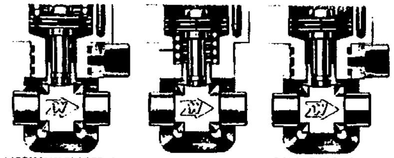
7 of 14



- Valve and actuator are joined in a single compact unit
- Standard actuator material is aluminum; valve material same as Toggle Valve
- Operates on standard shop air or fluids compatible with the actuator materials
- Gageable SWAGELOK® Tube Fitting, male and female NPT end connections
- Positive stem retraction prevents accidental cycling due to vibration or shock
- O-Ring stem seal standard — no packing adjustment required
- Moveable turret allows easy installation into any system
- 100% factory tested

TECHNICAL DATA

Valve/actuator assemblies are standard with Viton A O-Rings, TFE stem tip, and silicone base lubricant.

To order pneumatically actuated toggle valves with optional O-Ring materials, refer to the OPTIONS/ACCESSORIES, O-RING SEALS, FACTORY-ASSEMBLED IN VALVE section on page 2.

ORIFICE			VALVE PRESSURE RATING@ MAXIMUM TEMPERATURE			
in.	mm	C_v	Normally Open & Double Acting	Normally Closed	High Pressure Normally Closed	Temperature Rating
0.080	2.0	0.11	450 PSIG (3100 kPa)	300 PSIG (2000 kPa)	450 PSIG (3100 kPa)	-20°F to 200°F (-29°C to 93°C)
0.125	3.2	0.20				

	MATERIAL	SPECIFICATION
Cap	Aluminum	ASTM B211
Cylinder	Aluminum	ASTM B211
Piston	Aluminum	ASTM B211
Turret	Aluminum	ASTM B211
O-Ring	Fluorocarbon FPM	Dupont Viton A
Mounting Bracket	18-8SS	Commercial
N.O. Spring	302SS	ASTM A313
N.C. Spring	17-7PH SS	ASTM A313

Lubrication: Silicone base lubricant. For valve materials, see Page 2.

MINIMUM ACTUATING PRESSURES

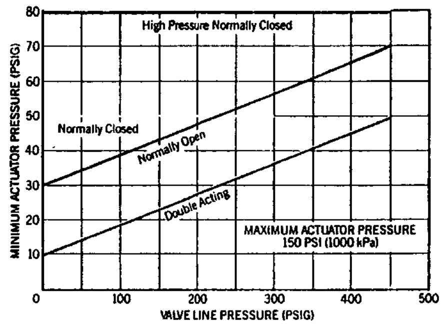
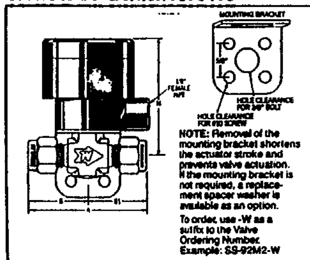


TABLE OF DIMENSIONS



NOTE: Removal of the mounting bracket shortens the actuator stroke and prevents valve actuation. If the mounting bracket is not required, a replacement spacer washer is available as an option.

To order, use -W as a suffix to the Valve Ordering Number. Example: SS-92M2-W

BASIC ORDERING NUMBER	ORIFICE in.	ORIFICE mm	CONNECTION SIZE INLET	CONNECTION SIZE OUTLET	A	B	B1	H 92-C	H 92-O	H 92-D
-92M2*	0.080	2.0	1/8 Male NPT	1/8 Male NPT	1.50	.75	.75	2.22	2.22	2.22
-92M2-S2			1/8 Male NPT	1/8 SWAGELOK	1.72		.97			
-92S2			1/8 SWAGELOK	1/8 SWAGELOK	1.94	.97				
-92F2	0.125	3.2	1/8 Female NPT	1/8 Female NPT	1.62	.81	.81	2.16	2.16	2.16
-92M4			1/4 Male NPT	1/4 Male NPT	2.00	1.00	1.00			
-92M4-S4			1/4 Male NPT	1/4 SWAGELOK	2.13		1.13			
-92S6MM			6mm SWAGELOK	6mm SWAGELOK	2.26	1.13	1.13			
-92S4			1/4 SWAGELOK	1/4 SWAGELOK	2.26	1.13	1.13			
-92S8MM			8mm SWAGELOK	8mm SWAGELOK	2.20	1.10	1.10			

*Orifice at the seat is 0.125" (3.2mm). 0.080" (2.0mm) port orifice sets the maximum flow.

Dimensions shown with SWAGELOK nuts finger-tight, where applicable. All dimensions are in inches — for reference only, subject to change.

ORDERING INFORMATION

Materials/Actuator Type: To specify *valve* material, use SS for stainless steel or B for brass as a prefix to the Basic Ordering number. To specify *actuator* type, use the designator of the desired actuator, below, as a suffix to the Valve Ordering Number.
Example: SS-92M4-S4-D

- -C Normally Closed
- -O Normally Open
- -D Double Acting
- -HPC High Pressure Normally Closed

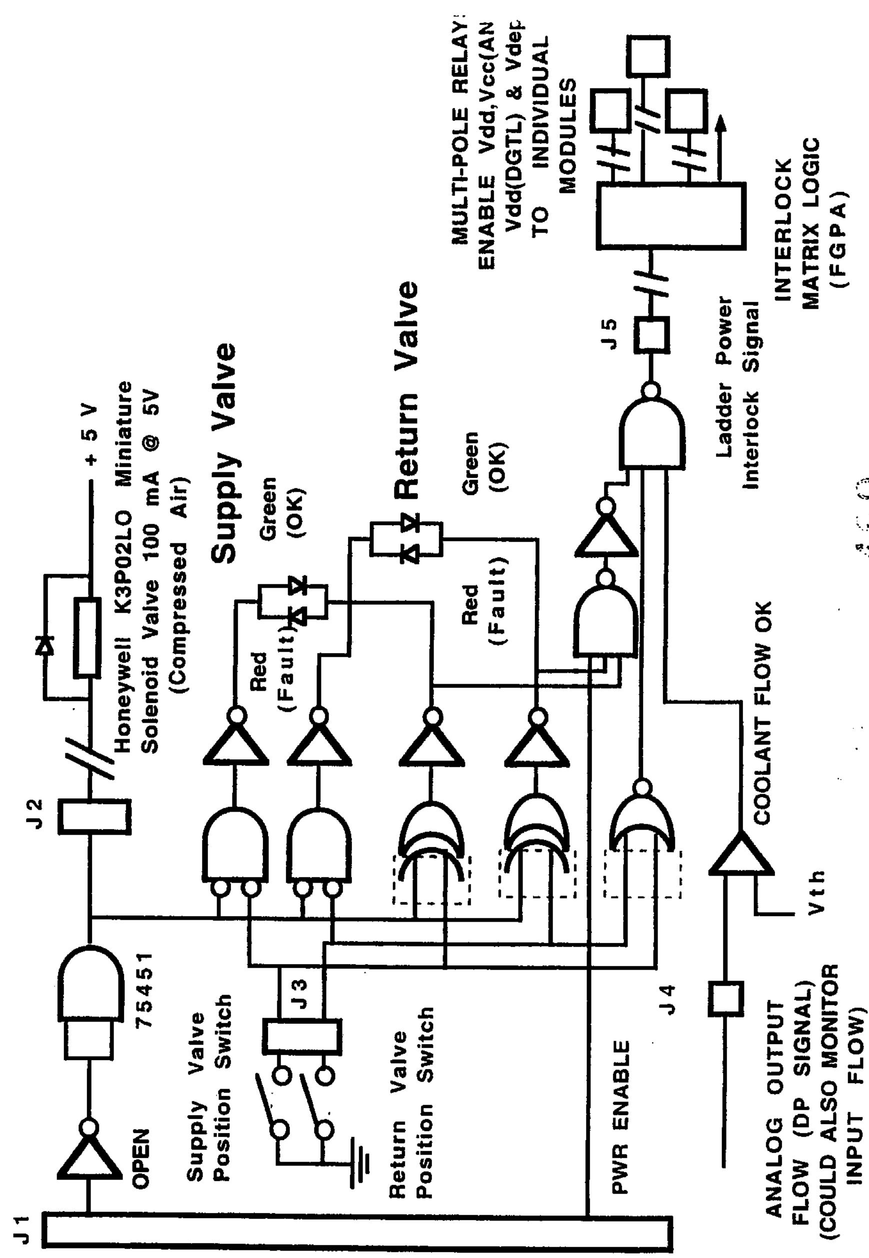
Patterns: To order angle pattern valves, insert -A before the actuator designator in the Ordering Number. Example: SS-92M2-A-O. Some of the above valves are available in a cross pattern. Cross pattern valves offer uninterrupted flow between side ports at all times; on-off flow through bottom port. Contact your Authorized Sales & Service Representative for more information.

Special Applications

WHITEY Pneumatically Actuated Toggle Valves are available for use in low temperature, high temperature, and fluorocarbon-free applications (see SPECIAL APPLICATION OPTIONS section on Page 3). To order, use the designator of the desired application, below, as a suffix to the Valve Ordering Number. Example: SS-92F2-C-LT

APPLICATION	DESIGNATOR
High Temperature	-HT
Low Temperature	-LT
Fluorocarbon Free	-NF

Printed in U.S.A. SWG-1164-C 09-92-SP MS-01-54



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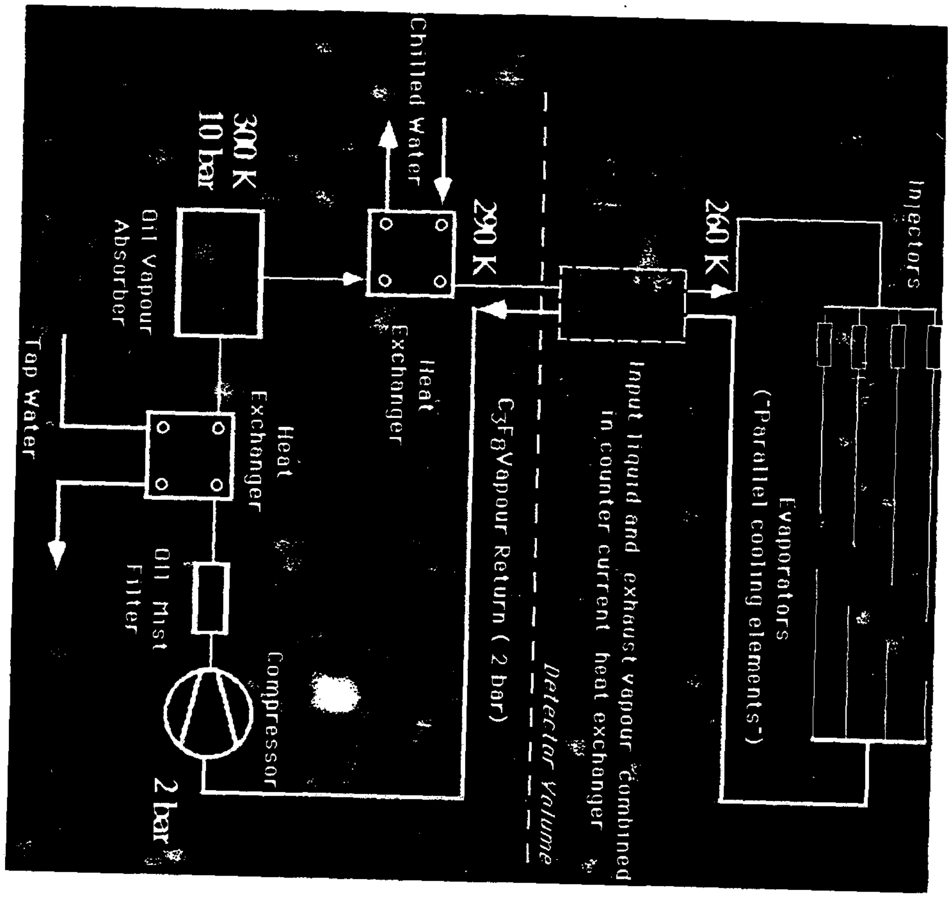
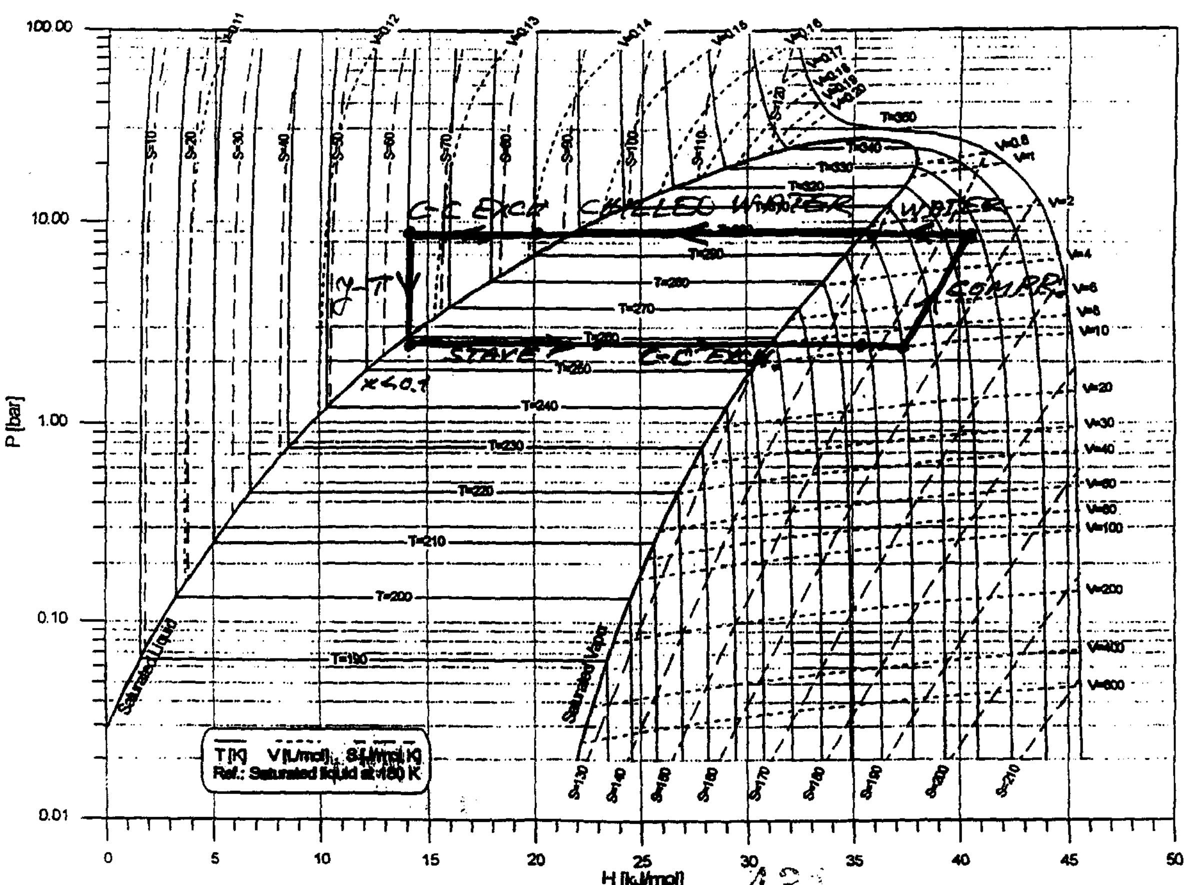


Pressure-Enthalpy Chart for PF-5030



EVAPORATIVE COOLING WITH C_4F_{10} FLUOROCARBON HAS BEEN SUCCESFUL WITH ALL ATLAS PIXEL STRUCTURES SO FAR TESTED. [illegible] BASELINE [illegible]

C_4F_{10} EVAPORATION GIVES COOLING TUBE WORKING PRESSURES AROUND 500 mbar (abs) FOR TEMPERATURES AROUND $-10°C$ (S.V.P. CURVE), ALLOWING USE OF THIN WALL (LOW X/X_0) TUBE ACROSS DETECTOR ACTIVE AREA.

ONLY PART OF SYSTEM ABOVE [illegible] MANIFOLD)
[illegible] F INJECTION [illegible]

INJECTORS CAN BE VERY SMALL, ROBUST, ACCURATELY MATCHED AND INEXPENSIVE: RUBY WATCH JEWELS

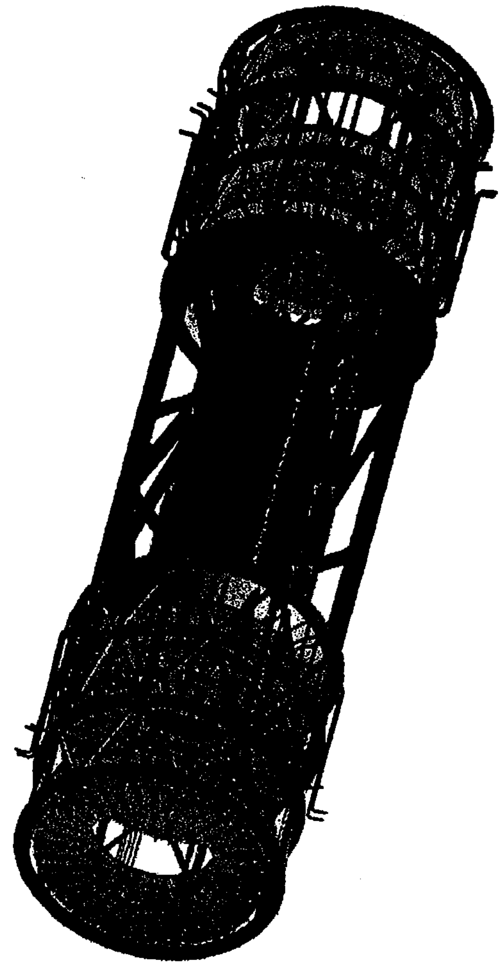
TESTS WILL CONTINUE IN ATLAS WITH NEW PIXEL STRUCTURES AND WITH STRUCTURES FROM THE BARREL AND FORWARD SCT.

[illegible]

ATLAS Pixel Disk Mechanics

E. Anderssen, D. Bintinger, J. Emes, M. Gilchriese,
F. McCormack
Lawrence Berkeley National laboratory

W. O. Miller
HYTEC Inc.



Disk Layout Considerations

Modules arrayed on both sides of disk for complete coverage

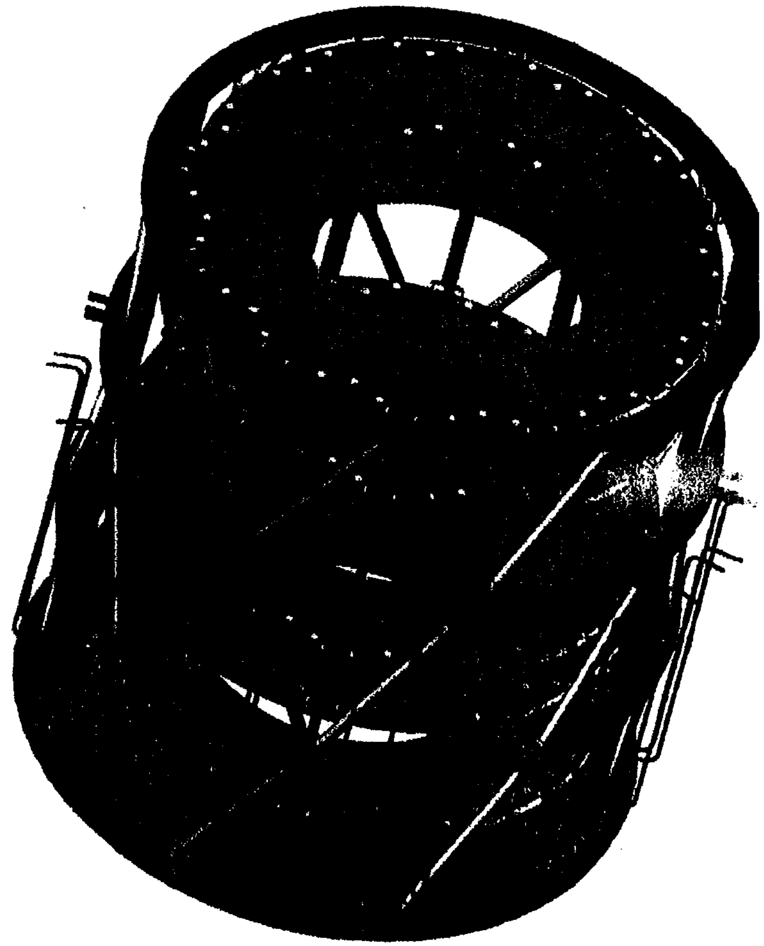
Leads to: Balanced mechanical structure

Reduced heat flux into coolant flow

Provide cooling over entire active area ~ 400 W/disk

Desire similar disk and barrel modules

Divide disks into sectors ~ 12 sectors/disk
As alignment units
cooling units
assembly units



Pixel Disk Mechanical Design

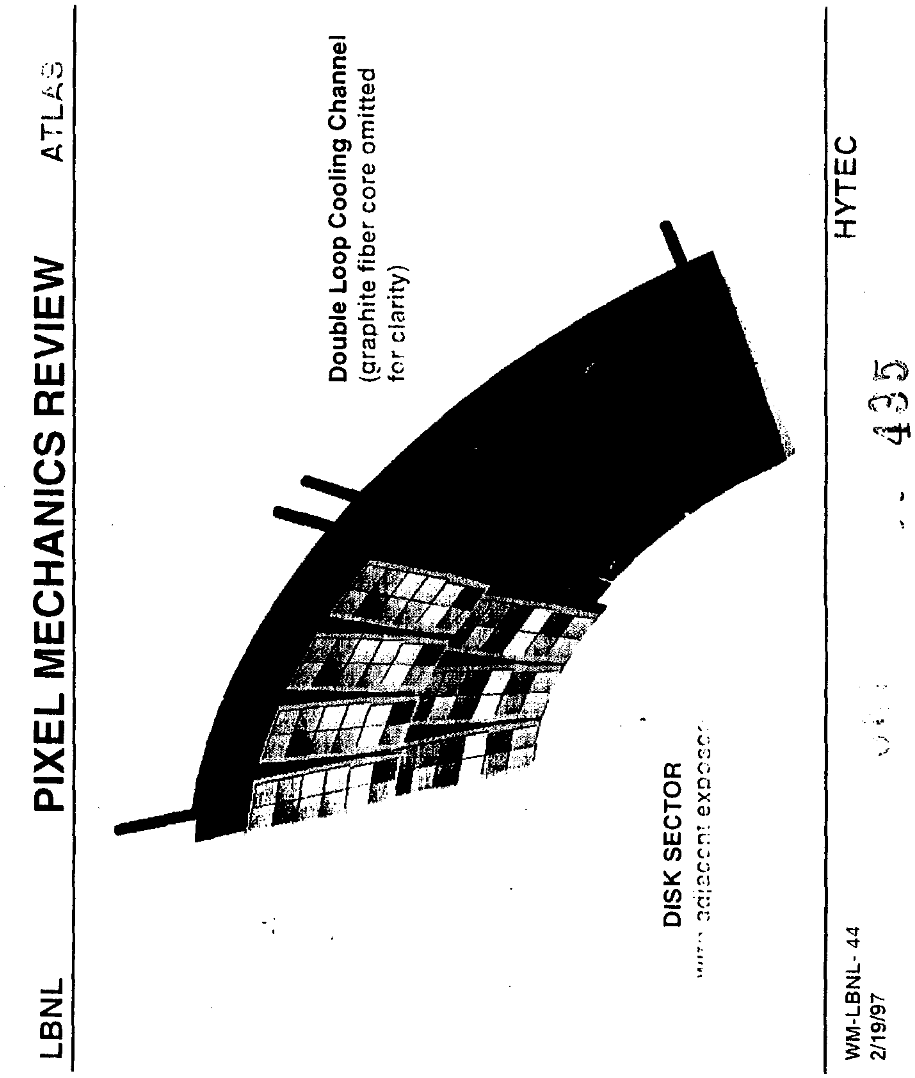
Basic design unit is the Sector.

A sandwich design for a sector is natural given layout:
- Stiff, heat conducting, low CTE Face Plates
- Shaped Cooling Tube between face plates
- Fill of minimal mass

Face Plates: investigated aluminum, beryllium, albemet, CFR composites, Carbon-Carbon, graphites, etc.
- Have chosen Carbon-Carbon:
  - CTE xy: -1.0 ppm/K, z: 6.0 ppm/K
  - Modulus ~ 185 GPa
  - Thermal conductivity ~ xy: 200 W/mK, z: 32 W/mK
  - Radiation length 23 cm
  - Nonhygroscopic

Cooling Tube: investigating glassy carbon, sealed carbon-carbon, sealed graphite, and aluminum
- No decision at present. Prototypes underway.

Interfacing Fill: investgating carbon fibers (with glassy carbon tube) and reticulated vitreous carbon
- No decision at present. Prototypes underway.



Pixel Disk Sector Prototype Programs

Prototype program 1: Carbon-carbon facings (0.5 mm thick), shaped glassy carbon coolant tube (3.2 mm id), high thermal conductivity carbon fiber fill (goal 5% density).

Prototypes constructed by Energy Science Laboratories, Inc. (ESLI). ESLI has succeeded in fabricating shaped glassy carbon tubes of appropriate ID and wall thickness.

Prototypes 4 and 6 have average radiation lengths of 0.73% and 0.65% respectively.

Prototype 4 is currently undergoing ESPI testing.

Main concern is thermal connection via fibers between coolant tube and facings.

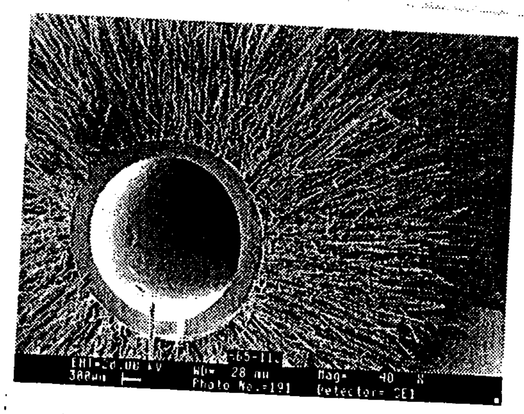
Prototype program 2: Carbon-carbon facings (0.5 mm thick), shaped and flattened aluminum coolant tube (3.6 mm id, 0.2 mm wall), and reticulated vitreous carbon fill (3% density).

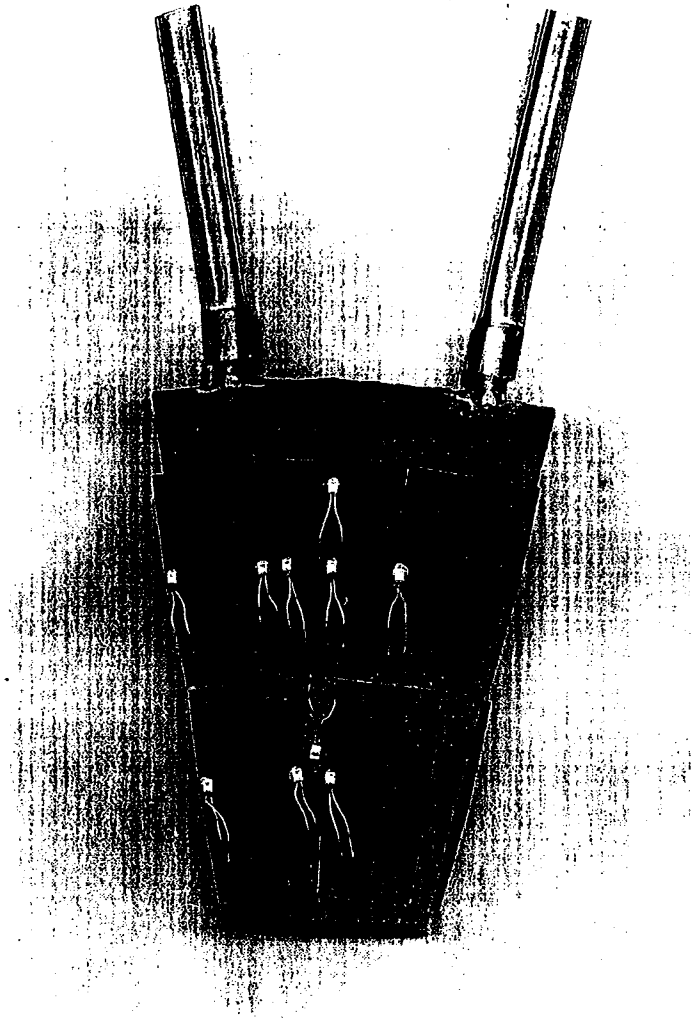
Have succeeded in shaping 0.2 mm wall aluminum tube.

Prototype 3 has average radiation length of 0.76%.

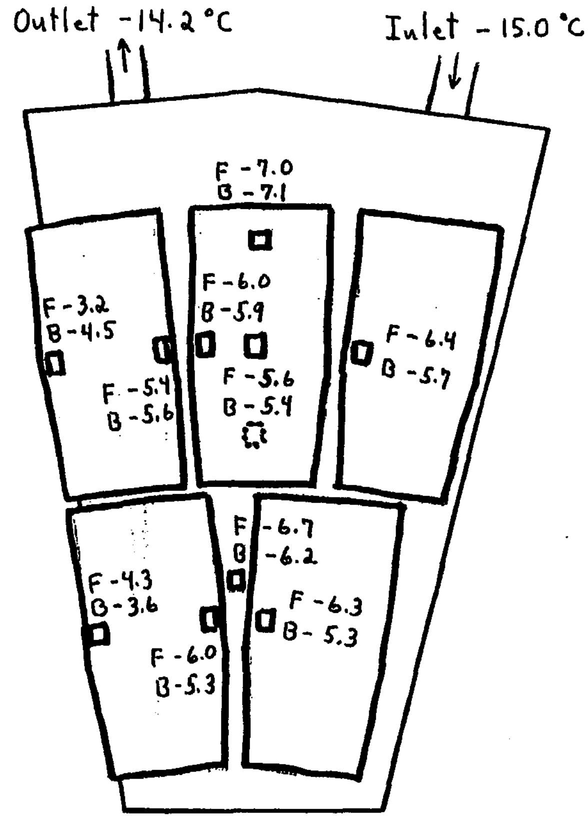
Prototype 2 showed good structural characteristics in ESPI tests without dummy silicon modules.

Prototype 3 has shown excellent thermal characteristics with water based coolant.





ESL1 Sector 4



Coolant: 30% Methanol by volume

Flow: 11.8 cc/sec , Δp = 208 mb

Adhesive for Silicon: 125μ of CGL7018

Power: 36 W , Ambient -8.7 °C

Title:
Sub-region size: 752,576 Layer: 1 Scaling factor: 0.5 Range: 2,20 Current date: 22-May-1997 Current time: 10:10:54

Picture size: 752,576,1 Class: Image Form: Byte Creation date: 27-Apr-1998 Creation time: 16:15:42
Title:
Sub-region size: 752,576 Layer: 1 Scaling factor: 0.5 Range: 1,10 Current date: 27-Apr-1998 Current time: 16:18:02

Pixel Mechanics Meeting

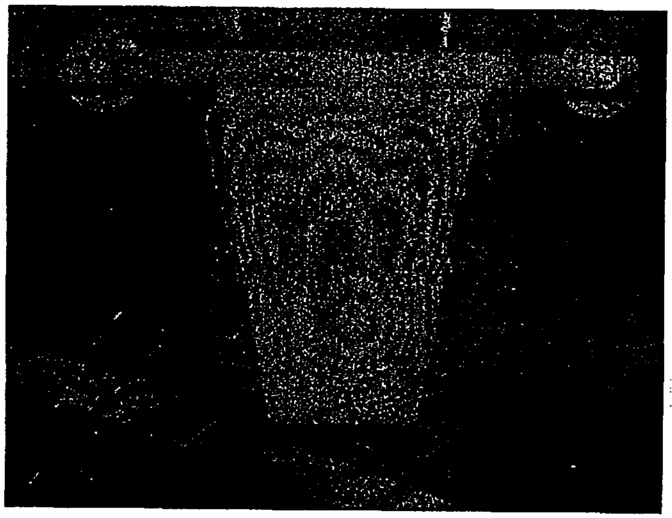
ESLI Sector #3

0.96 °C ΔT $T_1 = 6.14$ °C No Heater Pwr Coolant 1.7 cc/s

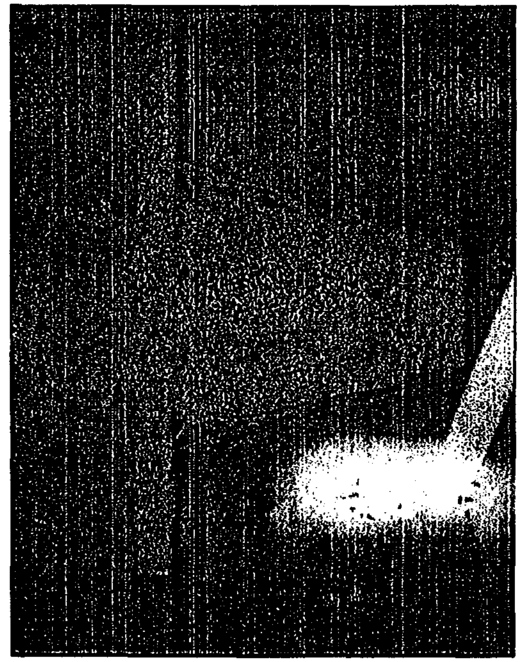
"Bear Paw" Pattern 4 Fringes over wafer region 1.04 μm's

2 Fringes along sides, some at bottom ~ 1.3 μm's

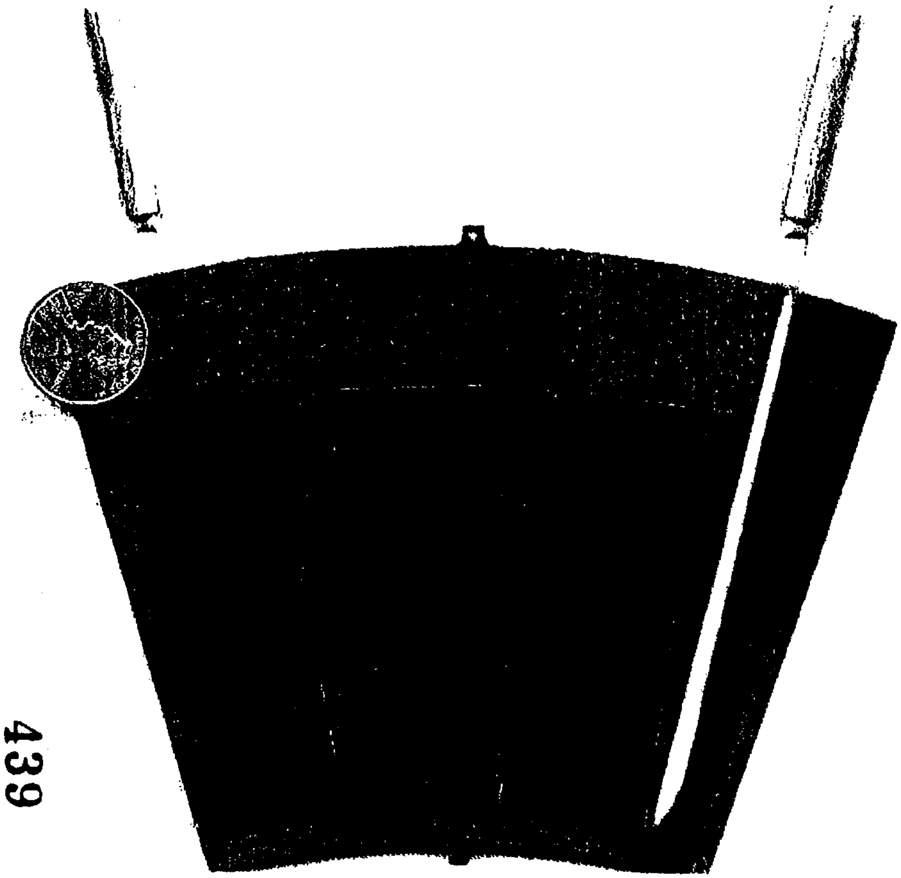
438



21/May/1997 ESLI #3 1630-1640



27 Apr 2:14-2:16 -7.0 to -11.0 C



RETICULATED VITREOUS CARBON (RVC)*

WHAT IS RVC?

RVC is a new open pore foam material composed solely of vitreous carbon. Vitreous carbon, as the name implies, is a form of glass-like carbon which combines some of the properties of glass with some of those of normal industrial carbons. RVC has an exceptionally high void volume (97%), high surface area combined with self-supporting rigidity, low resistance to fluid flow, and resistance to very high temperatures in non-oxidizing environments. It is now available in a wide range of pore size grades weighing about 3 pounds per cubic foot.

WHAT IS DISTINCTIVE ABOUT RVC?

- Exceptional chemical inertness over a very wide temperature range.
- Unique high-temperature strength combined with low bulk thermal conductivity.
- Unusual rigid geometry which provides a large surface area combined with low pressure drop to fluid flow, along with great ability to hold infused materials within controlled porosity sizes.
- Electrical conductivity.

HOW CAN RVC BE USED?

- Porous Electrodes—for electrochemical processes that require very high current distribution areas, low electrical or fluid flow resistance, and minimal cell volume loss to electrodes.
- High Temperature Insulation—for inert gas and vacuum furnaces where its ease of fabrication, self-supporting nature, low density, low outgassing, low heat capacity and excellent K value combine to improve efficiency and reduce costs over conventional insulating materials.
- Filters and Demisters—for molten metals, corrosive chemicals, high or low temperature gases and liquids, where maximum chemical inertness combined with good filtration and detrainment is needed.
- Storage Batteries—in high energy density batteries, such as the sodium/sulfur and lithium aluminum/iron disulfide systems, where its unique "caging" effect on infused materials benefits performance, reduces cost.
- Scaffolds—for biological growth (it is non-toxic and biologically inert) in pollution-control systems, as a catalyst or catalyst support, in tower packings, where low pressure drop combined with large available surface area and chemical inertness is required.
- Semi-Conductor Manufacture—offers unique advantages in etching and diffusion treatment carriers, reduces manufacturing cost.
- Acoustic Control—a specially densified form combines outstanding high temperature resistance in non-oxidizing environments with excellent noise absorption in the 250 Hz to 3 kHz range.

WHAT ARE RVC'S PROPERTIES?

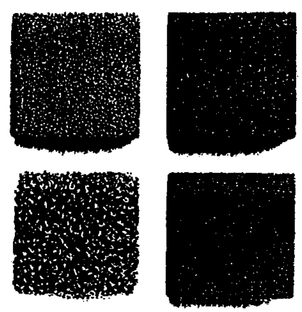
CHEMICAL PROPERTIES

RVC is composed of one of the most chemically inert forms of carbon known. Its oxidation resistance is unusual for a carbon. In spite of RVC's large surface area it does not support combustion after heating to bright incandescence in air followed by removal of the heat source. It is also highly resistant to intercalation by materials which disintegrate graphite.

RVC is also inert to a wide range of very reactive acids, bases, and organic solvents. At high temperatures it will form carbides, but is inert to non-carbide forming metals and is not wetted by many molten metals. Heating in air at 600°F enhances its adsorption properties. Because of RVC's large surface area, heating above 600°F in air will result in significant oxidation at rates which increase with increasing temperature.

30 PPI

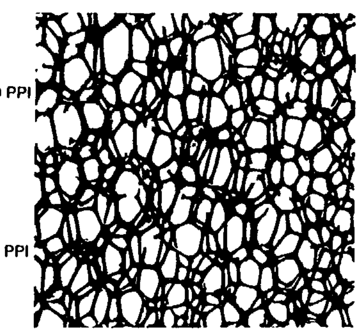
10 PPI



Several of the available pore size grades of RVC (PPI = Pores Per Linear Inch)

80 PPI

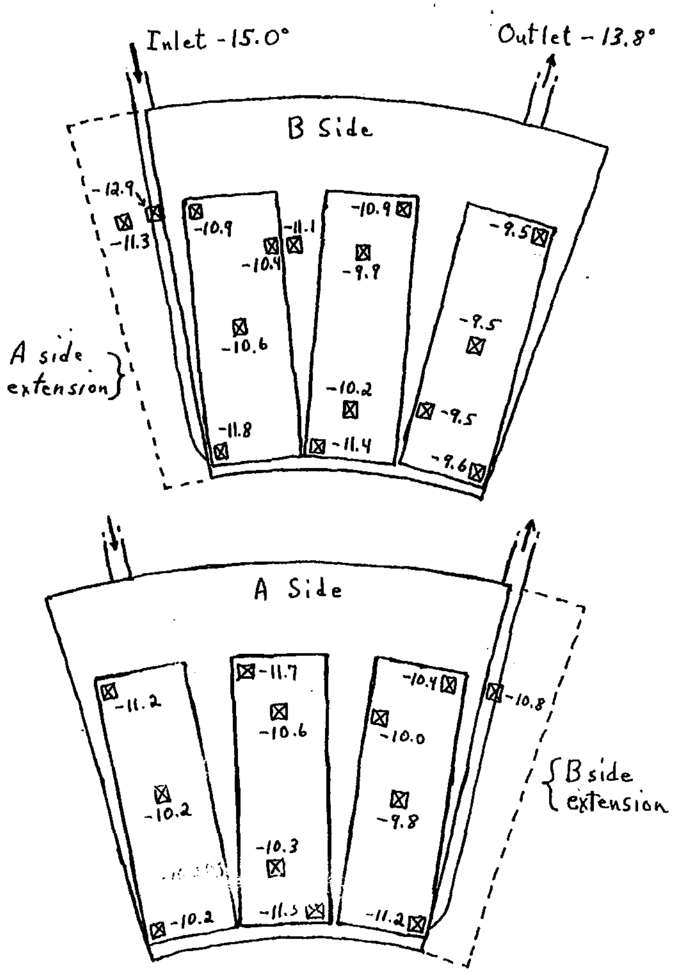
60 PPI

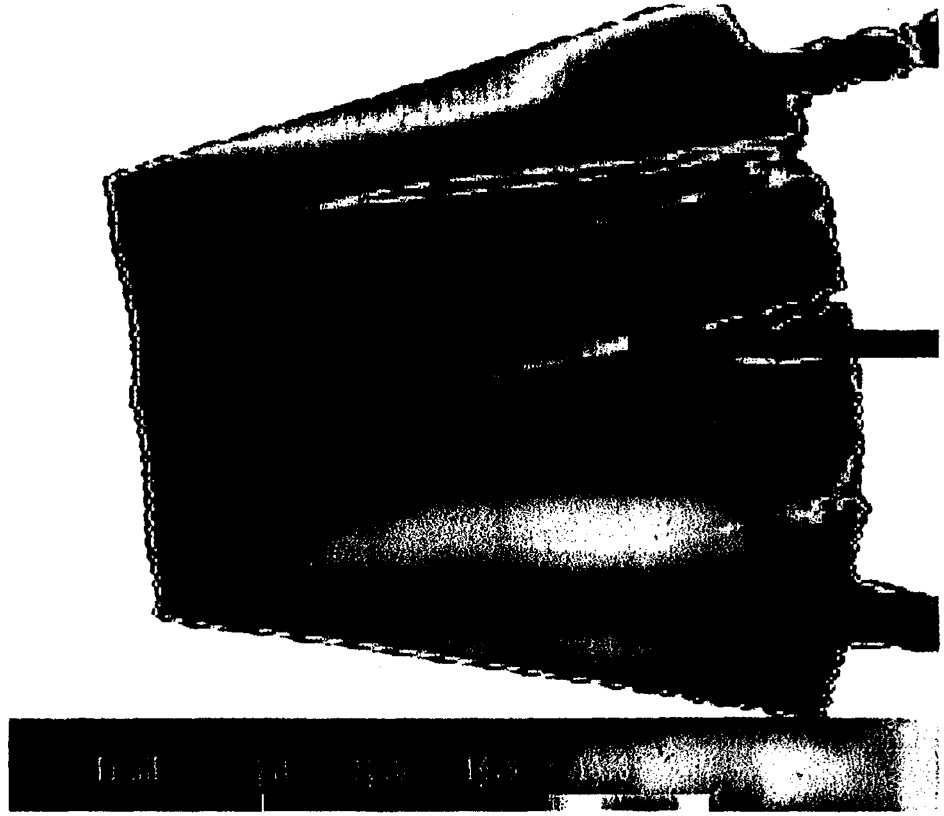


Enlarged view showing the open cell (reticulated) structure of RVC.

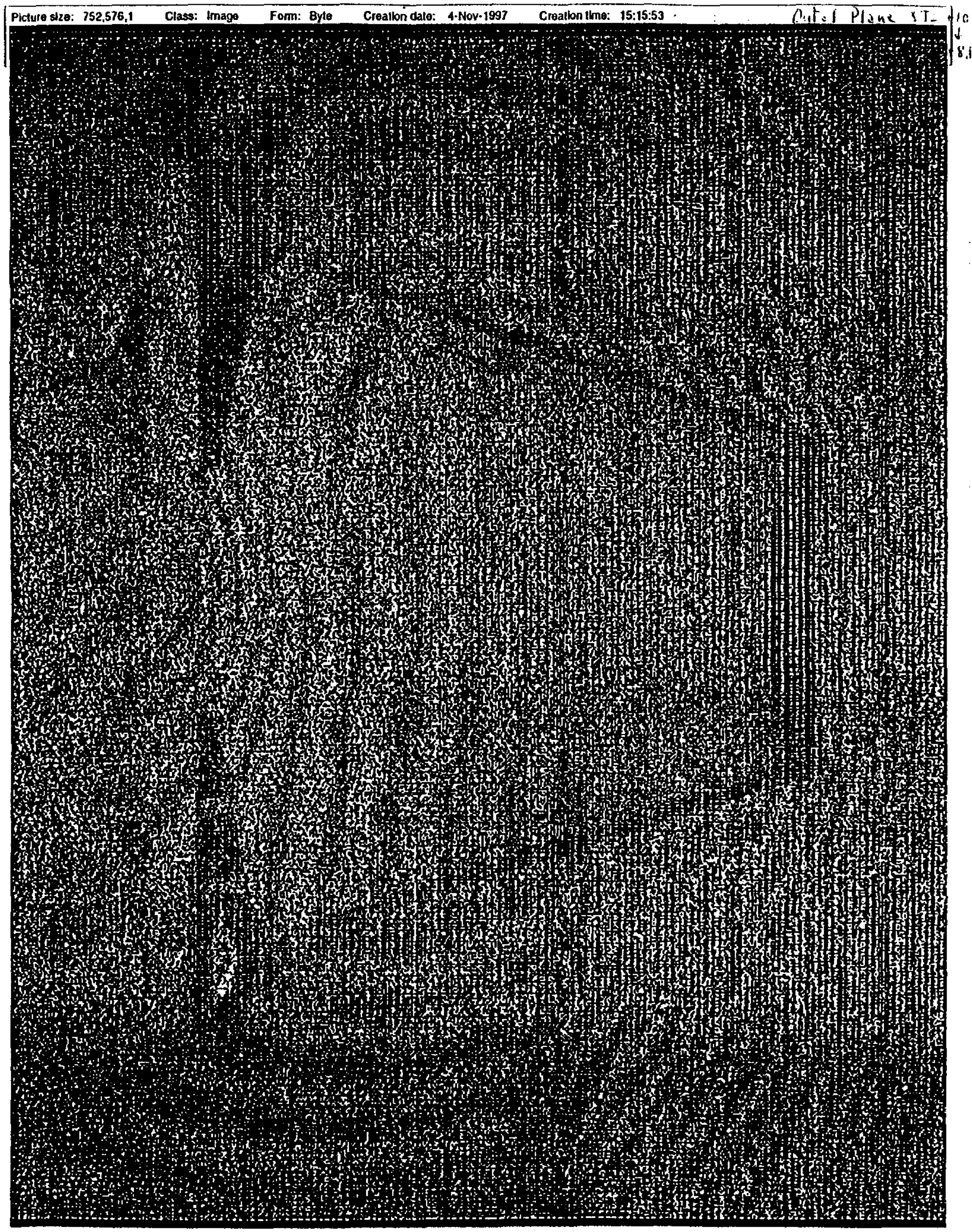
* Trademark

Aluminum Tube Sector Nr. 3
Five Disk Design





Coolant: 22% Methanol by volume, Flow 10 cc/s
ΔP = 196 mbar, Power 38.8 Watts, Ambient -9.2 °C
Adhesive for silicon: 85μ of CGL7018



Prototype program 3: Carbon-carbon facings (0.5 mm thick), machined and sealed carbon-carbon or graphite coolant tube (3.2 mm id), may not need fill material.

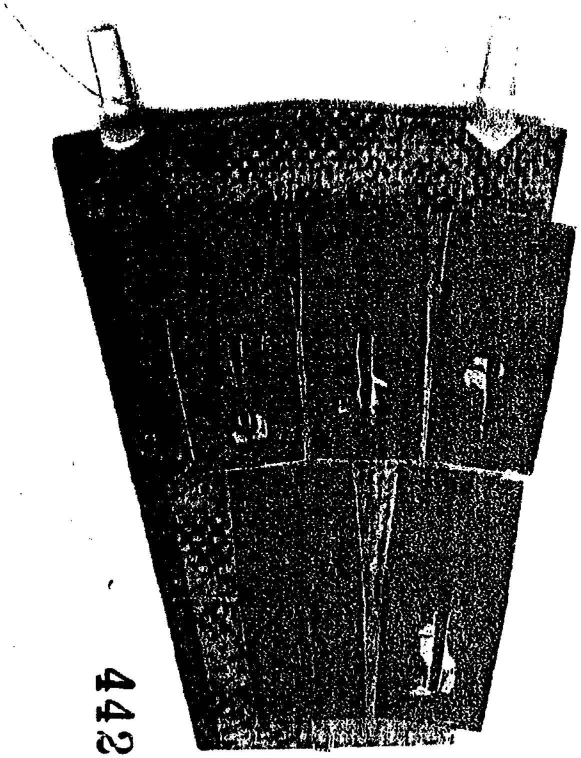
Structural properties are assumed to be excellent as the sector is all carbon with no adhesives.

Prototype 2 radiation length of 1.24% can be reduce to less than 1.0% with reduced mass coolant tube.

Prototypes 1 and 2 had excellent thermal properties.

Main concern is sealing the carbon-carbon or graphite coolant tube. Coolant tube of prototype 2 has been sealed with Parylene and was found to have a Helium leak rate of approximately 10^{-6} cc/s after 24 hours of coolant exposure.

Module Attachment: investigating adhesives to provide thermal conductivity, electrical insulation, removability, and low stress



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Silicon Adhesive Tests

Adhesive	Therm. Cond. (W/K*m)	Bulk Resist. (Ohm*cm)	Removable	Comments
AI Technology CGL7018	1.5	$9 * 10^{8}$	Yes	X_0 ~ 15 cm Curable paste
AI Technology CGR7018	1.6	$1 * 10^{12}$	Yes	X_0 ~ 15 cm Paste, Flows
Dow Corning 340	0.6	NA	Yes	X_0 ~ 8 cm Paste
Master Bond EP21AN	0.6	$2 * 10^{11}$	No	Room temp. cure
Thermagon 1KA08	1.6	$3 * 10^{12}$	No	Sheet adhesive
AI Technology CP7508-MP	0.5	$7 * 10^{13}$	Maybe	Mica sheet Brkdown >2.5kV
Cotronics Duralco 134	0.7	$2 * 10^{8}$	Yes	Paste
Norland NEA 123	NA	$> 10^{14}$	Yes	UV Cure For tacking

Radiation Tests have begun for items 1 and 3.

Infrastructure Session
May 8, 1998

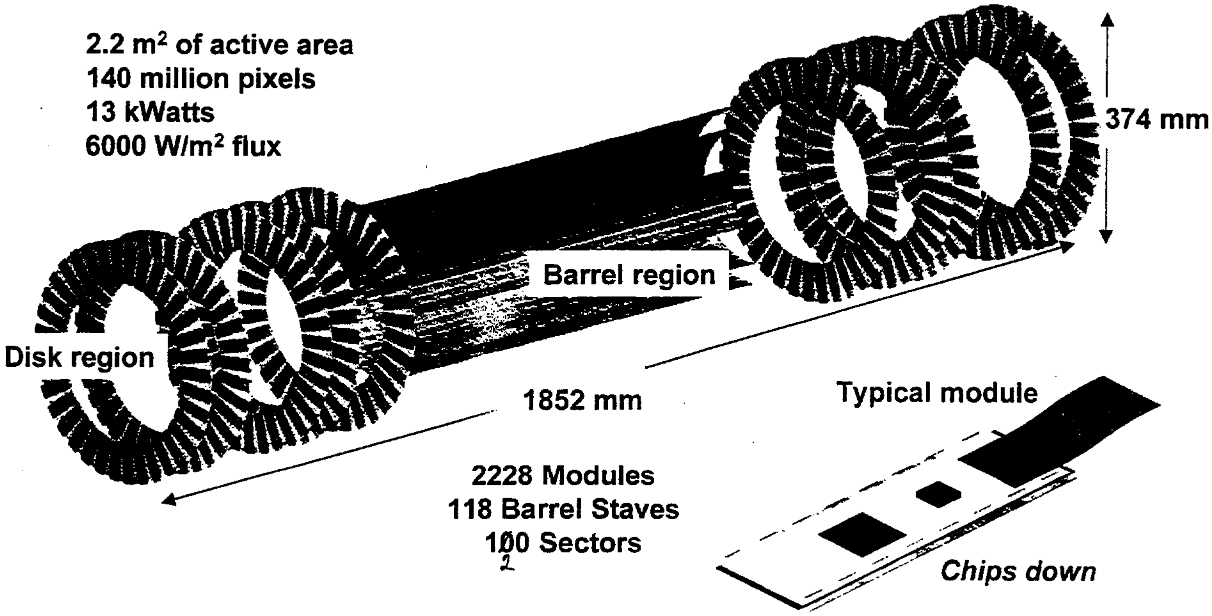
W. Miller

Pixel Mechanics

- Topics-Pixel Detector Developments for LHC
  - Overview of ATLAS Pixel Detector
  - Disk Region
    - thermal design issues/choices
  - Primary detector structures-FEA Studies
    - outer frame structure
    - barrel and disk supports

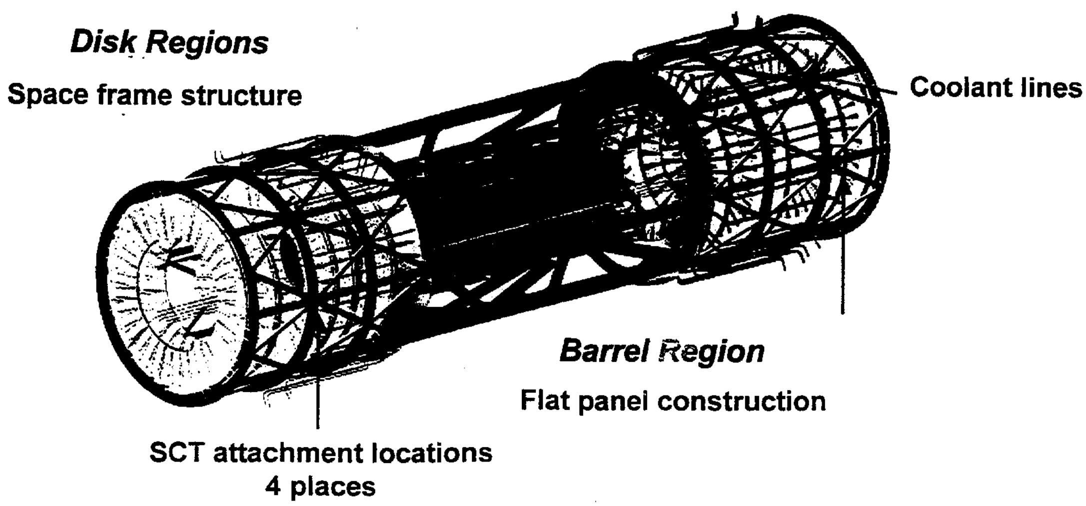
ATLAS PIXEL DETECTOR

2.2 m^2 of active area
140 million pixels
13 kWatts
6000 W/m^2 flux



Support Concept for ATLAS

General Arrangement



Mechanical Design Issues

Issues

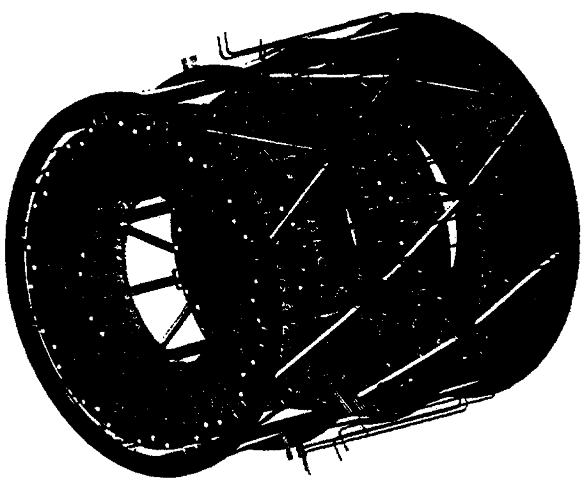
- Stability
  - Short and long term <10 μm's
  - Thermal strains from 40 °C change
  - Avoidance of flow induced vibrations--laminar flow
- Material limitations/Radiation length
  - High stiffness to weight ratio structures--stability problem
    - support mass 5 or times structural weight
  - Low Z Materials-- narrows options
- Cooling
  - Pixel array uniformly distributes heat
    - dictates use of coolant in tracking volume
  - Coolant thermal boundary effects
  - Coolant compatibility with module

Investigations

- Materials
  - Focused on ultra-stable composites
    - Radiation length second only to Beryllium
    - Extremely high stiffness to weight ratio
  - Introduced use of carbon-carbon composite for pixel module support (*widely accepted*)
    - Rad-hard
    - High thermal conductivity
    - Stiff and high strength
- Experimental studies
  - Sector thermal/stability tests
  - C_4F_{10}, and water-based testing
  - Thermal interface materials, rigid adhesives, greases, and gels
  - Sealing carbon-carbon channels

Pixel Detector Disk Region

Planar array
•5 Disks/Region
•12 Sectors/Disk
•Individually Supported
•Integral Cooling

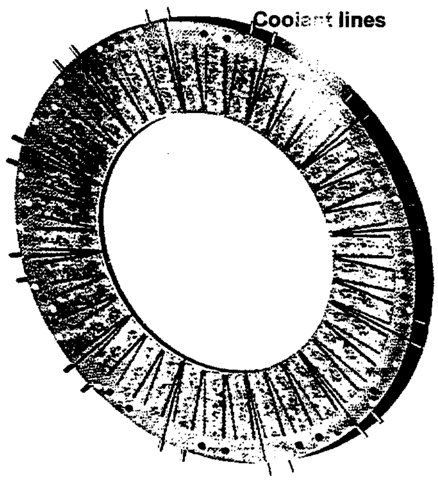


Stability
5 μm's φ
20 μm's Z
10 μm's R
Globally
Final Position
25 μm's φ
80 μm's Z
50 μm's R

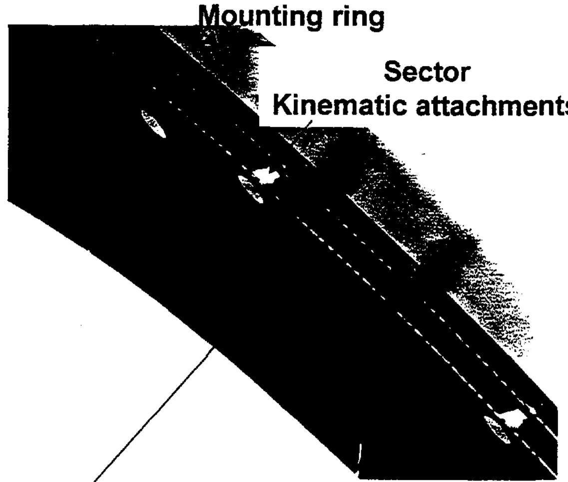
General Concerns, both disk and barrel regions
•Heat Removal
•Detector Stability
•Local and Globally
•Precision Construction/Alignment

Pixel Disk Assembly

Disk with 12 Sectors



Enlarged view



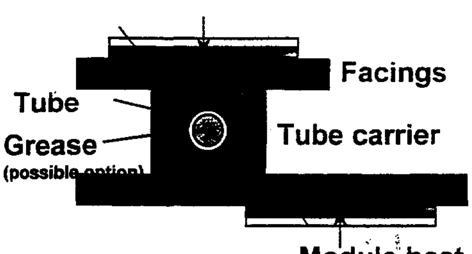
Sector support, cantilevered from outer edge

Carbon-Carbon thermostructure (fiber core omitted)

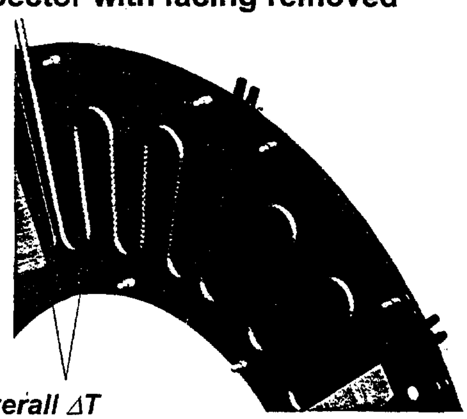
Temperature Gradient Issue- For 0.6 W/cm^2 (Cut-Away Of A Typical Sector)

	°C
• <u>Potential ΔT's-</u>	
– Adhesives	0.5 to 1.0
– Module Carrier	6.0 to 0.5
– Tube carrier	2.0 to 1.0
– Grease Film	1.0 to 0.5
– Cooling Tube	0.7 to 0.1
– Coolant	6.0 to 2.0
• Probable Range	16 to 5
• Objective	< 9.0

- *<u>Actual ΔT's:</u> Set by cooling fluid used, heat flux at tube surface, configuration, and materials chosen*



Sector with facing removed



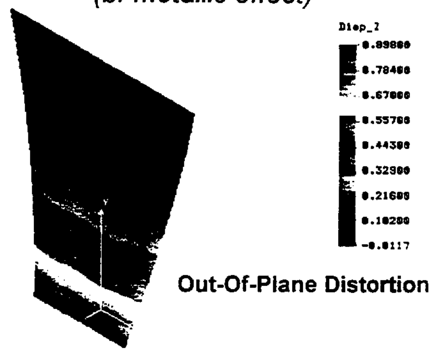
Overall ΔT module surface to coolant

Material Options -Limited To Low Z Materials

- <u>Metals</u>
  - Beryllium, best choice, 35 cm Radiation length
    - Disadvantage-High CTE
    - High cost
    - Can be brittle in thin sections
  - Aluminum, second choice, 9 cm Radiation length
    - Disadvantages, high CTE, poor radiation length
- <u>Composites</u>
  - Typical graphite fibers, XN50, P75, P120, etc.
    - Laminates have high stiffness to weight ratio, superior to metals
  - Low CTE
  - Demonstrated stability
  - Radiation resistant
  - Easy fabrication

<u>Influence of different CTE's</u>

(bi-metallic effect)



<u>Single sector facing with 7 modules</u>

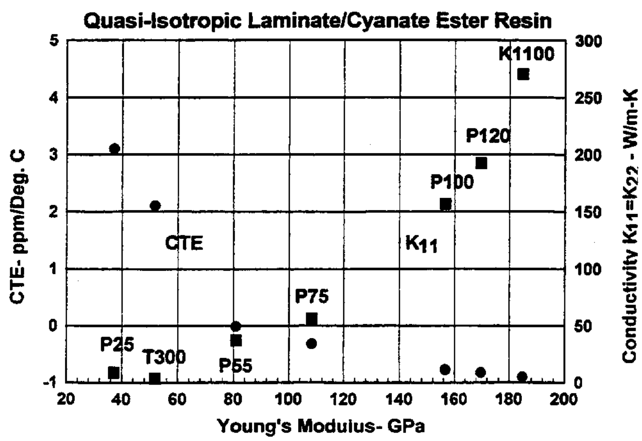
•C-C/Silicon, peak distortion 0.9 mm

•Be/Silicon, peak distortion 1.92 mm

Overcome this effect by a sandwich construction for the sector

Material Options-Composite Laminate Material Properties Polymeric Resin Systems Poor Thermostructure Choice

- Quasi-Isotropic laminate properties
  - For positive CTE close to silicon
    - Stiffness ~that of Al
    - Thermal conductivity <u>very poor</u>
      - K_{11}=8.9 W/m-K
      - K_{33}=0.7 W/m-K
  - High Modulus
    - Stiffness ~that of Steel
    - Thermal conductivity improves in-plane
      - K_{11}=200 W/m-K
      - K_{33}=1.2 W/m-K, <u>Still Too Low</u>
    - CTE becomes negative
      - CTE -1 ppm/ °C
- Benefit Of Carbon-Carbon Composite
  - Fiber (e.g. XN50)
    - K_{11}=K_{22}=185 W/m-K
    - K_{33}=25-40 W/m-K

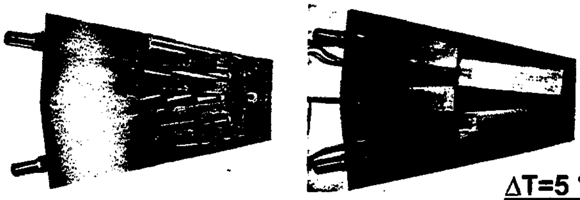


Sector Construction Concepts

- Selected criteria to achieve stability and thermal performance
  - Constructed from materials with low CTE's
  - Avoided mixing materials with significant differences in CTE's
  - Materials chosen on basis of high radiation length and high thermal conductivity
  - Sandwich structure with embedded coolant channel
- Sampling of prototype configurations
  - Carbon tube thermostructure
    - uses C-C carbon facings
    - carbonized structure
    - fiber core sandwich
  - Machined C-C channels, bonded sandwich with C-C facings
    - requires sealing C-C channel with resin or e.g., glassy carbon
  - Thin-wall C-C tube, bonded sandwich with C-C facings
    - well balanced CTE
    - high conductivity
    - options investigated for sealing are resin and glassy carbon

Sector Cooling/Structure Developments

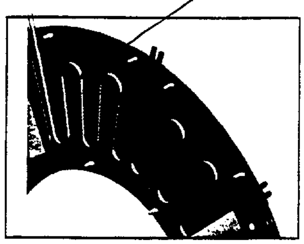
Bonded structures



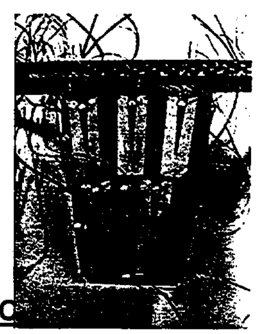
ΔT=5 °C

Machined graphite
and carbon-carbon channels

Thermal Design Parameter: 0.1 W/mm @ tube
3.2 mm diameter tube



Carbonized structure



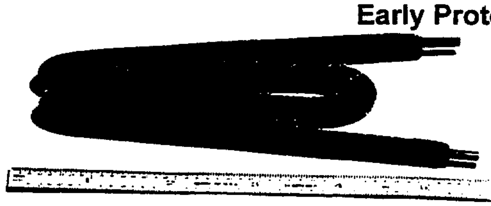
ΔT=9 °C

Early Prototype

ΔT=4 °C

C_C Tube/Bonded Interface

Carbon-carbon tube, 3.4 mm ID, 0.27 mm wall. Left side of figure shows the tube after densification; right side shows similar a tube after coating with glassy carbon.

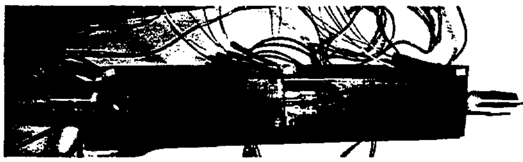


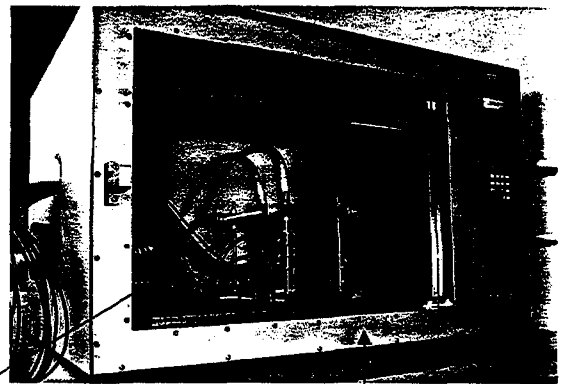
Carbon Tube/Fiber Carbonized Interface

Detector Thermal Performance Experiments

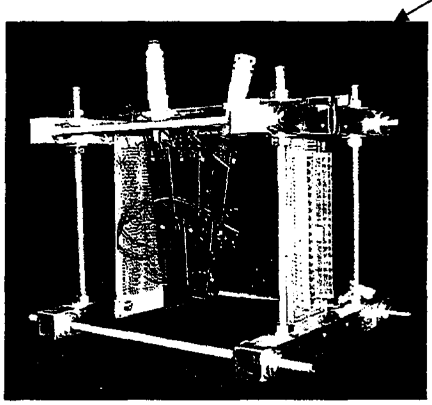
Precise Thermal Measurements

Carbon-Carbon tube structure



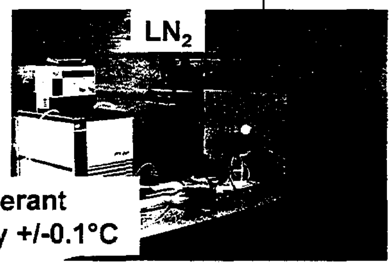


Typical Sector



Chamber control +/- 0.1°C

LN_2



Refrigerant supply +/-0.1°C

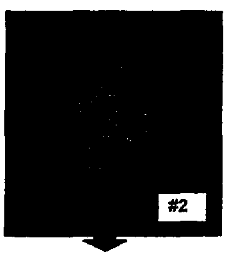
Alcohol/water based coolant

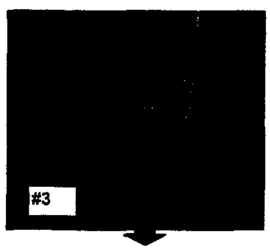
Stability Measurements/FEA Modeling

Experiments
(Oxford Univ.)

Desired Condition

10.6 °C ΔT





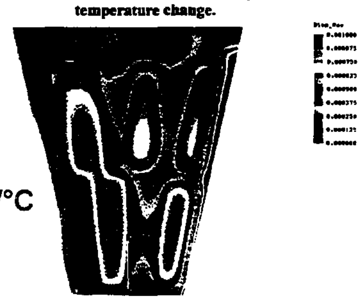
Low Core Shear Modulus

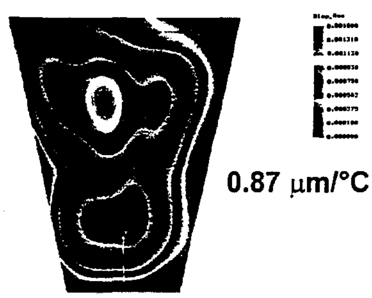
1.72 °C ΔT

Figure 6. Sector #2 fringe pattern for 10.6 °C temperature change (0.78 μm's local wafer bowing) and fringe pattern for Sector #3 (1.5 μm's bowing) for 1.72 °C temperature change.

Predictions

0.094 μm/°C





0.87 μm/°C

Figure 8. Finite element thermal strain solutions for Sector #2 and Sector #3, for temperature changes of 10.6 °C and 1.72 °C respectively. The predicted peak module deflections are 1 μm and 1.5 μm respectively. Approximate ESPI values of 0.78 μm's and 1.5 μm's respectively (Fig. 6)

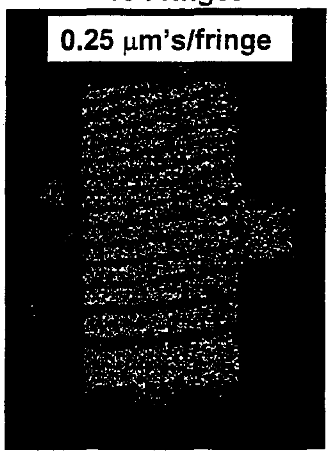
Detector Stability Measurements

TV Holography System under construction at HYTEC

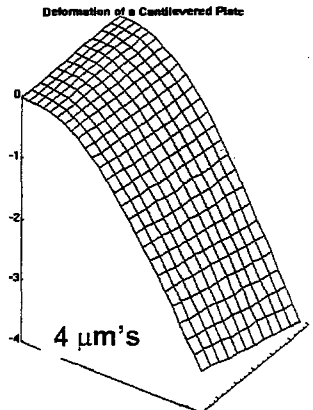
Real-time thermal and vibration measurements

Example of Precision
Bending and Twisting of a Cantilevered Wafer

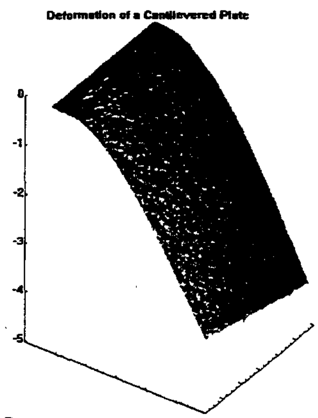
16 Fringes



Wire frame model



Shaded reconstruction



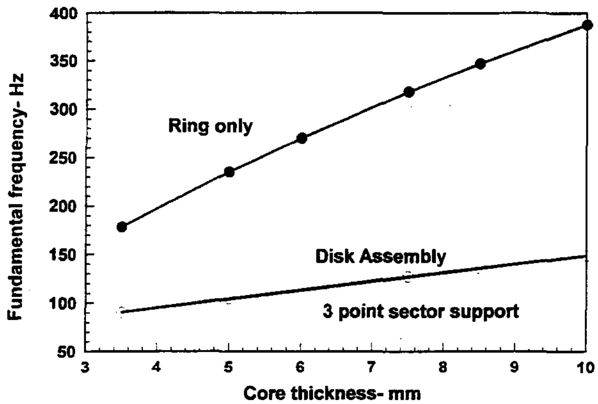
Static displacement-μm's

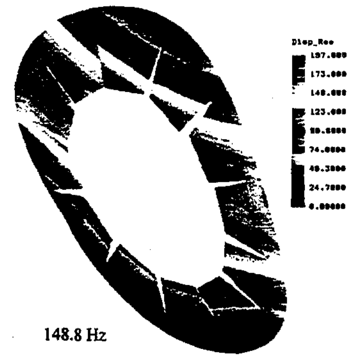
Pixel Disk Sector

- Development progressing
  - desired thermal performance is attainable
  - investigations with C_4F_{10} evaporative fluid in progress and results are encouraging
  - stability testing far from complete
- Issues of mixing construction materials are not resolved, particularly different CTE's
  - cause thermal strains at times in excess of stability criteria
  - force solutions requiring compliant interface materials
- Most stable structure to date
  - achieved with carbonized thermal structure
    - little mismatch in CTE's
    - stiff sandwich construction

Pixel Disk/Support Dynamic Stiffness

Disk and Supporting Ring Structure





10 mm thick sandwich

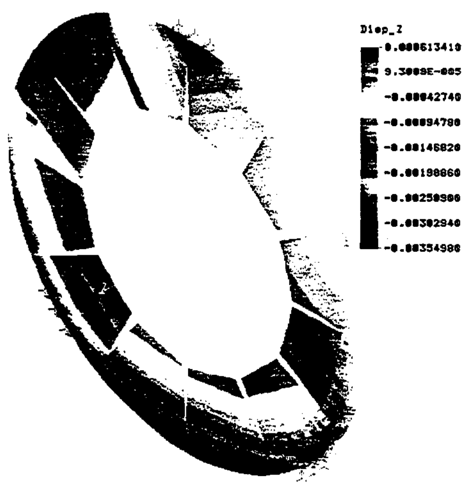
Ring Parameters
R_o=210 mm R_i=180 mm

Sector
C-C Sandwich with fiber core

Pixel Disk Thermal Strains

- Support conditions
  - Three point support of composite ring
  - 12 sectors with three point rigid connection
- Materials
  - Sector, Carbon-Carbon, graphite fiber core sandwich
  - Ring, Carbon-Carbon facings, honeycomb core
- Temperature effects
  - Cool-down from room temperature, ΔT=40 °C

Out-of-plane illustration

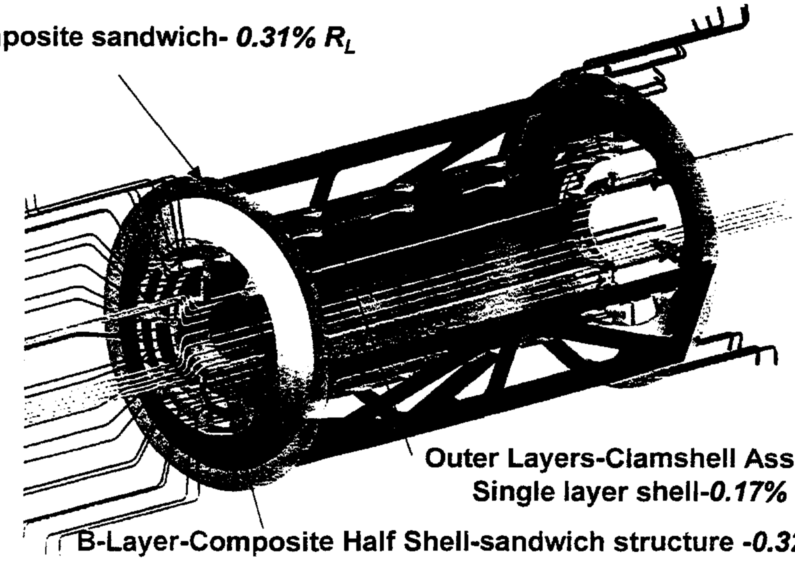


Peak sector displacement at support-3.5 μm's

Barrel Region Structures

Stable Ultra-Lightweight Composites

End Cones-composite sandwich- *0.31% R_L*



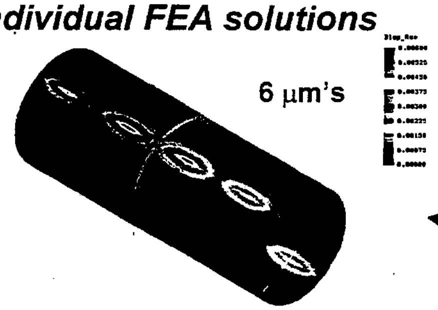
Outer Layers-Clamshell Assembly
Single layer shell-*0.17% R_L*

B-Layer-Composite Half Shell-sandwich structure *-0.32% R_L*
(Inserted into Inner Detector Assembly)

PIXEL98 PIXEL WORK SHOP

Frame Studies Barrel Region

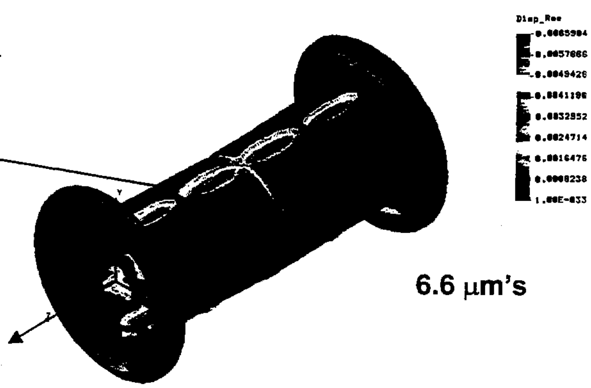
Individual FEA solutions



6 μm's

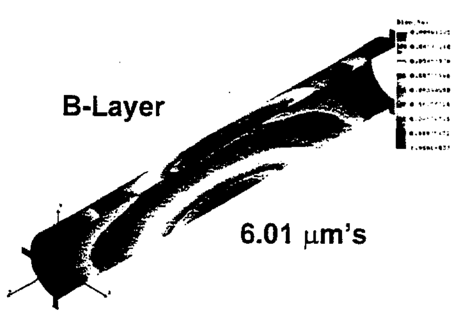
Outer Clamshell

Combined Solution
Including effects of End Cones



6.6 μm's

B-Layer



6.01 μm's

Mass of Stave/modules-8.7 kg's
Structure 1.98 kg's

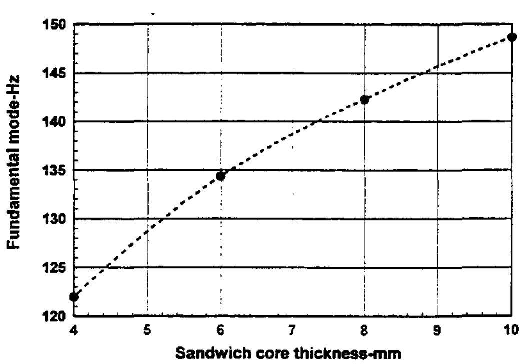
ATLAS Pixel Detector Weight Summary

Item	Number	Wt. Kg
Barrel staves	116	9.15
Barrel shells	3	1.43
Stave mounts	342	0.356
Disks	10	7.74
Interlinks-End Cones	2	0.387
SCT connection	2	0.47
Outer frame		2.66
Tubing (1/3 of mass)		4.8
Cables (1/3 of mass)		10.7
Total		37.693

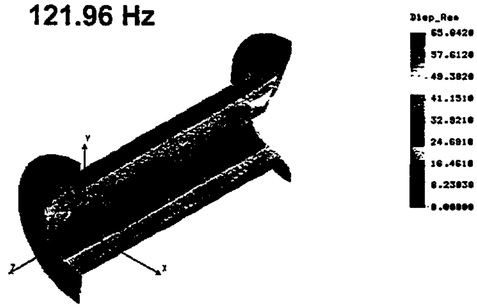
Barrel Structure Dynamic Stiffness

Stable Ultra-Lightweight Composites

Typical laminate: XN50 fiber/cyanate ester resin



121.96 Hz



End cones with 4 mm core thickness

DESIGN STATUS OF THE CMS FORWARD PIXEL DETECTOR DATA TRANSMISSION:

READOUT TO VME

Bruce A. Barnett

Department of Physics and Astronomy

Johns Hopkins University

3400 N. Charles. St.

Baltimore, Md. 21218 USA

Abstract

The CMS experiment at the CERN LHC includes a pixel system for tracking and vertexing charged particles. This system consists of two parts: the central and the forward detectors. This paper describes some features of the forward detectors related to data readout and power systems.

1 Overview

The initial design and research goals for the Compact Muon Solenoid (CMS) experiment for the Large Hadron Collider (LHC) at CERN have been specified in the CMS Technical Proposal [1]. The CMS pixel system includes a Central Pixel Detector and a Forward Pixel Detector, each having two pixel layers, as shown in Prof. Daniela Bortoletto's talk at this conference.

The four forward pixel wheels cover an annulus with inner and outer radii of 60 mm and 150 mm located on each side of the interaction region at Z $=\pm 325$ and 465 mm. They extend the solid angle to $\eta = 2.44$. Each wheel consists of 24 wedge-shaped panels called blades. A "turbine blade" configuration is used in which each blade is rotated by 20° about an axis perpendicular to the p-p beamline. This layout takes advantage of the Lorentz ($\vec{E} \times \vec{B}$) effect and the large particle incident angle to increase the charge sharing between neighboring pixels in the R and $R - \phi$ directions, respectively. Each blade is of trapezoidal shape with sensor arrays mounted on each side of a support structure. Square 150 μm pixel cells are used in both the forward and central pixel system.

A single readout chip (RO) is used in both the barrel and forward pixel system. It has a matrix of 52 columns and 53 rows of preamplifiers coupling through bump bonds to the individual pixel cells. A RO covers an area of 8mm x 10.45mm. Up to 10 RO chips connect to a single silicon pixel "plaquet". The detailed functions and drawings of the RO are described in talks at this conference by Kurt Gabathuler and Gary Grim.

2 Data transfer from RO to Portcard

The data from the RO is transfered to a "portcard", located near the outer edge of the blade. It transfers data to the outside world via an optical fiber system. The portcard is described in a talk at this conference by Bob Stone. The present design has 23 signals being transfered from the RO to the portcard: data(2), I2C bus (2), clock (2), trigger (2), reset (2), detector bias (1), guard ring current (1), monitors (3), counting token (4), and low voltage & grounds (4). The voltage levels are -2.5 V for the analogue and -5 V for the digital systems. The expected power is 40 microwatts/pixel for analogue and 10 microwatts/pixel for digital. These pixel currents translate into maximum currents from one supply of 5 amps analogue and 1 amp digital for the planned cabling scheme .

The communication between the RO and portcard will be done on multilayered Kapton cables. The limited space requires that there be a High Density Interconnect cable, or HDI, placed between the plaquets with connections to the RO using wire bonds. This cable runs in the $R - \phi$ direction, and will have three conducting layers, separated and protected by insulating layers:

1. The top conducting layer connects to the RO using wire bonds and carries the signals across

the HDI to vias connected to the third (lowest) layer. It also has conducting traces which carry the token counter signal from RO chip to RO chip expediting communication of the end of the readout of one RO and the beginning of readout from the next RO.

2. The middle layer carries the analogue and digital power input lines and their grounds. This layer will reduce cross talk between the regular signal lines. It also allows enough space for wider power and ground traces to reduce IR losses on the cable. The individual traces can be made of 0.5 oz copper and have 1.5 mm width. Vias from the top (first) to bottom (third) layer must pass through these traces.

3. The bottom layer carries the signals received through vias from the top layer out to the portcard. There is one trace on this layer for each of the signals, i.e. all of the information to and from the various RO chips are multiplexed onto this layer. For example, the 2 "data lines" or 2 "reset" lines on this layer feed to all the RO chips using the vias to the top layer. The trace widths and heights on this layer will typically be 150 and 25 microns, respectively, with 300 micron pitch.

A 90 degree bend is required in the cable to reach the port card. Two methods are now being considered to accomplish this.

1. The HDI cable could be made long enough to reach the port card where a simple fold would be made to change its direction from $R - \phi$ to radial.

2. The HDI could be wire bonded to a second, radial, 2-layer, cable, called a "pigtail".

The first method has the advantage of reduced cost and installation ease, but the disadvantages of more material and the danger of breaking traces by making the fold. Johns Hopkins University is communicating with Speedy Circuits, Huntington Beach, California regarding the technical and cost issues related to these cables.

Another issue to be determined is whether the sensor bias voltage is carried on this pigtail/HDI system or on a separate, dedicated wire. Because the pixel sensors will be adjacent to the cables it is simple to connect directly from the wire to the sensor bias lines. A coaxial wire of about 0.030 inch diameter manufactured by New England Electric Wire Corp could be used with a cost of less than a dollar per foot, not including connectors. Its radiation resistance needs to be checked. The advantage of a separate wire is that the potential 500 volts would not need to go through the portcard, and the voltage carrying capability of the HDI could be reduced. Also, procuring appropriate cable connectors is simplified. For example, the connector now used on the CDF HDI, manufactured by Berg Electrical, is rated only to 125 volts.

3 Optical Fiber Link

The CMS forward pixel project will use a fiber optics readout link to carry information between the central core of the CMS detector and the outside control systems. It will utilize the fiber optics specifications and equipment that is adopted by CMS for all of its other readout. CMS members of the RD23 research program are developing this system. A description of the data transmission from the pixels to the readout room serves to illustrate the general procedure. The optical link transmits analogue signals from the pixel transmitter hybrids to the readout room receiver hybrids. The dynamic range of the analogue signal will be 8 bits. The total path length is about 100 meters. Patch panels are included at each end to allow separability. Specifically, the forward pixel system will have patch panels about 30 cm from the portcards at the flexible interface of the support tube, another panel at the end of the service cylinder which is about 3.5 meters from the flexible interface, and then long fibers going to a patch panel near the VME crates.

A prototype analogue optical link has been developed and tested [2]. The link includes lasers, fibers and receiver PIN diodes representative of the devices intended to be used in the final system.

A version has been received by Johns Hopkins for testing and familiarization. Tests done by RD23 show that the system's pulse output shape has a bit of an overshoot, but that the pulse settles within 15 nsec to within 1% of the end value. This is within the required 25 nsec sampling period that is available at the LHC. The RD23 tests also show that the full system's relative distortion is well within the 2% linearity specified by the CMS requirements.

4 VME

The VME data collection system which the CMS Forward Pixel system uses will be as identical as possible to that of the rest of CMS. It may need some modifications to be completely compatible with the portcard system, but the intention is to keep modifications to a minimum.

5 Power Supplies

The characteristics of the power supplies for the CMS Forward Pixel system can be very similar to those used by the CDF SVX II system and by other CMS subsystems. The final vendor selection and power supply specifications will be made in conjunction with the other sections of the overall CMS collaboration.

We expect that a single cable will carry power for the chips and bias of a detector subunit. The number of sensor arrays and/or chips that will be assigned to a single supply is not yet determined. The decision on the routing will depend upon the current requirements for the final detector arrangement.

The bias power routing has been considered because we expect different sensor arrays will require different bias voltages. The biggest effect will result from the incident radiation which causes the required bias voltage to increase. The bias voltage is linearly dependent on the fluence after type inversion occurs, which in turn depends upon the distance from the beam approximately as $R^{-1.6}$. Therefore, the radiation received, and the bias voltage required, for the inner sensor arrays at 6 cm can be quite different from that for the outer sensor arrays at 15 cm. Accordingly, we believe that sensor arrays at the same radial distance could share bias voltages, and that it would be unwise to assume that all sensor arrays on a specific blade can share bias voltages. For example, when a bias voltage of 400 volts is required at 6 cm a voltage as low as 90 volts might suffice at 15 cm. Care in avoiding ground loops will be required, however, in connecting sensor arrays from different blades to one another.

We expect that a system similar to the C.A.E.N. Model 527 would be suitable. This allows many channels with positive, negative or floating voltages to be controlled from a single point. CDF uses a system like this, but the sensor bias voltage for CDF is lower than CMS will need.

6 Acknowledgments

I wish to thank my many colleagues on CMS for their essential contributions to this research program. I also wish to thank the Department of Energy and the National Science Foundation for their support of the US CMS and LHC programs.

References

[1] The Compact Muon Solenoid, Technical Proposal, CERN/LHCC 98-6, April 20, 1998.

[2] Prototype analogue optical links for the CMS tracker readout system, V. Arbet-Engels, et. al., CMS Note 1997/075,

Progress on the CMS Forward Pixels-

Mechanical and Cooling

Lucien Cremaldi,[1*] Mike Booke,[1] Bruno Gobbi,[2] Bob Tilden,[2] Paul Rubinvov,[2]
Muzzafer Atac,[3] Jay Hoffman [3]

[1] University of Mississippi, [2] Northwestern University, [3] Fermilab

* Presented at PIXEL98 – International Pixel Detector Workshop, Fermilab
May7-9 1998.

It is widely recognized that inner pixel tracking detectors can play an important role in the LHC's quest for new physics discoveries. The CMS pixel detector provides critical b-jet tagging and pattern recognition capabilities for the tracker near the busy collider interaction region. Over the past year this system has undergone significant design changes and testing of components. A brief description of recent progress in the design of the CMS forward pixel wheels is presented. More details are contained in the CMS Tracking Detector TDR [1].

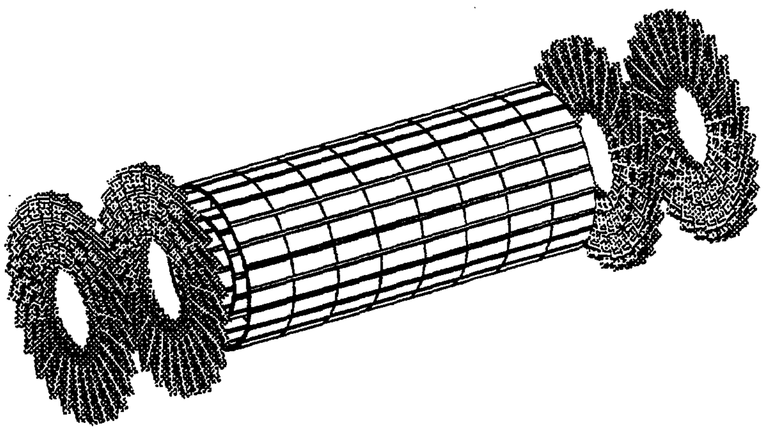


Figure 1: CMS Forward and Barrel Pixel Detectors.

Mechanical Design

The CMS forward pixel system consists of a two layer barrel and a two layer forward detector covering a range of pseudorapidity out to $|\eta| = 2.5$. The two forward pixel detectors are positioned at z=32.5 cm and z=46.5cm respectively. The radii of the wheels range from r = 6. cm to r=15. cm. The forward system is arranged in a turbine blade geometry, shown in Figures 1 and 2.

The following criteria are viewed to be of major importance in the design of the pixel system:

(1) The material budget must be minimized to a few percent of a radiation length to reduce electromagnetic showering into downstream detectors.
(2) The detector should be stable in position to an accuracy of less than±.01mm over a period of a few days, allowing slow alignment drifts to be tracked though the run.
(3) The pixel sensors must be kept at approximately T=-5degC during operation to prevent reverse annealing and the electronics must be kept uniform and stable to within ±1degC.

(4) Distortions due to changes in the operating temperature must by held to within ±.01mm over a few day period.
(5) The pixel detector must be fabricated in 2 halves to be inserted around the beam pipe after a beam pipe bakeout period.

Each of the four forward detector disks consists of 24 wedge-shaped blades (12 per half-wheel) which hold the pixel sensors and electronics. A cooling channel services four to six blades in series. Each blade assembly is rotated at 20 degrees to enhance charge sharing, forming the turbine-blade geometry.

Points of interest shown in Figure 2 are :
(1) That the cooling tubes form a structural part of the half-wheel assembly, thus reducing total material.
(2) The tubes are attached to an inner and outer carbon-fiber ring to complete this structure.
(3) Internal alignment of the system with tracks is made easier by a small blade-to-blade overlap as well as a front-to-back sensor overlap.

The detectors must be installed from points along the beam at z= 3m after a bakeout of the beam pipe. To aid in this installation the half disks are installed in a space cylinder, shown in Figure 3, which is attached to a permanent service cylinder. Between space and service cylinders all electrical, optical, and service connections are made. These low mass carbon fiber space and service cylinders are moved into place on a system of rails which are attached to the inner layer of the silicon strip detector (not shown). The service cylinder will also provide a buffer area for commissioning the pixels during early installation procedures.

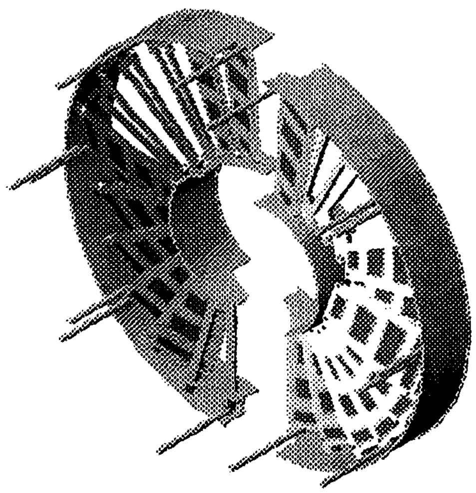


Figure 2: View of detector blades mounted in half-wheel configuration with cooling pipes.

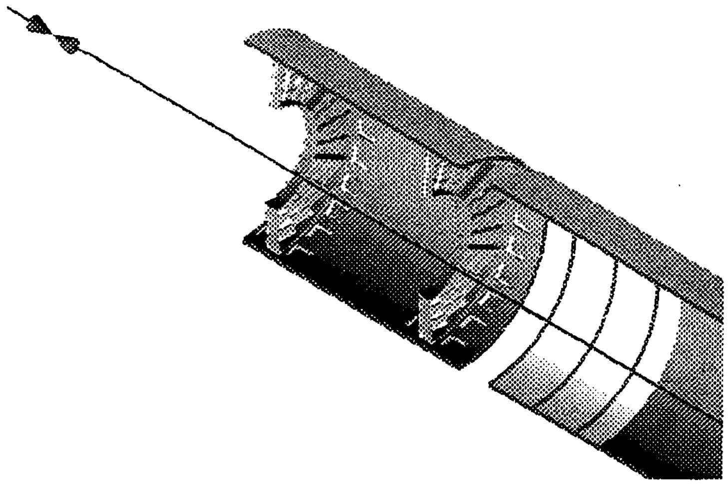


Figure 3: Forward pixel half-wheels are shown mounted onto its space cylinder. A portion of the following service cylinder is also shown.

Each blade is constructed from two low mass c-c carbon panels [2] mounted to an Al (0.2mm wall) cooling tube which runs directly under and at the edge of the electronic readout/sensor arrays. The c-c panels are aligned with respect to the cooling pipe by an alignment frame directly attached to the cooling pipe. An exploded view of the blade assembly is shown in Figure 4.

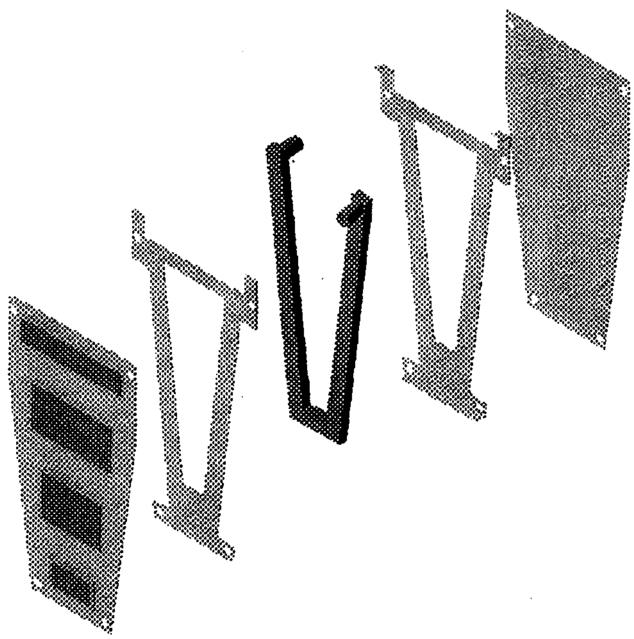


Figure 4: Exploded view of forward pixel blade, with cooling pipe and alignment frame.

Pressure Drop Measurements

Of special concern is the pressure drop in the U-tube sections of the detector blade assemblies. For safety reasons we want to maintain a pressure drop of <500mbar across the interior detector. A series of pressure drop measurements have been completed with water flowing at 20deg C. In these tests an open air and digital manometer apparatus was used to measure the pressure drop in a series of U-tubes similar in design and cross section to those proposed for the blade.

For calibration purposes straight tubes of various cross sections were tested and pressure drops compared to the Darcy equation $\Delta P = f\,(L/D)\,\rho v^2/2$ where P(pa) is pressure, L(m) is tube length, D(m) is tube diameter, ρ(g/cm^3) is the density, and v(m/s) is mean fluid velocity. The friction factor is f=64/Re for laminar flow (Re < 2600) and can be parameterized in the turbulent zone. In Figure 5 we show the pressure measurements for a number of straight tube cross sections of length L=30in. The onset of turbulent flow is at approximately (8-10)cc/s for this liquid.

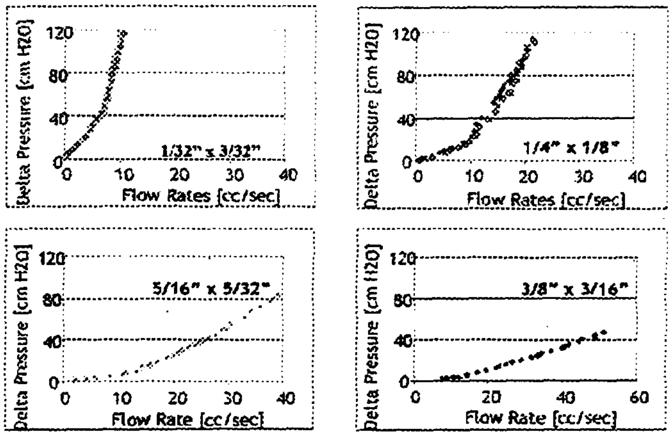


Figure 5: Pressure Measurements of straight tube section s of indicated cross sections.

The present design calls for a series connections of 4 to 6 U-tubes. Additional friction factors accounting for the pipe bends have been studied. These results are presented in Figure 6. A coolant like HFE-7100 at –15deg C has a viscosity similar to that of water at (20deg C) and 60% higher density. Thus the 6-U-tube result shown below and measured with water implies that the pressure drop across a 6-U tube configuration will be somewhat less than 200 mbar for flows of (5-10)cc/s.

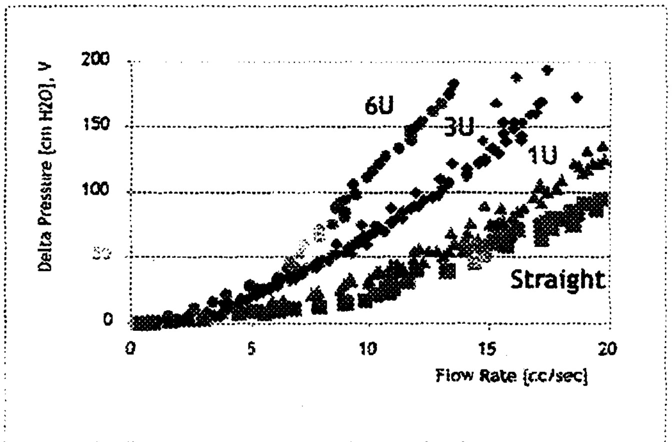


Figure 6: Pressure drop measurements in a 1/4"x1/8" U-tube of length 200mm for the indicated configurations.

Pixel Detector Cooling

Current estimates for the forward detector heat load including electronics are based on 66μW per channel for readout electronics and sensor. With 2756 pixels per chip and 45 chips per blade, each blade will heat to 8.2W. Adding an additional 50% for laser drivers, control chips, cables, and heating from IR losses in the service tubes, we estimate 1.2 kW of total power for the 4 disks.

The power load on the cooling tubes is expected to be 40mW/cm at the cooling pipe. We project that the sensor temperature must be maintained at T~ -5deg C to minimize reverse annealing biases. To cope with expected temperature differences due to thermal resistance and limited heat transfer a coolant inlet temperature of T~ -15deg C is required. Since the coolant must be supplied through long tubes with the smallest possible cross section, a liquid having a low viscosity at this temperature is most suitable. For safety reasons it is desirable that the coolant be electrically isolating, non-flammable, and non-toxic. A non-flammable and medium radiation length fluid from 3M, hydroflouroether HFE-7100 from 3M [3], is now under consideration.

HFE-7100 ($C_4F_9OCH_{10}$) is a clear, colorless, and low-odor fluid intended to replace ozone-depleting materials. It's chemical and thermal stability (Boiling Pt.= 61degC, Freezing Pt.=-153deg C) and non-flammability make it extremely useful for heat transfer applications. Materials compatibility tests performed by 3M have shown it to be safe to use with Al, low carbon steel, and titanium tubing, and many plastics and rubbers.

HFE-7100 has relatively poor thermal conductivity and near turbulent flow conditions may be necessary to effect proper cooling. In Table 1 we give material properties, flow, and pressure drop parameters for a system capable of removing 8W of power from a pixel blade. Ethanol(35%)/Water coolant is included for comparisom. Development of potentially lower mass evaporative fluorocarbon cooling techniques is also being pursued with fluids such as C_4F_{10} [4].

ρ(kg/m^3)	Cp(J/KgK)	K(W/mK)	μ(mPas)	Xo(cm)	dm/dt(g/s)	Re	ΔP(mbar)
(a) 1682	1096	.077	1.15	23.	8.8	2693	15
(b) 963	4045	~.55	30	34.	2.4	28	98

Table 1: Properties of (a) HFE-7100 coolant (b) Ethanol(35%)/Water at T=-20degC. The pressure drop and flow rate are also given for removing 8W of power through a L=220mm and σ =10mm^2 U-tube.

Selection of low mass and radiation resistant materials forming a low resistance heat path to the cooling channel is of utmost concern. The thermal resistance/temperature drops along the cooling path must be carefully studied as not to impede the heat flow. We mentioned previously that the pixel electronics will be bonded to a .3mm c-c panel[1]. This material has an in-plane thermal conductivity K_{ab}= 200 W/m-K and through-plane conductivity K_c= 30 W/m-K. These c-c panels have been shown to work well in conducting heat to the cooling tubes. A small temperature drop of < 3deg C is observed from center to edge of the electronics mounted on the c-c panel with a few tenths deg C drop through the c-c panel. The panel is greased to a .3mm thick c-fiber alignment frame, which is glued to the cooling tube. Measurements and calculations confirm about a 0.5deg C temperature drop through this structure from panel-to-pipe, although care must be taken at this junction. There is an additional 3 to 4deg C drop from pipe-to-bulk fluid (depending on cooling fluid), giving a total ΔT ~ 8deg C. A fluid circulating at bulk temperature T(bulk)=-15deg C is projected to keep the pixel electronics at approximately T(electronics)~ –7deg C. The projected temperature drops based on ANSYS simulations and conductivity measurements are shown in Figure 7.

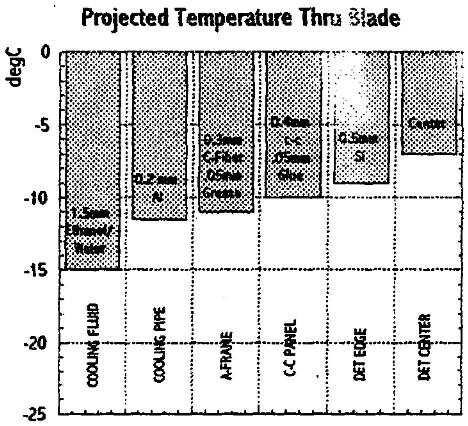


Figure 7: Projected temperature profile through a blade.

Cooling Tests

Thermal tests have been performed on prototype blades fabricated with c-c panels. Ethanol(35%) /water was used as coolant. The top and bottom panels are greased to a σ =7.6 mm^2 by L= 180mm cooling tube running along the edge. Coolant is supplied at -15degC. An 8W heat load is applied by an array of thermofoil heaters [5] carefully placed to mimic the pixel electronics. RTDs[6] measured the temperature profile on the simulated electronic packages. A schematic of this system is shown in Figure 8.

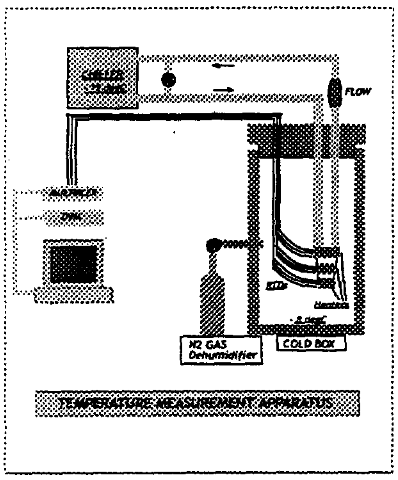


Figure 8: Schematic of apparatus used in the cooling tests.

The heat transfer mechanism is dominated by conduction to the cooling pipe, with small radiative and air-convective components. To minimize these effects the prototype wedges are tested in a dry-nitrogen filled cold-box nominally held at the surface temperature of the electronics (-7degC), also Figure 8. The inlet-to-outlet bulk fluid temperature increase for a single blade is measured to be ΔT(blade)=~1.5degC, collant flowing at 4.5cc/s. The mean electronics temperature on the blade is -5.8degC in this test. A typical temperature profile of the temperatures at the sensors is displayed in Figure 9.

Substrate thickness, glues, and greases are being optimized for thermal effectiveness, radiation survivability, and material budget. But already these tests have shown that adequate pixel cooling is feasible with this design.

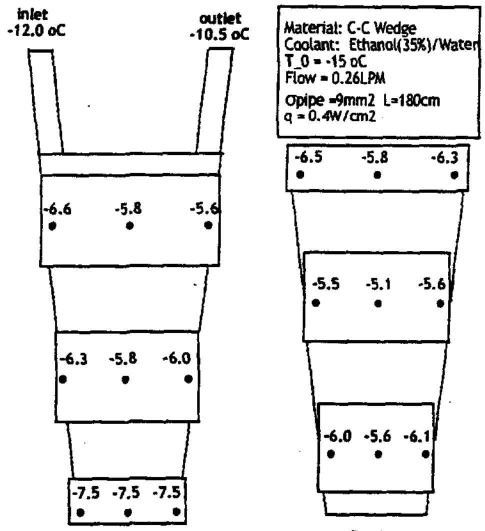


Figure 9: Measured temperature profile on a prototype c-c blade.

Refrigeration System

A system of refrigerators and circulating elements is being designed to provide cooling and dissipate the heat loads generated in the pixel, silicon, and MSGC tracker volumes for the CMS detector. Cooling supply lines for the forward pixels will enter near the beam pipe at a z = ±3m after long run from a central refrigerator complex. These supply lines must be compact and insulated insuring a small temperature drop from refrigerator to pixel enclosure. The bulk fluid temperature should be about T_b=-15degC. Supply and cooling pipe diameters are chosen to keep pressures below 1 bar at all points in the system. The circulation system should be designed with appropriate sterilization, particulate filters, de-ionizers, inspection stations, and sample ports as seen necessary. Evaporation tanks, air separators, spill tanks, etc. should be designed into the system. Of special concern will be the capability of this system to abort power to the pixel electronics or be fail-safe in case of emergency. Preliminary measurements have shown that the system has cooling latency sufficient to keep the sensors below room temperature for several minutes after coolant flow has stopped, giving ample time to abort power. We have calculated the total pressure drop in a conceptual refrigeration system flowing HFE-7100 to be approximately 650mbar across the inner pixel detector U-tubes + pixel detector service tube + 15m inlet and outlet service lines. We are presently working on the engineering design of a full test facility to verify these results.

Radiation Damage Measurements

We have begun to investigate a small sample of glues and epoxies for radiation damage properties. Our purpose is to find a low to medium viscosity, room temperature curing epoxy which we can use to bind silicon chips to the c-c panels. We believe a [illegible] µm thick layer is more than adequate for bonding, exhibiting little thermal resistance. The bond should retain over 75% of its strength after irradiation with Co^{60} gammas. In these investigations samples of silicon are bonded to c-c material and standard shear tests are performed before and after irradiation of 10^7rad. Presently we are testing EPON [7] epoxies with TETA hardeners.

We show the result of some of our first tests (Figure 10), in which multiple samples of carbon/Si/carbon assemblies are bonded with epoxy mixes of different viscosity. The samples are pull-tested before and after irradiation, measuring the breaking shear force in pounds per sq. in. (psi). Our first tests have shown that upon radiation the samples have retained practically full strength and would be acceptable. Further testing under gamma, charged particle, and n radiation is envisioned.

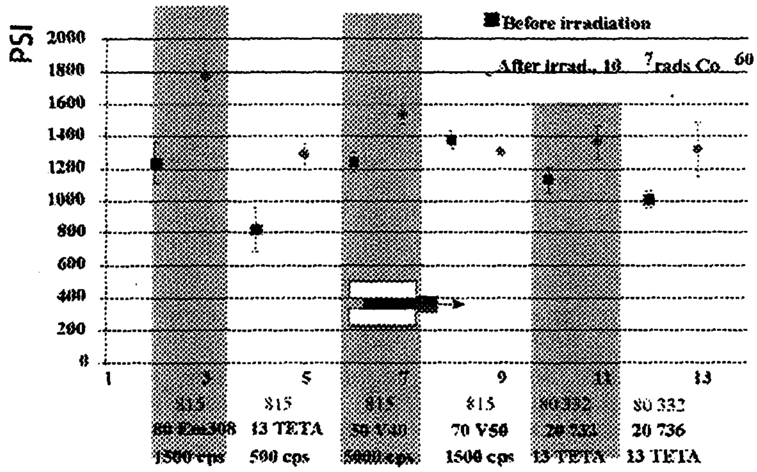


Figure 10: Shear test results for carbon/Si bonds with EPON epoxies.

Conclusion

Significant progress has been made in the mechanical design and testing of components for the CMS barrel and forward pixel detectors. Future work is focused on the optimization and final selection of materials, as well as complete engineering designs.

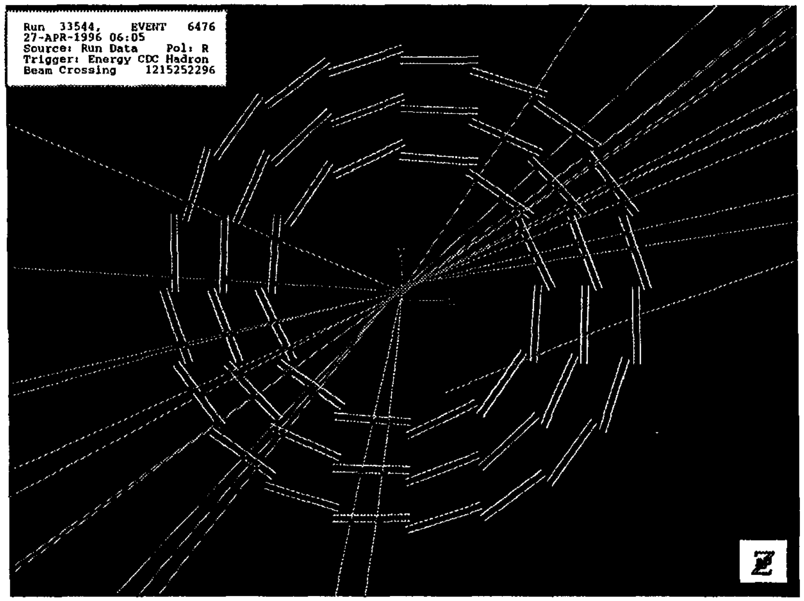
REFERENCES

[1] CMS Tracking Detector TDR, the CMS Collaboration.
[2] B.F.Goodrich Aerospace, Santa Fe Springs, CA.
[3] 3M Performance Chemicals, Minneapolis, MN.
[4] see talk by Greg Hallewell at this conference.
[5] MINCO Products Inc., Minneapolis MN.
[6] Omega Engineering Inc., Stamford CT.
[7] EPON, a registered trademark of the Shell Oil Company.

Experience with the SLD Vertex Detector

or

300 Million Pixels Can't Be Wrong



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Glen Crawford, SLAC

Pixel 98 / Fermilab

- Detector Cooling/Mounting/Alignment
- Data Flow

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NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH

Section A

Nuclear Instruments and Methods in Physics Research A 400 (1997) 287-343

Design and performance of the SLD vertex detector: a 307 Mpixel tracking system[1]

K. Abe[a], A. Arodzero[b], C. Baltay[c], J.E. Brau[b], M. Breidenbach[d], P.N. Burrows[e], A.S. Chou[d], G. Crawford[d], C.J.S. Damerell[f,*], P.J. Dervan[g], D.N. Dong[e], W. Emmet[c], R.L. English[f], E. Etzion[g], , M. Foss[d,] R. Frey[b], G. Haller[d], K. Hasuko[a], S.S. Hertzbach[h], J. Hoeflich[d], M.E. Huffer[d], D.J. Jackson[f], J.A. Jaros[d], J. Kelsey[e], I. Lee[e], V. Lia[e], A.L. Lintern[f], M.X. Liu[c], S.L. Manly[c], H. Masuda[d], A.K. McKemey[g], T.B. Moore[c], A. Nichols[f], T. Nagamine[a], N. Oishi[i], L.S. Osborne[e], J.J. Russell[d], D. Ross[e], V.V. Serbo[j], N.B. Sinev[b], J. Sinnott[c], K. Skarpaas VIII[d], M.B. Smy[k], J.A. Snyder[c], M.G. Strauss[h], Su Dong[d], F. Suekane[a], F.E. Taylor[e], A.I. Trandafir[h], T. Usher[d], R. Verdier[e], S.J. Watts[g], E.R. Weiss[l], J. Yashima[a], H. Yuta[a], G. Zapalac[j]

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VXD3 Milestones

- **Mar 94** VXD3 project approval.
- **Oct 94** Detailed design report completed.
- **Feb 95** First prototype CCDs arrive at SLAC.
- **Apr 95** CCD production phase begins.
- **Sep 95** First production devices shipped.
- **Dec 95** Delivery of production CCDs complete.

  VXD3 assembly and survey completed.

  VXD3 arrives at SLAC.

  Electronics and cryostat assembly in clean room.
- **Jan 96** Completed assembly mounted in SLD.
- **Feb/Mar 96** Extensive testing/debugging.
- **Apr 96** First VXD3 data logged.
- **Jul 96** End of commissioning run.
- **Aug 96** Detailed detector alignment begins.
- **Jun 97** Initial detector alignment complete.
- **Jul 97** Long datataking run begins...

Detector Cooling

Requirements

- **Maintain detector at operating T (185 ± 1 K)**
  Operating T set by minimizing in rad. damage
  Range set by need for alignment stability
- **Small heat load from detector ($\sim$ 20W)**
  → *no need for conductive cooling of detector substrate*
  Small heat loss from cryostat ($\sim$ 20W)
- **Low humidity to avoid condensation**

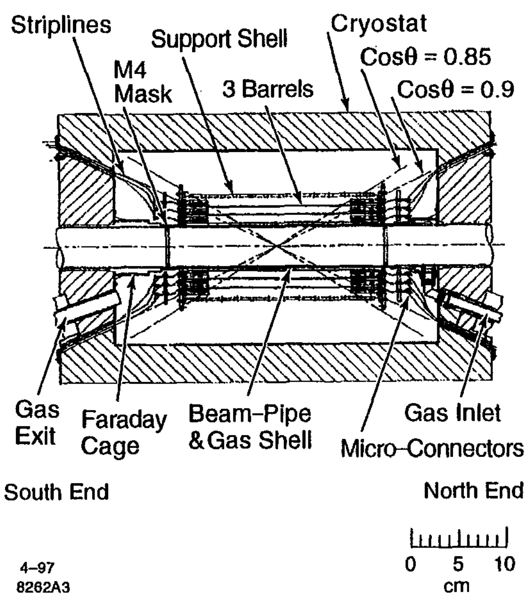
Solution: Boil-off LN_2

- Fed from dewar at 1gm/sec to 2-stage boiler
  Exit @ 135K to long ($\sim$ 15m) stainless vacuum lines
  → *most of heat loss is in cold gas transfer ($\sim$ 200W)*
- N_2 gas pressurizes small cylinder btwn beam-pipe + gas-shell:
  → *slow, radial gas flow over vertex detector*
- Outflow via similar (larger radius) vacuum lines, vent
  → *measure flow rate, pressure, moisture*

Cooling Details

Operating Parameters

- **Total temp. gradient in cryostat:** ~ 30 C
- **Total temp. gradient in detector:** ~ 15 C
- **Pressure in cryostat:** ~ 1.7 mbar
- **Moisture in cryostat:** ~ 2 ppm H_2O
- N_2 **flow rate:** ~ 60 liters/min



Cryostat

Basically a zero-mass, zero-strength foam cooler

- **Polyisocyanurate foam with filler gas**
  Denser foam in endcaps; lighter in barrel
  Also in last $\sim$ 1m of inlet gas pipe (in tracking solid angle)
  $\rightarrow$*inlet strengthened with carbon fiber sleeve*

- **Built in 6 sections (2 half-cylinders, 4 half-endplates)**
  Sealed with low-temp. silicone adhesive [NuSil]
  Penetrations for beam-pipe, stripline connectors
  Heater wire at joints to prevent condensation

- **Largest heat leak: beam-pipe**
  More heater wire to maintain beam-pipe $T > 15$ C

- Also a Faraday cage to shield detector from RF, elect. pickup

Mechanical Design Overview

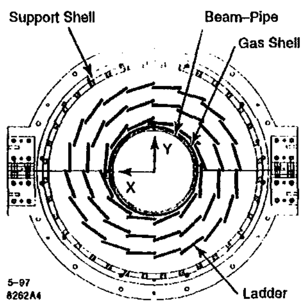
Design goals: low mass, stable, repeatable assembly

- **CCDs mounted on Be substrates**
  Substrates attached to annuli w/spring-retention blocks
  Annuli attached to cylindrical Be support structure

[Be chosen over C Fiber, Al for better isotropy, CTE match]

- **Assembly and survey done layer-by-layer**
  Several special jigs to ensure repeatability
  All components held + overconstrained by dowel pins
  All adjacent components match drilled and reamed
  All mating surfaces lapped flat and specially cleaned
  Final installation in half-shells around beam-pipe

- **Outer Be support shell a "mesh" for survey, gas flow**



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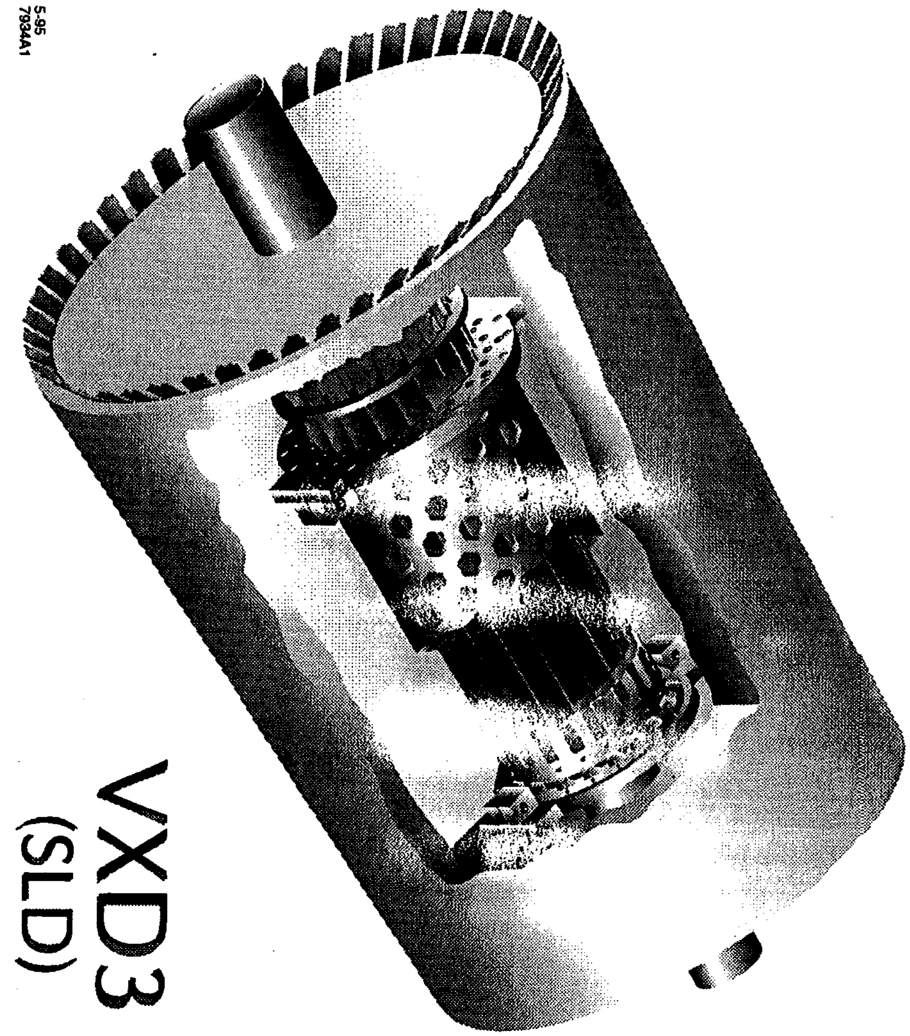
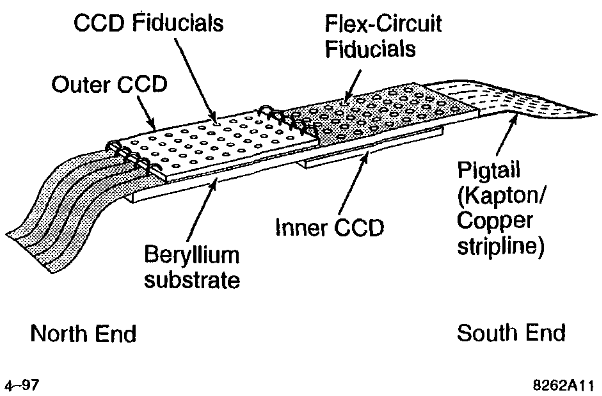


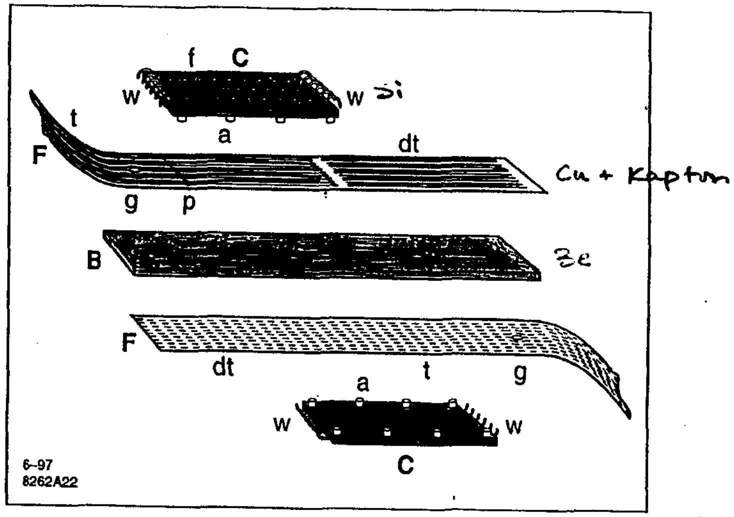
CCD Motherboards

Most challenging component to design (most constrained)

- **Solution: Thin Be beam (380 μm)** [BeO too fragile]
  + 2 Copper/Kapton flex circuits
  (13 μm Kapton, 18 μm Cu + coverlayer)
  + "pigtails" to μconnectors
- Bonded with acrylic adhesive at $T \sim 180$C
  Tested for de-lamination
- CCDs attached with adhesive pads and wire-bonded



The CCD Sandwich

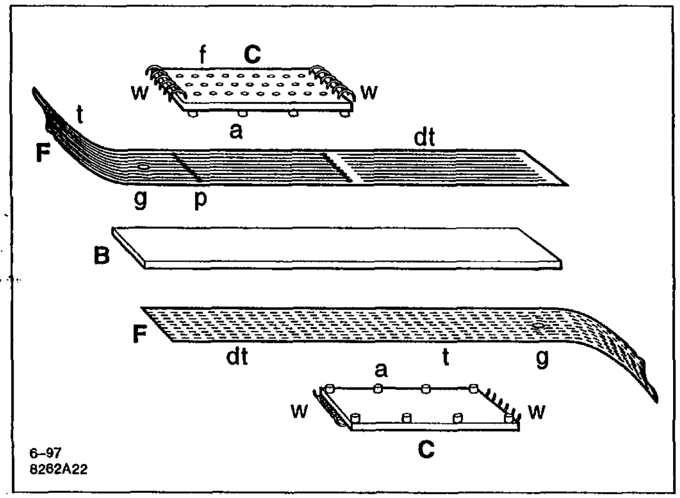


- Put 2 CCDs on a thin (15 mil) Be beam .11% RL (Be
  + .16% (CCD
- + Kapton flex circuits + .05%
- + Cu traces + Au bond pads + wire bonds + .09%
- + Adhesives (incl)

Σ = 0.40% RL

⇒ cf 1.15% RL VXD2

The CCD Sandwich



- Put 2 CCDs on a thin (15 mil) Be beam
- + Kapton flex circuits
- + Cu traces + Au bond pads + wire bonds
- + Adhesives

Thermal Issues

Goal: Balance structure as much as possible

Problem: CTE for Be: 9×10^{-6}
CTE for Si: 2×10^{-6}
CTE for Cu/Ka: 23×10^{-6}

Sol'n (I): "Dummy" traces on flex project thru opp. side

- ...but CCDs still not thermally matched

Sol'n (II): Thick (200μm) adhesive pillars take up CTE mismatch

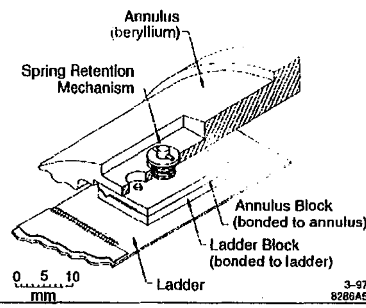
- even so...unsupported ladders [illegible] 100μm on cooldown

Sol'n (III): Clamp ladders to support structure w/blocks

$< 1\mu m$ flex when cooled

- ...but there are still local temp. gradients!

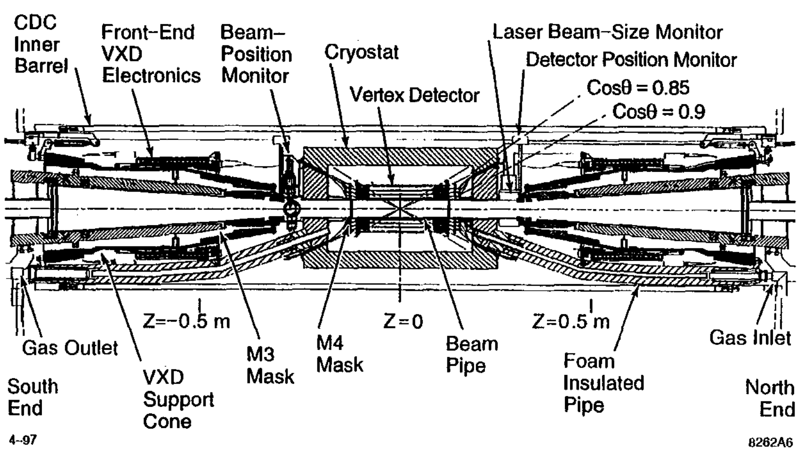
Sol'n (IV): Allow 1 dof (longitudinal) to take up differences



Mounting in SLD

Goal: Decouple vertex detector from machine

- Detector mounted off central beam pipe via 3pt. kin. mount
  Central beam pipe suspended from drift chamber
  3pt clamps w/adjustable jacks allow transverse adjustment
  → can tune VXD bkgds *in situ*
- Rest of beam pipe inside SLD "floats" between bellows
- Synch. rad. masks and outer beam pipe hung from FF quads



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Data Flow

Goal: Readout 300MB at up to 2Hz, reduce to < 100kB

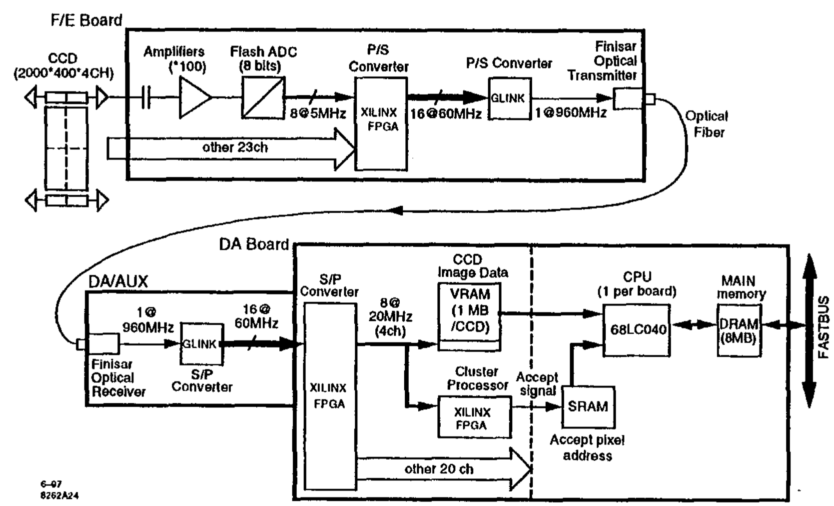
- **Solution: Digitize at front-end, sparsify at back-end**

  960 Mbit/sec raw data per frontend board (× 16 boards)

  Transmit 1.2 Gbit/sec/board via optical fiber + Glink

  Hardware cluster edge-finding + filtering

  1 CPU/back-end (Motorola 68040 @ 66MHz)



Data Acquisition Issues

Data Reduction

- **Cluster Processor (CP):**

  Form 2 × 2 pixel filtered kernel
  If above threshold, look for trailing edge
  Once trailing edge is found, tag cluster, pass to CPU
  Implemented via Xilinx FPGAs

Resource Allocation

- **Prioritize tasks:**
  1. Examine accepts from CP, save ROIs into memory
  2. Select pixels over threshold from ROI
  3. Assemble packets (26/event) into full event
  4. Sort by channel and CCD address, eliminate duplicates

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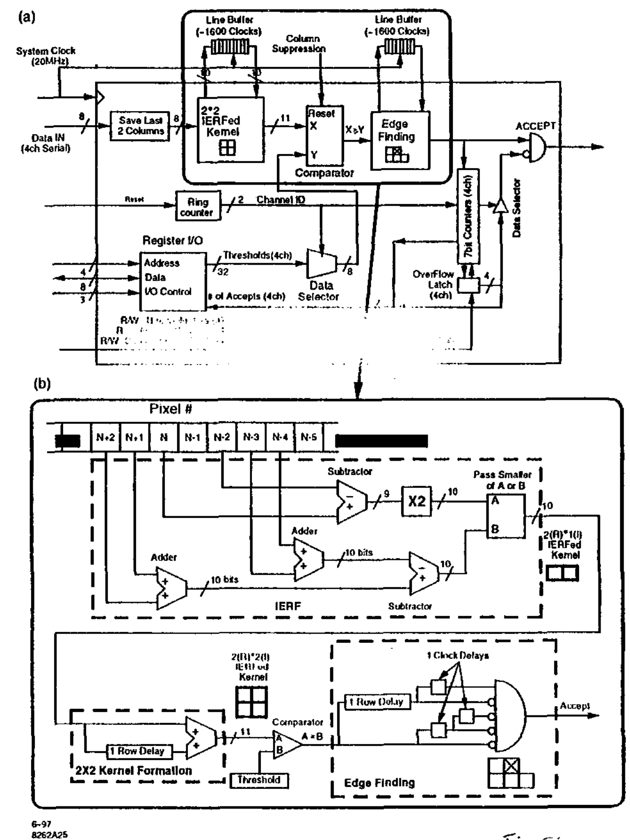
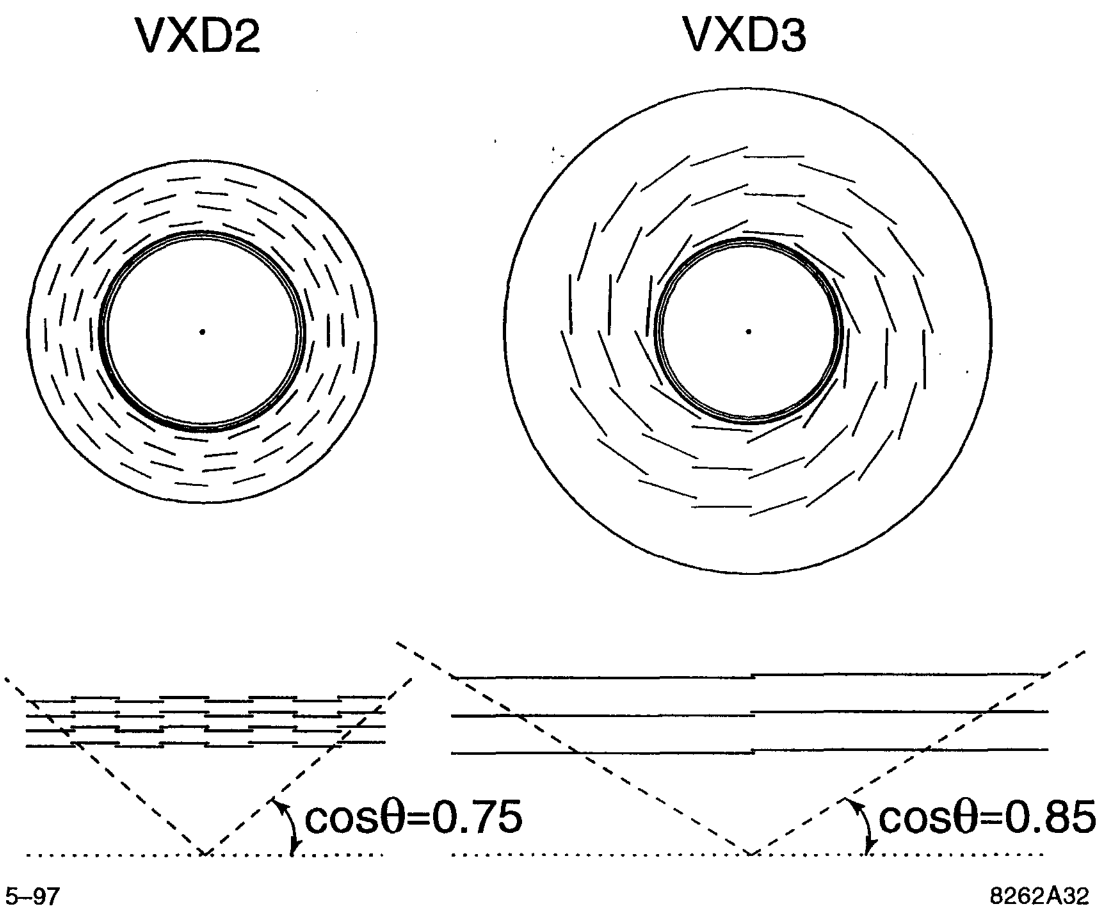
Subtleties

- **Very limited memory up front**

  Can store only $\sim \frac{1}{4}$ CCD full raw data
  Cannot handle worst-case scenario
  Data overrun cannot be prevented (only detected!)
  Events can overlap and share packets (i.e., pixels)



• **Final internal alignment from tracks in all events**



• **Internal**

"Shin

Lin

Derive "intrinsic resolution" from these comb.'s

"Doub

Li

h

"Tripl

Lin

@

Optical Survey Goals

MIT Group

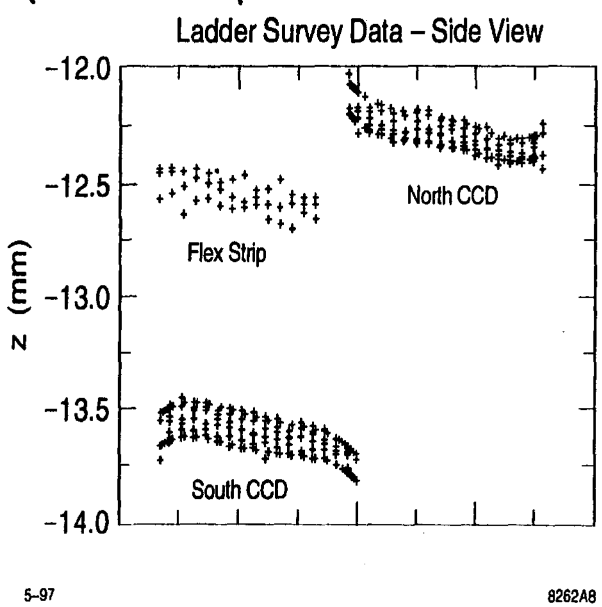
- **Align detector well enough for track-based alignment**

  Need $\sim 20\mu m$ precision overall

- **Determine complex geometric shapes**

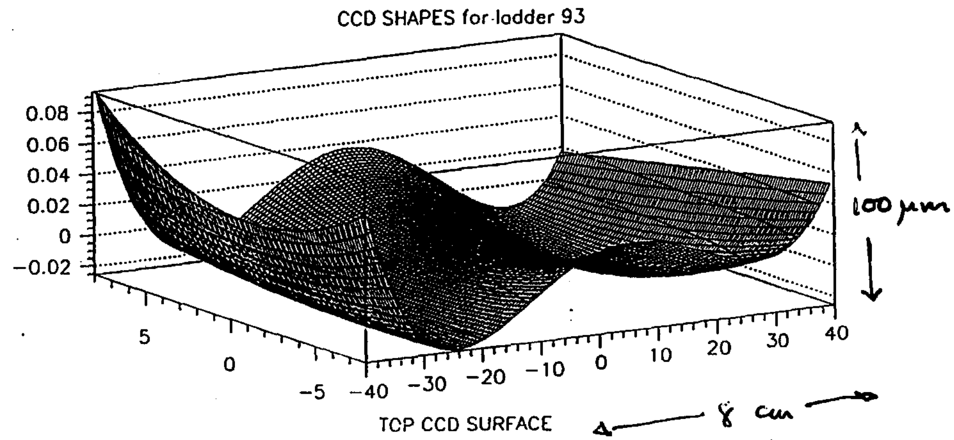
  CCD shapes, gravity sag

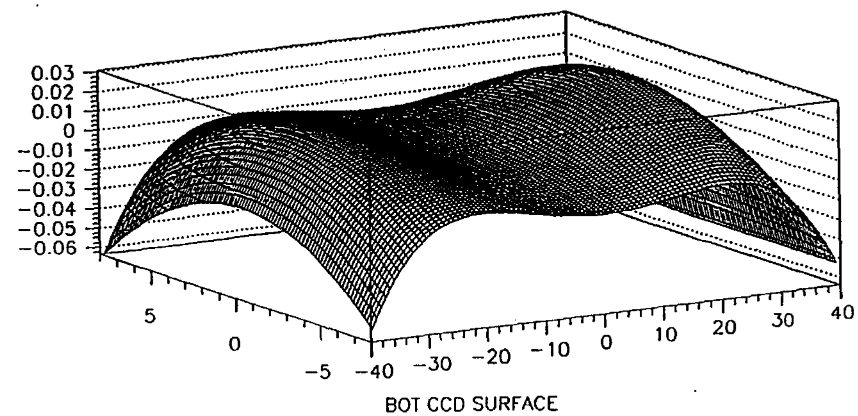
Optical Survey Data:



Fits to CCD Shapes

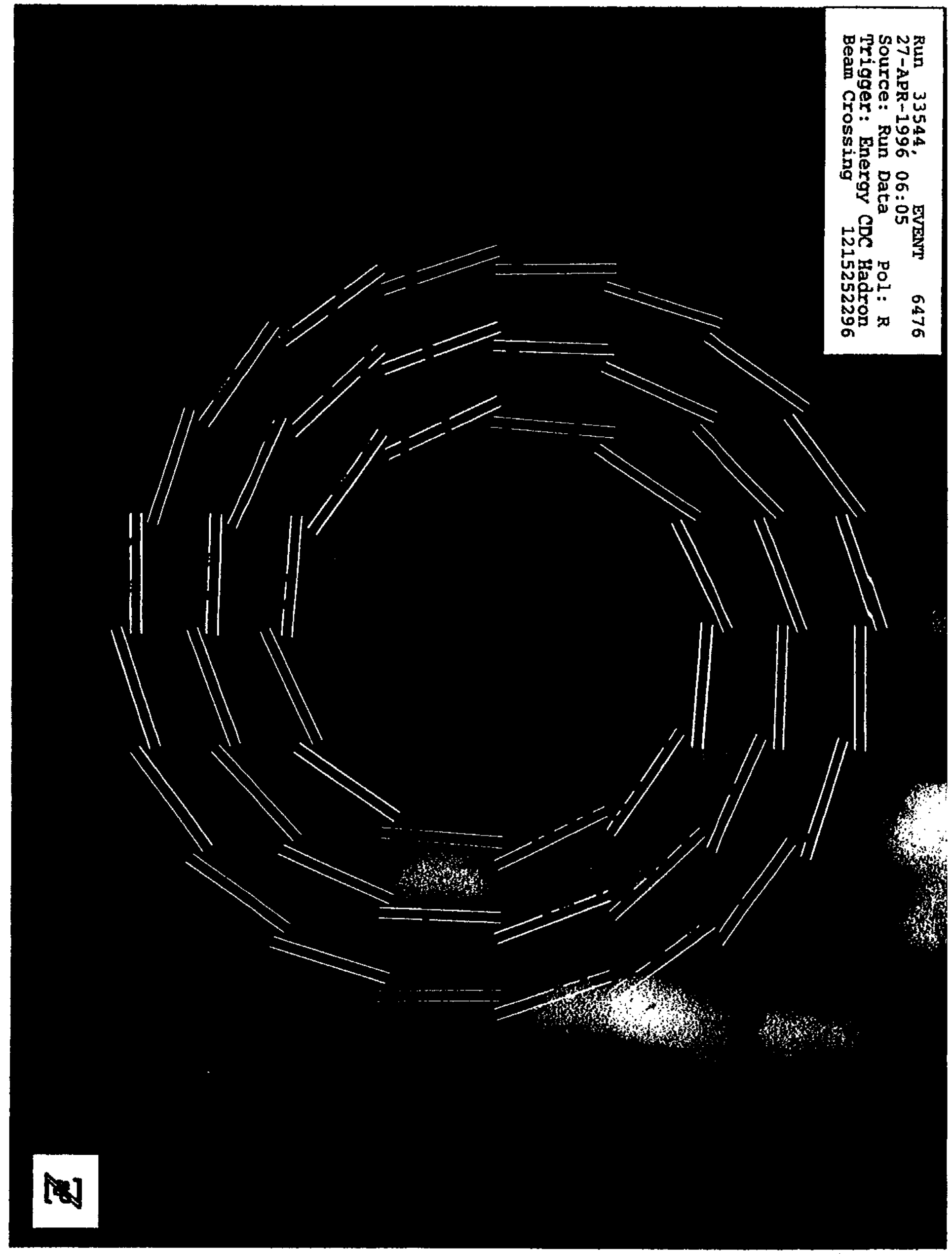
all dimensions in mm. note scale differences

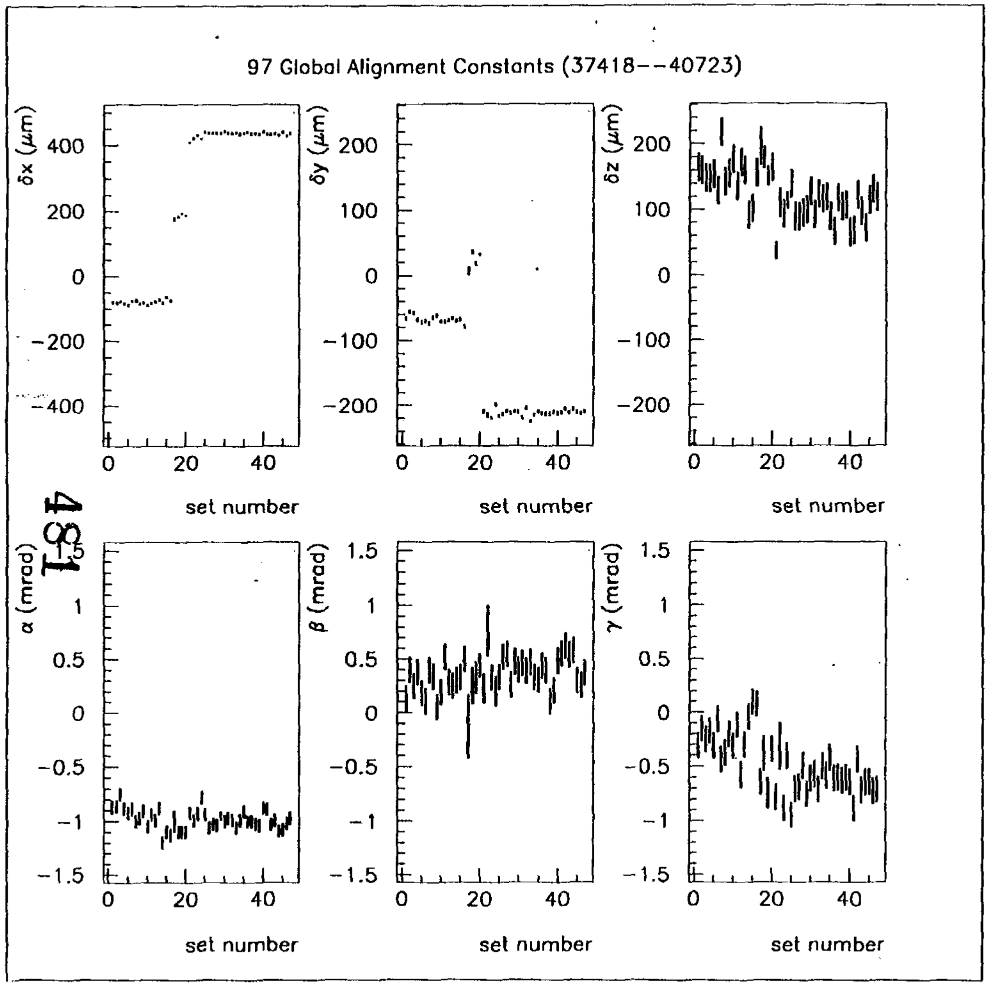




Optical Survey Results

- **Gravity sag:** up to 30μm correction/CCD
- **CCD shapes:** up to 50μm correction/CCD
- **Thermal corr'ns:** $\sim$ 50μm relative (Be/Si)
- **Precision:** 17μm $r\phi$. 14μm z
- **Systematics:** 20-30μm assembly repeatablility





Detailed Alignment

D. Jackson et.al

- **Goal**: Determine location and orientation of all 96 CCDs:

  (3 translations + 3 rotations) $\times$ 96 = 576 parameters

  Need $\sim 5\mu$m precision (!)

- **Track-based alignment**: Determine local geom. w/ VXD alone

  Use track residual fits from vertex multiplets.

  Use MC + ideal geometry to determine CCD weights.

  Solve multiple coupled equations with matrices:

$$\underbrace{\begin{bmatrix} w_{ij} & \cdots & \\ \vdots & & \\ & & \end{bmatrix}}_{\text{"Weight Matrix"}} \underbrace{\begin{pmatrix} \delta x_i \\ \vdots \\ \delta\alpha_i \\ \vdots \end{pmatrix}}_{\text{CCD displacements}} = \underbrace{\begin{pmatrix} c_j \\ \vdots \\ \vdots \end{pmatrix}}_{\text{Residual Fit coeff.s}}$$

- Invert W and solve for $(\delta x_i, \ldots, \delta\alpha_i, \ldots)$

  (576 x 1520) matrix inversion! Fortunately most $w_{ij} = 0$

  Need to account for correlations in data, linear approximations,...

- **Add more information**:

  $Z^0 \to l^+l^-$ data

  VXD3/drift chamber matching redux

Intrinsic Resolution

- Spatial resolution derived from hadronic event track residuals
- Intrinsic CCD resolution $\sim$ doublet, triplet resolution
- Single-hit spatial resolution follows from geometry

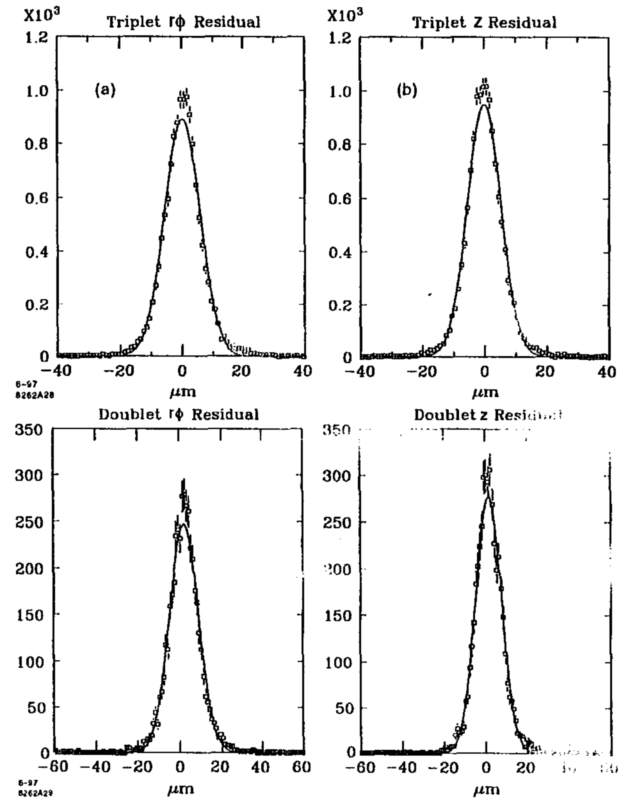
- **Results:**

$$\begin{aligned}
\text{Doublet } r\phi &= 6.0\mu m/\sqrt{2} = 4.3\mu m \\
\text{Doublet } rz &= 6.3\mu m/\sqrt{2} = 4.4\mu m \\
\text{Triplet } r\phi &= 5.0\mu m/\sqrt{1.5} = 4.1\mu m \\
\text{Triplet } rz &= 5.3\mu m/\sqrt{1.5} = 4.3\mu m
\end{aligned}$$

482

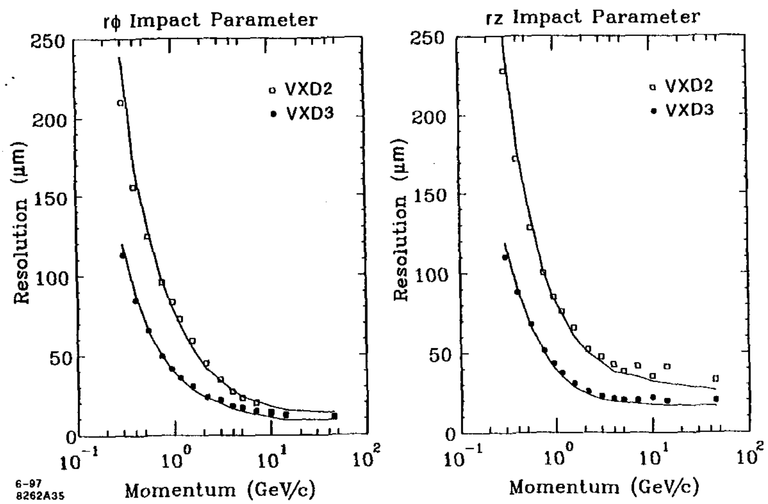
- **Significantly better than VXD2** ($\sim 5.5\mu$m)
- Unlikely to improve much (some small gains from final alignment)

Doublet and Triplet Residuals



Impact Parameter Resolution, cont'd

- Low $\overline{p}$ end from track imp. params wrt beam: → *beam positions.*
- Dominated by multiple scattering and lever-arm
- Roughly 2X improvement seen.



Lessons Learned

- **Screening devices very important (20% failed)...QC!**
- **BeO ladders fragile, substrates crack, traces irregular**
- **Many delicate assembly connections...avoid Au flash!**
- **EM pickup into frontend electronics**
- **Optical survey *very* useful**
- **Alignment will take longer than you think**

Dense Optical Interface Module for CDF – Design, Implementation, and Prototype Performance

M.L. Chu,[a] Y.C. Liu,[a] P.K. Teng,[a] M.T. Cheng,[b] M. Chertok[c]

[a] Institute of Physics, Academia Sinica, Taiwan
[b] Fermi National Accelerator Laboratory, Batavia, Illinois
[c] Texas A&M University

Abstract

The Dense Optical Interface Modules are general high speed communication links designed for the readout system of the CDF Upgrade Silicon Vertex Detector (SVXII). A 9-channel link consists of a transmitter (TX) module which converts electrical differential input signals to optical outputs, an intermediate multi-mode optical fiber ribbon cable, and a receiver (RX) module which senses the light inputs and converts them back to electrical signals. The targeted operational speed is 53 MHz, and higher rates can be achieved. The packaged TX and RX modules have embedded custom-designed laser diode arrays and photo diode arrays, as well as driver and receiver integrated circuits. These compact modules provide a good solution to data readout and interconnection problems common in future collider experiments. This article outlines the design goals, implementation methods, and prototype test results of these modules.

1 Introduction

High speed data readout modules and transmission links are crucial components for modern particle detectors. These devices normally have to be compact, low-mass, and capable of transmitting data at high speed without too much attenuation or error occurences. They also have to introduce very low electromagnetic interference (EMI) and be able to endure reasonable amount of irradiation after long periods of data-taking runs. Considering all the above factors, there are few commercially available products that meet most of the requirements for particle experiments.

The Dense Optical Interface Modules (DOIM) [1], [2], are custom-designed for the readout system of the CDF Upgrade Silicon Vertex Detector (SVXII). It is a cost-effective solution to the data readout tasks that meets most of the above stringent requirements.

As shown in the layout diagram in figure 1, a full DOIM communication link includes three parts - the transmitter (TX) module, the intermediate optical fiber

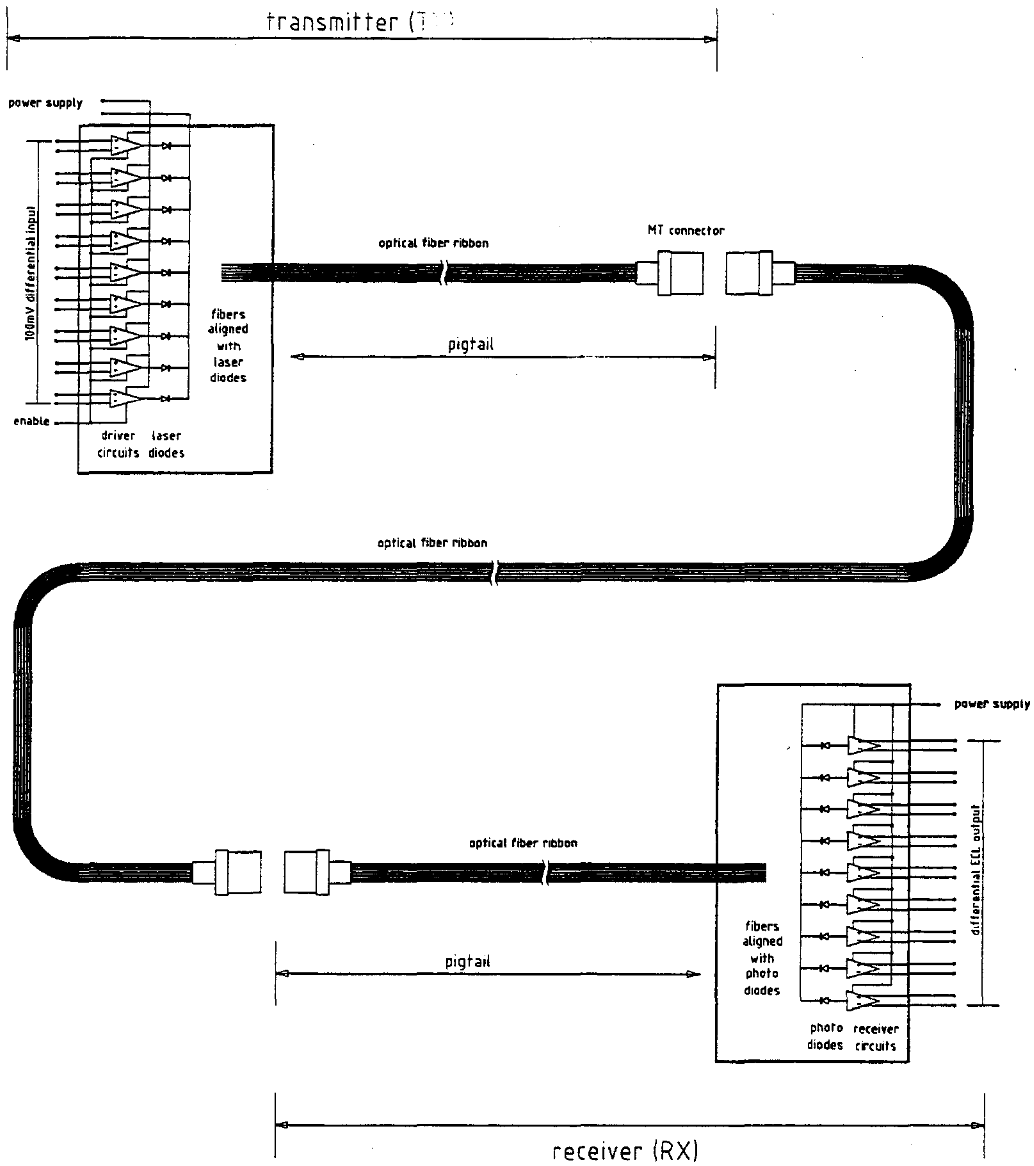


Figure 1: Layout of a DOIM data link.

ribbon cable, and the receiver (RX) module. It will take totally 360 such links to read out the whole SVXII detector.

The TX module encapsulates the driver integrated circuit which conditions the input differential electrical signals [3], and the 9 channel laser diode array which converts the signals to light outputs to be sent out via the optical fiber ribbon.

Between the transmitting and receiving ends, we use 9-channel commercial multi-

Table 1: Transmitter Module Design Parameters

Parameter	Typical	Unit
Input Signal	> 20 (differential)	mV
Data Rate	53	Mbit/sec (per channel)
Optical Output Power	> 200	μW (per channel)
Rise Time	< 2	ns
Power Consumption	< 1.2	W/module
Duty Cycle	50	%

Table 2: Receiver Module Design Parameters

Parameter	Typical	Unit
Data Rate	53	Mbit/sec (per channel)
Output Signal	differential ECL	
Photo Diode Responsivity	1	A/W
Rise Time	< 2	ns
Power Consumption	< 1.6	W/module
Input Threshold	40	μW (per channel)

mode fiber ribbon cables to guide the light outputs from the TX modules at the inner layers of the detector to the second stage of the data acquisition system that is external to the detector. These are $62.5\mu m$(core)/$125\mu m$(cladding) fibers operated at a wavelength of 1550 nm. For ease of deployment, small segments of fiber ribbon *pigtails* are attached on both TX and RX modules, with one end of the fiber cable terminated with standard MT(TX)/MTP(RX) type connectors, and the other end aligned with the diode arrays on the module substrate.

The RX module contains a 9-channel photo diode array (PDA) as light sensors and the transimpedance amplification and decision integrated circuits.

2 Design Specification

The specification is separated into two parts for the TX and RX modules. The operational parameters were chosen based on the detector application requirements and the availability of various technologies. Tables 1 and 2 list the design parameters for either type of modules.

The power connection scheme for the TX is a bit more complicated than the RX module. A separate supply level, *Vld*, are provided for the laser diode arrays as the common to all cathodes. The driving scheme for the laser diodes is as shown in figure 2. This is required so that we can adjust the laser driving currents for optimal

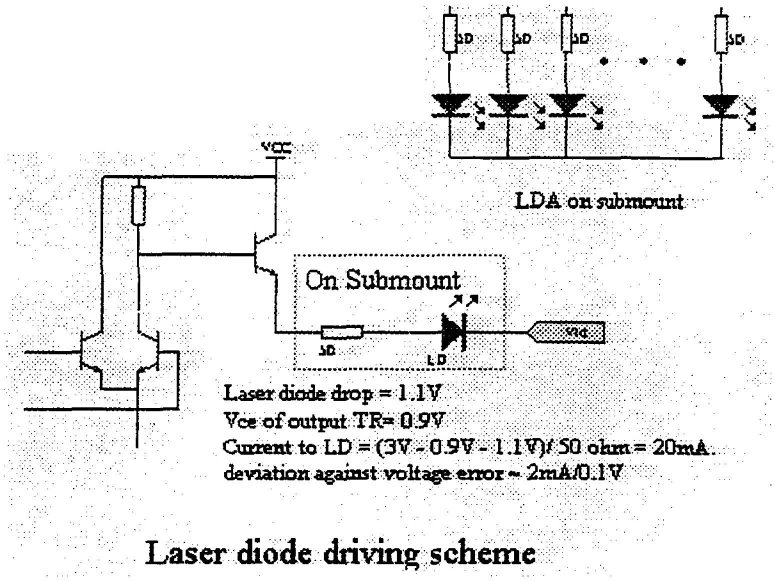


Figure 2: Driving scheme of the TX laser diode array.

light outputs from the TX modules. After years of running in the high radiation environment, we expect the light output levels to be gradually degrading. By having a separate and adjustable supply level for the laser diodes, we will have the capability to raise the light output levels back to acceptable ranges later on.

3 Component Implementation

Various issues have been taken into consideration when deciding on which technologies to adopt for making the prototype DOIM Modules. The most important factors are,

- High operational speed
- Compactness
- Radiation hardness
- Power consumption

The following section summarize the implementation methods of each component.

3.1 Driver and Receiver Integrated Circuits

The prototype driver and receiver ICs were implemented successfully with a BiC-MOS/BiPolar technology, based on its high speed capability and reasonable endurance in radiation environment compared to CMOS technologies. Production chips have been fabricated based on this successful design.

3.2 Laser and Photo Diode Arrays

The LDA technology used for the current version of the TX modules is the edge-emitting ridge-waveguide $InGaAsP/InP$ quantum well lasers. The pitch between lasers is 250 μm, and we make multiple-channel arrays and simply pick up the ones that have 9 consecutive functioning channels. Before module assembly, every laser is required to have at least 700 μW output power to leave enough margin for coupling losses expected during the alignment process with the optical fibers.

For the PDA in the RX module, we used $InGaAs/InP$ PIN photo diode arrays. Again, the pitch between diodes is 250 μm.

Both the LDA and PDA technologies are developed and fabricated for the CDF SVXII application at the Telecommunication Laboratories, Chung-Li, Taiwan.

New technologies like Vertical Cavity Surface Emitting Laser (VCSEL) is being evaluateded for possible replacement of the currently used edge-emitting diodes. This can further improve on light coupling, laser driving current reduction, and array fabrication yield.

4 Module Assembly

To package the various components into functioning TX and RX modules, we started by bonding the laser and photo diode arrays onto their submounts. After the array DC and burn-in tests, the submounts were installed on the ceramic module substrate.

On the other hand, the driving and receiving integrated circuit chips are bonded on the substrate and tested separately.

Then, the optical fiber ribbon cable is stripped at one end to expose the fibers. The fibers are then aligned with the diodes on the LDA or PDA, and hold in place by silicon V grooves as shown in figure 3.

Finally, plastic covers are placed on the module substrate to secure the components mounted on it. This will make the whole module more hermetic. Figure 4 shows the dimensions of the finished prototype TX and RX modules.

5 Prototype Tests

The first prototype of the fully packaged TX and RX module came out in the Spring of 1997. Various tests have been performed on these modules to establish their basic operational characteristics and to understand their behavior under temperature and humidity fluctuations and their survivability in radiation environment.

5.1 Basic Characteristics

The configuration of the test set-up for measuring the basic operational characteristics for the TX modules is as shown in figure 5. The module is powered up with two

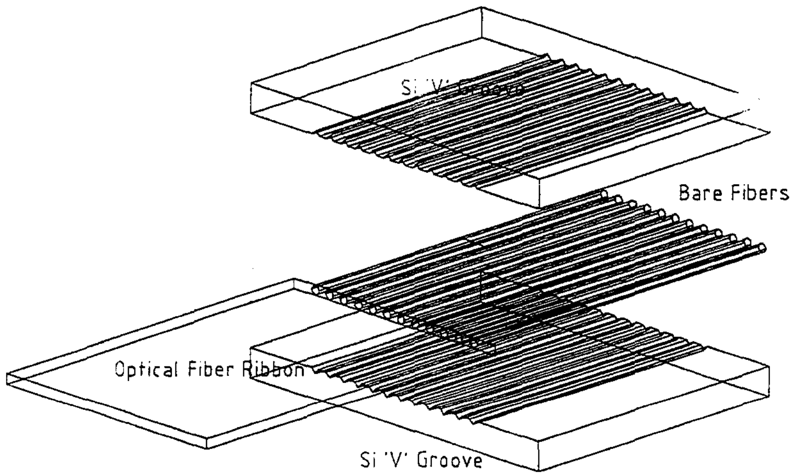


Figure 3: The optical fibers are hold in place by silicon V grooves.

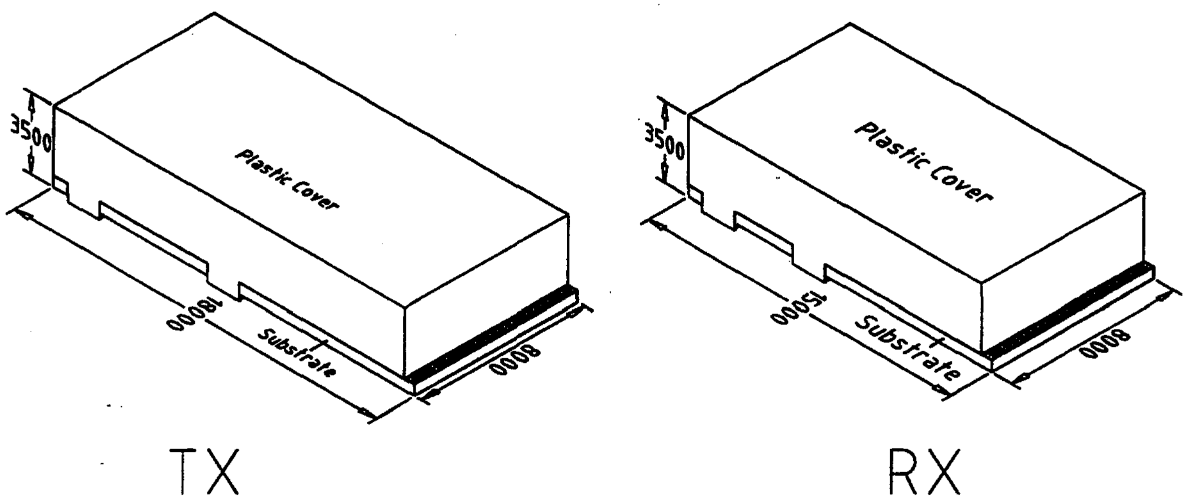


Figure 4: Finished TX and RX module dimensions (unit : μm) , after the module plastic cover is placed.

separate power levels, one for the driver circ[illegible] (Vcc [illegible]V) , one for the laser diode array (2V, or 3V below Vcc). Input signals are fed to all 9 channels, so they are switching simultaneously. The opitcal power levels and waveforms for each channel were converted to electrical signals by the Tektronix P6703B 0/E converter and observed on a digital oscilloscope. Normal channels that meet the design specification would have peak output power greater than 150-200 μW. A typical output waveform

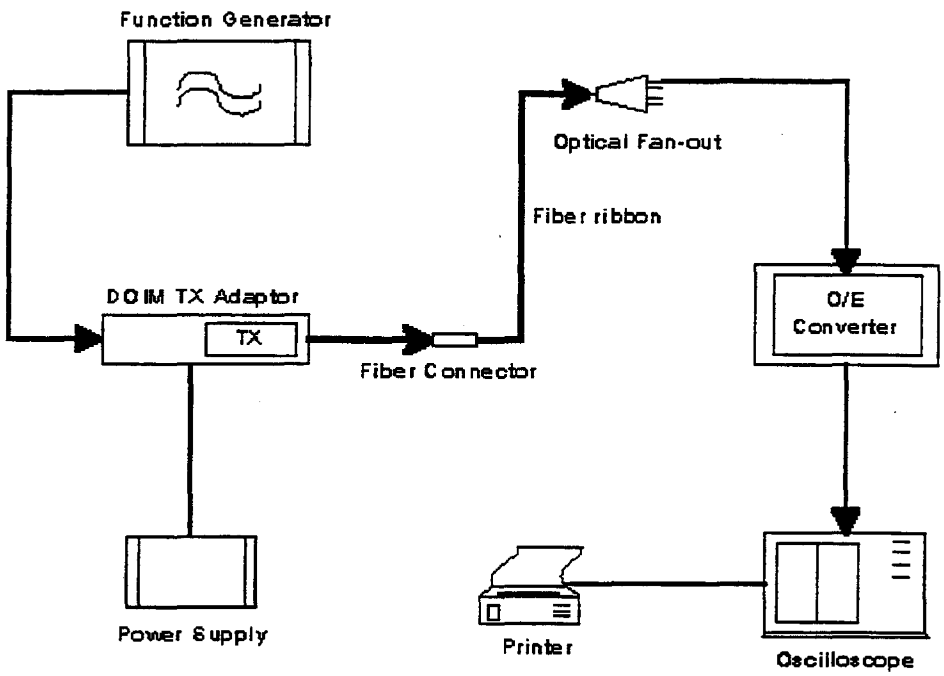


Figure 5: Transmitter module basic operating parameter test set-up.

is shown in figure 6.

For the RX module, we used a calibrated TX module as the input light source and observed the differential ECL output waveforms. A typical RX output is shown in figure 7.

5.2 Bit Error Rate Test

A crucial performance parameter for data communication modules is the Bit Error Rate (BER), which is defined as the number of bits decoded in error versus the total number of bits received. The DOIM design specification requires that the BER be $< 10^{-12}$.

To measure the BER for the prototype DOIM TX-RX link, we used the Fermilab custom-designed Bit Error Rate Tester (BERT) [4]. The test set-up is as shown in figure 8. Both random and alternating data patterns were generated at the TBERT module, and transmitted to the RBERT module via a full DOIM TX-RX link. The data received at the RBERT end were then compared to the pattern originally sent to locate any burst of errors.

The test was conducted for more than 7 days with both data patterns, before the first error came about on one of the 9 channels. This corresponds to a BER of better than $< 10^{-14}$, two order of magnitude better than what the design specification required.

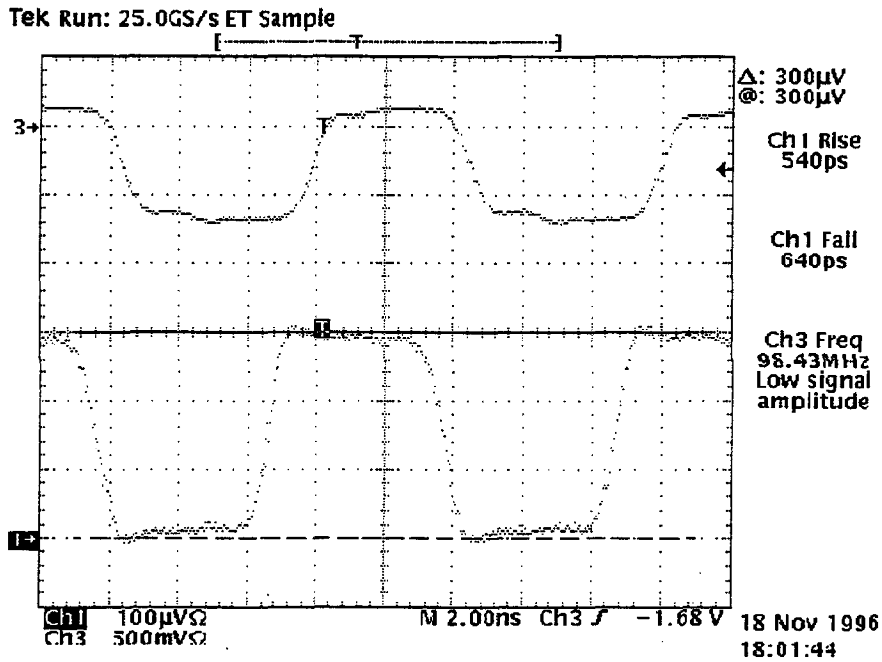


Figure 6: Typical transmitter optical waveform, as shown on Ch1 of this captured digital scope display. Note that this module is operated at 98 MHz to test its capability at higher frequencies.

5.3 Power Consumption

For the TX module, the power consumed by the driving circuits is relatively constant independent of the data patterns. The power drawn by the laser diode array depends on the adjustable Vld supply level and the data pattern. The worst case senario is when all 9 lasers are on all the time. A typically averaged range is for a duty cycle of 50%, at which a total power of 1W is consumed by the whole module (9 channels). The power scheme for the RX module is simpler. There is only one Vcc supply. The power consumption is measured to be 1.6W per module. The above measured power dissipation rate is well within the power budget required by the design specification.

5.4 Radiation Hardness

For the projected 3 years of running periods for the Fermilab Tevatron Run II, the DOIM TX modules are expected to receive an average total dose of close to 250 KRad. To establish their functionality under radiation environment, we have carried

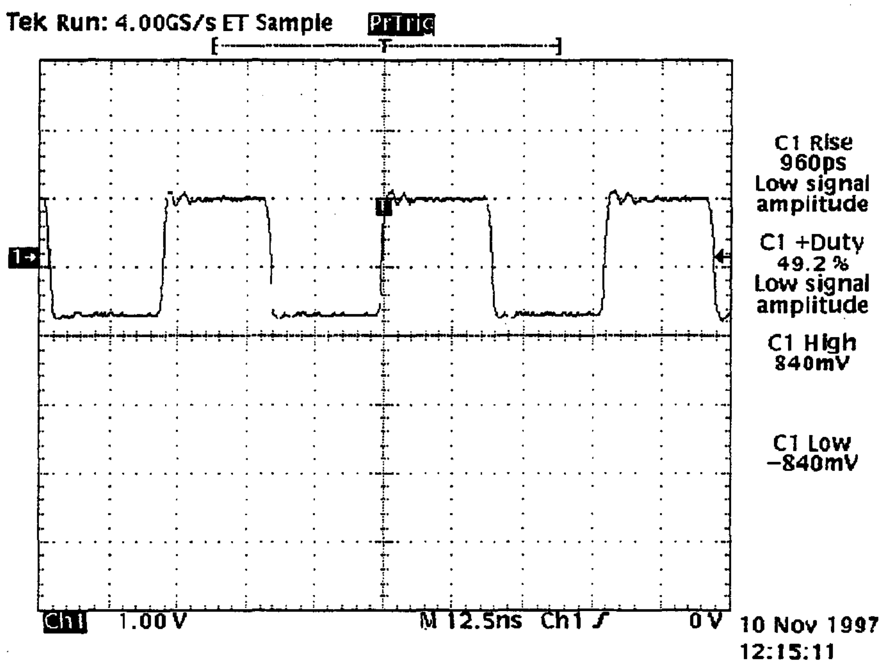


Figure 7: Typical receiver differental output waveform.

a few tests at the Fermilab Booster area with 8 GeV proton beams.

The first test on just the BiCMOS/BiPolar driver circuit (July 1997) showed no observable degradation of the switching characteristics on the chips up to a total dose of 1 MRad.

We also subjected 1 fully packaged prototype TX module in the same beam for up to 1.5 MRad. The module was powered up and fed with 50 MHz input signals during irradiation, and the output waveforms were monitored periodically throughout the irradiation. For the 4 consecutive runs as shown in figure 9, we observed that the light output decreased consistently by 25% after roughly every 250 KRad of accumulated dose, and the degradation corresponded roughly to the time when the beam swept through the module. This is a combined effect since degradation in output came from both the LDA in the module and the darkened fibers.

After the 1.5 MRad total radiation dose, the TX module still had output power level beyond that is required by the RX switching threshold/sensitivity. Therefore, the prototype modules are capable of dealing with the 250KRad in the Run II environment.

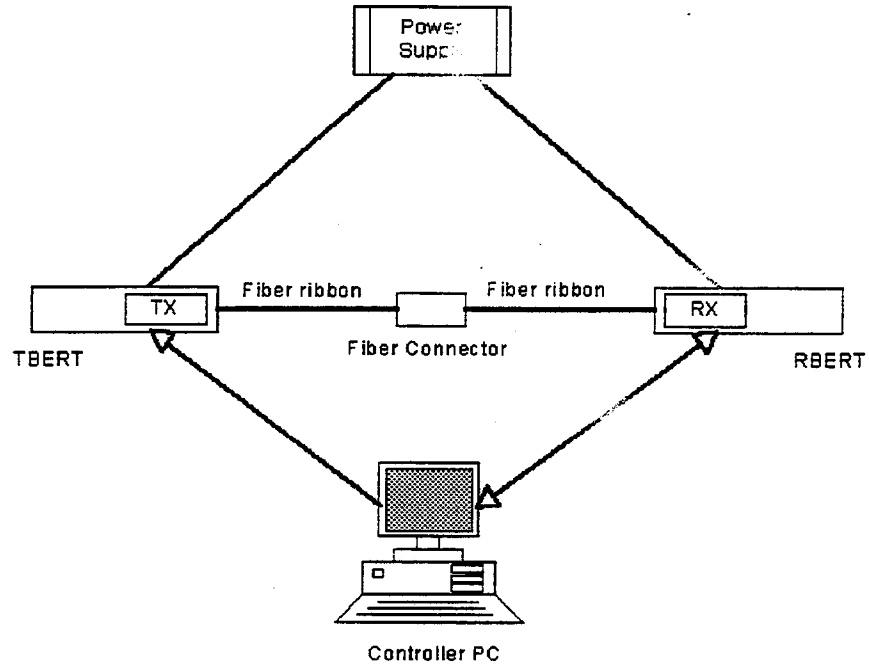


Figure 8: Bit Error Rate test set-up.

5.5 System Integration

The DOIM TX modules are to be installed on the Port Cards [5] of the SVXII detector data acquisition system. These are custom-designed boards that control the front-end readout chips at the silicon sensors and send the data out via the 5 DOIM TX modules on each Port Card.

On the other end, the RX modules are located on the Fiber Interface Board (FIB) [6] which are installed in racks outside the whole detector structure. They translate the data from the differential ECL outputs from the DOIM RXs to TTL levels and transmit them out to trigger system and readout controllers.

The prototype DOIM TX-RX link has been tested with the prototype Port Card and Fiber Interface Boards. The full link has been demonstrated to be transmitting valid data from the front-end readout chip. This is a milestone for the successful implementation of the SVXII data acquisition system. Larger scale system integration test is currently underway.

6 Conclusions

From the various tests performed on the prototype TX and RX modules, we found that the DOIM design was sound and that the first implementation met the design

DOIM TX MI8 Irradiation Test
(Dec 10-14, 1997)

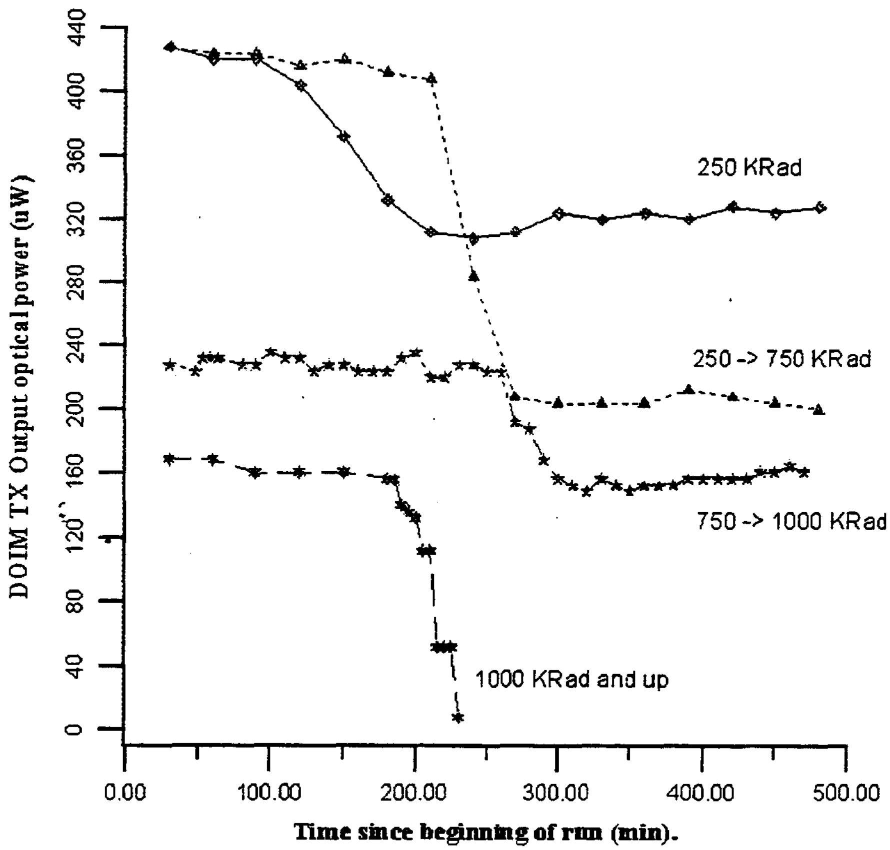


Figure 9: TX module 8 GeV proton irradiation test - Optical Output Power (μW) vs. Elapsed Time (min) during 4 runs, with accumulated dose for each run indicated on each curve.

requirements. The production process of these modules is currently underway, and full delivery for CDF SVXII application is expected by Spring of 1999.

We are currently exploring further improvement on TX laser diode optical output uniformity, by fine-tuning the alignment process. Production level burn-in and system integration tests are also in progress.

7 Acknowledgement

This project is supported by the National Science Council of Taiwan, Republic of China.

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Pixel Detectors using MCM-D Technology

May 8th 1998

Peter Gerlach
Bergische Universität-Gesamthochschule
Wuppertal

K.H.Becks
P.Gerlach

E.Beyne
P.Pieters
C.Truzzi

O.Ehrmann
J.Wolf

Workshop Pixel98

FNAL May 7-9th 1998

MCM-D, what's that ? (1)

- Thin film technology, integrating bus systems on a substrate
- Developement (a.o.) at
  - Interuniversity Microelectronics Center (**IMEC**, Leuven, Belgium)
  - Frauenhofer Institute for Reliability and Microintegration (**IZM**, Berlin, Germany)

MCM-D, what‘s that ? (2)

conductor layers

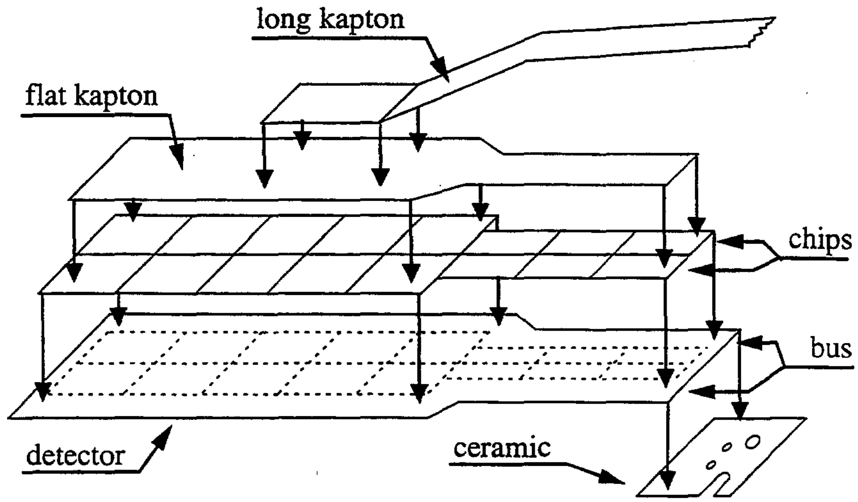
- Up to 5 copper layers:
  - magnetron sputtered up to 2 µm Ti/Cu/Ti $\Rightarrow$ 10 mΩ/□
  - additive electroplating up to 5 µm Ti/Cu
- Minimal width and spacing 15 and 20 µm
- Final metallisation: electroless 5µm Ni:P/ 200nm Au

dielectric layers

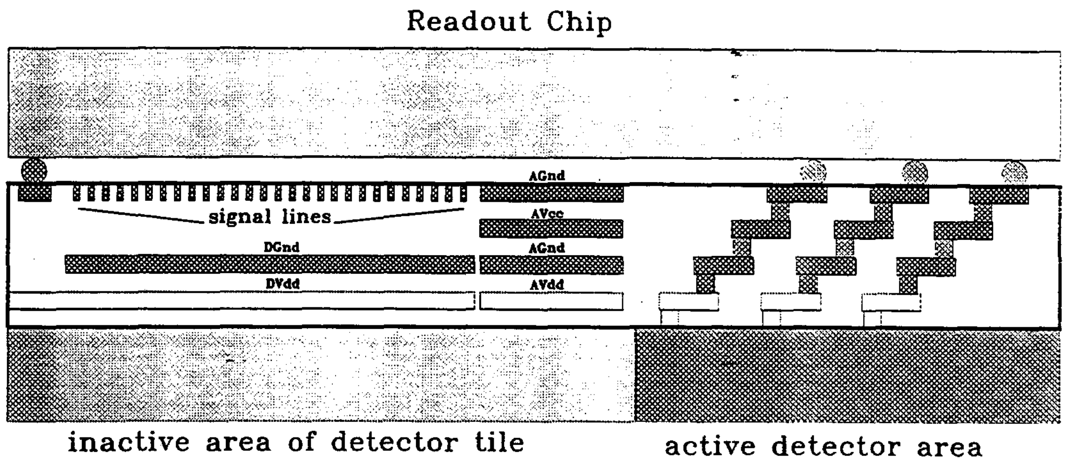
- “Spin-on” polymer: BCB (Benzocyclobutene / DOW:CYCLOTENE™)
- Photosensitive
- Specific dielectric constant $\varepsilon_r = 2.7$
- Process temperatures : 1h 220°C per layer, last layer 1h 250 °C
- Thickness / layer 4 - 10 µm
- Via ∅ >20 µm, Pad 30µm

Structure of a Module **without** MCM-D

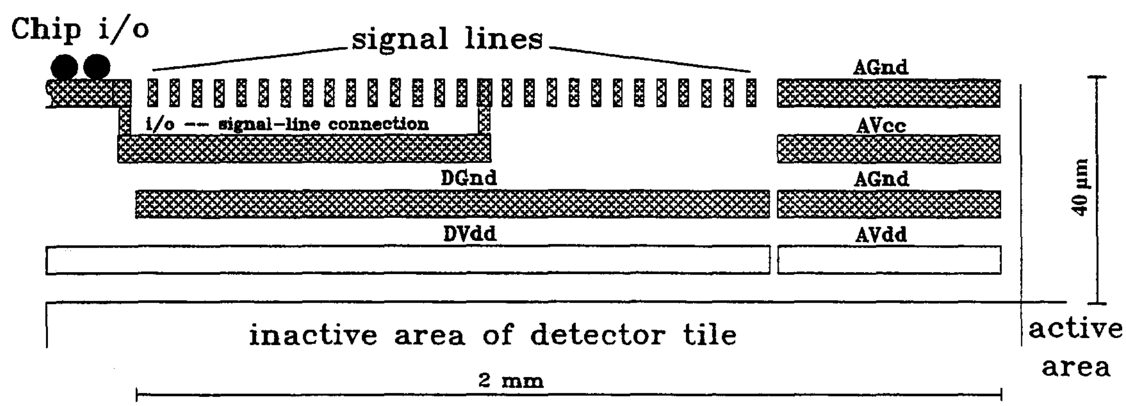
Example: DELPHI vertex detector pixel module (Raquette)



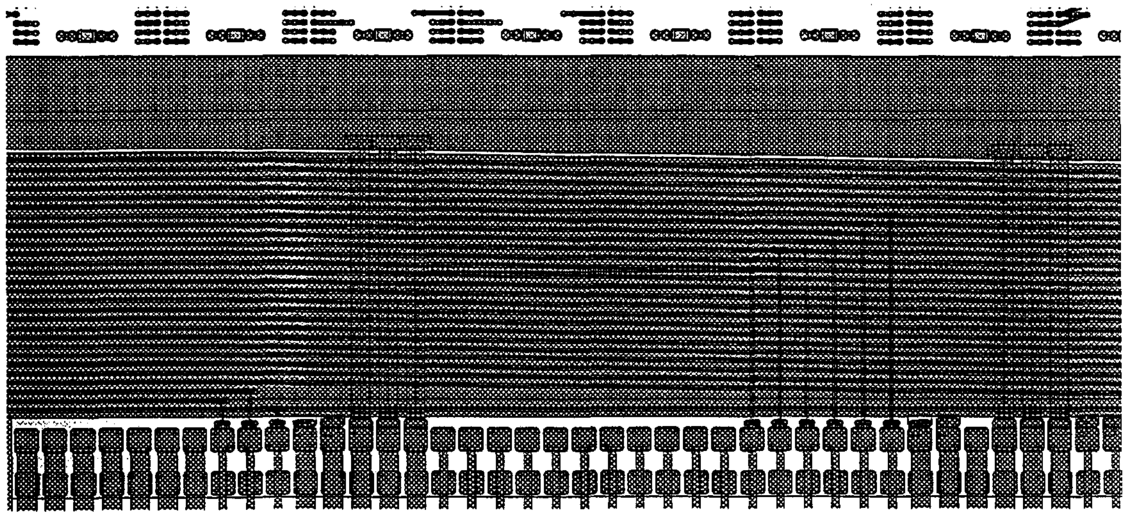
Structure of a Module **with** MCM-D



Cross-Section of a Bus System



Top View of a Bus System



R&D Program

☑ Geometric requirements
☑ Radiation hardness
☑ Bump-bonding tests
☐ Test on active silicon
☐ Demonstrator module

Performance of the Bus System (1)

Bus system for 8 readout chips

Signal-Bus:

A 7cm long bus made of microstrip-lines 20 μm wide with 30 μm spacing shows

- $Z_0 = 68\ \Omega$
- Crosstalk < 3%
- Signal-attenuation < 4 dB (<1GHz)

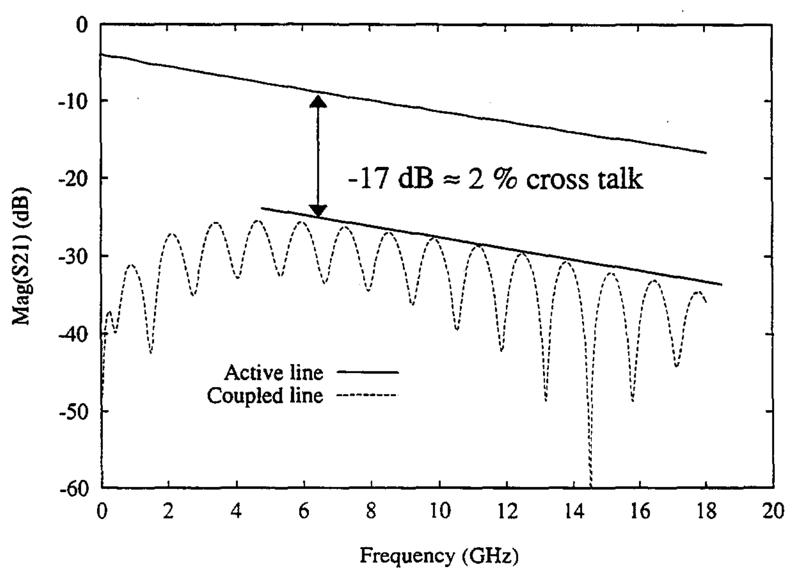
Power Supply Bus:

Calculations

$\Rightarrow$

- Power loss < 150 mW
- Max. difference of potentials 100 mV

Performance of the Bus System (2)



IMEC

Radiation Hardness (1)

P.Gerlach University of Wuppertal

- 10^{15} e^-/cm^2 at 40 keV cause a change in ε_{r_eff} of **2%**. (Irradiation by C.Becker, Univ.Dortmund)
- Irradiation of the same test-wafer with $5 \cdot 10^{14}$ p^+/cm^2 at 24 GeV protons causes a change in ε_{r_eff} in total of **3%**. (Irradiation at CERN)

⇨ *Due to absorption of moisture, a change in ε_{r_eff} of **1.4%** is expected.*

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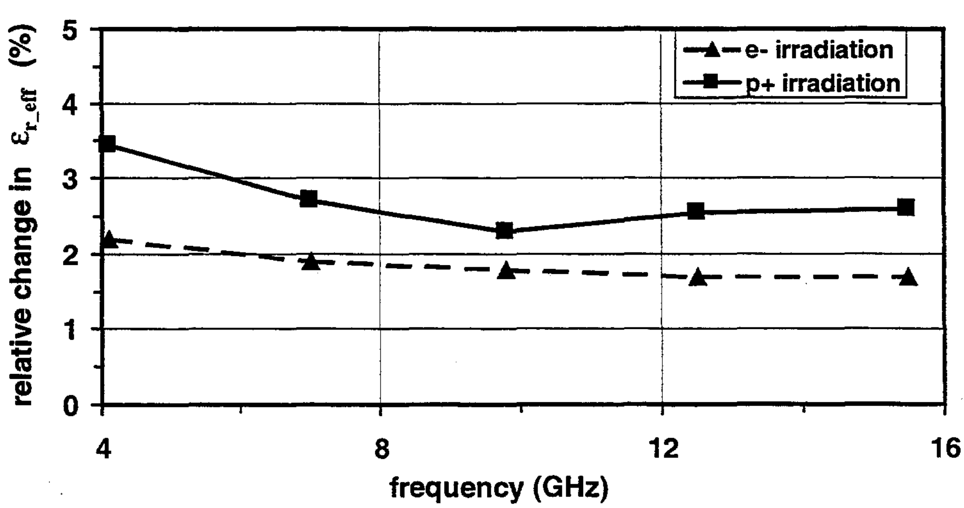
Radiation Hardness (2)

P.Gerlach University of Wuppertal



IMEC

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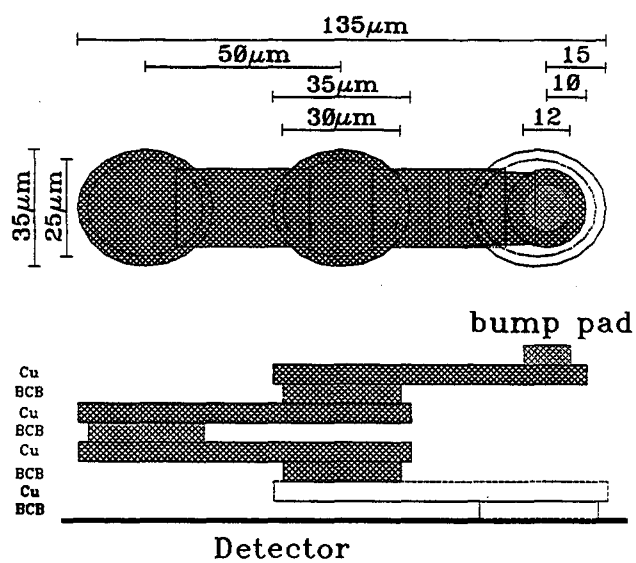
Bump-Bonding Tests

- Two wafer layouts
  (detector and r/o-chips)
  with “daisy-chain” of bump connections
  (University of Bonn / IZM Berlin)
- 1.1 $\cdot 10^6$ monitored vias with a diameter of 25μm indicating an error rate **< 10^{-5}**

Layout of a Feed-Through Structure

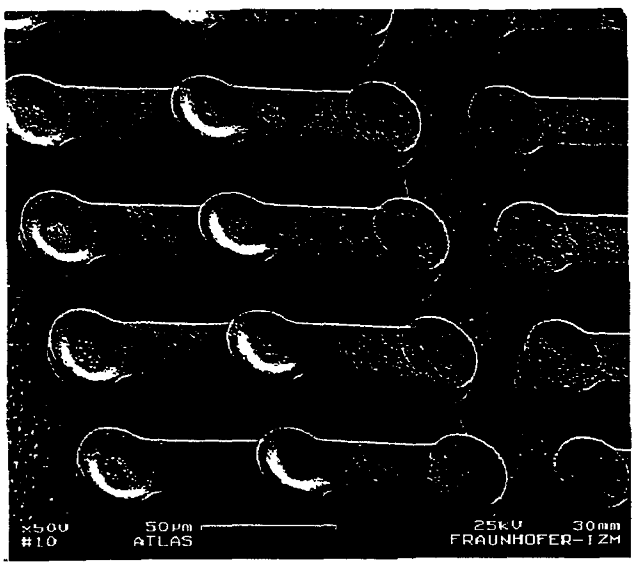


Cut through Bump Region

Photograph IZM

- Cross-section of flip chip bondet IC's on silicon substrate
- Bump pitch 50 µm
- 4 Cu layers and 5 Photo-BCB layers
  Photo-BCB: 5 µm thick, 25 µm vias

Feed-Through Structures



- Four copper layers
- BCB etched for better visualisation
- Measured defect rate
  $8.13 \cdot 10^{-6}$
  (9 defects in 1 105 920 vias)

Photograph IZM

Feed-Through Parasitics

P.Gerlach

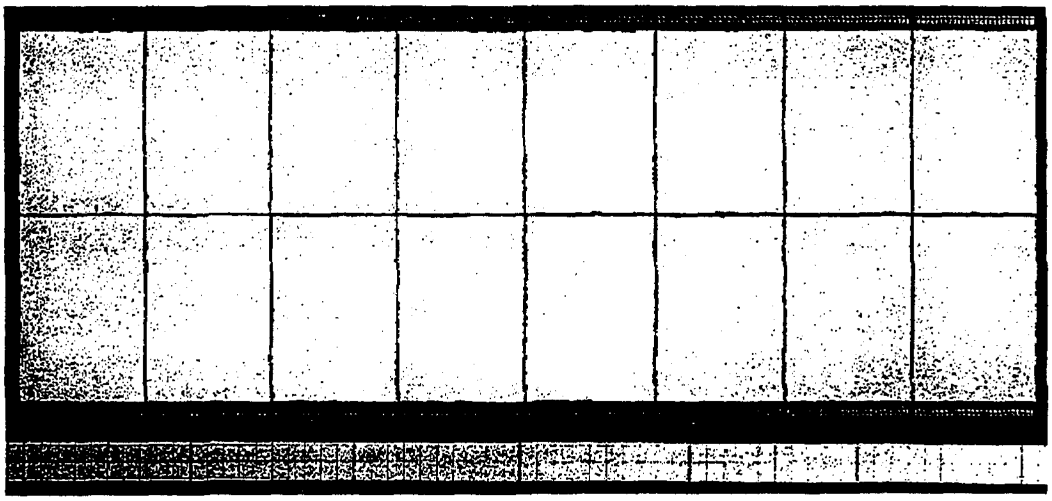
University of Wuppertal

- Resistance:
  - 2µm Cu-Layer ⇒ 10 mΩ / □
  - 5 mΩ per Via
  - ⇒ 60 - 160 mΩ per feed-through
- Coupling Capacitance:
  - 20 - 40 fF between 2 adjacent feed-throughs

Photograph of IZM MCM-D Prototype

P.Gerlach

University of Wuppertal



Multi Chip Module - Deposited Conclusions

radiation hard thin film technology

Up to **5 copper** layers

- Layer thickness up to **5 µm** (2µm Cu-Layer ⇒ 10 mΩ / □)
- Line width/pitch **20/50 µm**
- Impedance controlled

Benzocyclobutene (**BCB**)

- $\varepsilon_r = 2.7$
- Layer thickness **4 to 10 µm**
- Via down to **∅ 25 µm** (~1mil) failure rate **< 10^{-5}**

In progess:

- Test on active silicon
- Demonstrator module

The CDF SVXII HDI and Long Cu-Kapton Flex Cables

Mark Bailey
New Mexico Center for Particle Physics
University of New Mexico
for the CDF SVXII Group

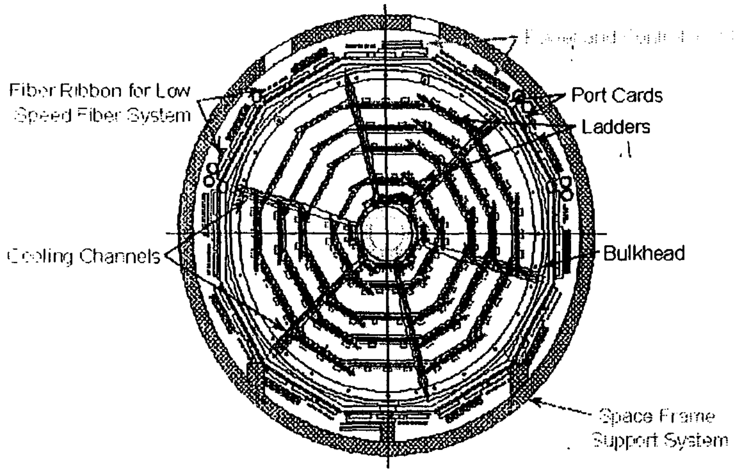
PIXEL98 Workshop
May 9, 1998

- Overview
- **High-Density Interconnect Cable**
- **Long Cu-Kapton Cable**
  - **General Design**
  - **Special Features**
- **Summary**

Overview

- **The CDF SVXII Detector is a five-layer silicon strip detector. Each cylindrical barrel is divided into twelve wedges.**
- **Each wedge has at its outermost radius a port card. The port card receives electrical timing signals from the external DAQ electronics, and sends back data via optical fibers.**
- **The detector power and timing signals for a given wedge are carried on a single Cu-Kapton cable, called the Long Cu-Kapton cable.**
- **This cable connects between to the port card, and runs 6 feet out of the detector volume, where it connects to standard flat cables.**

Cross Sectional View of Barrel End



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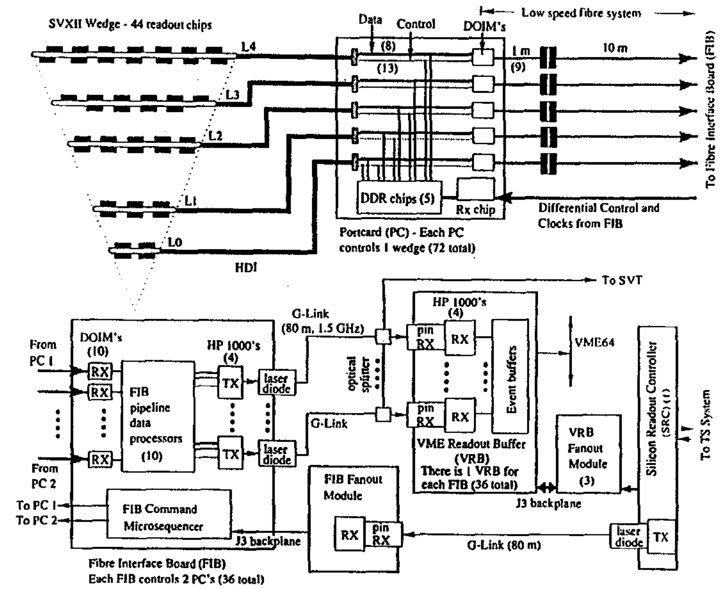
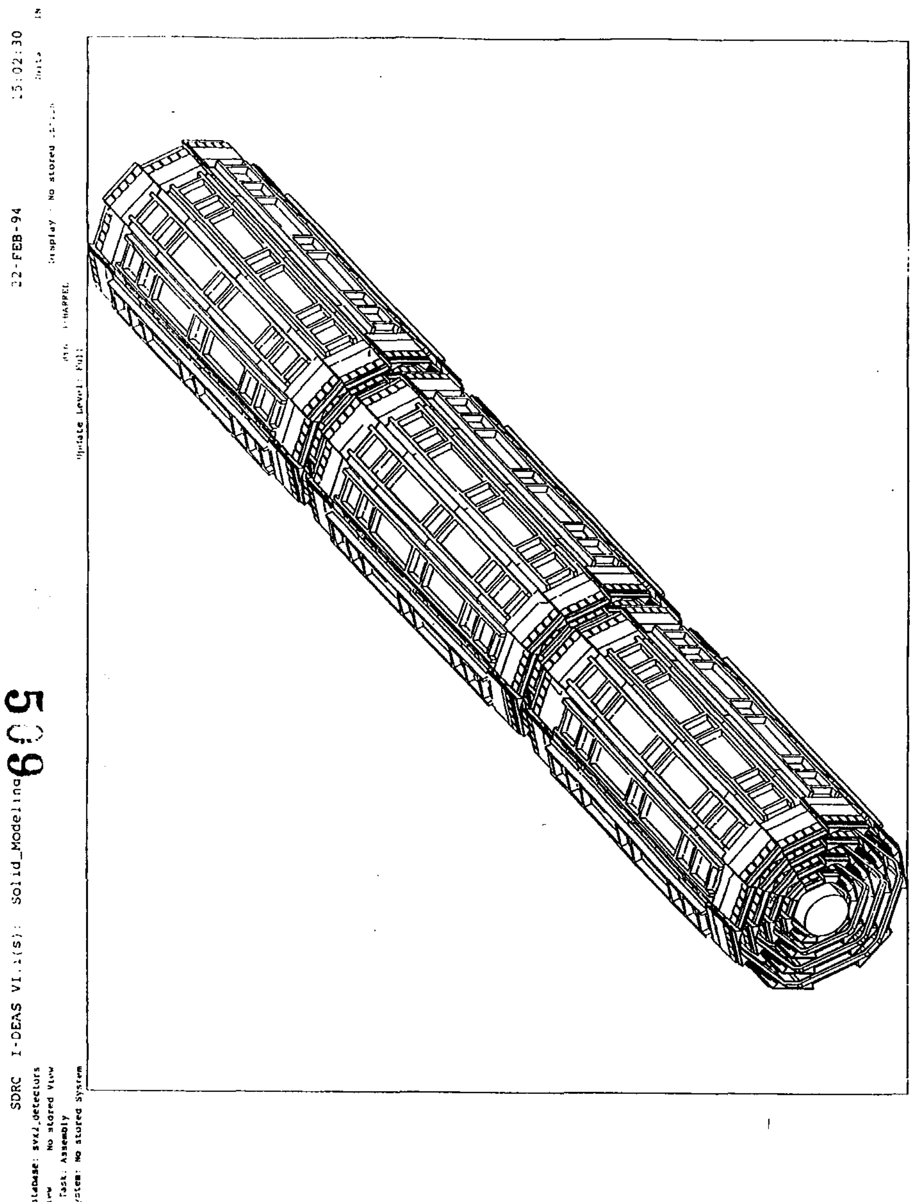


Figure 5: Schematic of the SVX II data acquistion system. The upper half shows the frontend readout mounted on or near the SVX II. The FIB system is in VME crates on the sides of the CDF detector, and the VRB system and SRC are in the counting room.



- **Each layer of a wedge has SVX3 custom readout chips, mounted on a hybrid. The port card connects to each of the 5 layers using a compact HDI cable.**

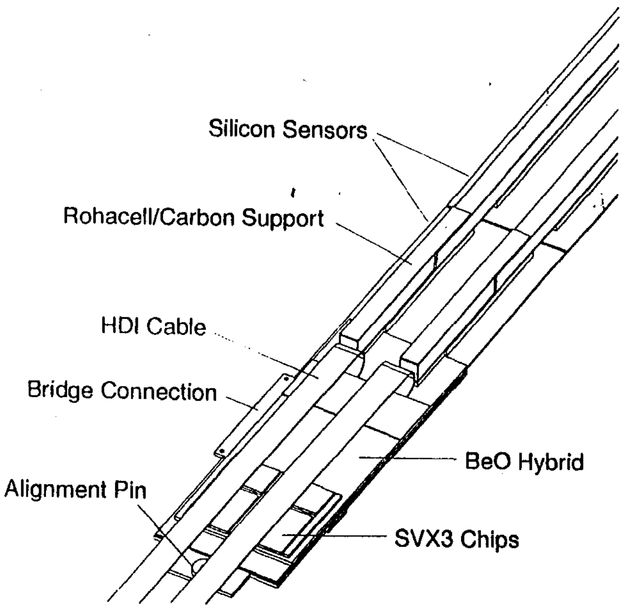
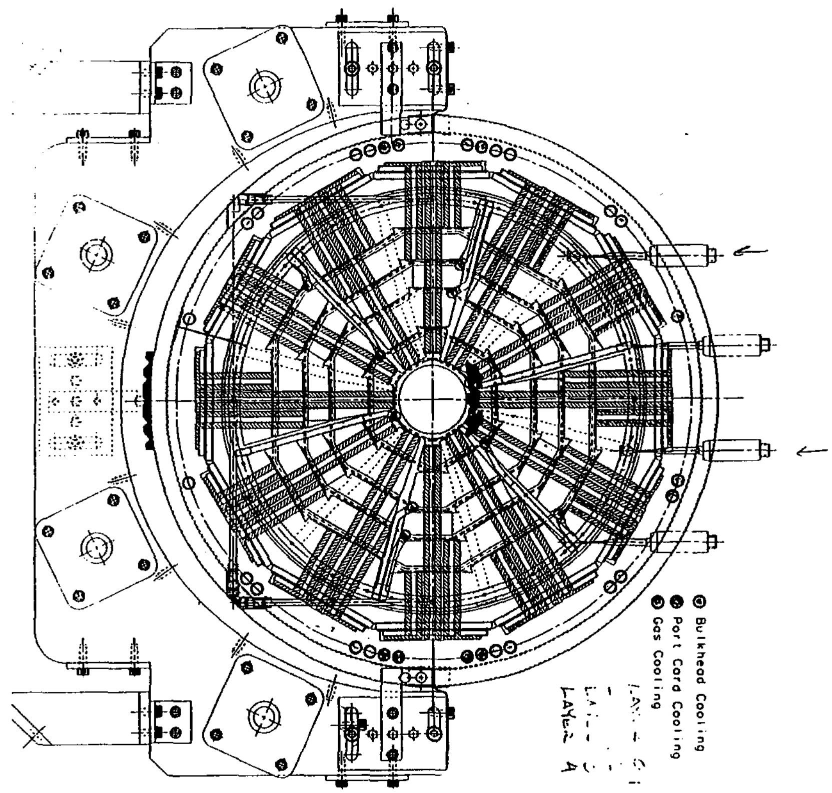


Figure 3: Schematic of an SVX II layer 0 half-ladder consisting of 2 silicon sensors. Electronics for the readout are mounted on the first sensor. The z-side SVX3 chips are on the underside and are not visible.



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High-Density Interconnect (HDI) Cable

- Carries power and timing signals between port card and layer hybrids
- Tight space constraints demand high trace density and compact design

- Design/layout at University of New Mexico (with M. Gold, J. Behrendt, and M. Garcia-Sciveres(LBL))
- Prototypes fabricated by Dynaflex Technology, San Jose, CA.

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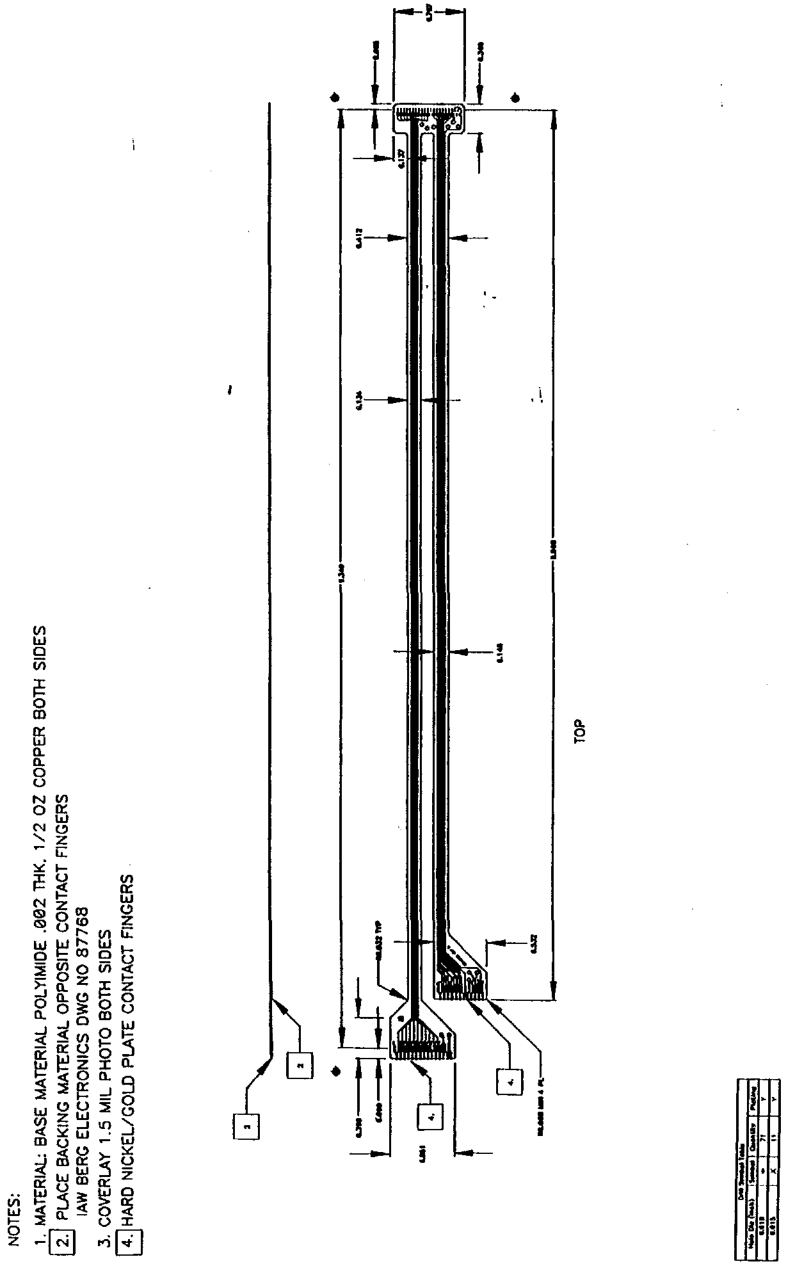
HDI Cable General Design

- **1/2 oz./ft^2 copper on 2 mil Kapton**
- **Signal traces are 3 mil wide, with a 7 mil pitch, broad-side coupled (signal and its complement are on opposite sides of the Kapton)**
  - (This is near the limit of most vendors' capabilities)
- **Power is carried on discrete 34 AWG wires, soldered onto the cable**
- **Total size** $9.9'' \times 1.1''$



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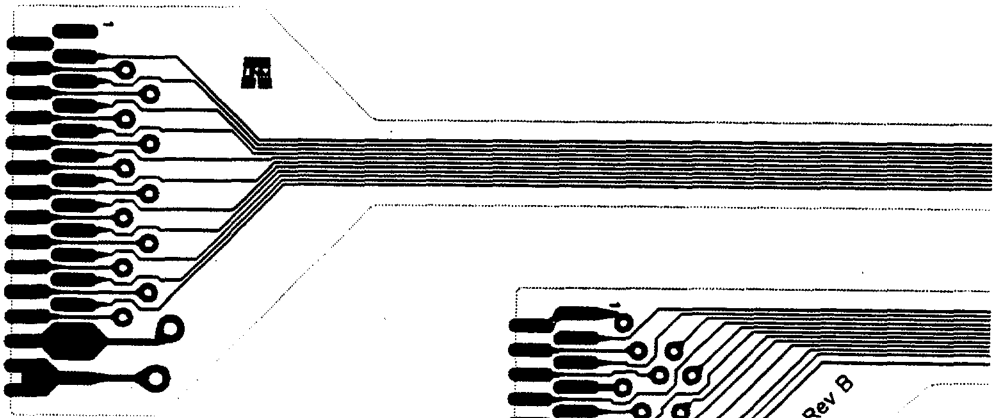
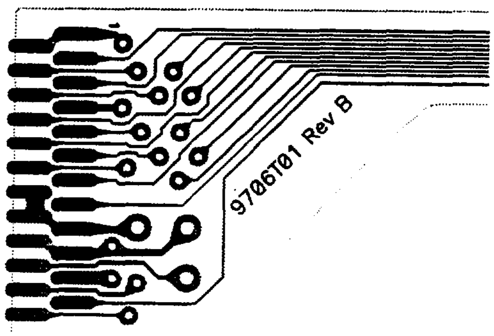
HDI Cable
Special Features

- **Densely packed solder pad array: Holes are 5 mil in diameter on a 10 mil pad**
  - Most vendors can't meet such a tight tolerance
  - More easily done when pads are close together in a regular pattern
  - For single pads, usual tolerance is a 10 mil annular region about the hole
- **Accommodates Berg Electronics "zero insertion-force" connectors**
  - Teardrop transition from traces to pads
  - Tin plating on contact fingers

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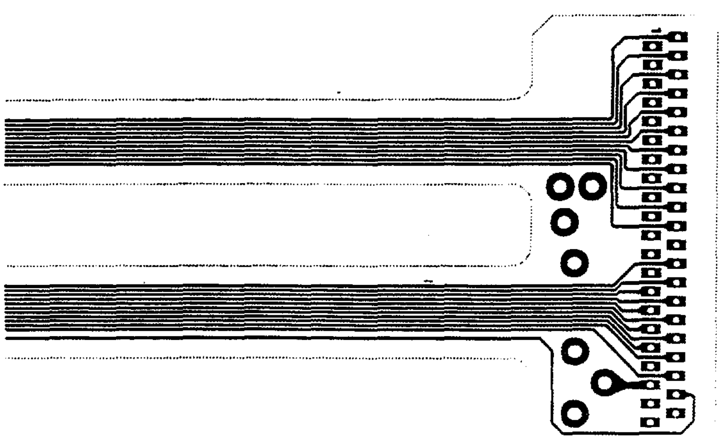

Long Cu-Kapton Cable

- Carries power and timing signals from standard flat cables outside the detector in to the port card, along the beamline near the interaction region
- Relatively low-mass Cu-Kapton solution was chosen to reduce multiple scattering in the region
- Also need to control voltage drop along the cable, and match the impedance of signal lines with the external flat cable

- Design/layout at Fermilab (with J. Anderson and J. Franzen)
- Prototypes fabricated by Speedy/Metro Circuits, Huntington Beach, CA

Long Cu-Kapton Cable General Design

- 1 oz./ft^2 copper on 5 mil Kapton
- Signal traces are 8 mil wide, with a 15 mil pitch, broad-side coupled, giving an impedance of 101Ω
- Power traces are opposite respective return lines, for low inductance
- Total size $6' \times 2.4''$

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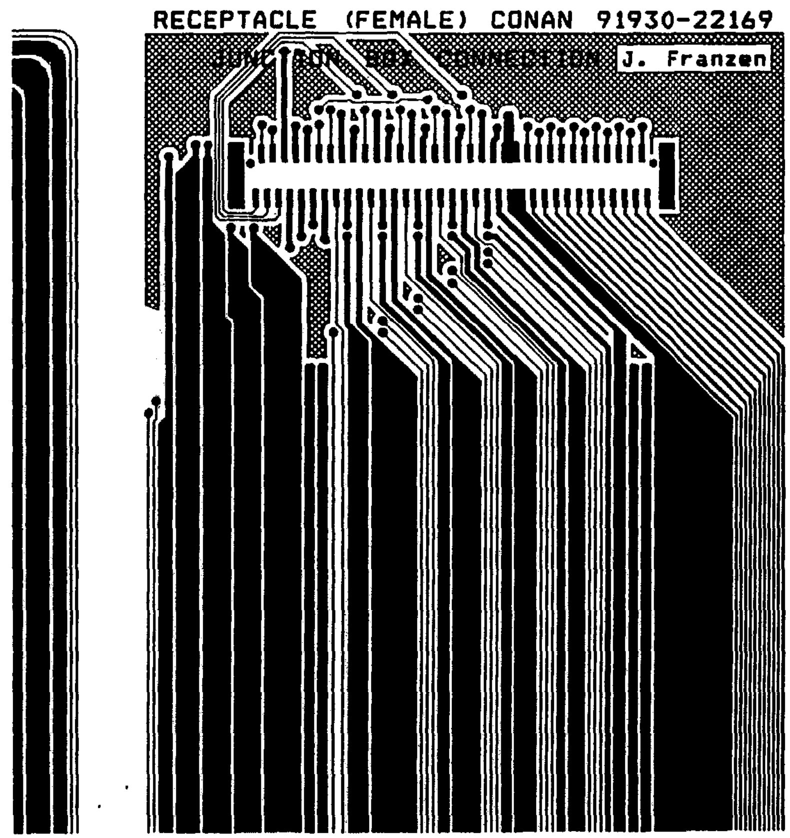
TOP LAYER

Long Cu-Kapton Cable Special Features

- SIZE:
  - Length greatly limits number of vendors available, and raises the cost
  - Many long cable vendors can etch on only one side
- **Signal trace width set to give $\sim 100\Omega$ impedance, well matched with standard flat cables**
- **Trace widths of power lines chosen to give a drop of less than 0.5 V across the length of the cable**
- **Cable mass averaged over phi is about 0.55% X_0**



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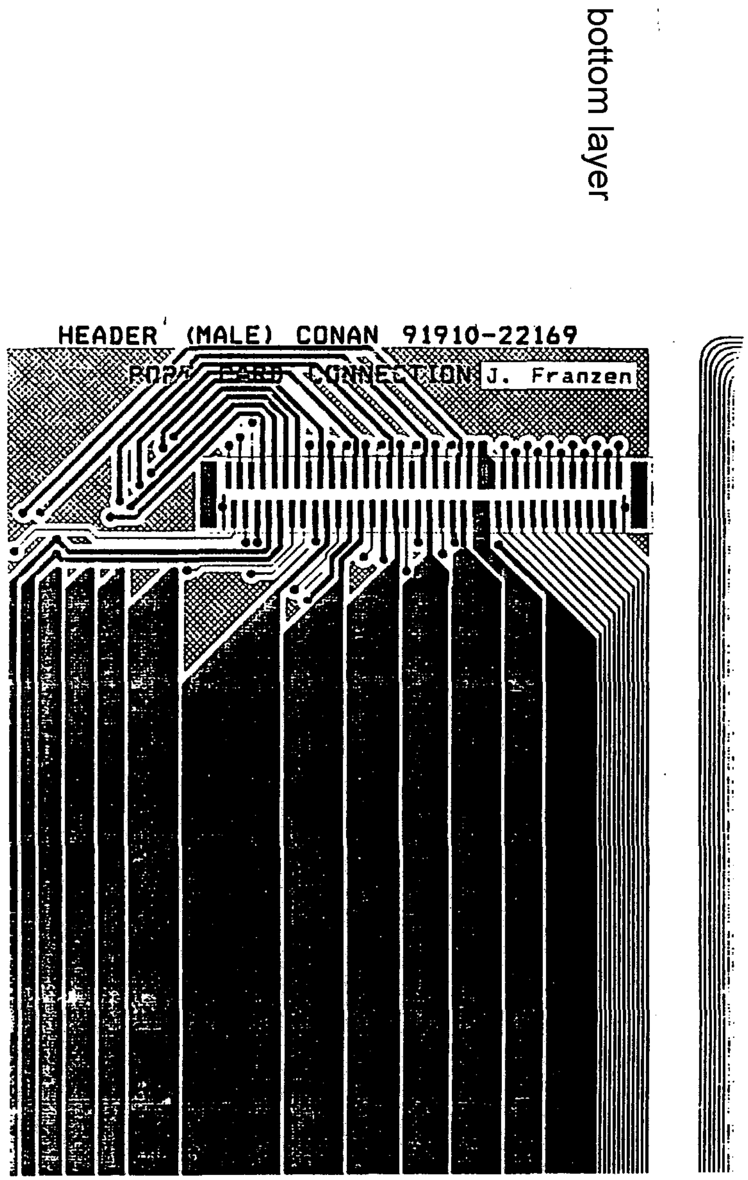
Long Cu-Kapton Cable Special Features



- Small prototype runs at reasonable cose aren't available for long cables
- Prototype uses a serpentine layout, which folds out to give full length. Might be a reasonable solution, but signal propagation and susceptibility for traces to break needs to be investigated
- Inaccessibility of the cable in this area precludes connecting several shorter cables together

Summary

- The CDF SVXII group has exploited Cu-Kapton flexible circuit technology to provide two of its interconnection cables
- The HDI cable uses a small trace width size and dense solder pad array which are near the limits of most vendors' technical capabilities
- The Long Cu-Kapton cable tests another limit: the maximum circuit size available. Serpentine design might be a viable solution, which uses a circuit dimension more typical in the industry
- Cu-Kapton cable design properties and limitations should be considered at an early stage in the design of the components to which they are to be connected
- Fortunately, there are a large number of vendors with complementary capabilities. With some persistence, one can usually find one who can meet one's design requirements

Flex Circuits for the ATLAS Pixel Detector

P. Skubic,[a*] R. Boyd,[a] W. Hennessy,[b] S. Krishnama,[a] K. Neriyanuri,[a] H. Severini[a]

[a] *University of Oklahoma, Norman, OK 73019*
[b] *GE Corporation, Schenectady, NY 12301*

Abstract

Recent progress on designs of low-mass, flexible circuits for the ATLAS pixel detector will be discussed. Thin flexible circuits can be used to provide power and signal connections between front-end readout chips and data acquisition chips on the 2 cm by 6 cm ATLAS pixel detector module. Layouts and SPICE simulations will be presented for such circuits based on non-standard printed circuit board design rules. Test results from circuits fabricated for other applications using similar design rules will also be presented.

*Corresponding author. E-mail: *pskubic@ou.edu*

1 Introduction

An array of hybrid pixel detectors is being developed for use at the Large Hadron Collider (LHC) by the ATLAS collaboration. The detector layout consists of three barrel layers, and five disk layers at each end. Each pixel module has sixteen front-end (FE) chips bump-bonded to a single sensor. One module design option utilizes a thin flexible circuit (Flex Hybrid) which is mounted on the back of the sensor to provide interconnections for power and digital signals between the FE chips, a Module Clock and Control chip (MCC), and an optical link which are mounted on it. Wire bond pads on the edge of the hybrid will be used to connect power and signal lines to corresponding wire bond pads located on the FE chips, which extend beyond the edge of the sensor. The module is 2.14 cm wide and 6.24 cm long. This conceptual module design is illustrated in Figure 1. Several possible designs for the Flex Hybrid are presented here along with results of simulations of expected performance.

2 Flex Hybrid Designs

Minimizing mass in the active tracking volume is of crucial importance in obtaining the optimum physics performance of the ATLAS detector. We are therefore required to use thin (flexible) substrate and metal layers in design of the Flex Hybrid. Flexible printed circuit technology typically uses film substrates such as Kapton with a minimum thickness of 25 μm containing patterned surface metal layers with or without cover insulating layers (passivation). Plated through via's can be used to connect traces in different layers. Many vendors use "standard" design rules allowing minimum trace widths

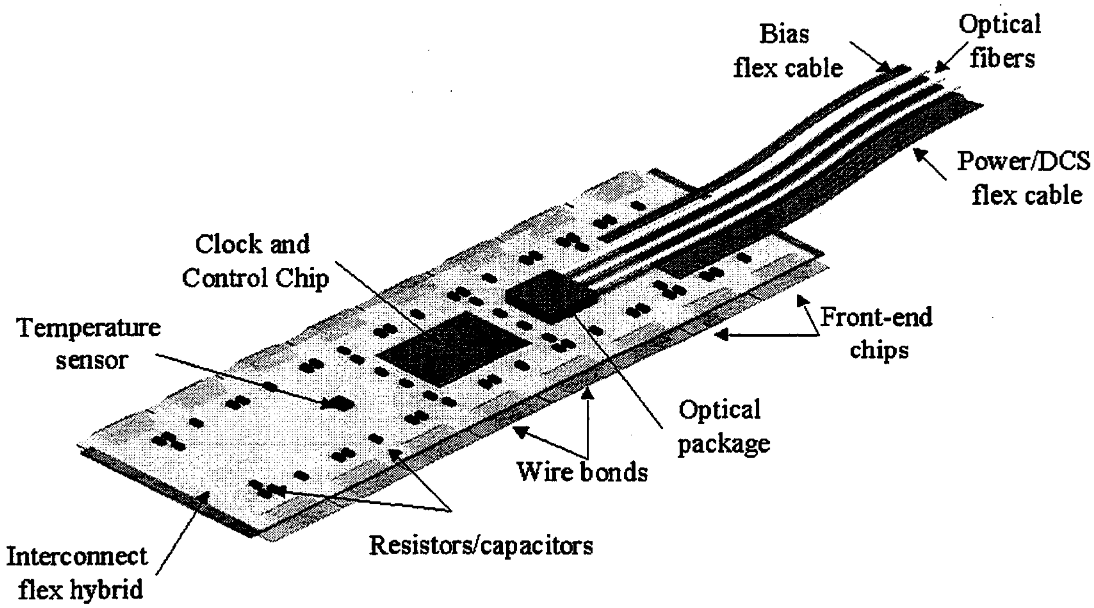


Fig. 1. Conceptual design for an ATLAS pixel module. The module is 2.14 cm wide and 6.24 cm long.

and spaces of 100 μm, 400 μm via cover pads, and 200 μm via through holes. Several vendors have developed High Density Interconnect (HDI) processes which can attain smaller feature sizes. For example the General Electric Corporate Research and Development (GECRD) HDI process can achieve 30 μm trace widths and spaces, 75 μm via cover pads, and 25 μm via through holes.

In the designs to be described here, the optical link has been replaced by an off-module Ladder Control Chip (LCC). The required signal and power connections between the FE chips, the MCC chip, and the LCC which are provided by the Flex Hybrid are illustrated in Figure 2. Low Voltage Differential (LVD) lines are used for the digital signals. "Broadside coupled" lines

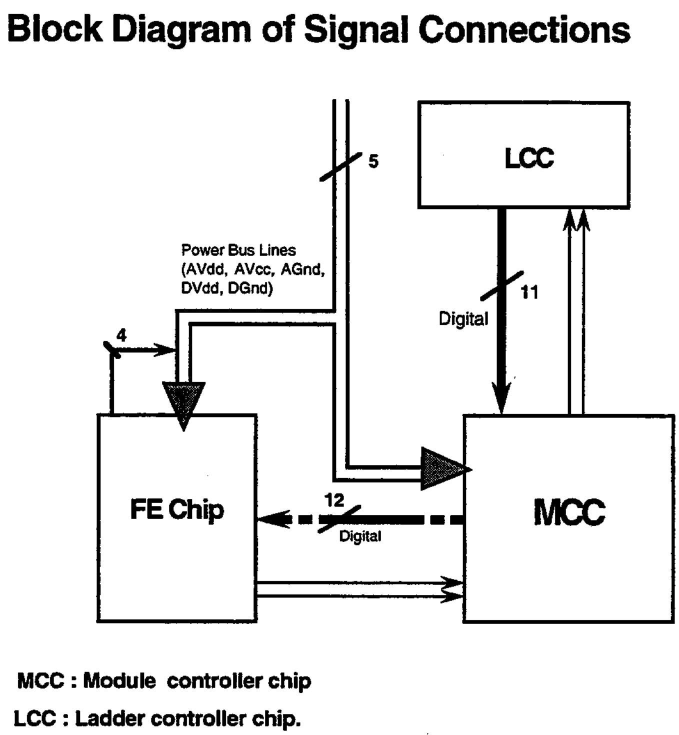


Fig. 2. Block diagram showing the signal and power connections required to be made by the Flex Hybrid.

with paired differential signals on opposite sides of a substrate layer were used whenever possible, particularly in designs using the standard design rules. In designs using HDI rules, it was often necessary to use co-planar paired differential lines in order to minimize the number of metal layers. The maximum current specifications for the FE chips were 25 mA for 3 V analog power, 50 mA for 1.5 V analog power, and 30 mA for 3 V digital power. The maximum current specification for the MCC chip was 100 mA for 3 V digital power. A maximum voltage drop of 100 mV was allowed in the power (and ground) lines over the length of the module.

The LHC beam crossing frequency is 40 MHz which is also the clock frequency for the pixel readout chips. Typical 40 MHz square waves have large-amplitude frequency components near 40, 80, and 120 MHz with smaller components at higher harmonic frequencies, so crosstalk and attenuation must be minimized for frequencies up to several hundred MHz.

A complete layout was done assuming prototype (demonstrator) designs for the FE and MCC chips using standard design rules. (It is also based on an older module design which had 12 FE chips per disk module.) It was found that six metal layers were required to make the necessary connections. This hybrid was over 300 μm thick and did not meet the material budget constraints for the pixel module. We were then motivated to use a two-piece approach in which routing near the MCC is done on a separate flex circuit called the MCC Mount (MCCM) using the HDI rules. The MCCM is then mounted on a Flex Hybrid which is designed using standard rules. This approach has the advantage that each flex circuit required only two metal layers and the overlap area is minimized. Wire bond connections must be made to connect the two flex circuits. The layout of the Flex Hybrid is shown in Figure 3 and the layout of the MCCM is shown in Figure 4.

3 Performance Simulations

To estimate the performance of the flex hybrid designs, a transmission line analysis including calculation of attenuation and crosstalk was performed using the commercial software package Maxwell Spicelink [1]. This package does a finite-element calculation of electric and magnetic fields using the multipole method in order to extract the resistance, capacitance, and inductance of conductive circuit elements. The RCL values obtained can then be loaded into SPICE so that the circuit performance can be simulated.

In order to verify this method, a simulation was first done on an existing flex circuit of relatively simple geometry which was developed for the CLEO III

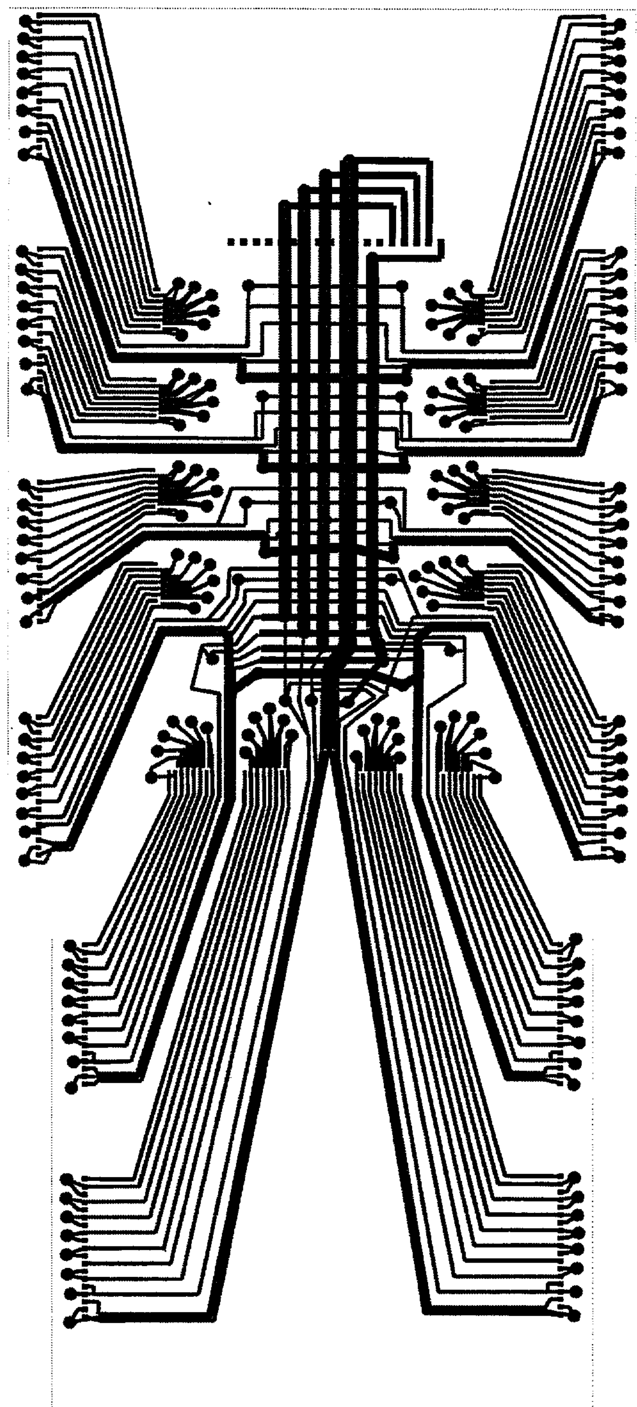


Fig. 3. Layout of the two metal layer Flex Hybrid using standard design rules.

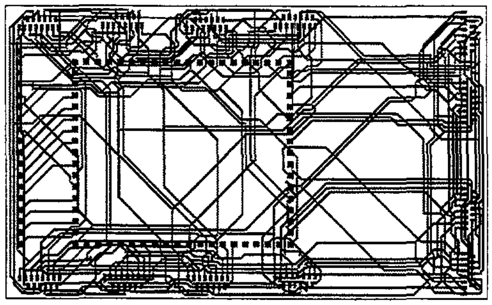


Fig. 4. Layout of the two metal layer MCCM using HDI (GECRD) design rules.

silicon microstrip detector [2]. We have established a collaboration between the University of Oklahoma and GECRD to develop the CLEO III flex circuits based on their existing high density interconnect process [3]. The flex design uses two metal layers patterned with traces on either side of a 25 μm Kapton substrate. Each side is coated with a layer of acrylic passivation 12.5 μm thick except for the area on top where wire bond pads are located. Traces are 30 μm wide and are made of 6 μm of Cu, 0.7 μm of Ni, and have 1.0 μm Au plating. A thin layer of Ti is sputtered on the Kapton before the Cu is applied to improve the adhesion of the Cu layer. The top layer (defined by the presence of bond pads) has 255 traces and the bottom layer has 256 traces. Via's with 25 μm square plated-through holes and 75 μm square cover pads are used to connect the bottom traces to bond pads on the top side. Bond pads are typically 170 μm x 60 μm.

The process, which is proprietary, uses a direct-write laser rather than conventional lithography to expose resist and thereby form the patterns. The laser is also used to construct the via holes through layers of Kapton. The total trace capacitance has been measured to be < 1 pF/cm and the trace resistance has been measured to be < 1.2 Ω/cm. The rate for defects such as non-continuous traces and shorts has been determined to be $< 0.1\%$ of all traces with about 50% of the circuits containing no defects [4]. Wire bonding

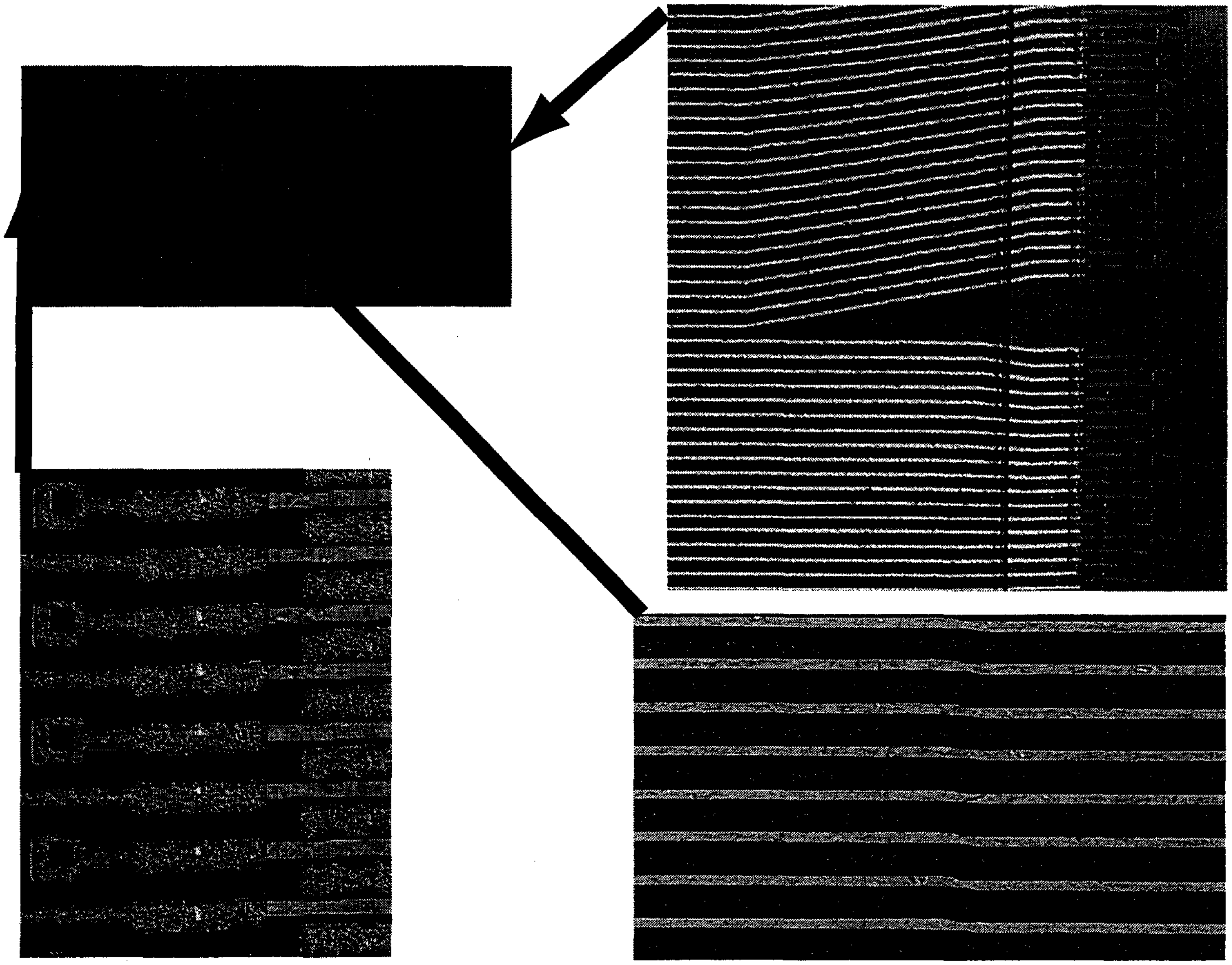


Fig. 5. Photographs of several key regions of a CLEO III production flex circuit.

to the flex circuits can be done easily with reasonable pull-strengths. The flex circuits are fabricated in a "frame" consisting of a single layer of Kapton stretched over a 17.5 cm inner diameter metal ring. A typical production flex circuit is shown in Figure 5. This process meets all the requirements for fabrication of the ATLAS MCCM design.

Simulation of the transmission line properties of a portion (up to seven traces) of the CLEO III flex circuit was done using the Maxwell Spicelink package and the results were compared to measurements. The method and results are described in detail in Ref. [5]. The Maxwell Extractor uses finite element analysis and the multipole method to extract RCL matrices for 3-dimensional structures and discontinuities. The extracted quantities can be exported directly in matrix format, or can be used to automatically generate SPICE models. In the simulation, a square wave clock signal with 2 ns rise and fall times was used as input to one ("active") trace. The attenuation (output voltage/input voltage) on opposite ends of the active trace and crosstalk (output voltage on neighboring trace/input voltage on active trace) were determined from the SPICE simulations as a function of clock pulse frequency. All traces were terminated by 50 Ω resistors although the expected characteristic impedance of the CLEO III geometry is expected to be $> 150\ \Omega$. This mismatch in impedance made the crosstalk and attenuation larger and easier to measure.

The attenuation and crosstalk were measured using a microprobe station and an HP 4194A impedance phase/gain analyzer. The measurements were dominated by noise for frequencies below 100 Hz and above 10 MHz. Figure 6 shows the minimum portion on the CLEO III flex circuit used in the simulations. Figure 7 shows the attenuation (in decibels) obtained from the simulations and Figure 8 shows the crosstalk on the nearest neighbor on the opposite side of the flex circuit. The X's in Figures 7 and 8 show the results of the measurements. Reasonable agreement is obtained between the simulations and measurements for frequencies between 100 Hz and 1 MHz where the measurements are most reliable.

Sections of the Flex Hybrid and MCCM designs were also simulated using the same methods as for the CLEO III flex circuit. A typical section of the Flex Hybrid is shown in Figure 9. In this case, LVD signal high is applied to

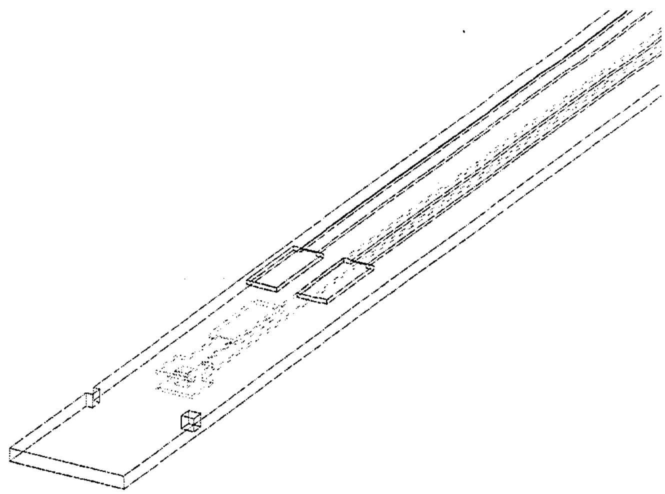


Fig. 6. The minimum portion on the CLEO III flex circuit used in the simulations.

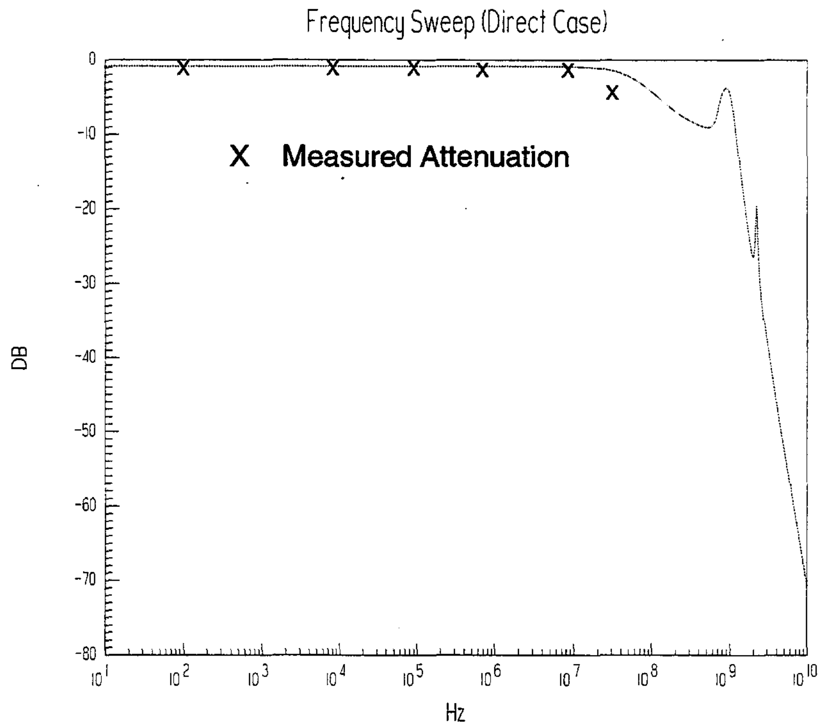


Fig. 7. The attenuation obtained from the simulations. The X's show the results of measurements.

the active trace and LVD signal low is applied to the trace on the opposite side of the two layer Flex hybrid. All traces are assumed to be terminated with 100 Ω resistors at both ends. Typical simulation results for the input and output (on opposite ends) for a 40 MHz clock pulse for signal high are

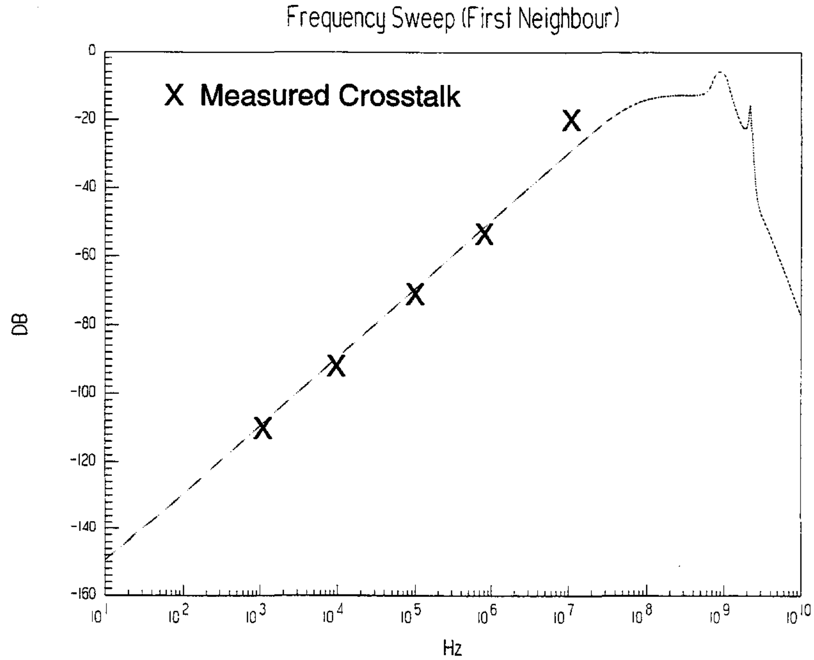


Fig. 8. The crosstalk on the nearest neighbor trace on the opposite side obtained from the simulations. The X's show the results of measurements.

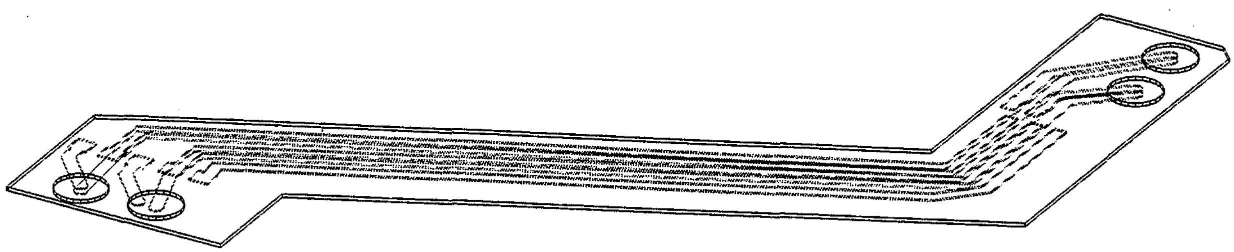


Fig. 9. A typical section of the two metal layer Flex Hybrid used in the simulations.

shown in Figure 10. The frequency dependence of the crosstalk on the nearest neighbor (same side) trace is shown in Figure 11.

A typical section of the MCCM is shown in Figure 12. Square wave clock signals were applied to the LVD high and low signal pairs as in the case of the Flex Hybrid. The MCCM has mostly co-planar LVD lines. Simulation results for the attenuation and nearest neighbor crosstalk as functions of frequency are shown in Figure 13. Figure 14 shows the phase change relative to the

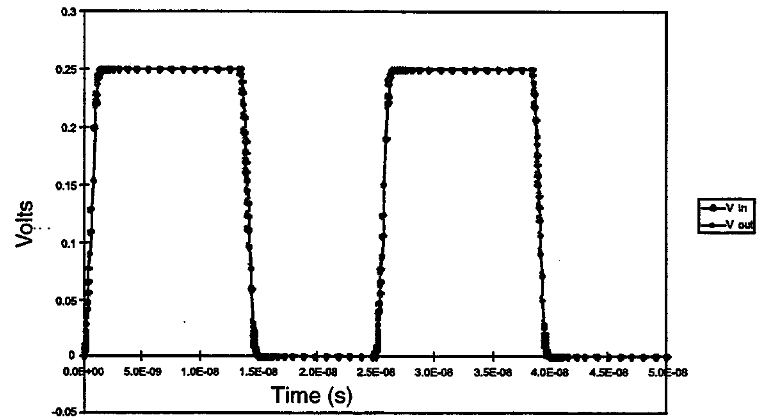


Fig. 10. Simulation results for the input and output (on opposite ends) for a 40 MHz clock pulse for LVD signal high on a Flex Hybrid trace.

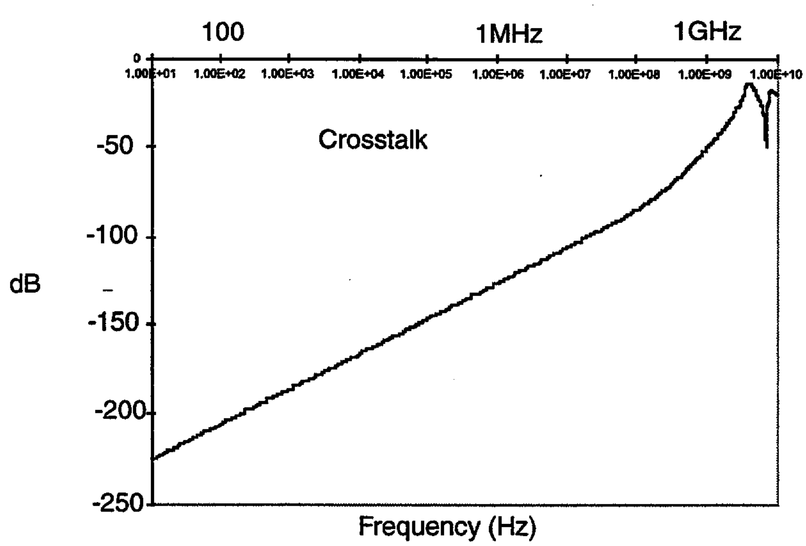


Fig. 11. Simulation result for the frequency dependence of the crosstalk on the nearest neighbor Flex Hybrid trace for LVD signal high.

generated clock phase for the active and crosstalk signals versus frequency. A large variation of phase change is observed above 5 GHz when the wavelength of the input pulse approaches twice the length of the trace as expected. Qualitatively similar results are obtained when portions of the Flex Hybrid and

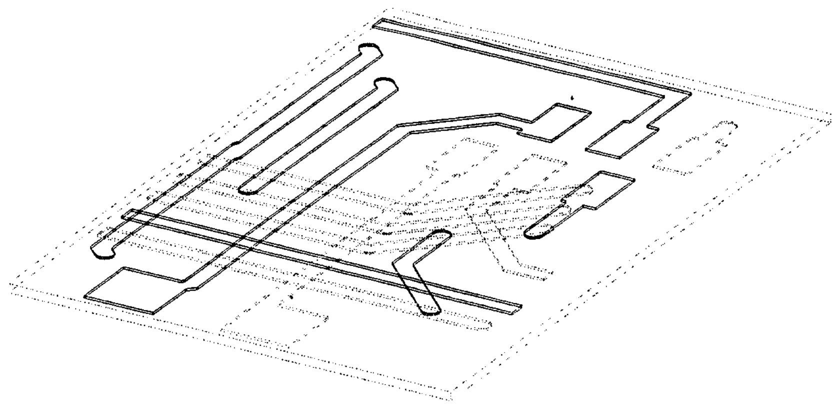


Fig. 12. A typical section of the two metal layer MCCM used in the simulations.

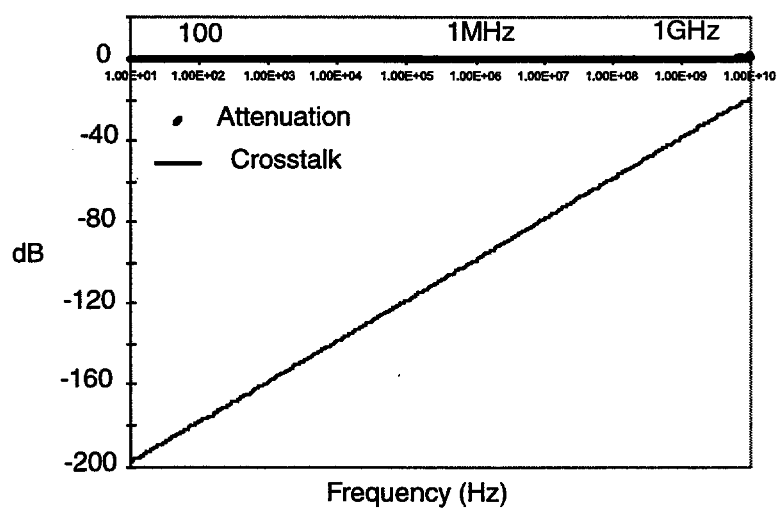


Fig. 13. Simulation results for the frequency dependence of the attenuation of the MCCM active trace and crosstalk on the nearest neighbor trace for LVD signal high.

MCCM are simulated simultaneously.

The simulation results for the two layer Flex Hybrid and MCCM show that the crosstalk on the nearest neighbor is less than -40 dB at 1 GHz and less than -60 dB at 40 MHz. Signal attenuation is negligible up to 500 MHz. Encouraged by these results, we have designed a prototype Flex Hybrid for fabrication as described in the next section. Evolution of the disk mechanical

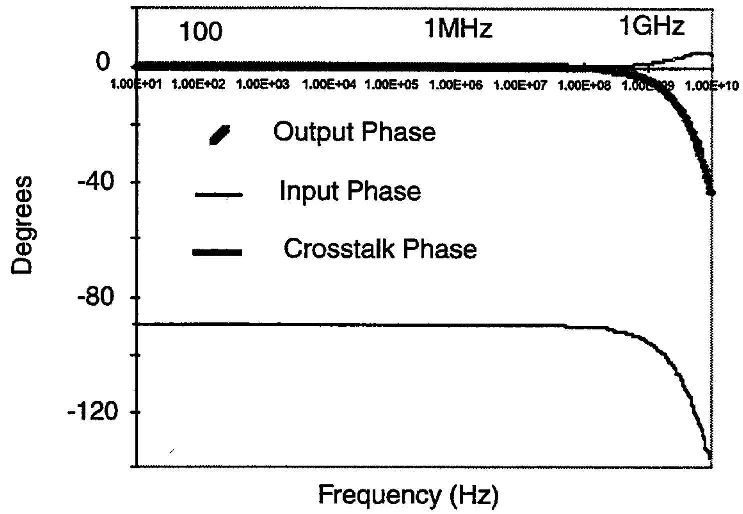


Fig. 14. Simulation results for the frequency dependence of the phase change of the MCCM active trace and the nearest neighbor trace for LVD signal high.

design has led to a solution which allows the same pixel module to be used in both the barrel and disk regions. The two metal layer monolithic Flex Hybrid described below can be used on this pixel module which was shown in Figure 1.

4 ATLAS Prototype Flex Hybrid

A prototype hybrid has been designed which will allow performance tests to be made in the CERN test beam. The prototype hybrid consists of a Kapton substrate with a thickness between 25 and 50 μm and with metal traces on both sides. Signal and power lines connect the wire bond pads at the edge of the module to wire bond pads near the MCC. The bottom traces are connected to the traces and bond pads on top with via's which have 70 μm diameter holes and 130 μm diameter cover pads. Both sides of the hybrid can be covered with a passivation layer except for the areas where bond pads are located. Power and ground lines as well as differential signal lines are placed

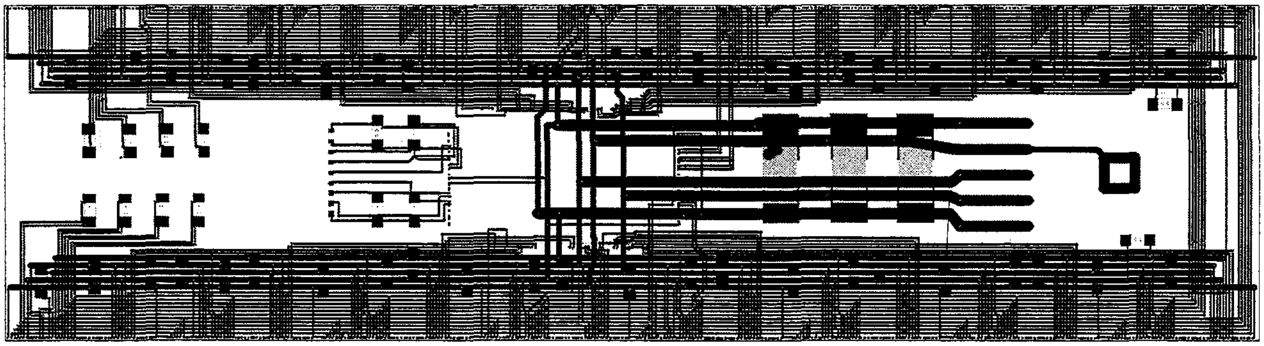


Fig. 15. Layout of both sides of the complete prototype Flex Hybrid.

parallel to each other on the same metal layer. Typical signal traces are 75 μm wide with 75 μm spaces between them. The Flex Hybrid also has passive components mounted directly on it including 12 termination resistors and 51 decoupling capacitors, although the number of decoupling capacitors may be reduced based on empirical testing. The present design calls for 0402 form factor SMD's (Surface Mount Device) for the discrete components, except for 3 tantalum capacitors, which are EIA size A. Figure 15 shows the layout of both sides of the complete prototype hybrid. The wire bond pads at the edge which allow connection to the FE chips have a pitch of 150 μm.

We are actively exploring options with several vendors including the one used for the flex connectors for the CLEO III project (GECRD), Dynamics Research Corporation (Wilmington, MA), and CERN. The first prototype will have Cu traces approximately 6 microns thick, with a barrier metal (e.g., Cr or Ni) and Au plating for the bond pads which is the same as that used for CLEO III. However, CERN has the capability to manufacture flex circuits with Al traces and that option will also be pursued.

5 Conclusion

Flex circuit designs have been made which provide required pixel module interconnections between front-end and module control chips and allow mounting of passive components such as decoupling capacitors and termination resistors. Material constraints favor high density, non-standard design rules which allow the routing to be done in two metal layers. Simulations indicate that the designs meet signal integrity requirements. Fabrication of a prototype Flex Hybrid during the next several months will allow full characterization of a complete pixel module during high energy beam tests.

6 Acknowledgments

I would like to thank my ATLAS colleagues for help in preparing this presentation. I also thank the organizers of Pixel '98 for a very enjoyable and productive workshop. This work is supported by the U. S. Department of Energy.

References

[1] Maxwell Spicelink, Ansoft Corporation.

[2] CLEO III Proposal CLNS94/1277 (unpublished).

[3] James C. Lyke et al., J. Microelectronic Systems Integration 1 (1993) 99.

[4] The flex circuits were tested in a class 10,000 clean room with a Signatone 261 microprobe station. The x, y, and z axes of the probe station were installed with stepping motors which were operated by Highland drivers and controlled by VME cards. A 486 PC computer running windows NT is used with National Instruments VXI and GPIB interfaces to automate the data taking.

[5] K. Neriyanuri, "ATLAS Pixel Detector High Density Interconnect Design and Testing of ASIC Analog Multiplexer", Masters Thesis, University of Oklahoma (1997).

CMS Forward Pixel Port Card: A Smart Interface between Pixel Readout and DAQ

R. Stone, E. Bartz, S. Schnetzer, S. Sherman

Rutgers University

Abstract

To coordinate the data acquisition of many pixel readout chips for the CMS Forward Pixel Detector, there will be a local, high-speed interface located relatively close to the readout chips. This interface, know as the Port Card, handles environmental monitoring, houses optical couplers for data transmission, and issues slow control commands to the pixel readout chips. One special function of the Port Card is to prevent data corruption due to sudden trigger overload conditions.

Overview of CMS Forward Pixel Tracker and Port Card

The CMS Forward Pixel Tracker consists of 2 modular disks of pixel detectors mounted on each side of the interaction region. Each disk is divided into sectors with 24 "blades". Each blade has sensors with attached readout chips mounted on both sides of the blade. There are approximately 12 x 10^6 piexls bump-bonded to 4,320 readout chips. A 15 cm long high density interface cable (HDI) handles the data, low voltage, slow control signals and readout sequencing lines from the readout chips (ROCs) to a Port Card.

The local control of the CMS Forward Pixel Tracker will be provided by the Port Card. This is a low-mass PC board that will be situated at the outer radii of each blade. It will interface the front-end Readout Chips (ROC's) with the Front End Digitizer (FED) and the Front End Controller (FEC) modules of the CMS DAQ System. There will be two Port Cards per blade; one card controlling the entire side of a blade. The Port Card and its associated electronics provide the following functions:

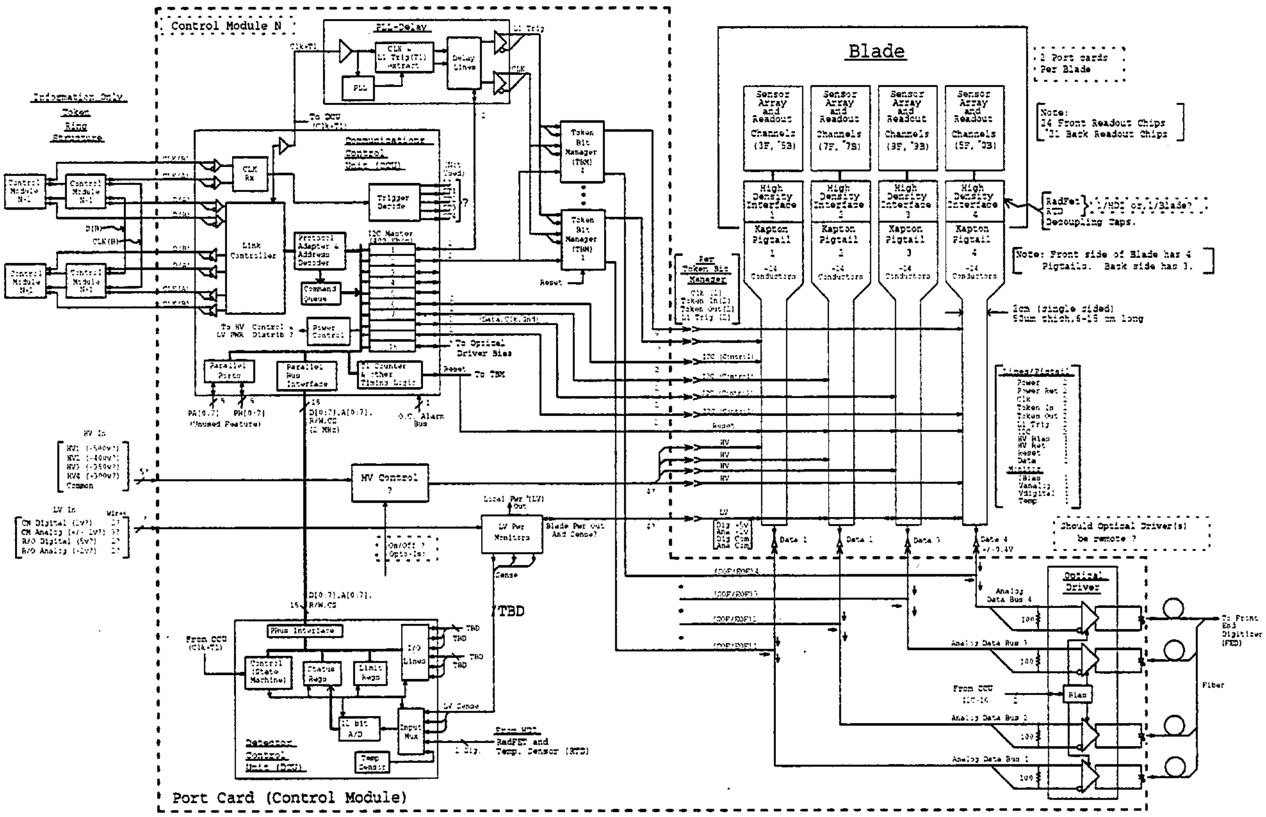
- send phase adjusted Clock and Level 1 Trigger signals to the Readout Chips
- send slow control signals (set pixel thresholds, enable/disable readout, calibration, etc.) to the Readout Chips
- monitor the temperature, bias current and low voltage levels of each blade
- provide a location for the optical link transmitters which will send the analog pixel data (pulse height, address and event number) via optical fiber to the Front End Digitizer
- distribute the sensor bias voltages
- issue hardware resets to the Readout Chips
- manage the readout by initiating and terminating a readout token pass
- temporarily suspend readout if there is a local trigger pile-up
- write Start of Frame and End of Frame records to the FED for each token pass

Port Card Design Details

The Port Card consists of the following major components: a Communications Control Unit (CCU), a Phased Locked Loop (PLL), a Detector Control Unit (DCU), four Token Bit Managers (TBM's) and a set of four optical-link drivers and laser transmitters. These are shown in a layout diagram of the Port Card in Figure 1. The CCU, DCU and PLL are custom ASIC's that are currently under design and development by the CERN/ECP division for the CMS Tracker.[1, 2] The TBM, on the other hand, is a custom chip that must be developed specifically for the CMS pixel system for use by both the disks and the barrel. The optical links are under development by the CERN/ECP division and will also be used by the CMS trackers and calorimeters for transmitting data.[3, 4, 5] All components must be radiation hard.

At the Port Card, there will be one Token Bit Manager and one optical driver for each HDI cable. Upon receipt of a Level 1 trigger, the TBM will send a token bit down the HDI which will be passed along among a group of front end chips. Upon receipt of the token bit, each chip will send its data directly to an optical-link driver via a data line on the HDI. Once a Readout Chip receives the token bit, the readout is automatic with no further intervention required.

Below, we describe each of the four custom ASIC's needed for the Port Card.



Block Diagram of the Port Card

Figure 1: Block diagram of the port card

Communication Control Unit (CCU)

The CCU ASIC is the master control unit. It performs the following functions:

- receives control commands from the Front End Controller (FEC)
- receives the Clock and Level 1 signals from the FEC
- issues slow control commands to the Readout Chips
- issues control commands to the TBM
- interfaces to the PLL and DCU
- sets the threshold bias of the optical-link drivers.

The CCU communicates with the DAQ via a token ring structure shown in figure 2. It communicates the slow control signals to both the TBM and to the Readout Chips via I^2C

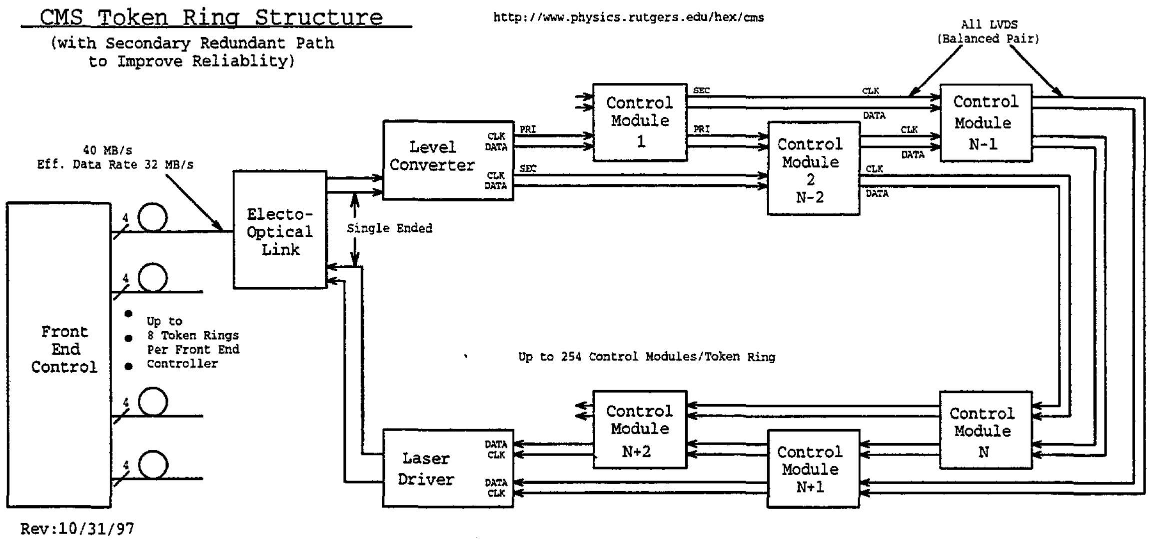


Figure 2: CMS Token Ring Structure

ports which is an industrial bus standard used for slow control. As currently designed, the CCU contains 16 I^2C master ports which are more than the number needed for the Port Card functions as indicated in figure 1.

Detector Control Unit (DCU)

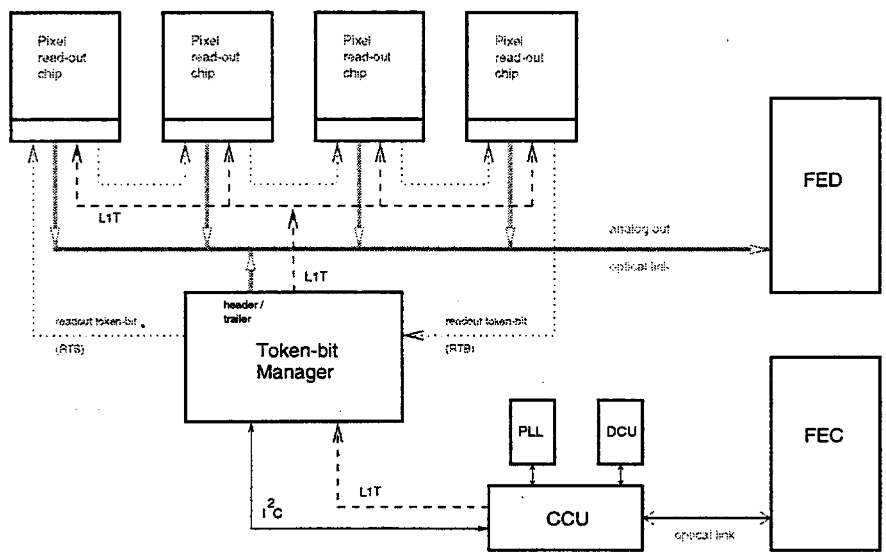
The DCU ASIC will have the function of receiving input monitoring signals and issuing alarms if these inputs exceed certain specified ranges. For the forward pixel disks, the DCU will monitor the temperature, low voltage levels and bias current of each plaquette. The chip will be designed and developed for use by the entire CMS tracking system. Although the design of this chip is not finalized, it is envisioned that it will contain a 12-bit ADC which can address several sources via an input multiplexer. There will be an internal state machine that will perform repetitive measurements on selected inputs signals and compare them with a set of limit registers. When one of the monitored inputs exceeds the set limits, an alarm will be sent to the external FEC via the CCU. The DCU will communicate with the CCU via a parallel bus interface.

Phase Locked Loop (PLL)

The PLL ASIC will supply phase-adjusted Clock and Level 1 trigger signals to the reaout chips. It receives a signal from the FEC via the CCU consisting of a coded Clock plus Level 1 signal. It decodes this signal and separates the Clock and Level 1 signals onto two separate lines and sends them to each of the four Token Bit Managers for distribution to the ROCs. The timing phase of the Clock and Level 1 are set by a programmable delay. The Clock output can be shifted in steps of 1 ns and the Level 1 signal can be shifted in multiples of the clock period.

Token Bit Manager (TBM)

The TBM is a custom ASIC that needs to be specially made for the pixel systems (both barrel and forward pixel detectors). Its primary function is to manage the local readout by initiating a token bit pass among a group of Readout Chips when a Level 1 trigger is received and by monitoring the return of the token bit. It is needed to deal with the situation in which the readout of a local area of the detector is momentarily not able to keep up with the trigger rate due either to a locally large concentration of hits due to jet events or local noise hits. A separate function of the TBM will be to write the Start of Frame and End of Frame data records for each data stream associated with a token bit pass. It will also keep track of the event number and pass this information to the DAQ in the Start and End of Frames.



Pixel Read-Out Using Token-Bit Manager

Figure 3: Pixel read-out using the Token-Bit manager.

A schematic of the TBM is shown in figure 3 and a functional block diagram is shown in figure 4. Upon receipt of a Level 1 trigger from the PLL the TBM will:

- increment a 6-bit event counter
- increment a trigger stack.

If the trigger stack is not full (less than 8), it will then:

- issue the Level 1 trigger to the group of readout chips
- increment a 3-bit trigger counter
- wait until all previous queued readout is finished

- write a Start of Frame header on the data line
- issue a readout token bit to the Readout Chips.

When a readout token bit returns, it will:

- write an End of Frame record on the data line.

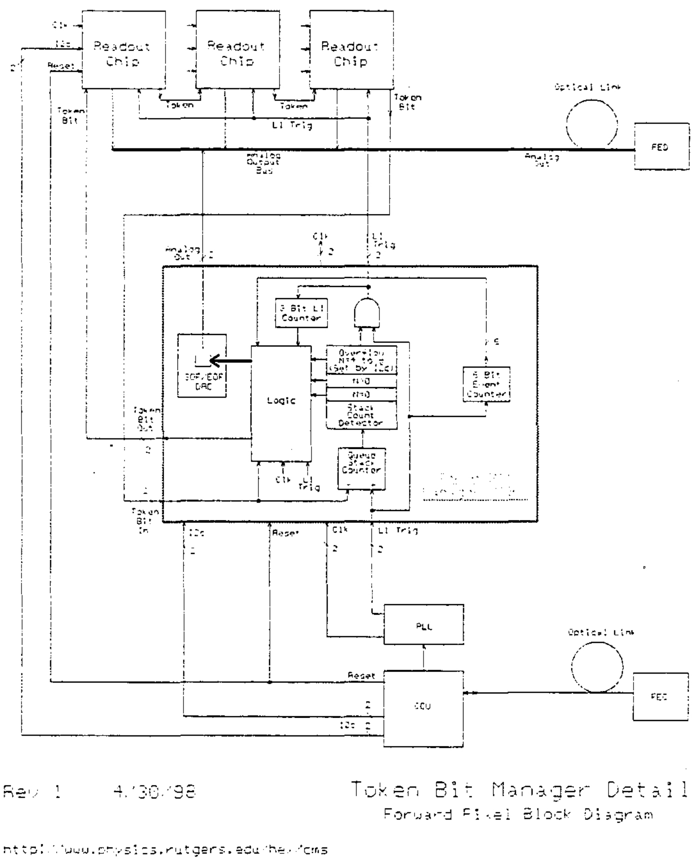


Figure 4: A diagram of the readout subsystem detailing the Token Bit Manager.

The format of the Start of Frame and End of Frame records is not yet specified. However, these records will contain both the current 6-bit event counter and the 3-bit trigger counter. Each of the Readout Chips will also contain 3-bit trigger counters which are incremented whenever they receive a Level 1 trigger from the TBM. The contents of the Readout Chip trigger counters will then be identical to the contents of the trigger counter in the TBM. When a readout chip writes its data, it associates the data with a particular trigger by writing the trigger counter as a 3-bit coded analog signal. By reading the Start of Frame header, the FED can then unambiguously associate the 3-bit trigger number received from the Readout Chip with the global 6-bit event number. Note that 3-bits are sufficient for the trigger number since the TBM will not allow more than 8 unserviced Level 1 triggers to be outstanding. The End of Frame will contain the current 3-bit trigger counter. Comparison of this trigger number with the trigger number in the Start of Frame will inform the FED of how many event triggers are contained in the readout pass. Note that when a Readout Chip receives a token bit it will write out the data for the trigger associated with the token along with any data from a later trigger that may exist.

We have had discussions with Honeywell on production of the TBM chip. Since it will be located at the end of the blades at about 15 cm from the beam line it must be implemented in a radiation hardened process such as the Honeywell SOI process. The digital portion of the chip can be implemented on an existing Honeywell gate array, HX2040. This array has 27,000 usable gates which are far more than the approximately 1000 gates needed for the TBM. Since the TBM will need to write analog data, namely, the Start and End of Frame records, it will need a radiation-hard high-speed DAC.

We are investigating several options for implementing this analog function. One would be to produce a separate analog chip containing a DAC developed by another group. The Readout Chip itself will need a high-speed DAC for sending the trigger counter number. Since both the Readout Chips and the TBM will talk to the same data line, these DAC's and associated drivers should be identical. A second option, if the design for this DAC were to exist in a Honeywell process, would be to incorporate it as an embedded or "dropped-in" cell as part of the digital TBM chip. This can be done at a reasonable cost by Honeywell.

References

[1] CMS Tracker Technical Design Report, Section 5.6

[2] A. Marchioro, A system for Timing Distribution and Control of Front End Electronics for the CMS Tracker, Proc. 3rd Workshop on Electronics for the LHC Experiments. CERN/LHCC/97-60 (1997) 208.

[3] CMS Tracker Technical Design Report, Section 5.4

[4] G. Hall *etal.*, Fibre optic link technology for the CMS tracker, Technical note CMS Note 1996/012, Dec. 1996.

[5] F. Vasey *etal.*, Laser based optical links for the CMS tracker, options and choices, Technical note CMS Note 1997/053, Jul. 1997.

Bump Bonding for ATLAS

M. Gilchriese
Lawrence Berkeley National Laboratory
on behalf of the ATLAS Collaboration

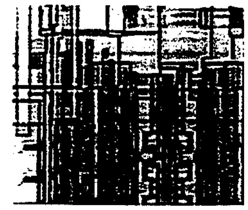
May 1998

Outline

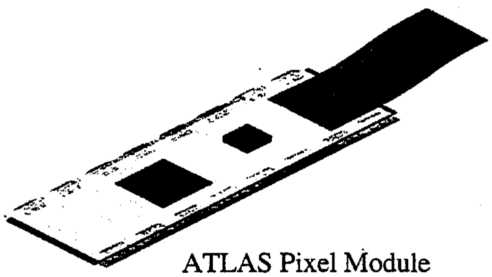
- ATLAS bump bonding requirements
- Prototype program plan
- Prototype results
- Vendor summary
- Outstanding issues
- Conclusions

ATLAS Bump Bonding Requirements

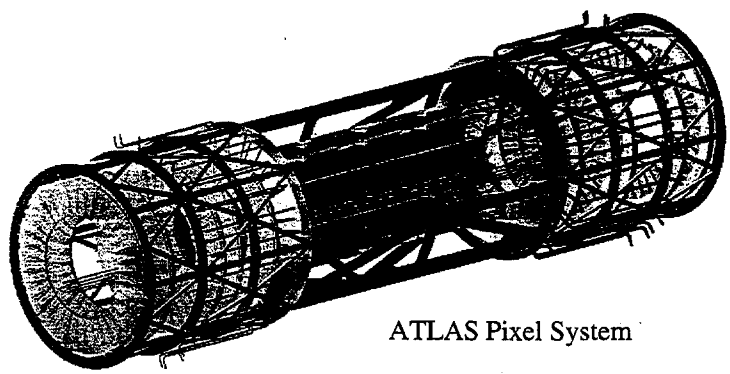
- Number of bumps/placements
  - 2228 modules
  - 16 front-end chips per module
  - 35648 front-end chips => placements(+ yield losses)
  - 24x160 pixels per chip
  - 1.4 x 10^8 channels => bumps (+ yield losses)
- Bump spacing and size
  - Spacing currently 50μ in both x and y(center-to-center)
  - Sized for good yield and no shorts(roughly 20μ diam.)
- Wafers
  - 4"(for silicon detectors, which have "backside" processing), 250-300 microns thick (desire some small percentage to be 200 microns thick for innermost layer).
  - 6" for front-end integrated circuits(standard thickness, will thin later)



Bump bond pads on ATLAS prototype front-end B IC



ATLAS Pixel Module



ATLAS Pixel System

3

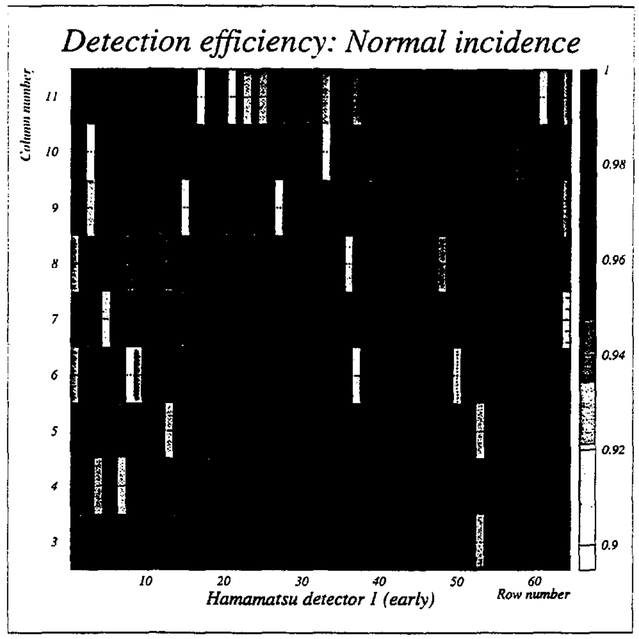
ATLAS Prototype Program

- Bump bonding of active silicon detectors and front-end ICs
  - Supports detector and electronics testing
  - Also see if bump deposition process affects detector properties(including after irradiation)
- Bump bonding of dummy parts
  - Bump deposition on dummy wafers(4" only so far)
  - Replicate bump pattern expected on detectors and ICs but connected to allow simple continuity tests to be made after flip-chip assembly to assess yield
  - Much cheaper than active parts, can do many more
- Thinning and dicing of bumped wafers
  - Require IC wafers to be thinned to 150 microns
- Verification of mechanical properties of bumps(tensile and shear strengths)
  - Dummy parts first
- Understand impact of stresses induced by mounting to mechanical structure
  - Coefficient of thermal expansion mismatch (although small) => thermally induced stress and creep
- Indirectly support bonding to alternatives to silicon eg. diamond(not discussed here).

4

Bump Bonding of Active Components

- Have successfully bump bonded silicon detectors to ICs with good yield at Boeing(indium, USA), IZM(solder, Germany), LETI/Tronics(solder, France).
- Some dozens of single-chip assemblies have been completed, and a few 16 chip modules have been done or are just about to be done.
- Number of devices is too small to characterize yield, but it's easily good enough to allow testing of ICs and detectors.
- Devices have been tested over the last year or so for ATLAS in test beams.



Efficiency of single-chip assembly

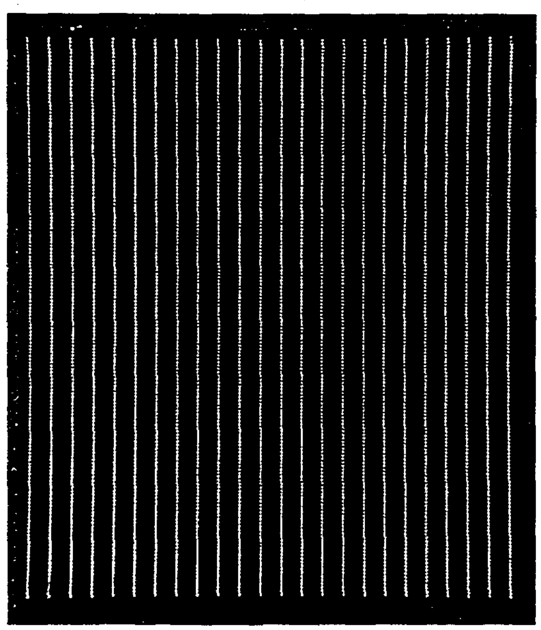
5

M. Gilchriese LBNL May 9, 1998

Bump Deposition on Dummy Components

- Four inch dummy wafers (of slightly different types) have been made by LBNL, CIS(Germany) and Seiko(Japan).
- Bumps have been deposited on these wafers (different vendors used different wafers) by
  - Alenia(indium, Italy)
  - Boeing(indium, USA)
  - Diamond Tech One(indium and solder, USA)
  - IZM(solder, Germany)
  - Seiko(solder, Japan)
  - Tronics(solder, France)
- Visual inspection of the bumped wafers has shown that the defect rate (largely missing bumps apparently from photoresist defects - my guess) is better than 10^{-4} (typically a few x 10^{-5}) except for Diamond Tech One (which was unacceptable).

6



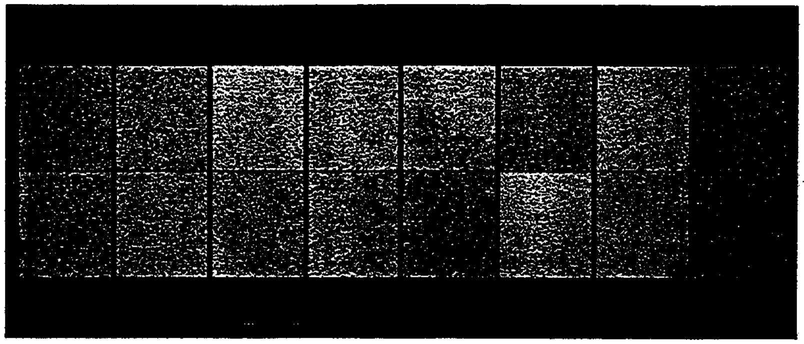
Dummy IC chip from Boeing

M. Gilchriese LBNL May 9, 1998

Flip-chip Assembly of Dummy Components

- The bumped dummy wafers have been used to make dummy, 16-chip modules.
- Boeing, Diamond Tech One, IZM, Seiko and Tronics have all assembled 16-chip modules. Alenia is in the process of doing so. A 16-chip module using parts from Boeing was assembled by UC Davis also.
- Continuity tests have been done on modules made by Boeing, IZM and Seiko.
- The number of modules measured is small, too small to allow one to separate the yield of flip-chip assembly from the bump deposition yield. However, the measured defect rate on these 16-chip modules(from loss of continuity) is less than 10^{-4}, which is acceptable.

Dummy 16-chip module assembled by Boeing



M. Gilchriese LBNL May 9, 1998

Mechanical Tests

- Only very preliminary mechanical tests have been done.
- Very rough measurements have been made of the strength in tension and shear. For about 3800 bumps, each 20-25 microns in diameter
  - Minium strength in tension and shear for indium bumps is about 2.5 lbs
  - Solder is stronger, and the minimum strength in tension(shear) is about 14 lbs(10 lbs).
  - These are very rough numbers. Strength depends on strain rate, other factors and can easily be different by factors of two or more. More tests are needed, or more vendor data.
- We have also done preliminary tests of the effect of cooling dummy modules from room temperature to -20°C while they are attached to simulated mechanical supports.
  - Temperature cycling tests(up to 15 cycles) have been done for both solder and indium dummy modules with different attachment schemes, including rigid attachment. No changes have been observed so far.
  - We have also started creep tests by keeping modules at the lower temperature (in a vertical position). No changes seen so far for indium after four weeks, tests are continuing
- Bottom line. Strength looks adequate so far. Thermally induced stresses appear to be tolerable.
- Just in case, one 16-chip module was assembled with underfill. We would like to avoid this because of possible interaction with the detectors(not known to be a problem, but why use it if not necessary). However, if strength problems do appear, this is a possible option.

Vendor Summary and Status

- Bump Deposition and Flip-Chip Assembly - Prototypes Made
  - Alenia - work in progress. Flip-chip currently outside company but will have inside capability soon. Can do both 4" and 6" wafers.
  - Boeing - corporate decision to no longer do bump deposition for outside customers. Still open to flip-chip assembly.
  - IZM - work in progress. All work done inside. Can do both 4" and 6" wafers.
  - Seiko - decision to abandon 4" wafer bumping line(only 6" supported). Am told other Japanese companies same.
  - Tronics - work in progress. All work done inside. Only 4" wafers at present. Need to get 6" capability.
- Bump Deposition and Flip-Chip Assembly - Contacts Underway
  - AIT - both solder and indium. All work done inside. Can do both 4" and 6" wafers.
  - Rockwell Science Center - indium. All work done inside.
  - In house at LBNL - transfer of Boeing bumping process to LBNL(no flip chip capability)
- Bump Deposition and Flip-Chip Assembly - Failed
  - Diamond Tech One
  - MCNC
- Bump Deposition and Flip-Chip Assembly - Not Capable/Not Interested but Contacted
  - Amkor
  - Aptos
  - Flipchip Technology
  - IBM(USA)
- Flip-chip Assembly - Not Capable/Not Interested but Contacted
  - Flextronics
  - Multichip Assembly
- Preliminary pricing information obtained from some vendors.

Outstanding Issues and Future Work

- Outstanding issues
  - Impact of bumping process on irradiated detectors. Bump detectors irradiated at LBNL, preliminary measurements made at New Mexico. Looks OK but need more statistics. In progress.
  - Possibility for rework. Is this possible at all? Everyone knows that the chip yield must be very, very high to have 16-chip modules with high yield, and burn-in is not possible. Alenia says they will study rework. No results. Very tough.
  - Improved inspection
    - Inspection after bump deposition so far done by eye. This works pretty well, but a number of different automated systems (3D profilers) exist and are in use in the bumping industry. We have contacted a few vendors and have had one do a dummy bump map. It's beautiful but expensive. Looking for cheaper alternative. Not clear it's needed but would be nice to have if cheap.
    - Inspection after assembly. Just started investigation of X-ray and ultrasonic scanning.
  - What is real yield?
- Future work
  - More active components are in the pipeline, including first 6" IC wafers
  - Need to assess results later this year and decide how to proceed on both real wafer and dummy wafer work.

Conclusions

- Proof-of-principle that bump bonding meeting ATLAS specifications with good yield has been obtained with multiple vendors.
- Sixteen-chip modules have been assembled by multiple vendors.
- Mechanical properties of assembled modules appear so far to be adequate to allow handling, etc and thermally-induced stresses that will result from mounting on mechanical/cooling structures appear tolerable.
- Both indium and eutectic solder appear to be viable candidates for ATLAS.
- We have a lot of work to do to go from our current prototype stage to production with good yield!

Flip Chip Bump Bonding at UC Davis

Gary Grim, Chris Hill, Richard Lander

Why is an academic Inst. doing this industrial work?

It goes back to D. Pellett's involvement in D. Nygren's SSC pixel group.

Key pieces of the pixel problem:

Readout electronics - LBL doing that.

Hybridization - No one doing much.

Sensors - We didn't worry about it at the time.

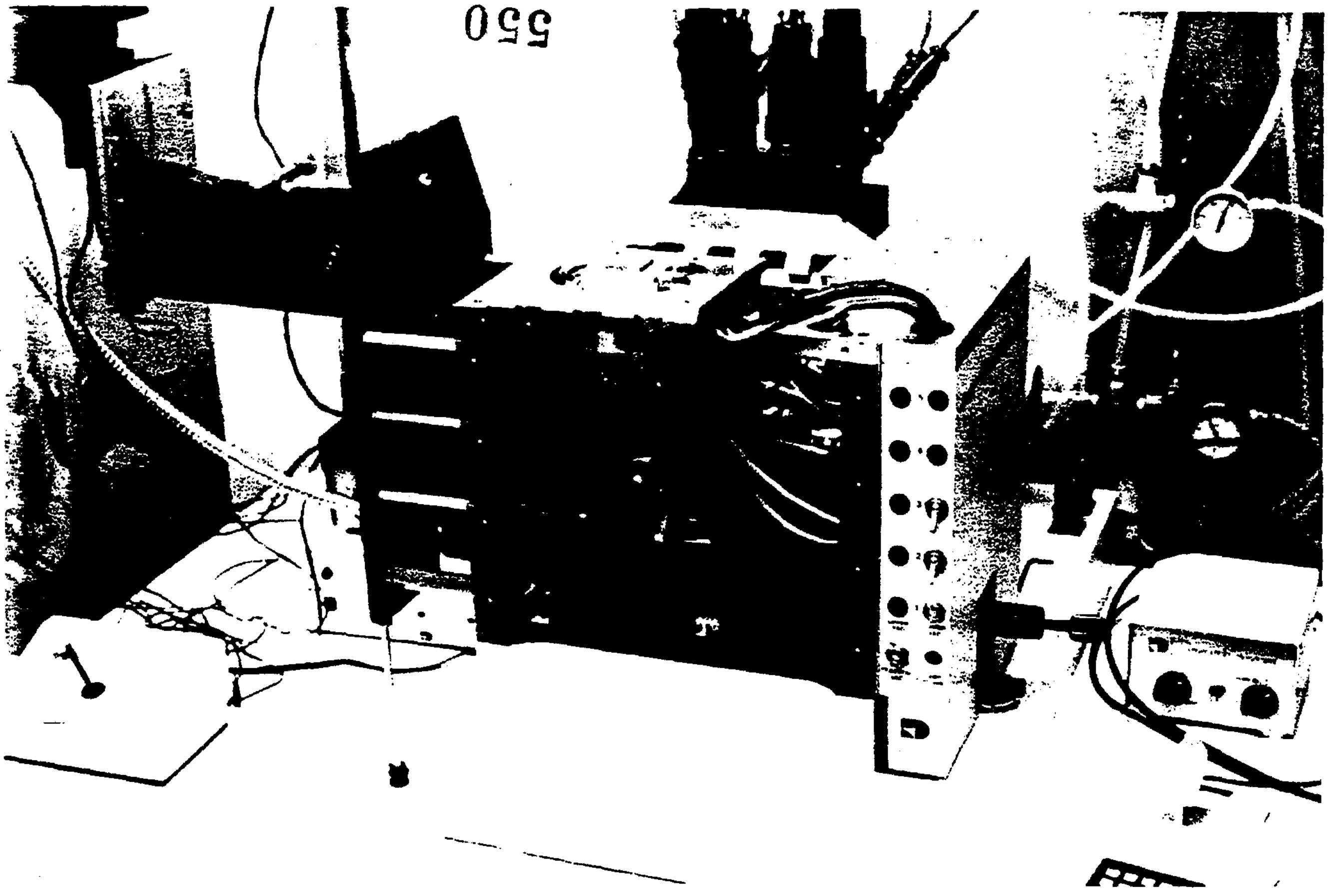
So we started with hybridization.

DOE grant from University Research Instrumentation Program

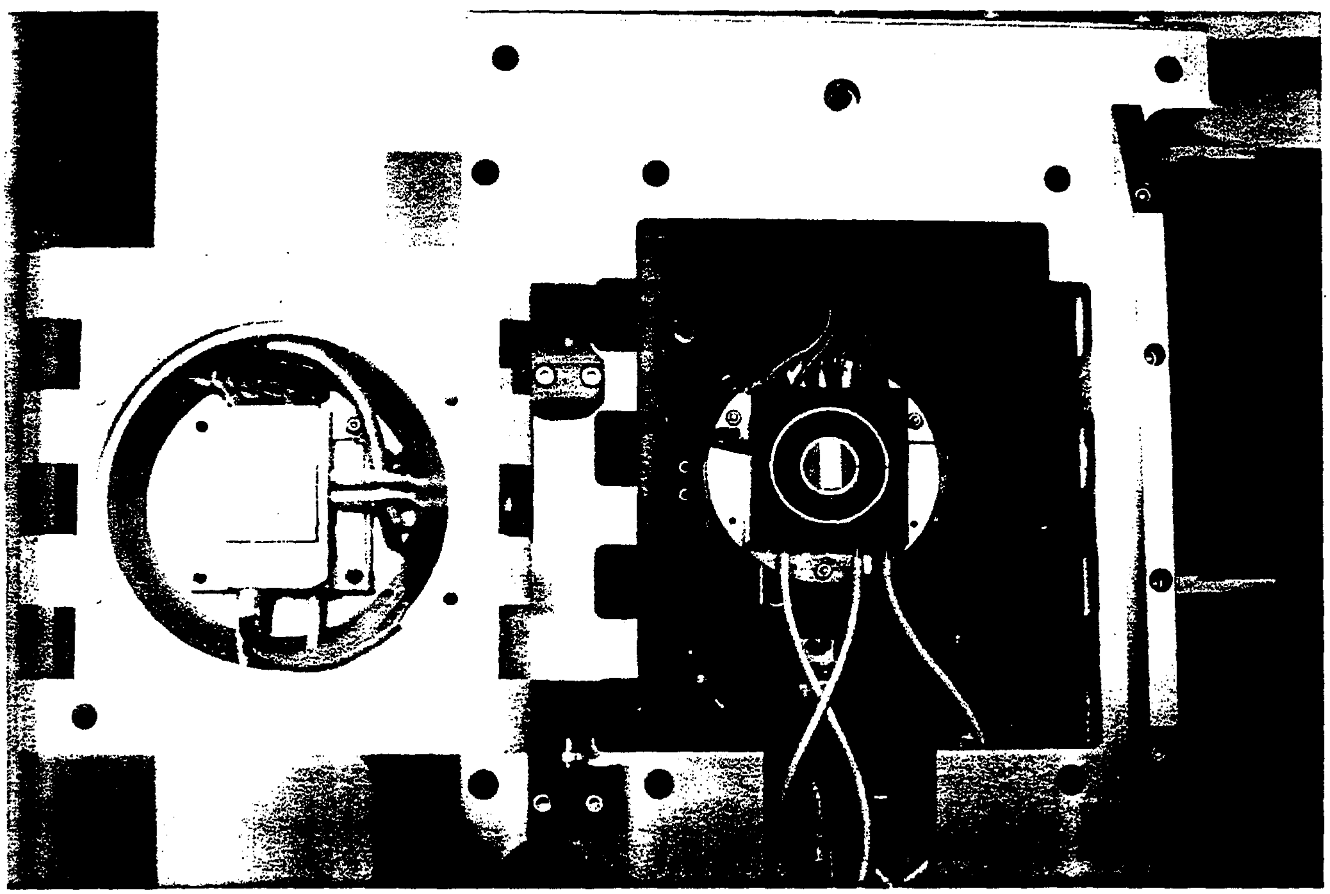
Bonder, Clean Room, Test Equipment

549

BONDING LAB - UCD



TOP CHUCK FLIPPED OPEN



Then....

SSC died $$
$
$
$
Slow Progress

But...

CMS ⟹ Pixels   UCLA meeting - Nygren   3/95
                 PSI meeting - Pellett   6/95

→ USCMS takes on foward pixels

→ UCD responsible for - forward pixel readout (with PSI)

- hybridization

551

But....readout will need a sensor to fully test

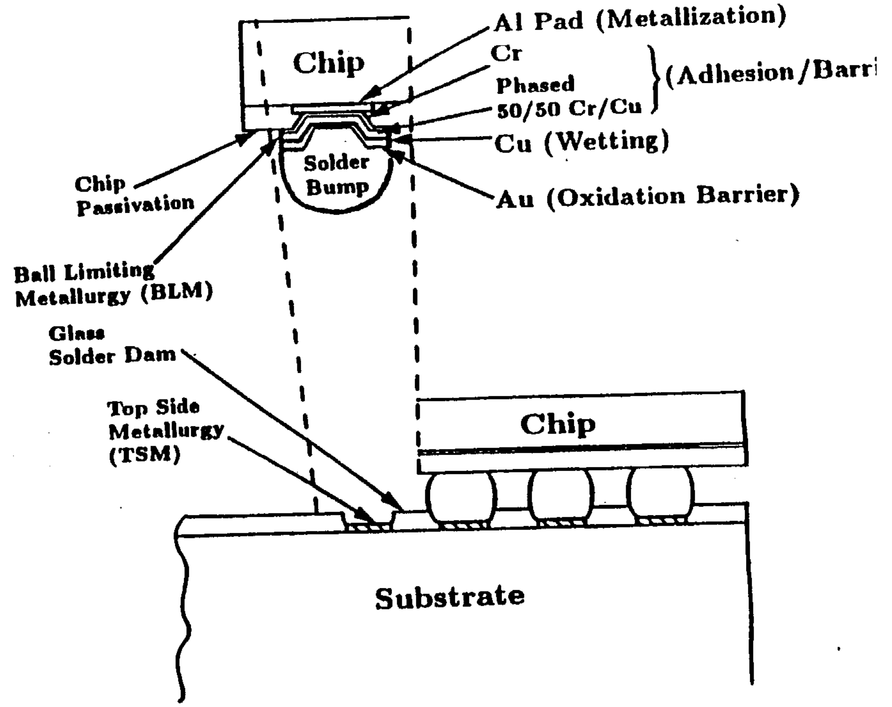
6/96 ---> BNL for sensor fabrication

- So we wound up involved in all three pieces

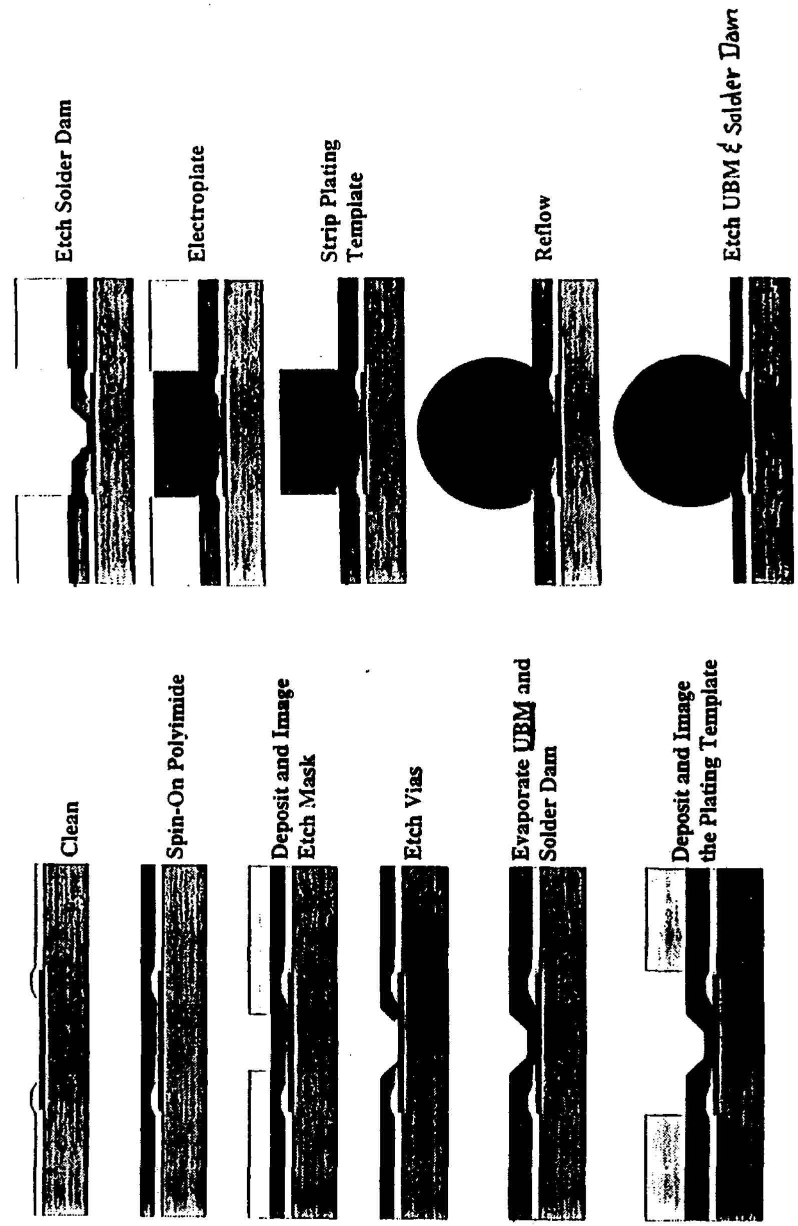
You heard about Column Architecture..........G. Grim

and Sensors.....................G. Bolla

- Now a few words about flip chip bump bonding



IBM C4 PROCESS
Pb/Sn Solder



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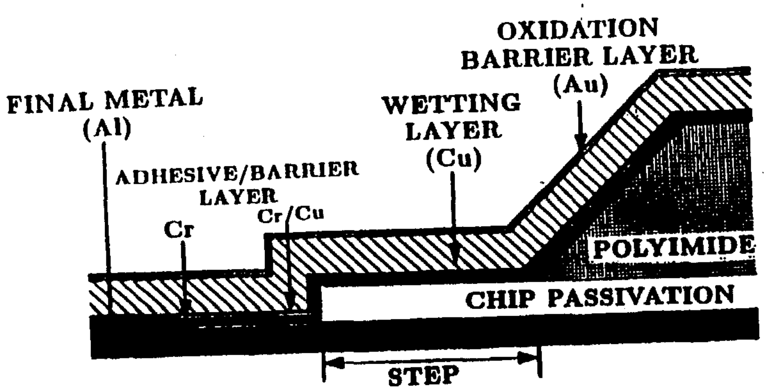
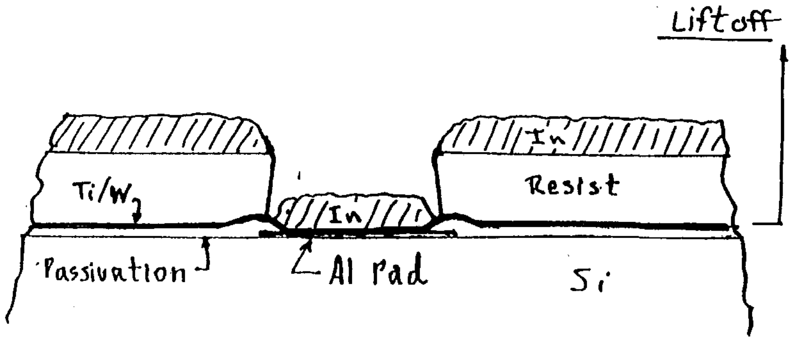


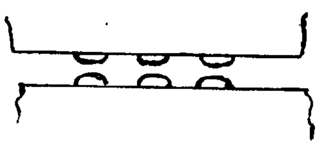
(b)

IBM's C4 (controlled collapse chip connection) technology; (*b*) IBM's ball-limiting metallurgy structure.

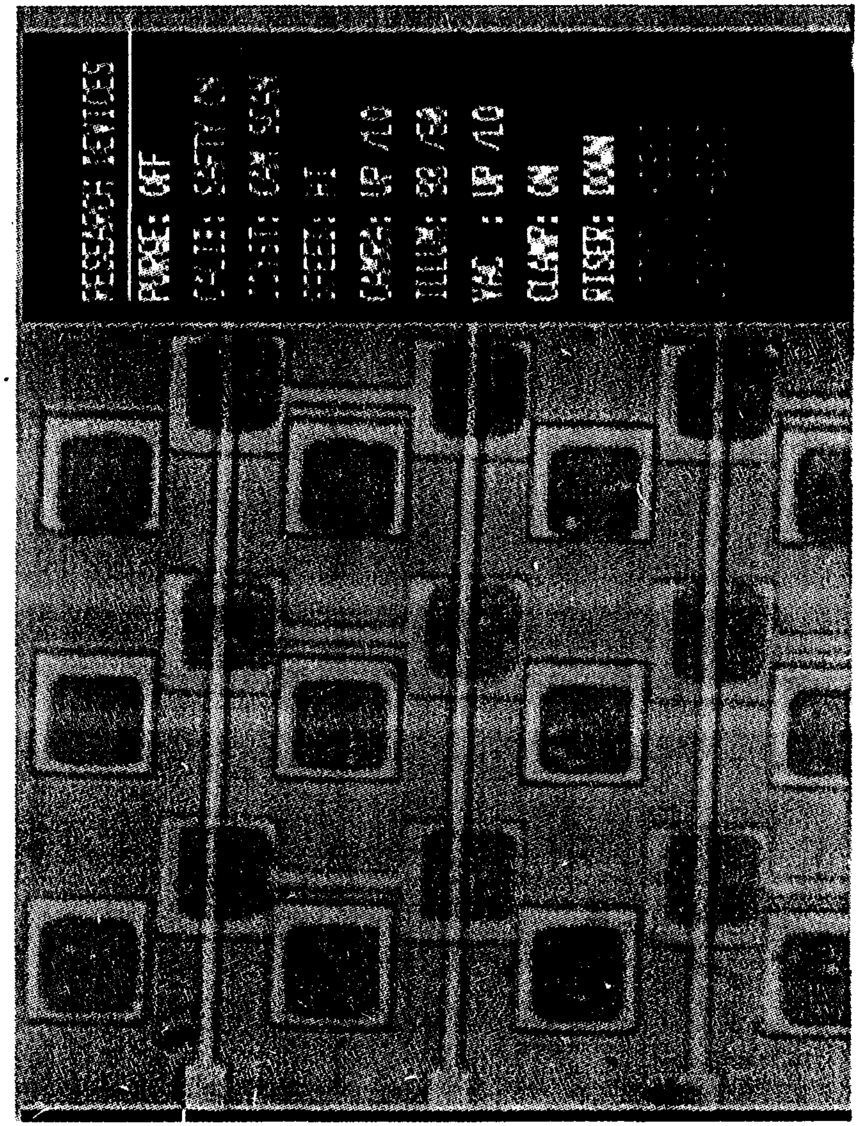
Bumps on both chips



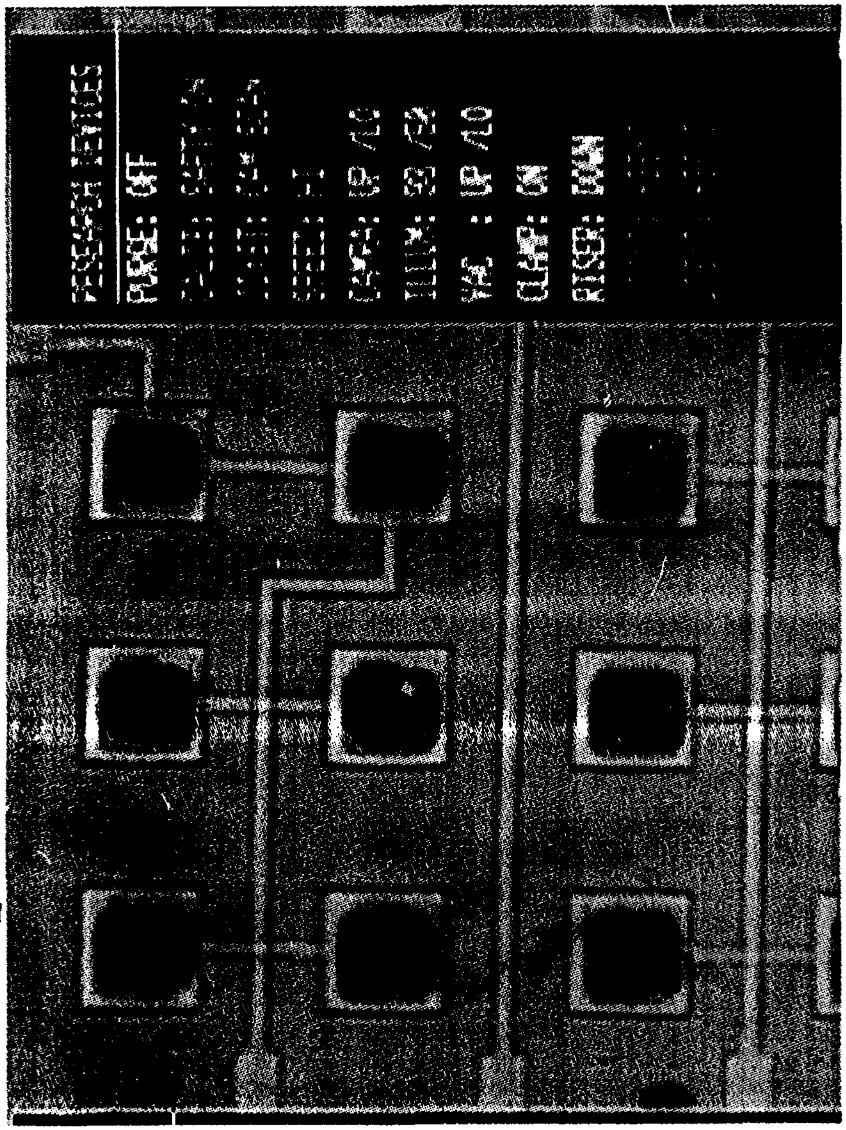
Clean
Deposit UBM (Ti/W)
Deposit resist and pattern it (etch)
Deposit indium
Lift off resist and excess indium
Selectively etch excess Ti/W



COLD WELD



BUMPS BEFORE ALIGNMENT



TECHNICAL CONSIDERATIONS

CAPACITANCE .... LOW
SMALL BUMPS

THERMAL CONDUCTANCE .... HIGH

RESISTANCE .... LOW

TEMPERATURE STRESS....... -10º C

MECH. STRENGTH ..... REASONABLE

YIELD PER BUMP .... VERY HIGH

CONNECTIVITY TEST

40X40 μm^2 BUMPS
100 μm pitch [AIT]

> 100 FLIP CHIP ATTACHMENTS,

PRESSURE	2 mg/μm^2
TEMP.	25 - 40 ^oC
TIME	60 SEC.

>10,000 INTERCONNECTS MEASURED

RESISTANCE < 1 OHM

CONNECT YIELD (99.78% +- 0.06)%

==> 99.7%, 95% CL

[RD19, Lisbon]

AN INDIUM ALLOY

IN/SN/AG ALLOY (w/ LBL)

10 FLIP CHIP ATTACHMENTS
> 5400 INTERCONNECTS MEASURED
20x20 μm^2

PRESSURE	15 -20 mg/μm^2
TEMP.	25 - 40 ^oC
TIME	60 SEC.

CONNECT YIELD >99.9% (0/5400)

-20 ^oC & 100 G's AT 2 KHZ,

OTHER BONDING

15

RESISTIVE TECHNOLOGY INC.

- AU STUDS ON MULTILAYER ALUMINA SUBSTRATE
- AU PLATED BUMPS ON CHIPS
  HEAT, HIGH PRESSURE

- AU STUDS ON MULTILAYER ALUMINA SUBSTRATE
- IN/PB BUMPS ON CHIPS
  ROOM TEMP, HIGH PRESSURE

PLANAR TECHNOLOGY OF AMERICA

-ANISOTROPIC CONDUCTIVE FILM
  ROOM TEMP, HIGH PRESSURE

HEWLETT/PACKARD

-QUARTZ - POLY - METALLIZED Si
  ROOM TEMP, LOW PRESSURE
-TRANSFER Si STRUCTURES
  ROOM TEMP, MOD. PRESS

556

16

BUMP GROWING FACILITY

● - EVAPORATOR SYSTEM SETUP

PRIMEX X-RAY IMAGER

ORBIT TI/W UBM 4-INCH WAFERS

- DEPOSITED BUMPS
  $18X30\ \mu m^2$
  60,000/CHIP
  $1X3\ CM^2$ CHIP PAIRS
- BONDED $1X3\ CM^2$ CHIPS
- GOOD IMAGES

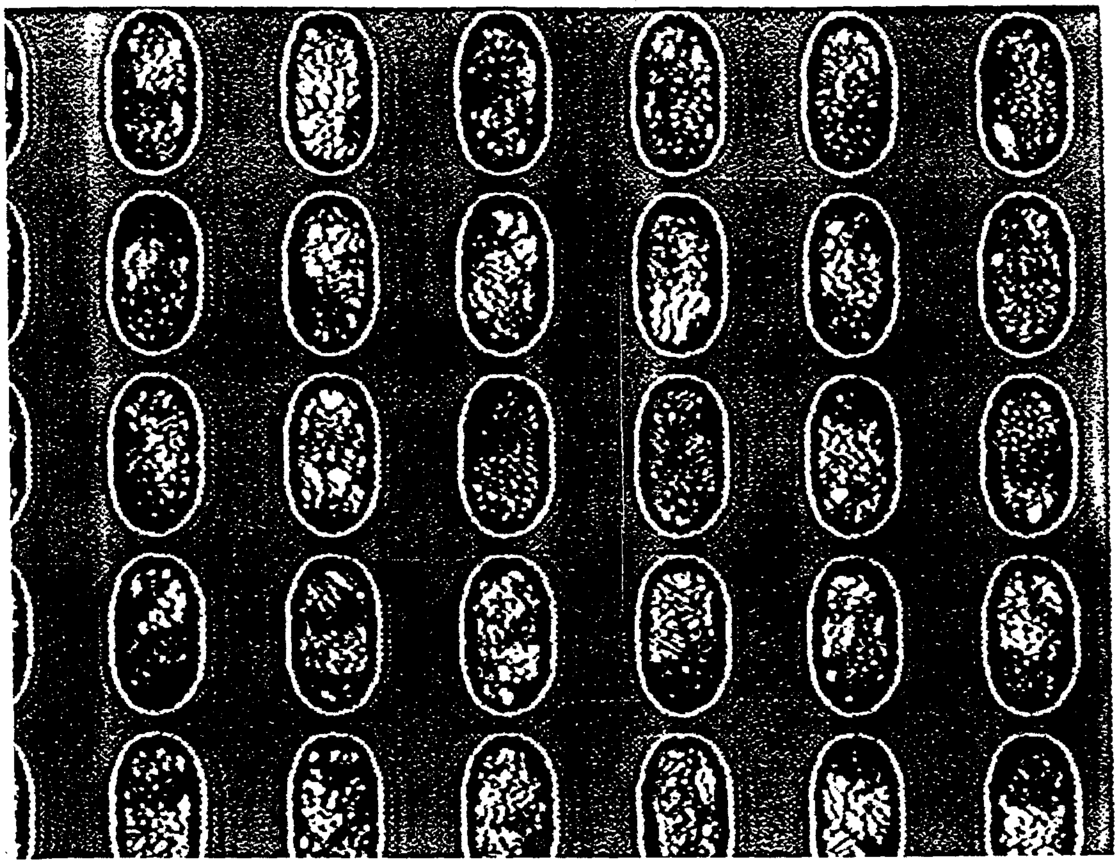
DUMMY CHIPS

80X80 ARRAY
$25X25\ \mu m^2$, $50\ \mu m$ PITCH

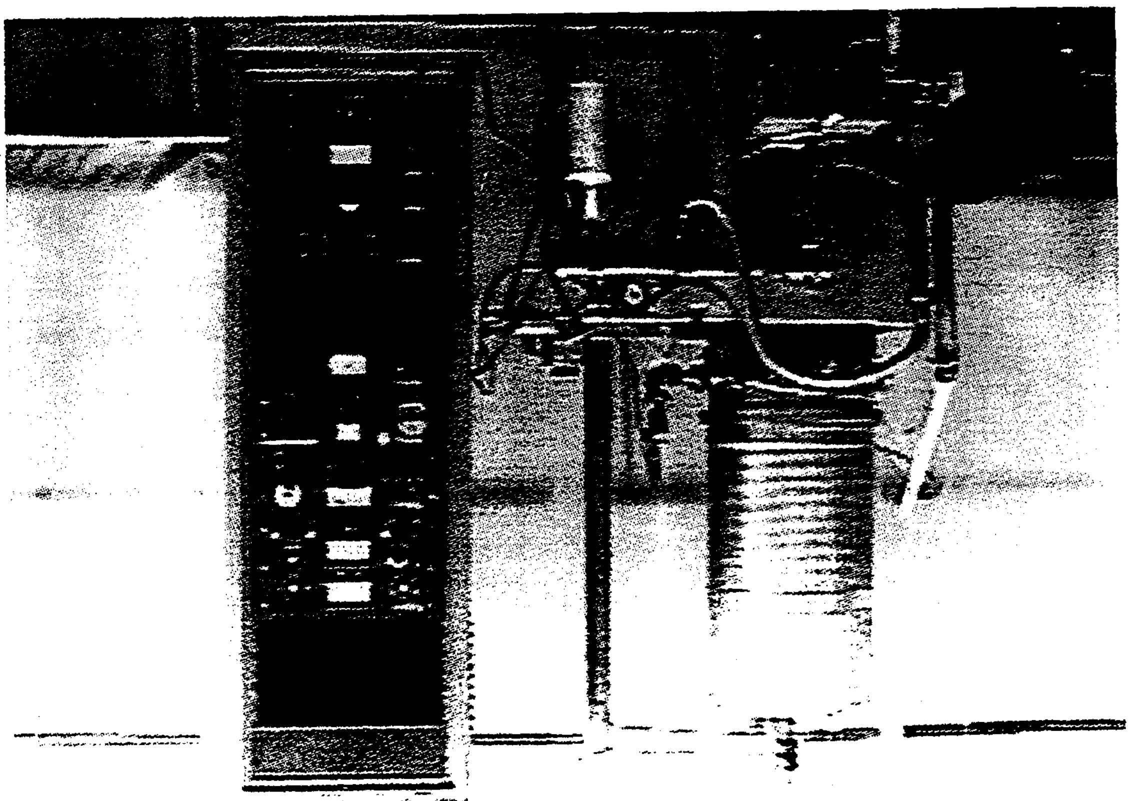
● - TENSILE STRENGTH
● - SHEAR STRENGTH
● - LIQUID NITROGEN

X-RAY IMAGER CHIP

~ 18 x 30 μm^2 Indium-UCD



INDIUM EVAPORATOR



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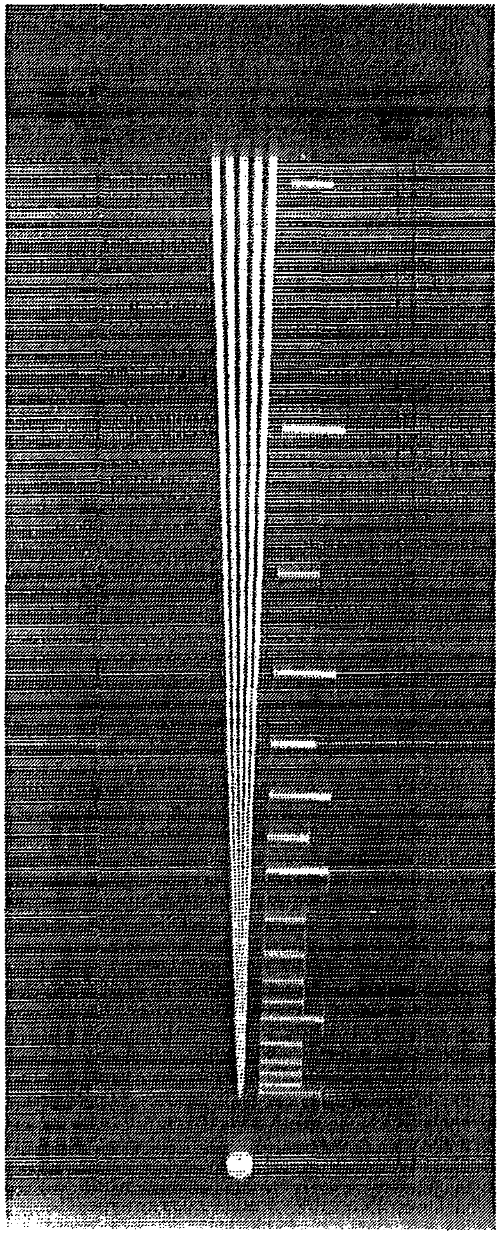
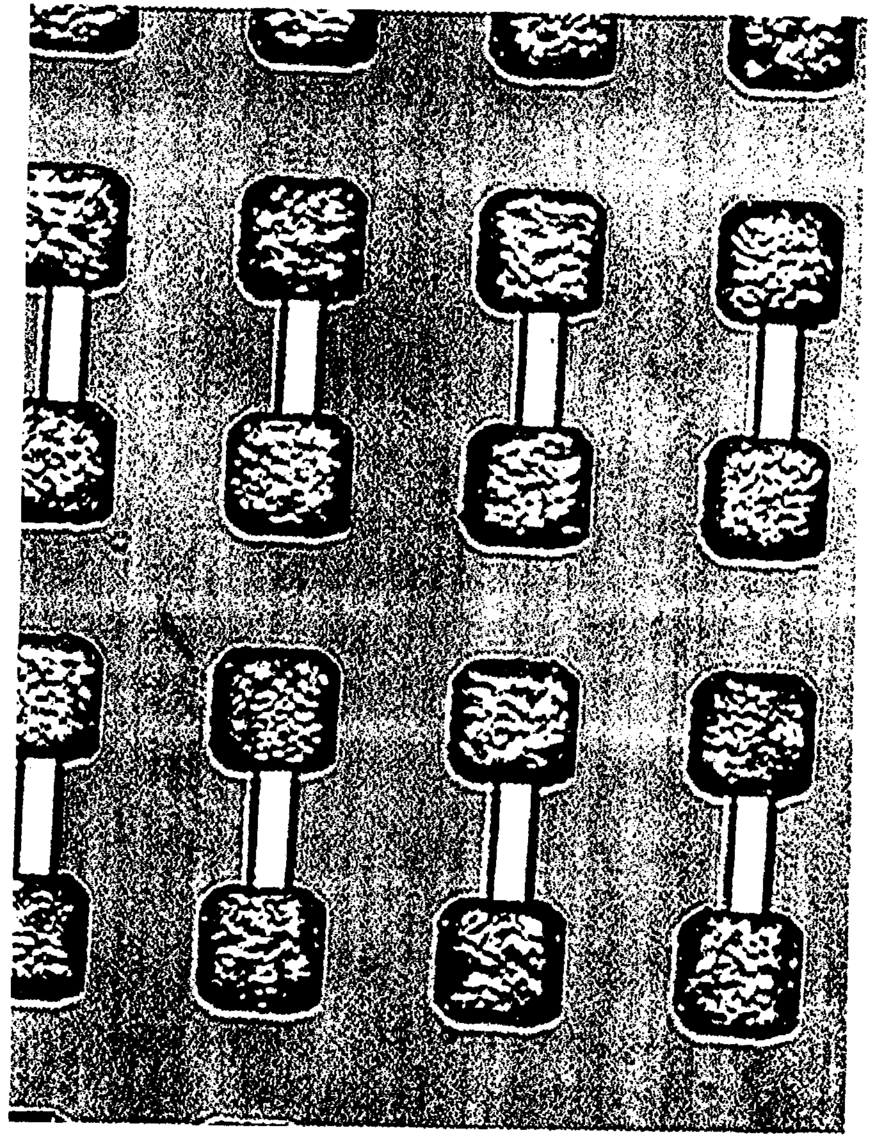
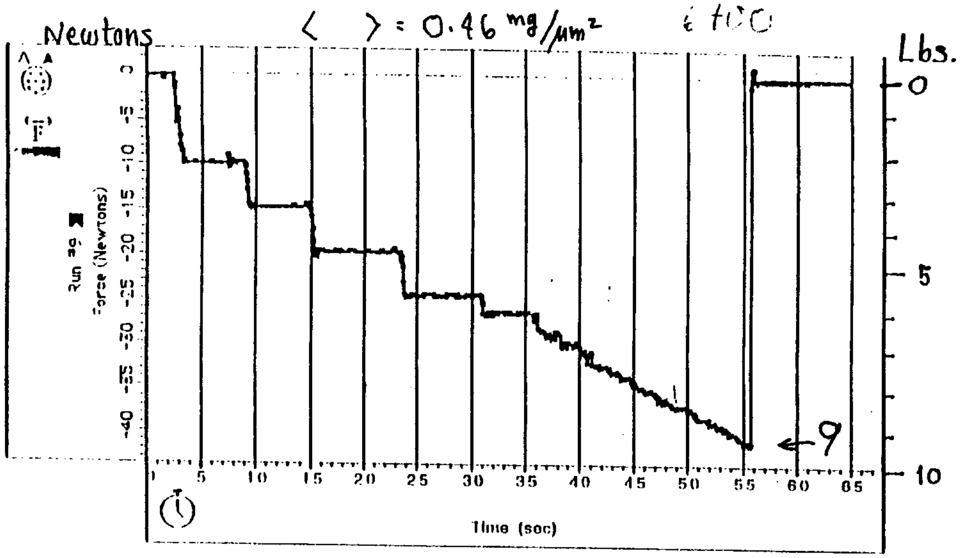
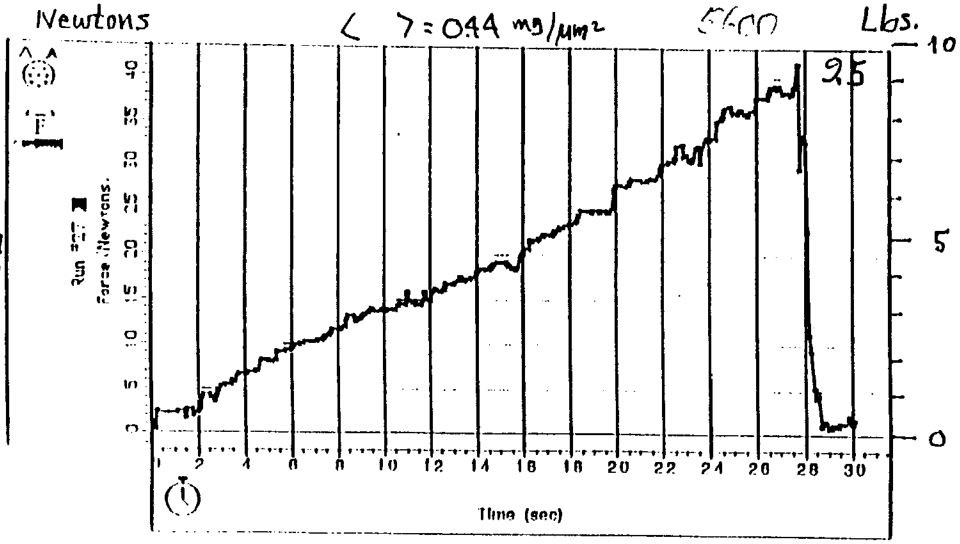


X-RAY
IMAGE

INDIUM - UCD
25 μm SQUARE, 50 μm PITCH







PSI readout 52x53 = 2756 bumps

0.46 mg/µm2 yield stress

22 µm diameter bump --> 1.1 lbs
25 µm " --> 1.4 "
30 µm " " --> 2.0 "

- Conclude:

Even small In bumps are strong enough to tolerate handling during assembly.

TIME STUDY

4 CHIPS PER SUBSTRATE
150 μm GAP BETWEEN CHIP EDGES

4 HOUR RUN BY TECH
- 4 MIN. PER PLACEMENT

SETUP, BREAKS, ETC.
→ 8 MIN. PER PLACEMENT TOTAL
60/day = 6000/20 weeks ≈ FWD PIXEL

- 150 μm GAP NOT A FACTOR

FUTURE

NOW SETTING UP UBM
- Ti/W
- ZINCATE

560

NEED HIGH PLACEMENT YIELD PER DIE

PLAQUETTE $Y_n = (\varepsilon)^n$

n \ ε	.99	.98	.95	.90
10	.90	.82	.60	.35
8	.92	.85	.66	.43
6	.94	.88	.74	.53

WANT Hi ε AND KNOWN SMALL $\sigma(\varepsilon)$

SOME BINOMIAL STATISTICS

n \ ε	.99	.98	.95
100	.010	.014	.022
200	.0070	.010	.015
300	.0057	.0081	.011
500	.0045	.006	.010

TO KEEP ERROR BELOW 0.01, NEED AT LEAST A FEW 100 PLACEMENTS TO QUALIFY VENDORS

SUMMARY

- We have substantial experience with flip chip bump bonding, the hybridization method of choice for CMS.
- We have in-house facilties for indium bump deposition and flip chip bonding, and will have facilities for cleaning & UBM (Ti/ W) deposition.
- We can bond US CMS prototypes with indium.
- If necessary, we could carry out the entire production bonding for US CMS.

Flip-Chip and Bump Interconnect Technologies for Sensor Applications

Zaheed S. Karim
Department of Electrical and Electronic Engineering
Hong Kong University of Science and Technology
Tel: (852) 2358-7070
Fax: (852) 2358-1485
E-mail: eekarim@usthk.ust.hk

Advanced Interconnect Technology Ltd.
Tel: (852) 2719-5440
Fax: (852) 2358-4766
E-mail: zkarim@hk.super.net

Flip-Chip & Bump Interconnect Technologies for Sensor Applications

Outline:

- Bump interconnect and flip-chip bonding requirements for sensor/detector applications
- Bump interconnection technologies:
  - Indium bumps: X-ray detectors, IR sensors, and RF applications
  - Lead-tin bumps: Flip-chip-on-board (FCOB) applications
- Comparison between indium and eutectic solder bumps:
  - Fabrication process
  - Minimum achievable bump dimensions and pitch
  - Electrical and mechanical characteristics
  - Bumping and flip-chip bonding yields
  - Manufacturability and cost
- Summary and Conclusions

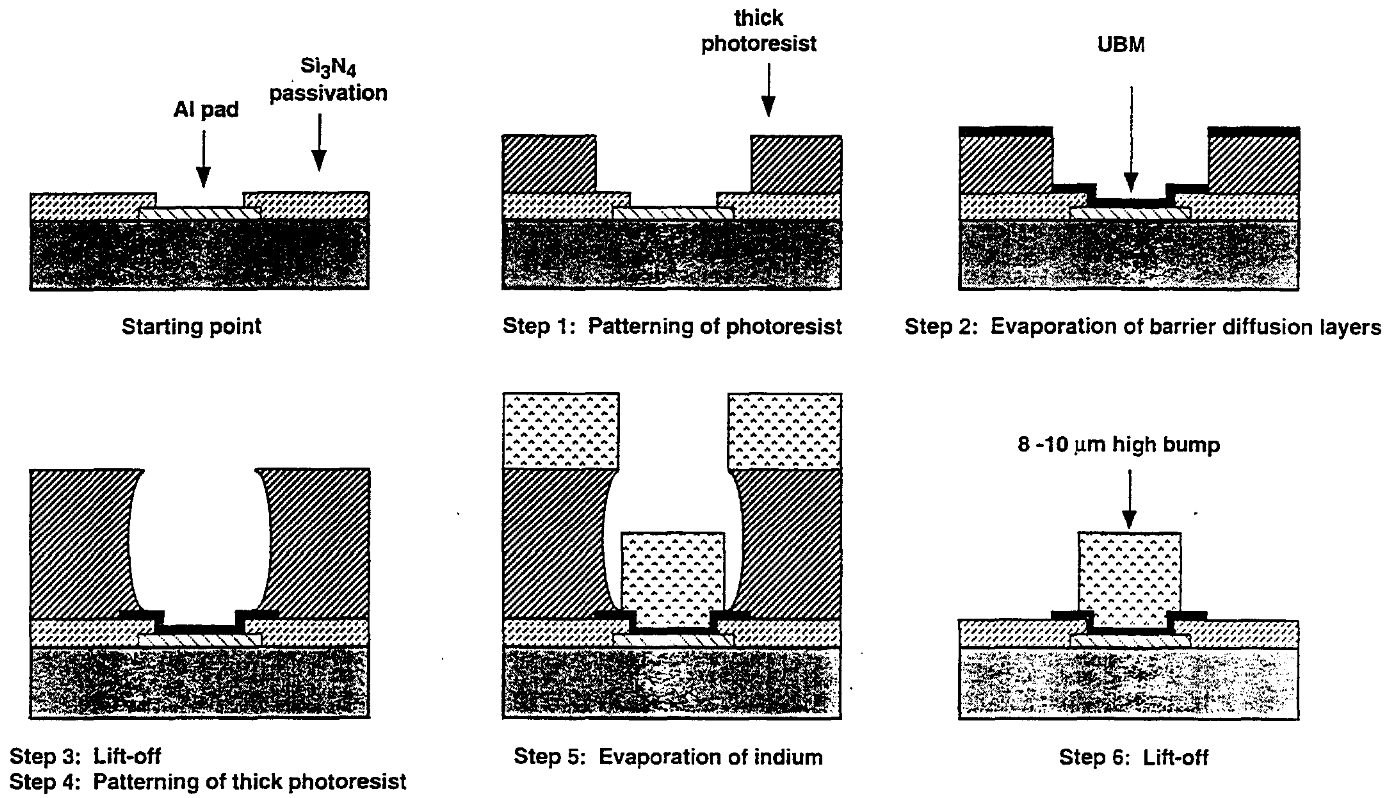
Indium Bumps

- Used primarily in the hybridization of semiconductor materials for sensors/detectors:
  - IR sensors (HgCdTe, InSb, GaAs to Si) and X-ray detectors (CdZnTe, Si to Si)
- Fabricated by thermal evaporation (using a lift-off process)
  - smaller bumps, finer pitch, better uniformity and control, single die bumping
- Sputter deposited 2-metal layer barrier diffusion UBM
- Soft compliant bump with a melting point of 156°C
- Forms a non-conducting oxide layer
- Enhancement of surface area of bump a factor in mechanical strength
- Both sides have to be bumped
- Typical bump sizes of 25-50 μm with a height of 8-10 μm
- Large arrays with 100K+ bumps possible - 12 μm diameter bumps on a 25 μm pitch
- Flip-chip bonding using compression only (room temperature process) requiring ~2-3 grams/bump (for 50 x 50 μm bump area with a height of 8-10 μm)
- Bump resistance of ~1-2 Ohms for a 25 μm square bump with a height of 10 μm
- Requires a flip-chip bonder with 1-2 micron alignment accuracy and planarization
- Expensive to fabricate

Flip-Chip & Bump Interconnect Technologies for Sensor Applications

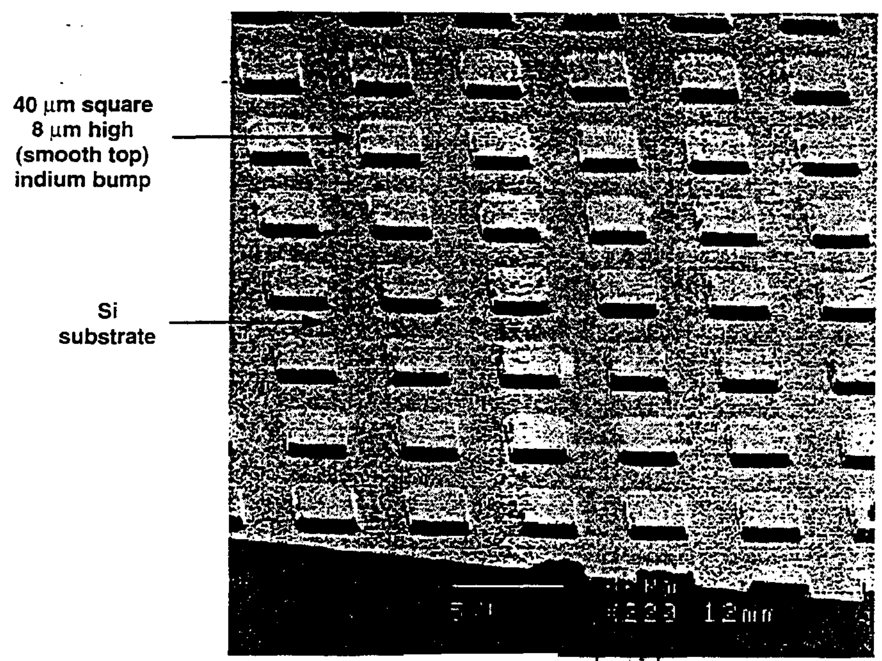
- Issues to be addressed in the choice of bump interconnect technology:
  - hybridization of sensor/detector to Si
  - required minimum bump dimensions and pitch
  - size of die and number and distribution of interconnections
  - availability of sensor material in wafer form
  - operating temperature (liquid nitrogen or room temperature)
  - electrical and mechanical characteristics
  - bumping and bonding yields
  - manufacturability
  - cost

Fabrication of Indium Bumps by Evaporation



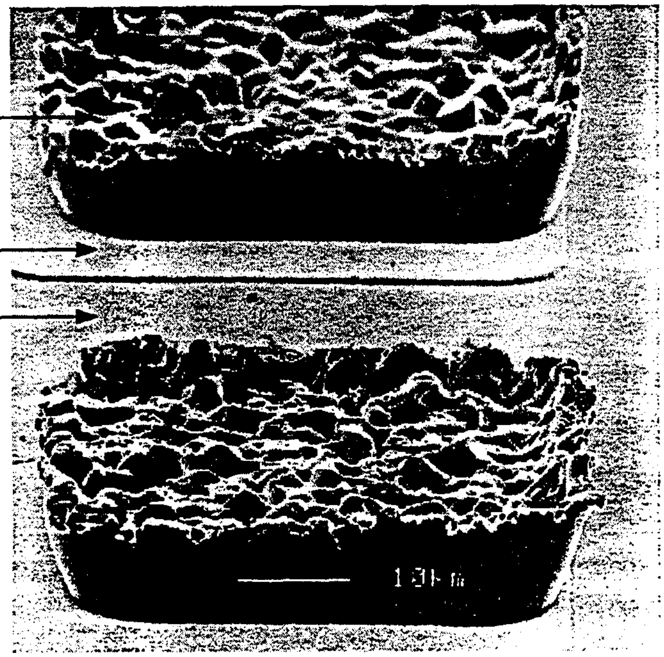
Evaporated Array of Indium Bumps

(scanning electron micrograph)



Evaporated Indium Bumps

(scanning electron micrograph)



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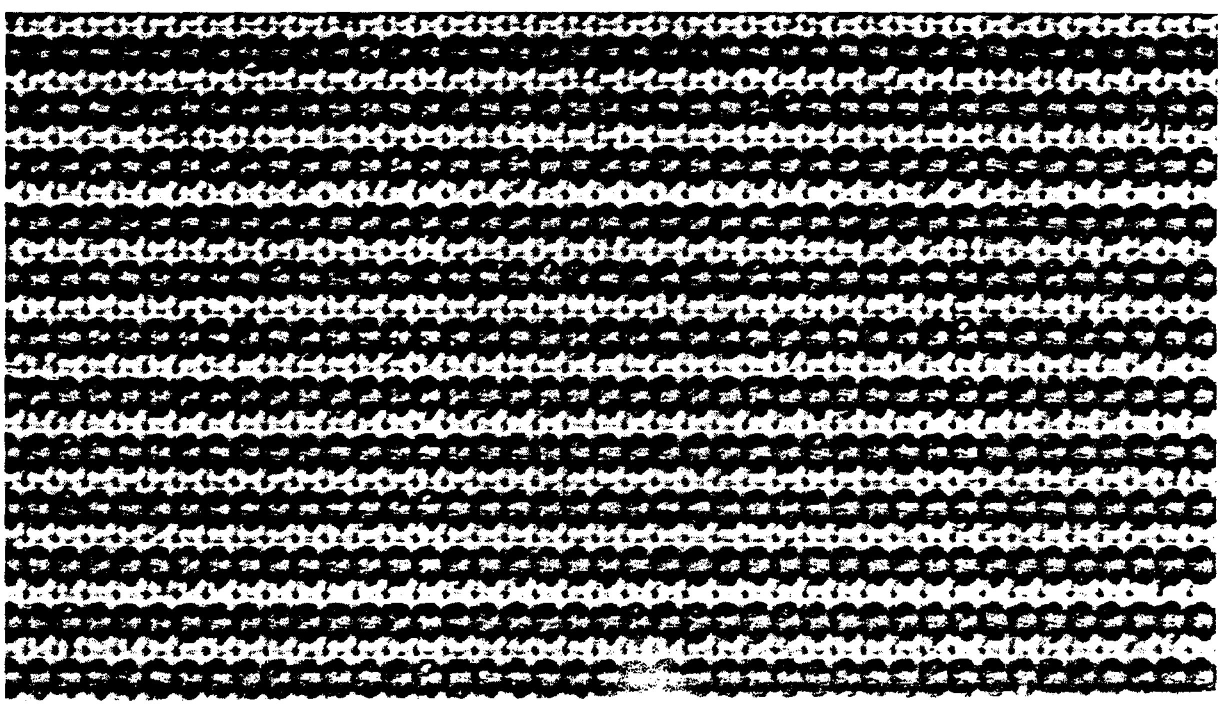
Array of Evaporated Indium Bumps

(optical micrograph)

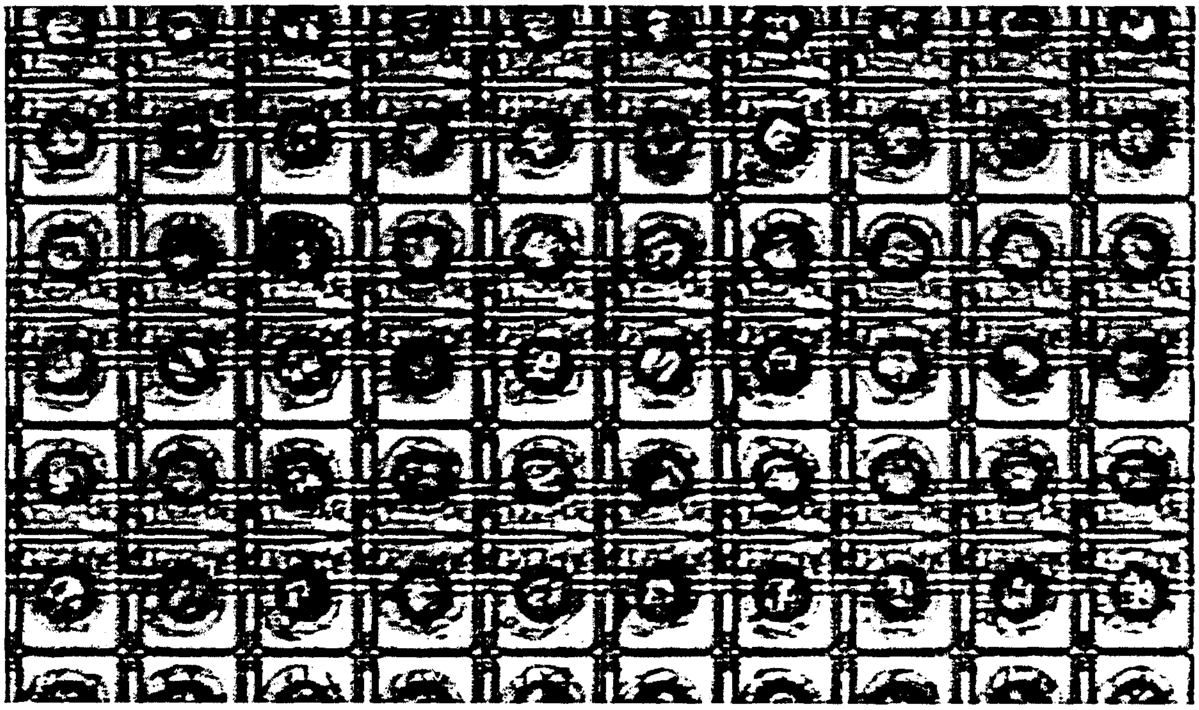
Partial array of 140,000 bumps: 12 µm diameter, 8 µm height, 25 µm pitch



Array of Evaporated Indium Bumps

(optical micrograph)

Partial array of 140,000 bumps: 12 μm diameter, 8 μm height, 25 μm pitch



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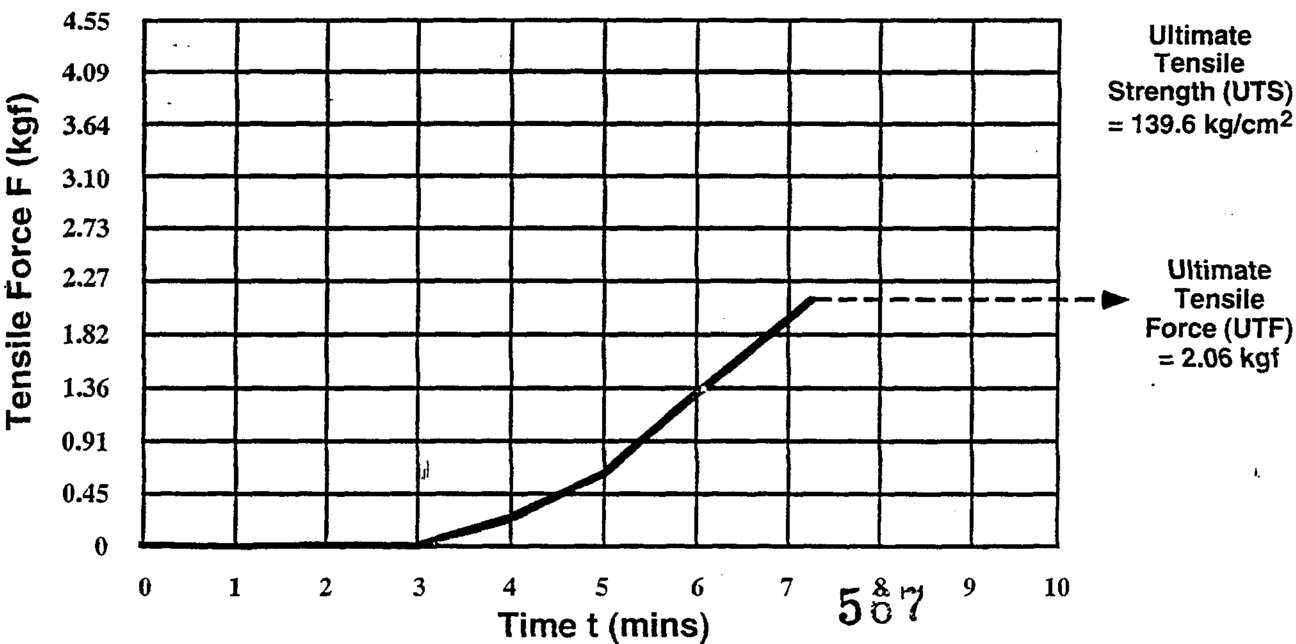
Mechanical Strength of Bonded Indium Bumps

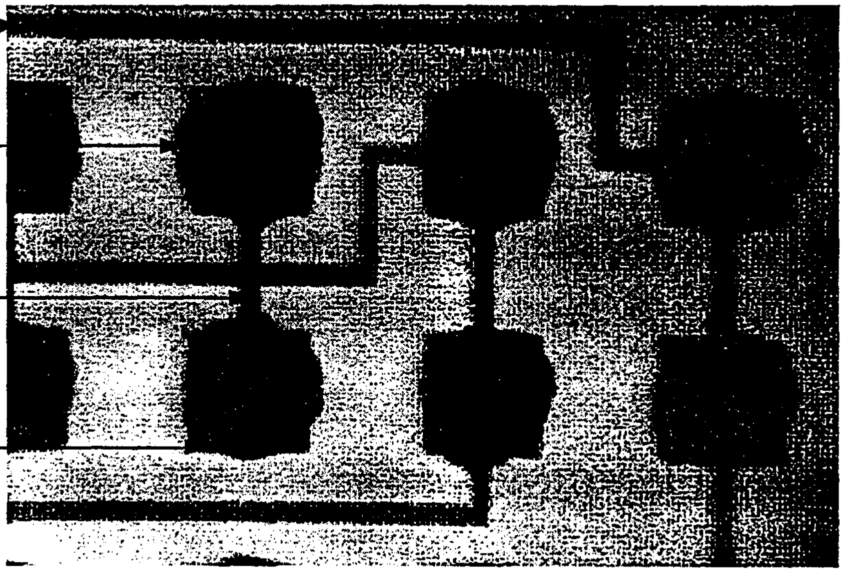
304 indium bumps, 70 x 70 μm area, 12 μm height



Notes:
Pull tester with a calibrated load cell of 9.09 kg with a pull speed of 0.21 inch/min
All failures were within the bulk of the indium

IR Illuminated Flip-Chip Bonded Array of Indium Bumps

(back-side illuminated Si substrate)



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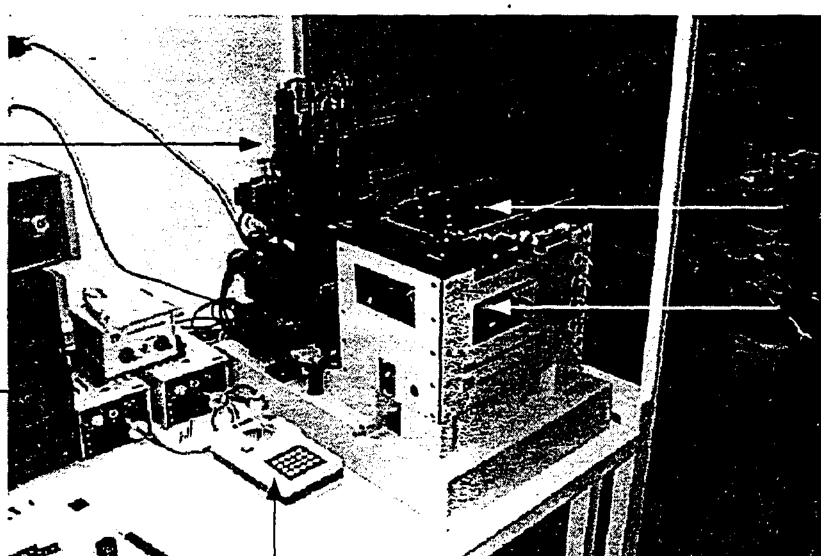
Flip-Chip Aligner/Bonder

Research Devices Aligner/Bonder Model M8-A



Indium Bumping and Bonding Yields

- Bumping yields of >95%
  Example: 6" wafer with 22 detector chips (each with 140K pixels)
  21 detectors had no missing bumps (visual inspection)
  1 detector (at the edge of the wafer) had a line of shorted bumps
- Manual flip-chip bonding yields of >85%
  Example: 20 modules fabricated, each detector with 140K bumps
  Lost one module in defective wire bonding
  Out of the remaining 19 modules, 16 were perfect with no defective bonds
  Remainder of 3 modules had 10-20 missing pixels (primarily at the corners/edges)

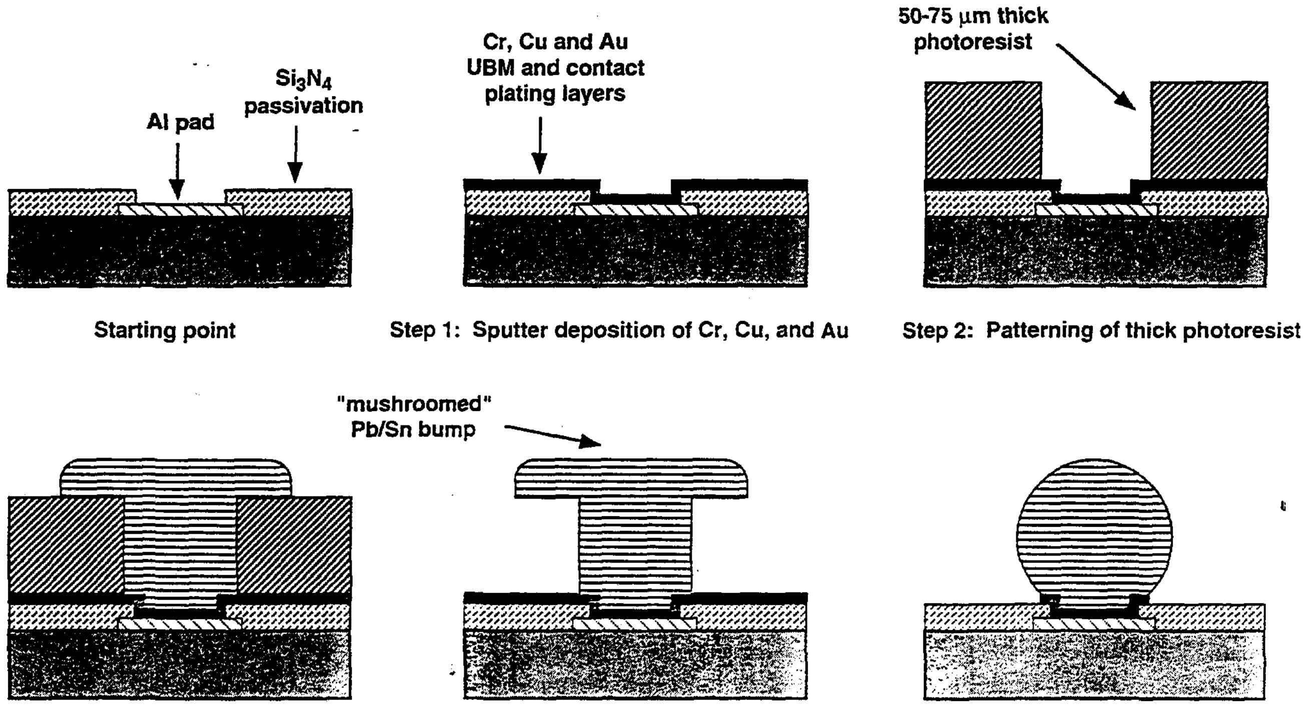
Electroplated Lead-Tin Solder Bumps

- Versatile in the choice of solder alloy composition (reflow temperatures)
- Self-aligning and self-planarizing bumps upon reflow
- Requires fabrication of solder bump on one side only with an opposing "wettable" pad
- Requires a complex under-bump-mettalurgy (UBM) - Cu, Ni, Au
- May require the use of flux and removal of flux residue
- Excellent electrical and mechanical characteristics:
  - low resistance electrical path (2-3 μOhms)
  - low inductance (~0.1 nH)
  - bump shear values in excess of 30 grams for a 50 micron diameter bump
- Does not require a highly accurate flip-chip aligner/bonder (±10 microns X-Y)
- Currently limited to minimum 35-50 μm diameter bumps on a 70-100 μm pitch
- Alpha particle emission from bumps and susceptibility to high radiation dose
- Potentially low-cost in high volume

Solder Types and Liquidus Temperatures

Solder Composition	Liquidus Temperature (°C)
Sn(62.5%)-Pb(36%)-Ag(1.5%)	178
Sn(63%)-Pb(37%)	183
Sn(92%)-Ag(5%)-Cu(2%)	210
Sn(95%)-Pb(5%)	223
Sn(100%)	232
Pb(75%)-In(25%)	250
Pb(90%)-Sn(10%)	268
Pb(97%)-Ag(3%)	304
Pb(95%)-Sn(5%)	308
Pb(100%)	327
Sn(3%)-Au(97%)	370

Fabrication of Lead-Tin Bumps by Electroplating



Starting point

Step 1: Sputter deposition of Cr, Cu, and Au

Step 2: Patterning of thick photoresist

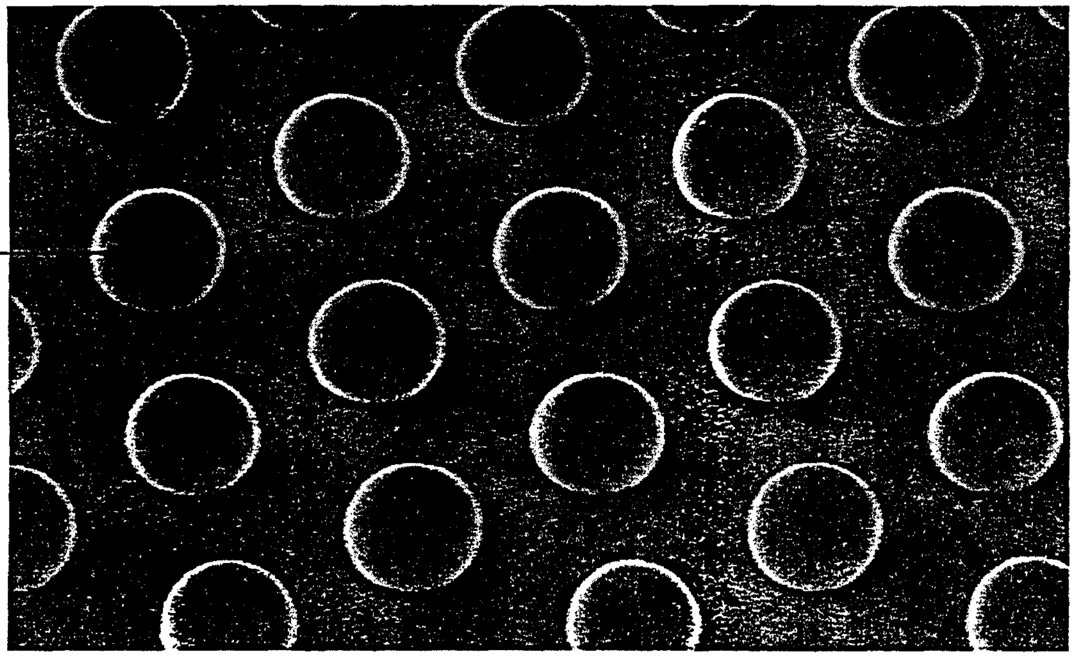
Step 3: Electroplating of Pb/Sn bump

Step 4: Lift-off

Step 5: Etching of contact plating layers

Array of Electroplated and Reflowed Eutectic Solder Bumps

(scanning electron micrograph)



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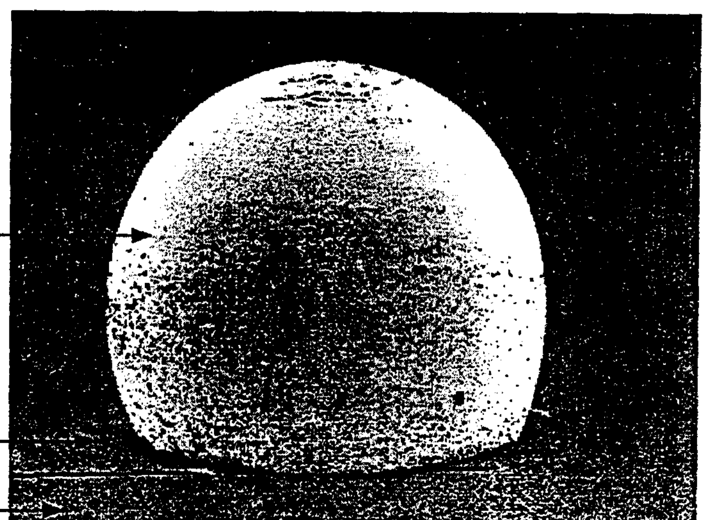
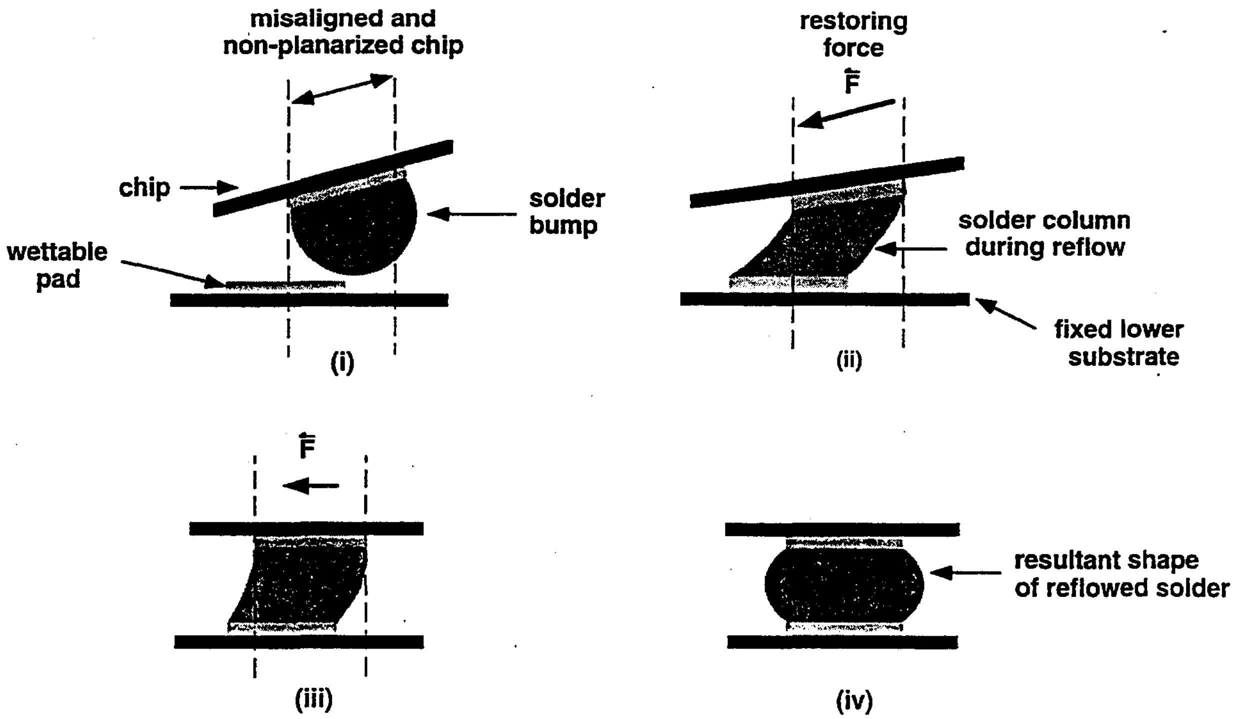
Electroplated and Reflowed Eutectic Solder Bump

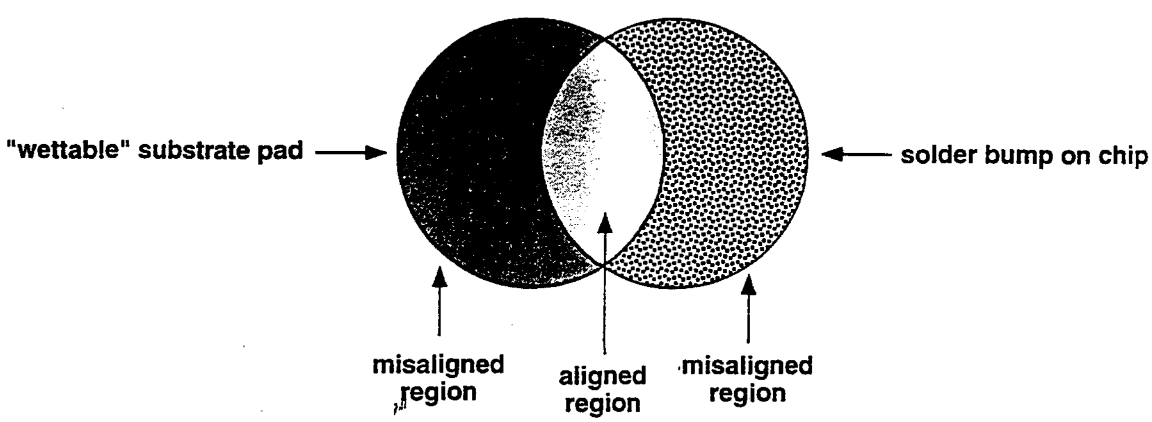
(scanning electron micrograph)



Self-Aligning/Planarizing Properties of Pb-Sn Solder Bumps



Self-Aligning Properties of Pb-Sn Solder



1) Can tolerate about a 50% misalignment between the substrate pad and solder bumped chip
2) Can be used to self-align a solder bump to a wettable pad to within an accuracy of ±1 µm

Flip-Chip & Bump Interconnect Technologies for Sensor Applications

Summary and Conclusions:

- Choice of indium or eutectic solder bumps for sensor/detector applications
- Indium has been proven effective, able to fabricate small bumps with fine pitch (by evaporation), soft and ductile bump, excellent mechanical characteristics, high-yields for both bumping and bonding, requires bumps on both sides, requires a flip-chip aligner/bonder with planarization, expensive to fabricate
- Solder bumps may provide an alternative if smaller bumps and finer pitches are achievable, versatile, eutectic solder has a reflow temperature of ~180°C, excellent electrical and mechanical characteristics, self-aligning and self-planarizing, requires a complex UBM, use of flux, lower fabrication cost in volume

Flip-chip Interconnection of 100k Pixel Hybrid Detectors

Dr Giles Humpston
GEC Marconi Materials Technology Limited
Caswell, Towcester
Northamptonshire NN12 8EQ
United Kingdom

Email: giles.humpston@gecm.com

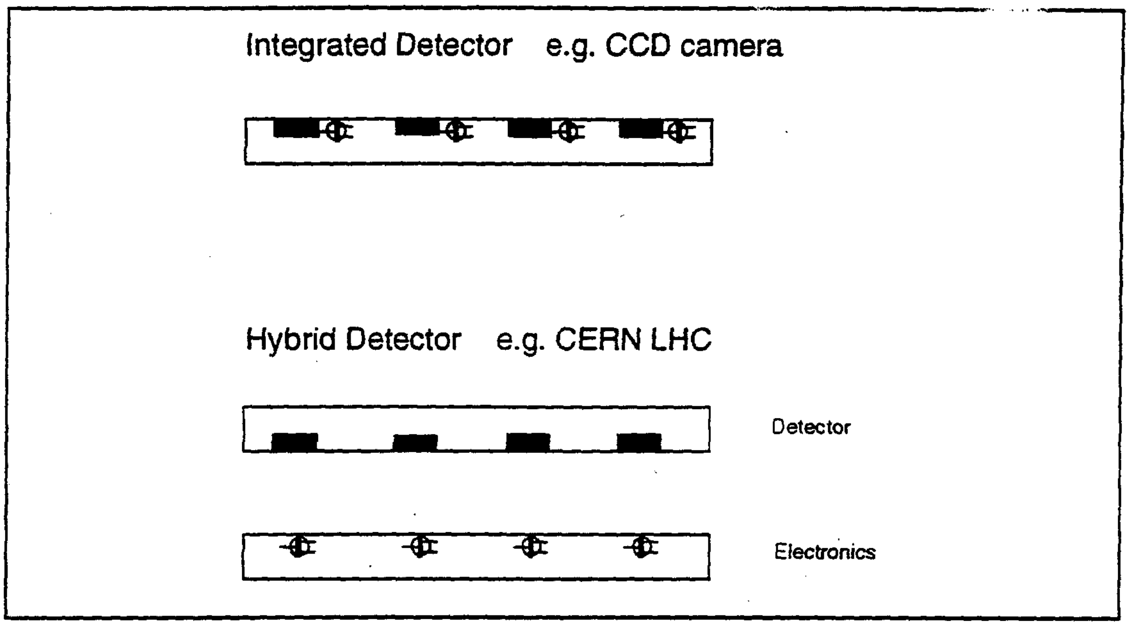
Abstract

Hybrid detectors use different components for the sensor element and read-out electronics. This approach allows the detector to be optimised for collection efficiency and the read-out electronics for functionality, but places severe demands on the interconnect technology, especially if the detector is pixelated in two dimensions. Interconnection of fine-pitch (<50um), 2D hybrid pixel arrays is usually accomplished by either flip-chip compression bonding or flip-chip solder bonding.

GEC-Marconi Materials Technology offers a commercial portfolio of fine-pitch flip-chip interconnect technologies specifically for pixel detector manufacture. The service includes the option for each interconnect to be sub 10um diameter at below 20um pitch. The technology is discussed and application examples are presented including the CERN Omega-3 device and an advanced infra-red detector array containing over 100,000 elements.

Introduction

Sensors can be made in two configurations. These are illustrated in Fig. 1, below.



Integrated detectors are single component devices that combine the sensing element and the read-out electronics on a single substrate, usually silicon. A common example of this technology is the solid state optical detector (ccd) used in camcorders and digital cameras.

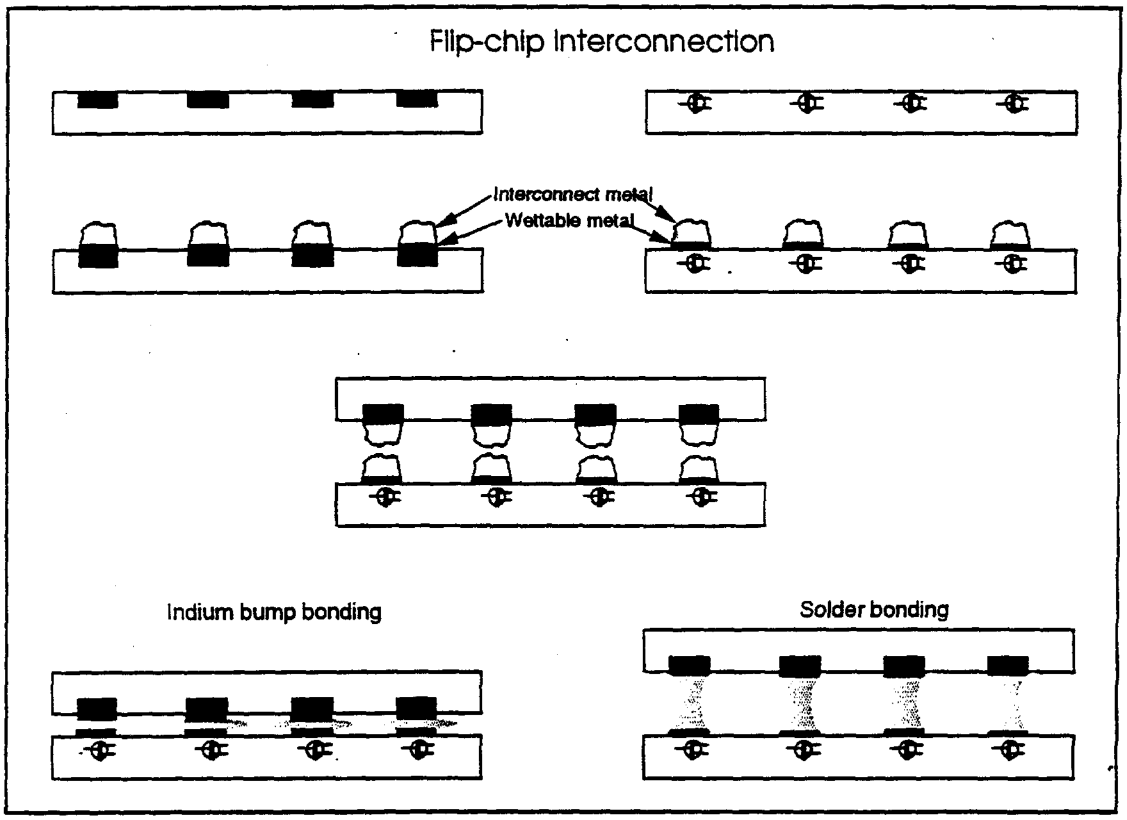
Hybrid detectors use different components for the sensor element and the read-out electronics. This approach allows the detector to be optimised for collection efficiency and the read-out electronics for functionality. A household example of this sensor type is the infra-red detectors used for burglar alarm systems. In these, the detector is a pyroelectric material (i.e. converts thermal energy to electrical charge), while the electronics system comprises a low noise amplifier and threshold gate.

Each pixel element in a hybrid detector needs to be connected to a separate electronics channel. If the hybrid detector is pixelated in two dimensions this places severe demands on the attachment and interconnect technology. Electrical interconnection and physical attachment of 2D hybrid pixel arrays is usually accomplished by flip-chip bonding.

Flip-chip bonding

Flip-chip bonding is the leading method for attachment and interconnection of high performance semiconductor devices, including multi-chip modules (MCM), monolithic microwave integrated circuits (MMIC) and pixelated imaging detectors.

There are two process variants, flip-chip compression bonding (commonly known as indium bump bonding) and flip-chip solder bonding. The principle of these two process is shown schematically in Fig 2, below.



Both processes involve applying a "wettable metal" to the surface of the components to be joined. This is often a multi-layer metallisation, designed to provide ohmic contact to- and metallurgical compatibility between the contacts on the detector and read-out electronics. To the wettable metal on one or both component is then applied the interconnect metal. One of the die is then inverted (flipped over) and mating pairs of contact pads are aligned. This operation is performed on a flip-chip bonding machine. To perform flip-chip compression bonding the two components are then simply pressed together until interconnect metal welds. For flip-chip solder bonding, the assembly is heated until the interconnect metal melts and wets.

Although flip-chip compression bonding and flip-chip solder bonding superficially appear similar processes, they actually require very different materials and process conditions, and the interconnects so formed have significantly different characteristics. The key features of each process and properties of the resulting interconnects are given in the following Tables.

	Indium Bump Bonding	Solder Bump Bonding
Process	Solid state diffusion	Solid-liquid alloying
Materials	In, Au, Pb, Pb/Sn	Any solder
Temperature	20-200°C	Solder melting point
Pressure	10 - 100 MPa	0 MPa
Max Height:Pitch	1 : 5	3 : 1

Technology Characteristics

Indium Bump Bonding	Solder Bump Bonding
Short (coin) interconnects	Tall (pillar) interconnects
Closed interconnect gap	Open interconnect gap
Fluxless	Flux required
Low residual stress	Residual stress
Service temp > bonding temp	Service temp < bonding temp
Alignment as placed	Self aligning (±2um X, Y ±0.5um Z)
Planar substrates	Topology tolerant

Fine-pitch Flip-chip

High resolution detectors require large numbers of small and densely packed pixels. If the interconnects can be larger than about 100um diameter, a wide diversity of methods can be used to apply the wettable and interconnect metals to the components. The lowest cost option for volume manufacture is predominantly wet plating. For substantially smaller interconnects, especially those below 10um diameter, the preferred approach is to exploit conventional semiconductor processing equipment and use photolithography to define features and vapour phase deposition to apply the wettable and interconnect metals.

GEC-Marconi Materials Technology, at Caswell, has over 25 years experience in fine-pitch flip-chip bonding and offers a state-of-the-art commercial service. Highly toleranced interconnections can be made for operation at over 40GHz on either whole wafers or individual known good die (KGD). Bumps can be made as high as 50um, for direct connection of integrated circuits to printed circuit boards, or smaller than 10um diameter for 2D detector arrays. Bump pitches can be below 20um. Equipment and facilities exist to provide advanced flip-chip bonding on a prototype scale through to volume production. This service is underpinned by extensive R&D resources, enabling one-off and highly specialised customer requirements to be met. An outline of this Service is given below.

Process	Indium- and solder-bump bonding
Feature size	10-100um dia., >10um between features, <50um high
Substrates	Single die - 6" wafers (300mm BY 1999)
Interconnect	Any commercially available metal or alloy
Fluxes	Reflow in choice of atm., custom flux design capability
Flip-chip	Full 5-axis alignment, 4 equipments
Component size	0.1mm to 100mm
Underfill	Any commercially available product
Environment	ESD protected Class 100 clean rooms
Modelling	RF, thermal, mechanical, static and transient

GMMT Fine-pitch Flip-chip Service

Process Yield

Flip-chip is attractive for volume manufacturing applications because it is an inherently high yielding process. As an example, GEC-Marconi manufacturers a pixelated sensor that contains approximately 10,000 elements, in batches of 10 units. Of this batch of ten it would normally be expected that six have all interconnects made and functioning, while the remaining four units have a few isolated dead pixels. The pixel yield per batch therefore routinely exceeds 99.99%.

During process development, or occasionally during manufacture, it is obviously possible to produce pixelated devices with substantial numbers of non-working elements. Because flip-chip assembly is a well understood and characterised process, most failures can be readily diagnosed to a particular process deficiency, enabling corrective measures to be applied.

Application Examples

LHC Omega-3 Pixel Sensors

CERN has designed a family of pixel sensors to track the path and momentum of sub-atomic particles. These sensors essentially comprise an array of P-N junctions in silicon, GaAs or diamond, each of which is connected to an individual silicon electronics readout circuit. Because the detectors are relatively simple structures they can be physically large yet made with very low defect rates. The readout electronics, by contrast, are extremely sophisticated chips and producing die to the required specifications clearly presents a challenge to the wafer manufacturer. For this reason the sensor has been designed so that six readout die are used to populate each detector and the die are fully probe-tested before bonding.

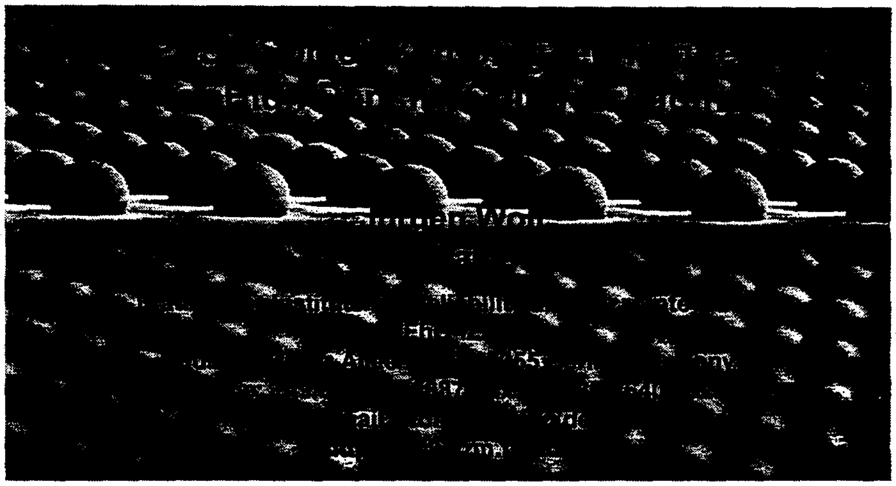
In the current generation of Omega-3 prime sensor, electrical connection between the detector and the electronics chips requires approximately 13,000 flip-chip interconnects, each 18um diameter on a 50um by 500um pitch. As an additional complication, the interconnects are required to provide the maximum possible physical separation between the two components, to minimise electrical cross-talk. For this reason flip-chip solder bonding, using eutectic lead-tin solder, is employed by GEC-Marconi Materials Technology for the assembly process. Despite the complexity of this product, the yield of useable 'ladders' currently stands at about 75% and it is anticipated that some planned process enhancements will further improve this figure and decrease the cost.

100k Pixel Hybrid Detectors

A thermal imaging camera responds to heat, as opposed to light. The majority of thermal imaging cameras operate in the 8-14um wavelength of the infra-red band because the image is then not degraded by either smoke or rain. The quality or precision of the image that can be obtained from an infra-red camera is simply a function of the number of pixel elements (exactly as for a computer monitor albeit working in reverse!). However, if the sensor is too large then the quality of the picture again degrades due to deficiencies in the camera optics. The technology drive is therefore to pack the maximum number of pixels into the smallest possible area.

The infra-red detector used in this example is a pyroelectric ceramic. This approach has the merit that the camera can operate at room temperature. Traditional infra-red detectors must be cooled to about -200°C in order for them to function. The ceramic is manufactured in large blocks, then sliced and polished to eventually yield 8um thick wafers, which are then diced by laser into individual pixel elements. Electrical connection between each pixel element and the custom read-out electronics is achieved by flip-chip solder bonding. To minimise thermal leakage from the detector to the electronic die the solder interconnects are made as small as possible, and in this instance below 10um diameter. By exploiting fine-pitch flip-chip as the interconnection and assembly method it is possible to realise sensors that measure no larger than 1cm^2 but which contain in excess of 100,000 individual pixels. A lower resolution variant of this product is sold by GEC-Marconi Infra-red Limited for use by firemen, police and the rescue services.

PIXEL98 Workshop - Fermilab Wilson Hall May, 7-9, 1998



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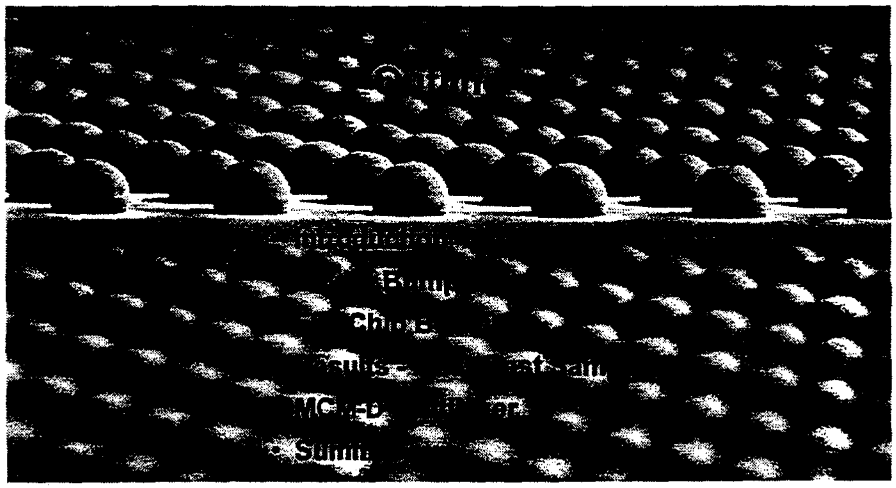

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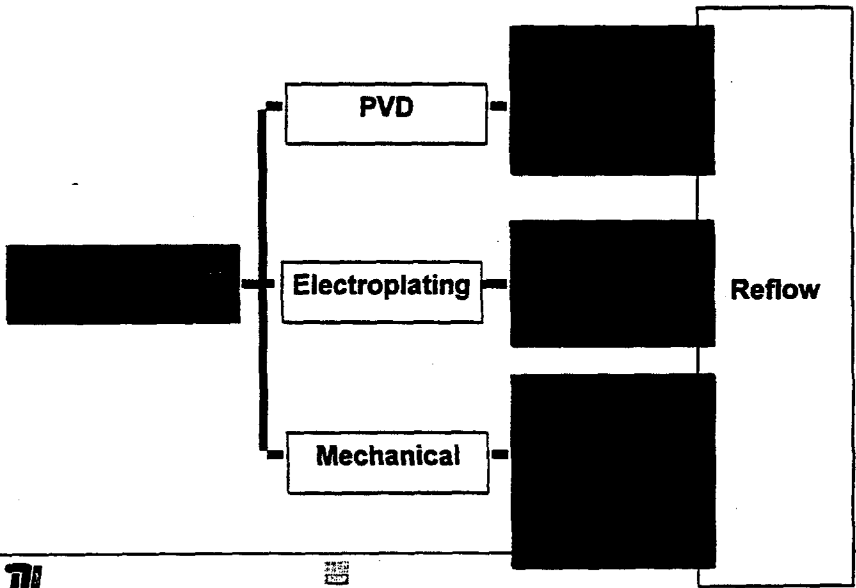
- research and development of advanced assemblies and packages
- prototyping and low volume production
- tutorials, seminars and consulting



Flip Chip Bumping

Bumping Methods

Sputtering / Evaporation ➔ longest experience	➡	**C4 Technology** CrCu/PbSn5
Sputtering / Electroplating ➔ very fine pitches	➡	**Galvanic Bumping** Au, PbSn, AuSn etc.
Electroless / Printing ➔ high throughput	➡	**Low Cost Bumping** NiAu/PbSn
Mechanical ➔ single chips	➡	**Stud Bumping** Au

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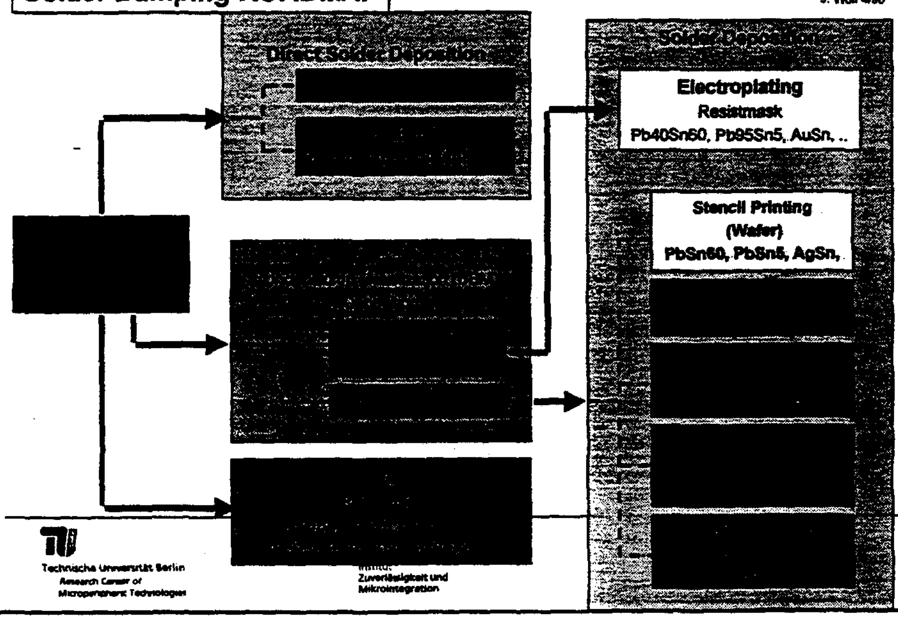
J. Wolf 4/98

Solder Bumping ROADMAP



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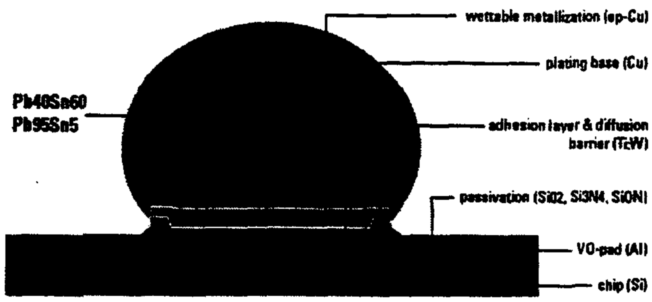
PbSn Solder Bump Structure



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Solder Bump Structure

UBM

Adhesion-Layer & Diffusion Barrier

- hermetic coverage of the chip pad
- good adhesion to Al chip pad
- minimum interdiffusion between bump metal and chip pad
- low degradation during temperature cycles imposed during reflow, bonding
- low internal stress
- low contact resistance

Solder Base

- sufficient wettability to the solder
- tolerable formation of intermetallics at the interface

Solder (e.g. PbSn63, PbSn5)

- mechanical contact to substrate
- stand-off chip-substrate
- good electrical contact
- high creep resistance to improve reliability under thermal loading
- high ductility to minimize mechanical stress due to different CTE of substrate and chip

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Under Bump Metallization (UBM)

Layer	Material	Thickness	C 4 (IBM)	IZM /TUB
Adhesion-Layer Diffusion Barrier	Ti, Cr	(30-200) nm	Cr [150 nm]	Ti:W [200-nm]
(Plating Base)	Cu, Au, Ni, Pd	(200-200) nm	Cr /Cu [150 nm]	Cu [300 nm]
Wettable Layer	Cu, Ni	(1 - 5) µm	Cu [1000 nm]	Cu [5 µm]
Oxidation Protection	Au	(100-200) nm	Au [100 nm]	

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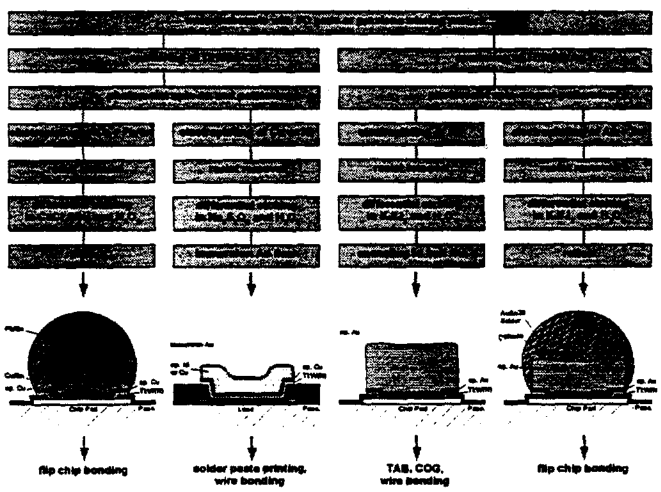
Electroplating Bumping Techniques



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Technology Determination

Project ATLAS

Si substrate & chip
Si3N4 / SiON passivation
I/O-pad: Al
small I/O-size & pitch (50 µm)
no 2nd soldering level

Bump Structure:
eutectic lead/tin solder
UBM: Ti:W/Cu

Technology:
Solder Deposition using electroplating and photoresist mask technique

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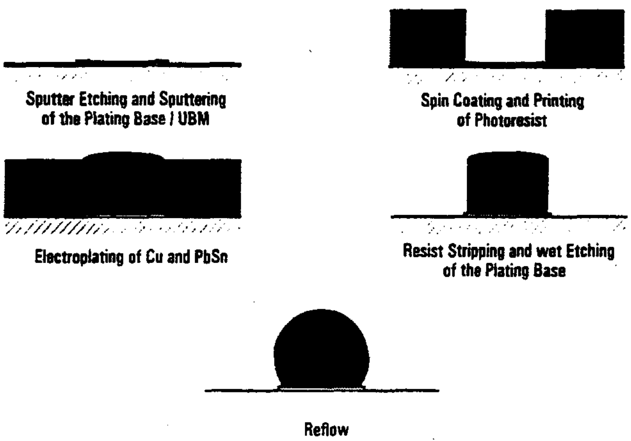
Processflow PbSn-Bumping using Electroplating



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Electroplating

	Cu electrolyte	PbSn electrolyte
contents	$CuSO_4$, sulfonic acid, chloric acid, grain refiner and leveler, wetting agent	$Sn(CH_3SO_3)_2$, $Pb(CH_3SO_3)_2$, methane sulfonic acid, grain refiner, wetting agent, oxidation inhibitor
metal concentration	20 g/l Cu	total of 28 g/l
temperature	25 °C	25 °C
agitation	2....5 l/min	3 l/min
pH value	< 1	< 1
current density	10....30 mA/cm^2	20 mA/cm^2
plating rate	0,22...0,66 µm/min	1 µm/min
current efficiency	nearly 100 %	nearly 100 %
hardness of deposit	80....100 $HV_{0,025}$	around 10 $HV_{0,025}$
appearance of deposit	glossy	matt
anode material	phosphorus-alloyed copper	appropriate Pb/Sn alloys

AU Bumping

Resist /AZ 4562)
thickness: 33 µm

Au-Bumps after Deposition
and Resist Stripping
Bump Size: 110 µm x 110 µm
Space: 30 µm

AU Bumping

Electroplated Au bumps
height: 20 µm, diameter: 15 µm

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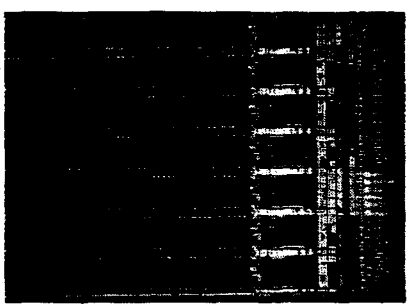
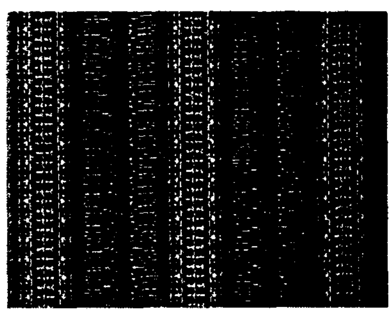
Solder Bumping Pb40Sn60





Read out Si-chip (Uni Bonn) with Solder Bumps
after Reflow
UBM: Ti:W/Cu / ep.Cu (5µm)

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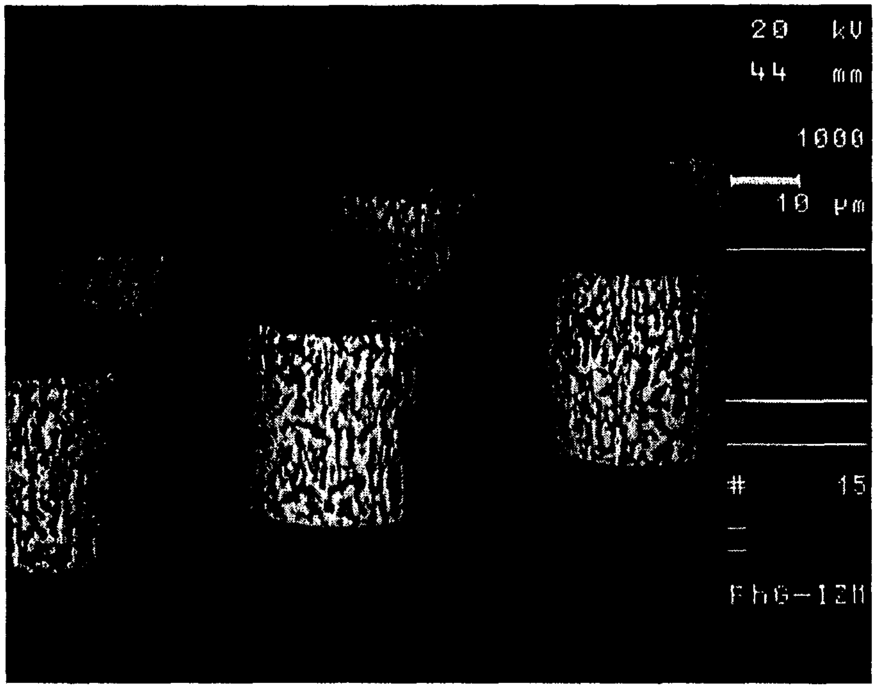
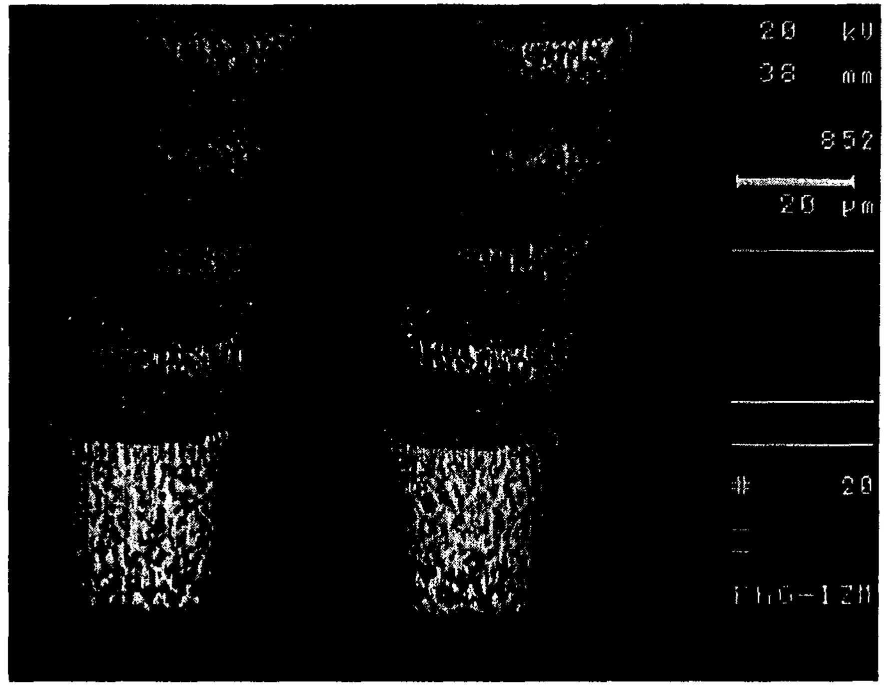
Solder Bumping - Pb40Sn60





Solder Bumps after Electroplating
UBM: Ti:W/Cu / ep.Cu (5µm)
Solder: Pb40Sn60

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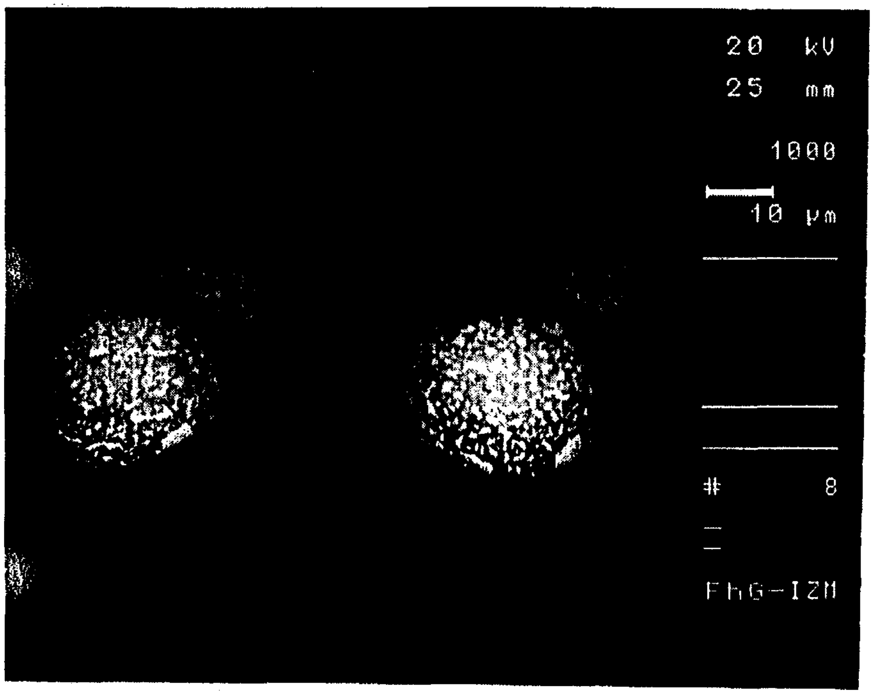
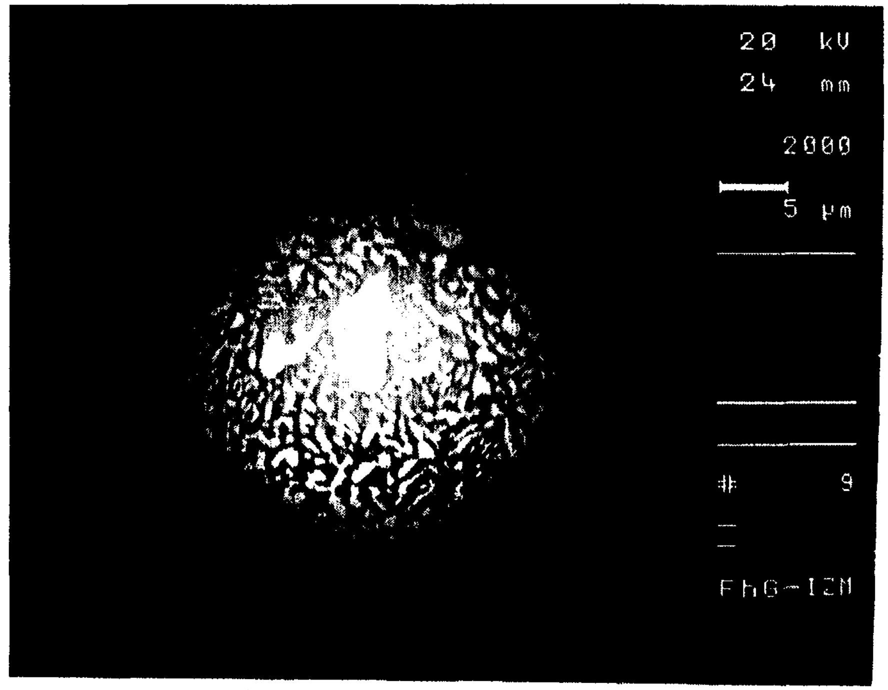
Department: Multichip Modules
Bumping
J. Wolf, LD ´97

Solder Bumping - Pb40Sn60





Solder Bumps after Reflow
UBM: Ti:W/Cu / ep.Cu (5μm)
Solder: Pb40Sn60

532

Solder Bump Reflow

Oxidelayers must be removed to allow solderball formation
Use of aggressive fluxes must be avoided
Melting point: T_m = 314°C (95/5 wt% Pb/Sn),
T_m = 183°C (37/63 wt% Pb/Sn

Reflow methods:

Heating under active atmosphere
Using Flux (RMA)

Some fluxless reflow methods:

Heating under reducing atmosphere
- 100 % H_2
- 95 % N_2 / 5 % H_2 (not sufficant)

(Reflow in vaccum)
(Reflow after Sputteretching or RIE)

Process: Pb40Sn60 (PbSn5)
Heating in a organic medium up to 240 (350) °C
followed by cleaning procedure

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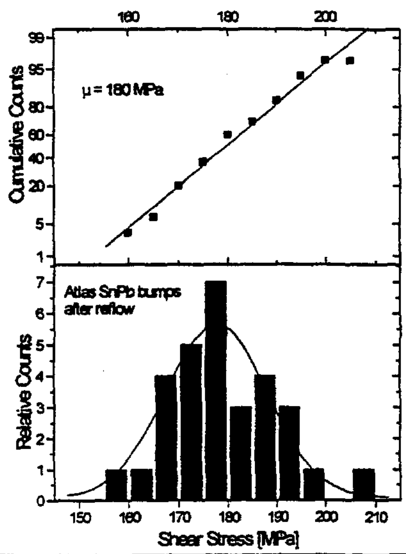
Under Bump Metallization (UBM)



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Bump Inspection after Deposition & Reflow (Pb40Sn60)

Wafer #	Chip defect # 61	%	Bump defect # 189588	ppm
2594/56	3	4,92	16	84,39
2594/57	0	0,00	0	0,00
2594/58	3	4,92	18	94,94
2594/60	0	0,00	0	0,00
2594/61	2	3,28	5	26,37
2594/64	2	3,28	3	15,82
2596/16	0	0,00	0	0,00
2596/17	2	3,28	15	79,12
2596/18	3	4,92	6	31,65
2596/21	2	3,28	6	31,65
	1,70	2,79	6,90	36,39

defect rate: 3.64 x 10-5**
total number of bumps: 1895880
bump defects: 69

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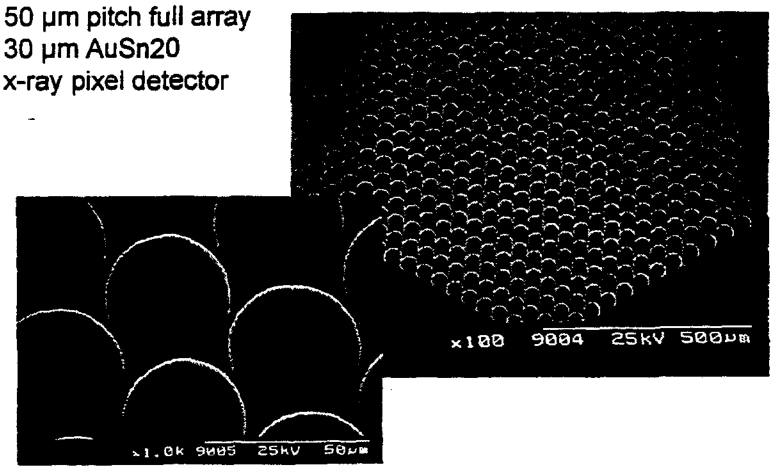
Solder Bumping

Electroplated Bumps

- 50 µm pitch full array
- 30 µm AuSn20
- x-ray pixel detector



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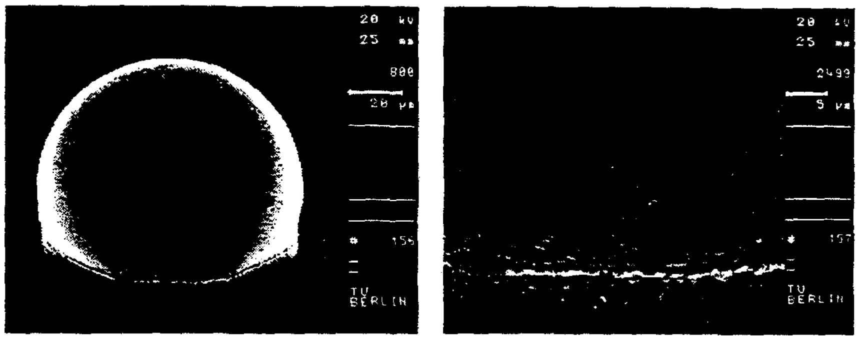
Solder Bumping Pb95Sn5



Solder Bump (Pb95Sn5) after Reflow
UBM: Ti:W/Cu / ep.Cu (5µm)

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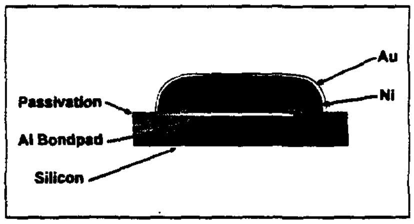
Solder Bumping

Process Flow

- **Backside Coating**
- **Passivation Cleaning**
- **Aluminum Cleaning**
- **Zincating**
- **Electroless Nickel**
- **Immersion Gold**
- **Coating Removal**



Electroless Ni/Au UBM

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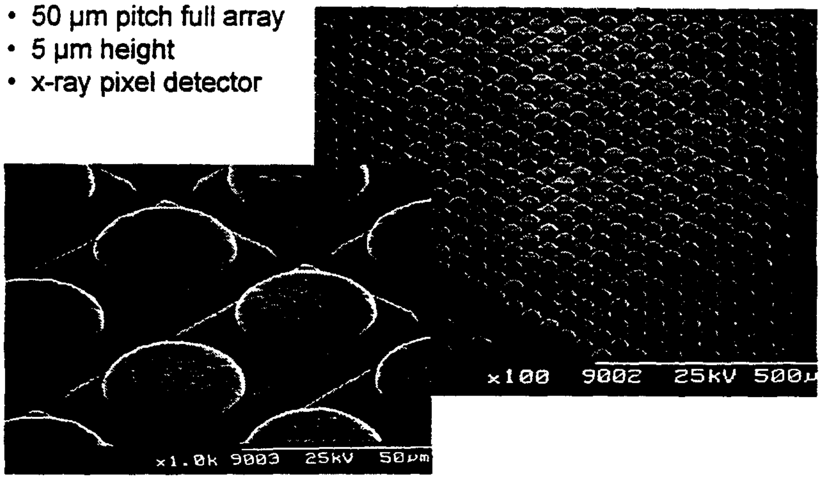
Solder Bumping

Electroless Ni/Au UBM

- 50 µm pitch full array
- 5 µm height
- x-ray pixel detector



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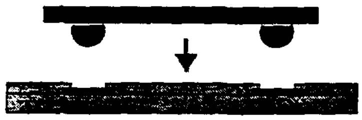
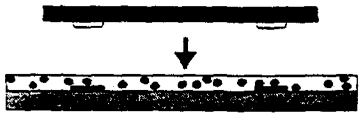
Flip Chip Assembly

Flip Chip Techniques

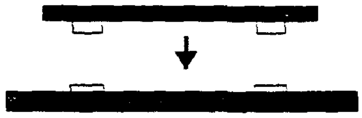
soldering
UBMs: TiWCu, CrCu, NiAu
solders: Pb40Sn60, Pb95Sn5, SnAg, AuSn, In
substrates: ceramics, FR4, flex



adhesive joining
bumps: Au, Ni/Au
adhesives: isotropic, anisotropic
substrates: glass, flex, FR4



thermo-compression
bumps: Au
substrate: silicon, ceramics



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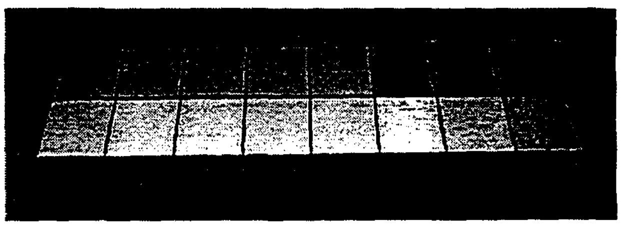
Flip Chip Assembly /1/

Pixel Detector Module
Detector substrate: 61.440 I/Os,

electroless Ni/Au (version 1)
electroplated Ti:W/Cu (version 2)

16 Read-Out Chips
24 rows, 160 I/Os

50 µm x 300 µm pitch
Solder Bumps: Ti:W/Cu - ep.Cu - PbSn



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Pixel Detector Module

Detector Tile 1 (Chip-Up)	62.4 x 17.0 mm², chip/detector ratio: 112 %
Detector Tile 2 (Chip-Down)	62.4 x 24.4 mm², chip/detector ratio: 78 %
Read-Out Electronic Chips	7.4 x 10.0 mm²
Chips per Module	16
Chip to Chip Distance	200 µm
Pixel Cells per Module	61.440
I/O Pattern (equal to Pixel Size)	50 x 300 µm
Total Numbers (3 Barrels)	2.37 m² Module Area, 1,534 Detector Modules 24,544 Read-Out Chips 94,248,960 I/O's

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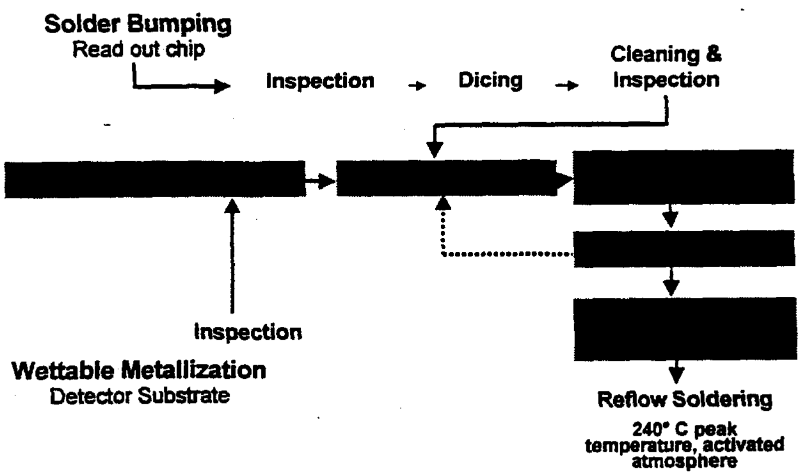
Flip Chip Assembly

Process Flow



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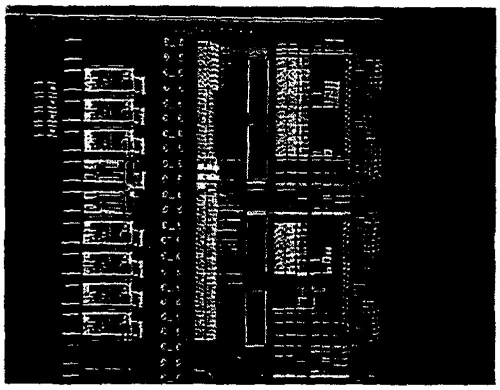
Flip Chip Assembly



Read out die flip chip bonded on Si-detector substrate

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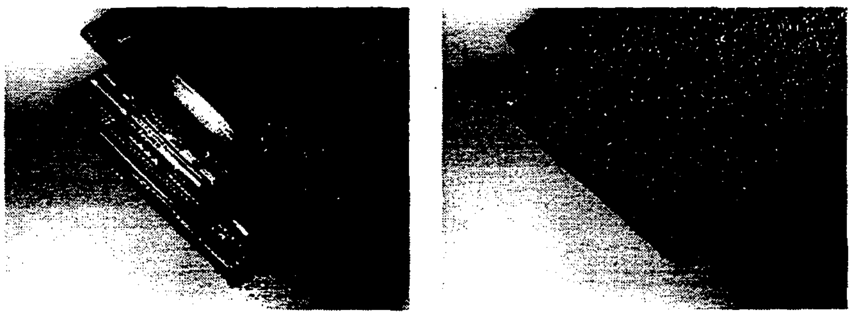
Bonn

Flip Chip Assembly



Read out die flip chip bonded on Si-detector substrate (single tile)

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Bonn

Flip Chip Assembly - Yield /1/

Electroless Ni/Au Metallization

Yield Evaluation of Detector Wafer by CERN partners				
wafer	bumps	failures	failure rate	remarks
-59	96,384	1	10 ppm	passivation failure (cracks)
-21	96,384	29	300 ppm	passivation failure (cracks, scratches)
-57	96,384	0	0	no failures
-22	96,384	0	0	no failures
Total	385,536	30	78 ppm	relevant failures

Electroless Nickel/Gold sensitive to passivation failures

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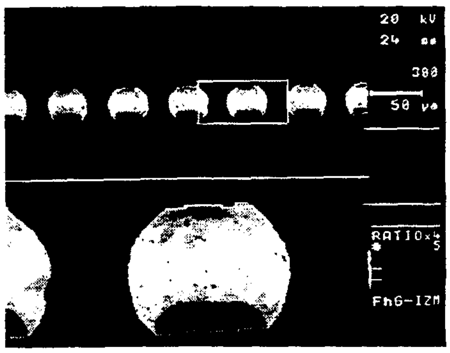
Flip Chip Assembly /1/



Chip wafer
UBM: Ti:W/Cu - ep. Cu
solder PbSn (eutect.)

Detector Si Substrate
passivation: Si_3N_4
wettable metallization:
electroless Ni /Au

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Flip Chip Assembly - Yield /2/

Overall Yield Evaluation of the Assembled Module by CERN partners				
substrate	**metallization**	**tests points**	**failures**	**failure rate**
-21	Ni/Au	25,920	2	77 ppm
-22	Ni/Au	25,920	0	0
-59	Ni/Au	25,920	2	77 ppm
-28	Cu	25,920	0	0
-17	Cu	25,920	0	0
Total		129,600	4	31 ppm

Overall yield includes
substrate, bumping and assembly yield

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Flip Chip Assembly - Multilayer Substrate

Chip
Al /(Cu) routing, passivation
Bump:Solder PbSn (eutect.)
UBM: Ti:W/Cu - ep. Cu
Si Substrate
Multilayer of 5 metal & 5 dielectric layers
Dielectric: Photo-BCB: 5 µm thick, 25 µm vias
Metallization: Ti:W/Cu - ep. Cu (2 µm)

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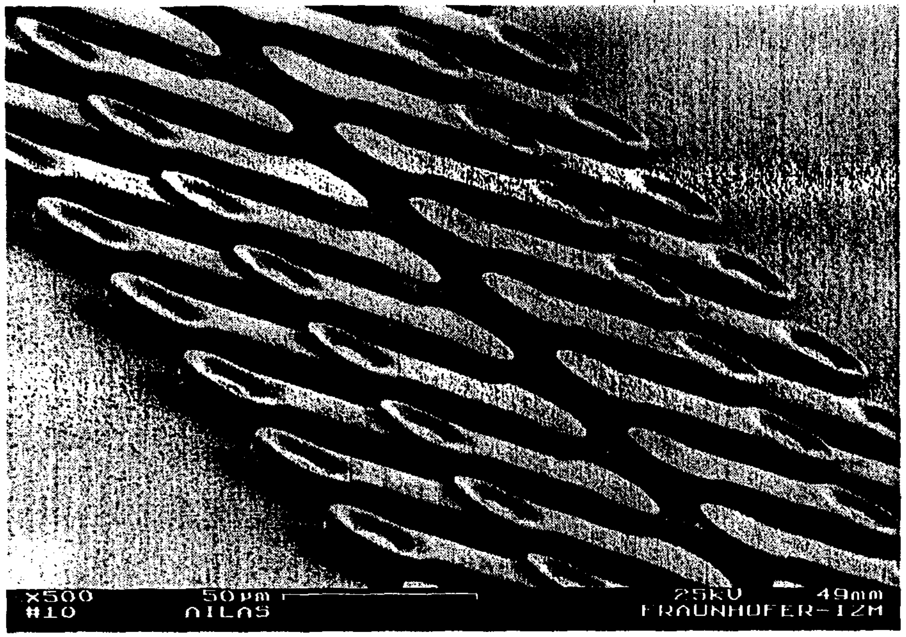
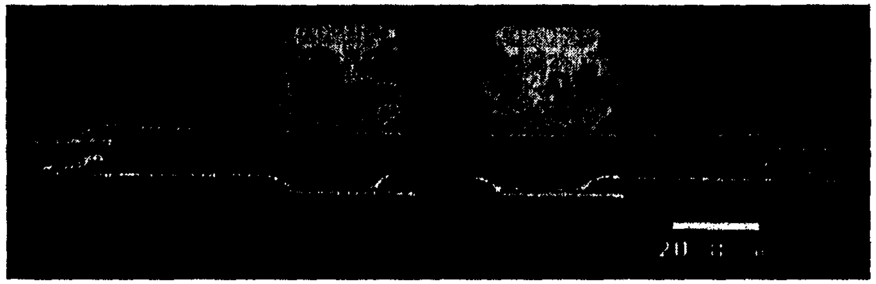
MCM-D Technology - High Dense Flip Chip





Multilayer of 5 metal & 5 dielectric layers
Dielectric: Photo-BCB: 5 µm thick, 25 µm vias
Metallization: Ti:W/Cu - ep. Cu (2 µm)

ATLAS Pixel Detector Collaboration

MCM-D Technology

Via Yield for Multilayer Substrate

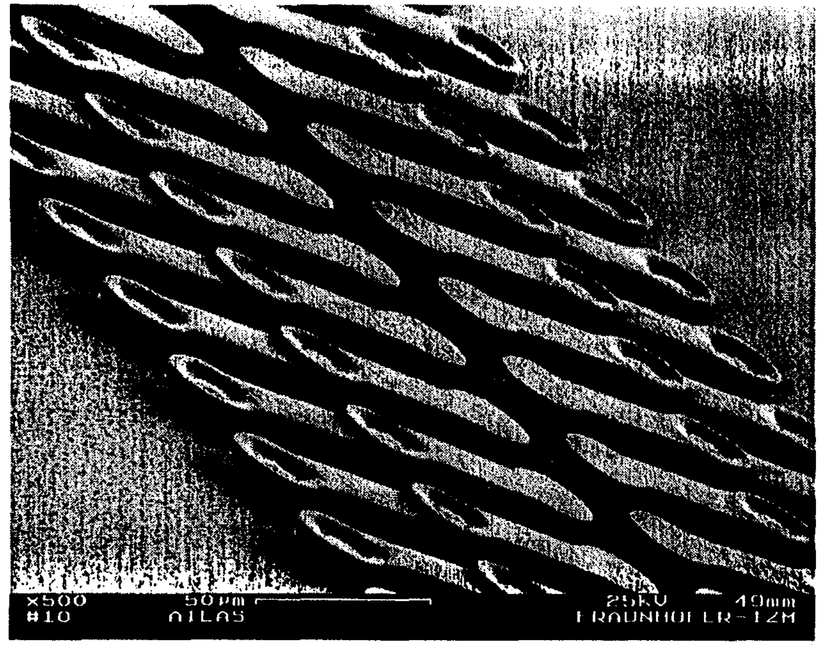
160 substrate contacts per row
x 18 rows per chip
= 2880 contacts per chip
x 16 chips per tile
= 46080 contacts per tile
x 6 tiles measured
= 276 480 contacts
x 4 metallization layers

609

= 1 105 920 vias monitored

9 defects

→ **defect rate: 8.13 E-6**



Multilayer of 5 metal and 5 dielectric layers
[dielectric BCB etched for visualization]

TRONIC'S microsystems

Electrolityc Flip-Chip Technology for Large Particle Detector

Dr. Stéphane RENARD - CEO

TRONIC'S MICROSYSTEMS S.A.
15, rue des Martyrs
F - 38054 GRENOBLE CEDEX 9
FRANCE

Phone : +33 4 76 88 56 86
Fax : +33 4 76 88 54 04
e-mail : Stephane.Renard@cea.fr

TRONIC'S microsystems

Electrolityc Flip-Chip Technology for Large Particle Detector

CEA/LETI - Flip Chip technology developing since 1991

- Two different technologies :
  - Lift-off ++ pitch < 50 µm -- high cost
  - electroplating -- pitch > 50 µm ++ low cost
- Many prototype devices have been achieved :
  - Infra-Red detectors
  - X and Gamma detectors
  - Chip on glass for flat-panel-displays drivers
  - High resolution MCM's

Electrolityc Flip-Chip Technology for Large Particle Detector

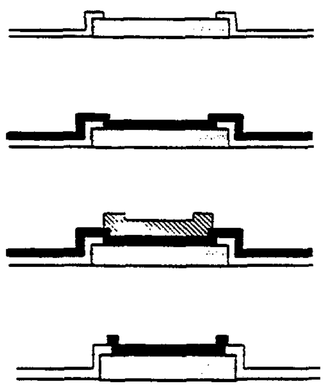
TRONIC'S MICROSYSTEMS S.A.

Start up company from LETI, created in May 97.
Production facilities shared with CEA/LETI.

- Activities
  - Wafer manufacturing of sensing elements (pressure, acceleration, magnetic field...) for microsystems.
  - Bumping of IC wafers and high resolution MCM's.
  - Medical microsystems under development.
- Active technologies
  - Silicon Bulk Micromachining
  - Epi SOI Surface Micromachining
  - Electroplating Sn/Pb or In for Flip-Chip Technologies

Process Flow Chart (1)

- IC Aluminum Pad Cleaning
- TiNiAu Sputtering Deposition
- Resist Coating, Insulation and Development
- TiNiAu Etching



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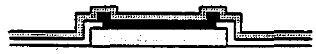
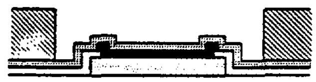
Process Flow Chart (2)

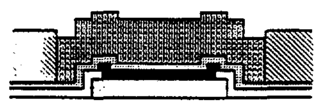
- Thin Metallic Layer Deposition



- Thick Resist Coating, Insulation and Development



- Solder Electroplating



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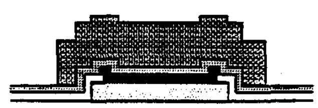
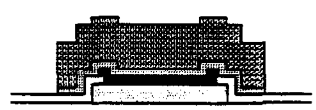
Process Flow Chart (3)

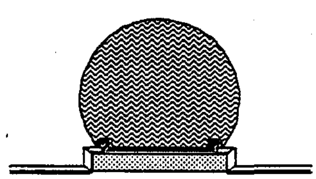
- Resist Stripping



- Thin Metallic Layer Etching

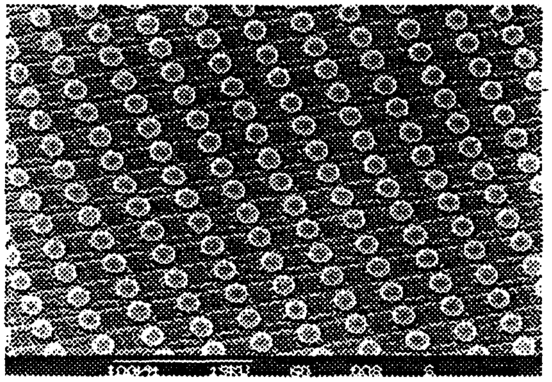


- Solder Fusing



TRONIC'S microsystems

Electrolityc Flip-Chip Technology for Large Particle Detector



S.E.M. VIEWGRAPH OF A BUMP ARRAY ON IC

TRONIC'S microsystems

Electrolityc Flip-Chip Technology for Large Particle Detector

TRONIC'S / CPPM COLLABORATION FOR ATLAS PIXEL DETECTORS

	Detector size (mm)	Read-out IC size (mm)	Wire bonding
[illegible]	[illegible]	[illegible]	On the read-out chip
[illegible]	[illegible]	[illegible]	On the detector

Each IC comprises 18 rows of 162 bonding pads

Pad pitch : 50 µm Detector thickness : 300 / 200 µm
Row pitch : 400 µm IC thickness : 500 / 300 µm

Number of pads / detector : 46 656

TRONIC'S microsystems

Electrolityc Flip-Chip Technology for Large Particle Detector

Conclusion

- The characterization results show only a few ponctual defects per detector
- Electroplating flip chip technology process is a good candidate for bump-bonding Atlas pixel detector

09/05/98 PIXEL 98 9

Inner Tracker and L1 Trigger Based on Pixel Detectors for DØ$\tilde{3}$3

Sudhindra Mani
University of California, Davis
Meenakshi Narain
Fermi National Accelerator Laboratory

1 Introduction

The upgraded DØ detector [1] for run II will have a new magnetic tracker in the cylindrical volume of 1 m diameter within the calorimeter cryostat. The pattern recogniton will be done by the outer scintillating fibers, while the inner silicon strip tracker will be used to reconstruct the various interaction and decay vertices in the event. Both of these trackers contribute to the momentum resolution of the device.

The fiber tracker is also used to form a level 1 (L1) lepton trigger based on the presence of a high p_T track in coincidence with either an electromagnetic shower or a track-stub in the muon system [2]. The tracker trigger itself is formed by requiring simple coincidences amongst binary signals from the scintillating fibers. It is a massively parallel and pipelined (fully synchronous) system that is implemented in commercial FPGA's [3].

Occupancy related problems for this trigger have been seen in our simulations for luminosities exceeding $10^{32}s^{-1}cm^{-2}$ at a 396 ns beam crossing interval,or equivalently, an average of 3 or more interactions per crossing. With the proposed increase in luminosity to $10^{33}s^{-1}cm^{-2}$ in run III (albeit, with a 132 ns crossing time), the occupancy related problems will resurface, even with the so-called luminosity levelling scheme. Furthermore, higher radiation levels will damage some tracker components beyond their tolerance limits.

Introducing silicon pixel detectors into the inner most layers of the tracker solves both problems, namely, radiation damage and high occupancy. The DØ collaboration has proposed a pixel based tracker for the region inside a radius of 10 cm [4]. Figure 1 shows the redistribution of technologies employed within the tracker volume. In this article we discuss some key technical aspects of a strawman design for the inner pixel tracker.

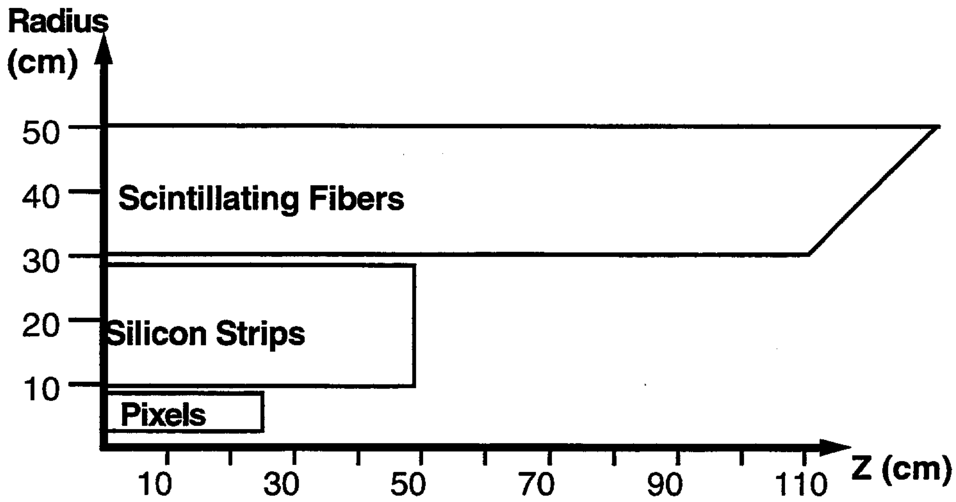


Figure 1: Strawman Tracker for DØ33. The inner fiber layers have been replaced by silicon strips which have themselves moved radially to make room for inner pixel layers. Forward tracker components are not shown.

2 Track Trigger Issues

It is desirable to solve the occupancy problems at the *L1 trigger level* as well. Hence, we also examine the possibility of having an L0 trigger pickoff in the pixel detector readout and feeding those data into the fiber tracker trigger electronics to arrive at a composite L1 trigger.

Recent studies within DØ [6] have shown that a silicon tracker based L2 trigger (STT) can be used for selecting events containing secondary vertices, thereby providing samples rich in various physics processes. The data from the silicon can also be used to find the higher p_T primary interaction vertex along the beam direction in the presence of multiple interactions [7]. Encouraged by these findings, we have been led to consider such a trigger using data from pixels. This will naturally lead to implementing a b-quark trigger which in conjunction with the presence of high p_T jets and/or missing E_T will be able to recognize, for example, production of top quarks, massive vector bosons, SUSY particles or Higgs.

We note that with adequate segmentation a pixel tracker can maintain the tracking resolution (especially at L1, where only binary data are available) that is provided by the fiber tracker of run II. The fiber tracker has a 30 cm radial lever arm and a 900 micron segmentation along the azimuth in each layer. Simple scaling (ignoring the effects of multiple coulomb scattering for tracks above 10 GeV/c) shows that a pixel tracker with a 30 micron segmentation will require a 5.4 cm lever arm to obtain the same sagitta resolution. Hence, if the inner detectors are placed at a radius of 2.3 cm, the entire pixel tracker will fit well inside the designated 10 cm radius, leaving about 2.3 cm for cable routing. This is shown in figure 2 and described in detail later. Hence, it can be argued that if the technology can acheive this 30 micron pitch, pixels will be able to augment the fibers as the trigger element for high p_T leptons. Of course, with at least an order of magnitude more detection elements, the pixels will have substantially higher pattern recognition power compared to fibers.

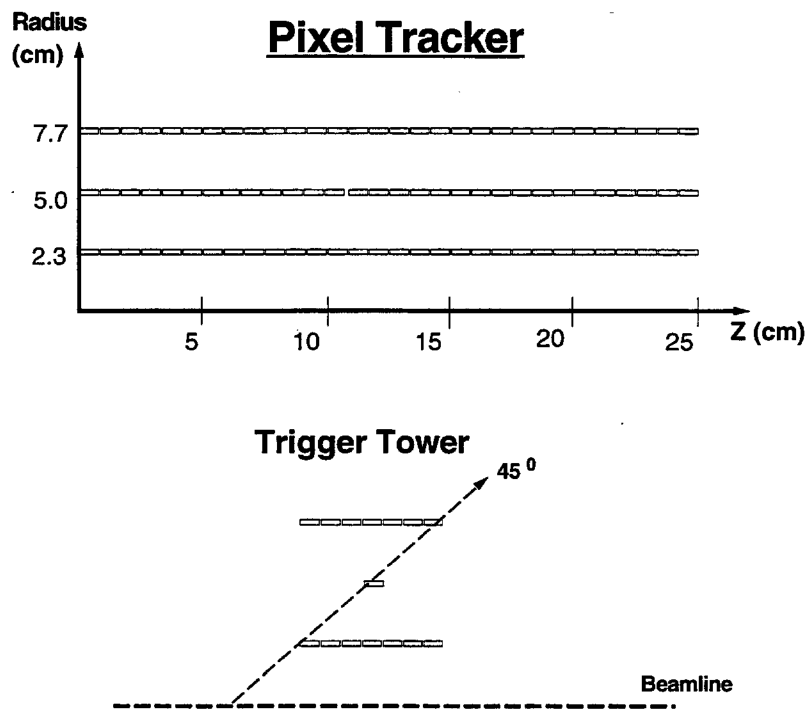


Figure 2: A 3 layer pixel tracker layout composed of $1cm^2$ tiles. Logical towers can be defined for triggering purposes.

We further argue that these improvements to the trigger should be implemented at L1 because DØ has a limited bandwidth ($<$ 10 kHz design goal for run II) into L2. It is likely that in run III we will continue to use trigger strategies similar to run II, ie, build L1 triggers using information from the calorimeter, muon system and the fiber tracker. The minimal high-p_T trigger menu is expected to require a bandwidth at the L1 trigger close to 5kHz during run II.

Various Tevatron running scenarios during run III indicate a dramatic increase (upto a factor of 4) in the expected number of events per crossing compared to run II. All triggers which incorporate a term based on calorimeter information are expected to increase by 30–40% for an average of 5 interactions per crossing. However, we expect rather large increases (factors of 4-10) in muon and CFT based triggers. This would result in the high p_T menu requiring a bandwidth of at least 15–20 kHz at the L1 trigger stage, which is currently a factor of 1.5–2 larger than the design goals of the L1 trigger system. Hence, only a higher rejection at a lower trigger level allows us to avoid prescaling and write all interesting physics events to tape.

The muon and CFT based triggers suffer a loss of rejection power primarily due to high occupancy with increasing number of interactions in the event. Adding information from the pixel tracker will be beneficial in alleviating this problem by improving the pattern recognition at the trigger level.

In summary, a pixel tracker not only eases overall problems due to occupancy and radiation damage but, if exploited at L1, the data from the pixels add rejection power to both the CFT and the STT triggers.

3 Physics Motivation and Trigger Concept

As mentioned earlier, various studies [6] have established the usefulness of an impact parameter trigger based on including the information from the silicon tracker at the L2 stage of the trigger during run II. This information also helps achieve gains in the momentum resolution for high-p_T tracks.

The proposed pixel tracker has similar (*or better*) resolution compared to the strip tracker and hence all the studies are applicable. As is the case for tracks reconstructed at L2 in run II, we expect a pixel based trigger to improve the momentum resolution for high p_T tracks at L1. However, there is one major difference. L2 triggers in run II will operate on all tracks above some minimum p_T threshold (provided by the CFT) which can be as low as 1.5 GeV/c. The total rate at such a low threshold may be prohibitive for an L1 trigger in run III.

The L1 pixel based trigger, proposed here, is designed to provide additional power to trigger on high p_T displaced tracks from heavy quark jets. We utilize the "natural" p_T threshold of the tracker, ie, the p_T above which the tracker is unable to distinguish the track from an infinite momentum straight line. For the CFT trigger this occurs at about 11 GeV/c. Since we have scaled the pixel tracker to the CFT (see above), we can use this same threshold in our studies. The usefulness of this straight line threshold lies

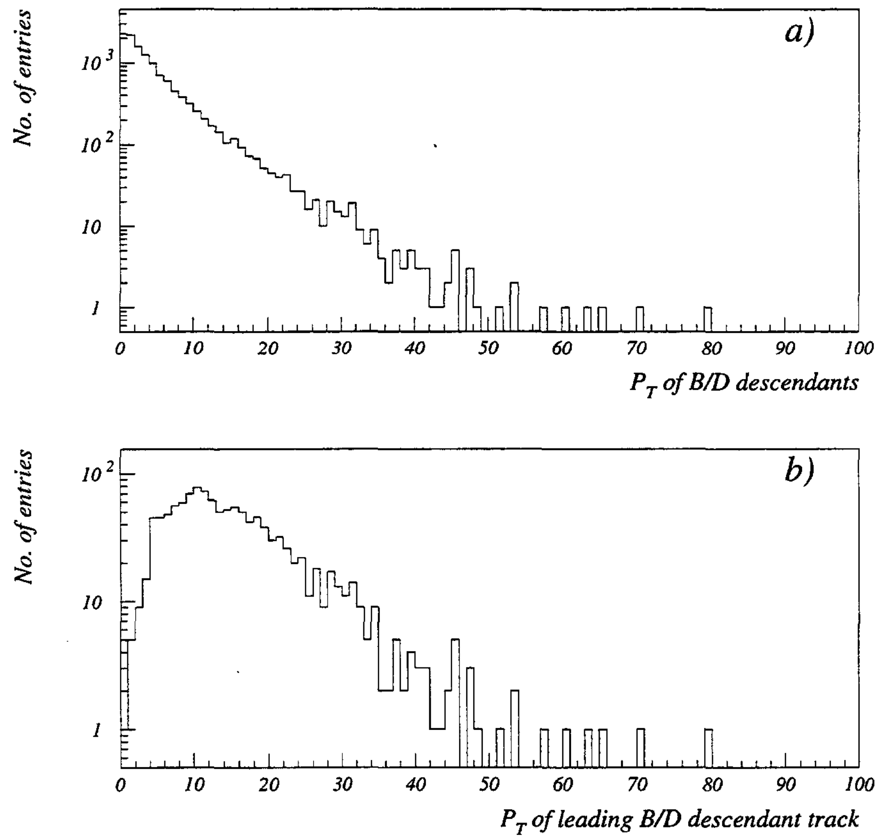


Figure 3: p_T spectrum of b- and c-quark decay products in a $t\bar{t}$ event. The top plot is for all decay partices while the bottom plot is for the leading particle.

in the simplicity of the pattern recognition which has to be performed in a few 100 ns, which is what we expect will be available out of the total effective latency of about 3 μs. The remainder of the time is spent initially in collecting the data from trigger sectors and arranging them logically and later on some more time has to be reserved for transmission delays to the trigger framework.

Since the mass scales of new physics are sufficiently high, this 11 GeV/c threshold on the track p_T does not result in intolerable inefficiencies. As an example of this, we consider the spectrum from the well known top decay. Figure 3a shows the p_T spectrum of the stable particles in the decay of the b-quark (or a subsequent c-quark) while Fig. 3b shows the spectrum for the *leading* particle. A large fraction (58%) of the spectrum is above 11

GeV/c, yielding a $t\bar{t}$ efficiency of about 82%. The overall tracker acceptance has not been taken into account in this figure.

The available q in top decay is of the order of 100 GeV, and hence new particles that have mass greater than 100 GeV and decay into b-quarks will produce a similar spectrum as the one shown in figure 3. Further studies are required to establish the efficiency of this trigger for particular models and specific channels.

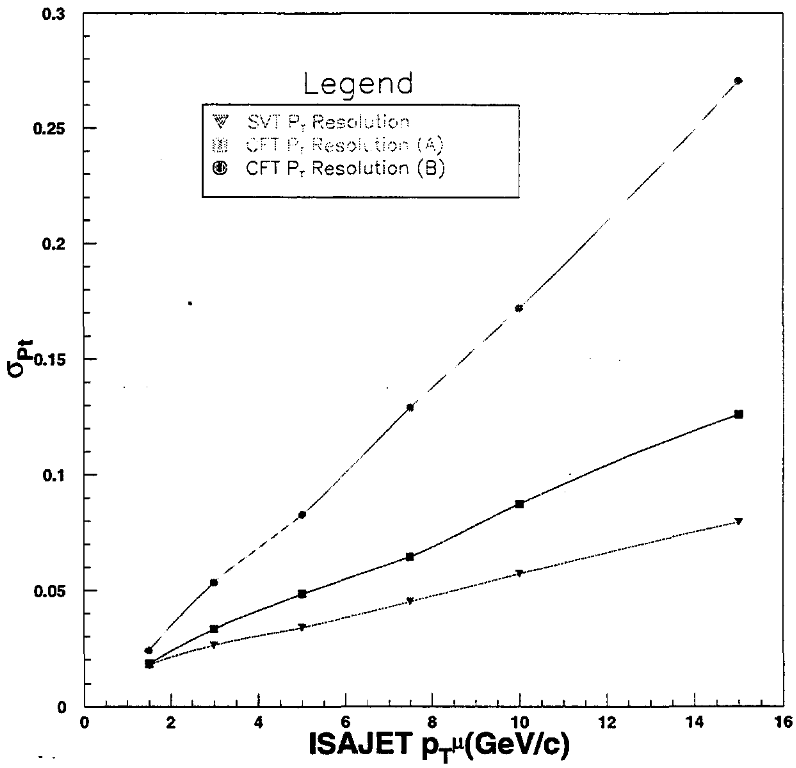


Figure 4: Momentum resolution as a function of p_T using the fiber tracker signals only (solid squares–best case scenario, solid circles–default case) compared to the resolution obtained by combining the fiber and Silicon tracker signals for DØ run II(solid inverted triangles).

3.1 Improvement in Momentum Resoultion

The silicon tracker of run II provides siginificant improvement to the momentum resolution, over that obtained from the fiber tracker alone[6]. This is shown in figure 4. This study employed single muons generated at various values of p_T in the range 1–15GeV using full GEANT simulation and digitization of the DØ run II detector. The momentum resolution obtained using only the signals from the fiber tracker are plotted using the solid squares and circles using two different implementations of the momentum determination at the trigger level. The curve with inverted triangles shows the resolution acheived by combining the signals from the silicon tracker at the L2 trigger stage. Compared to the best case scenario, for tracks above 5 GeV, the resolution improves by almost a factor of two after adding the hits from the silicon.

A 30–50% reduction in background rates is easily achieved by this improvement in momentum determination for high p_T tracks. These studies are directly applicable to the pixel tracker proposed for run III, and demonstrates that tracking points at radii of few cm are very effective in providing the longest possible lever arm within the tracker volume. We expect similar performance by including the pixel information along with the CFT signals at L1.

3.2 Displaced Track Trigger

In order to fully exploit the anticipated high luminosity during run III, it would be advantageous to enrich the data in their b quark content as early as the L1 stage. One of the primary goals of run III is to search for the Higgs or other new particles which could lead to insights into phenomena beyond the Standard Model, be it SUSY or an entirely new mechanism of electroweak symmetry breaking. Most of these models predict particles which strongly couple to b-quarks and hence lead to final states rich in b-quarks. In some cases, e.g. $WH \rightarrow q\bar{q}b\bar{b}$, triggering on events with b quark jets is the only way to reduce the trigger rate sufficiently to be able to operate an unprescaled trigger and acquire enough events to observe a signal.

Extensive feasibility studies of a displaced track trigger at the L2 trigger stage for run II have been carried out. For example, one study[6] which focusses on the advantages of such a trigger for new particle searches, B-meson physics, and measurements of the properties of the top quark, shows that a factor of 2–40 rejection of the background is easily achievable while retaining a signal efficiency of 90%–50%.

The impact parameter resolution curve is shown in figure 5. The plot is obtained from

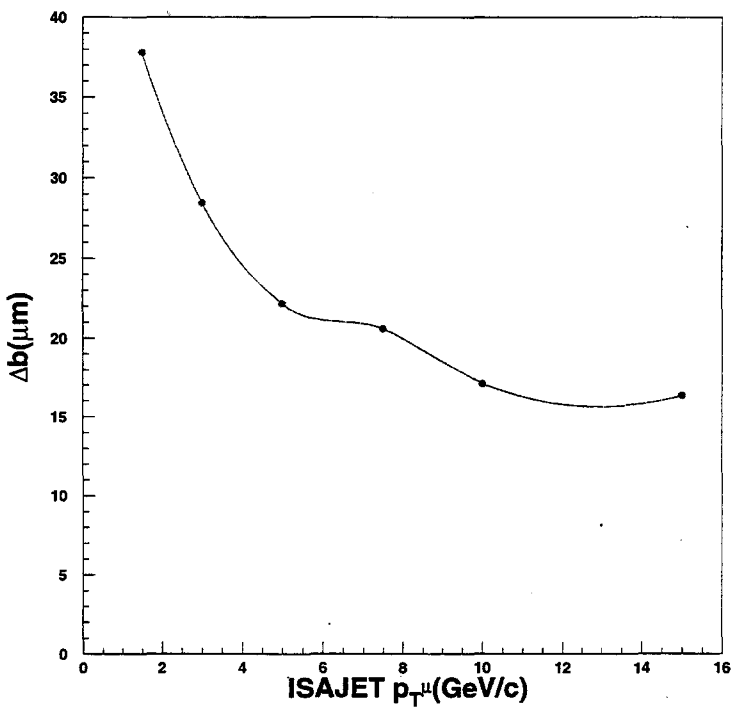


Figure 5: Impact parameter resolution as a function of track p_T for DØ run II tracker at Level 2 trigger stage. The asymptotic resolution is 15μm for tracks with high p_T. This study includes the full GEANT simulation of the DØ run II tracker.

the same GEANT sample described in the previous section. For tracks above 10 GeV the impact parameter resolution is better than 17μm, which is expected from the digital resolution of a 50μm pitch. The resolution degrades to 35μm for tracks with 2GeV p_T due to multiple scattering. The proposed L1 pixel trigger in this note will give us the same resolution for a 50μm pitch, while for a 30μm pitch, the digital resolution will improve to about 9μm. For the purpose of triggering, we have to also consider an error of about 30-40μm in the primary vertex position due to the finite width of the beam. As can be inferred, this error will dominate the overall impact parameter resolution at L1.

Table 1, summarizes the rejections expected for 80% efficiency from the impact parameter trigger at L2(L1) for various physics channels for the run II(run III) environments [6].

Trigger	factor from impact parameter trigger
$t\bar{t} \to \ell + jets$	
Use $\ell + jets$ triggers	1.5–2
$t\bar{t} \to alljets$	
Use multijet triggers	1.5–2
$W + Higgs \to \geq 4jets$	
Use 3 calorimeter jet triggers at L1*	10–20
(*Also applicable to any new particle decaying to heavy quark jets in the final state.)	

Table 1: Expected rejections for 80% efficiency from the proposed impact parameter trigger.

3.3 Secondary Vertex Determination

Triggering on the track p_T and impact parameter alone can give us enough rejection within the L1 bandwidth, provided the fake rate can be controlled. There is a component due to overlapping tracks (in the r-ϕ view) within jets which needs to be evaluated for the pixel tracker. We expect this to be small due to the very low occupancy in this detector. However, we propose to further enhance the rejection factor by employing simple algorithms for secondary vertex finding.

Figure 6a shows the impact parameter distribution for all tracks from the b-quark jet in a top quark decay. Figure 6b shows this for the leading particle only. It is interesting to note that while there is a substantial population above 100 microns, the impact parameter of the leading particle is well contained within about 1 mm. Hence, this track will provide discrimination over other high p_T tracks coming from light quark jets, but with a loss in efficiency if we cut, say, at 150 microns. However, this track is a very good measure of the b-quark *direction* and we hope to use this fact in our simple algorithm.

Hence, instead of imposing an impact parameter cut on this track, we propose to use it as a "seed" for secondary vertex finding. Depending on the amount of information available, this can be done only in the r-ϕ view, or in the r-z view as well. In the r-ϕ view, the computation is more complicated because the other tracks in the decay will have some curvature and the FPGA equation count may be prohibitive.

In the r-z view, all the other tracks (straight lines) will intersect this track at some

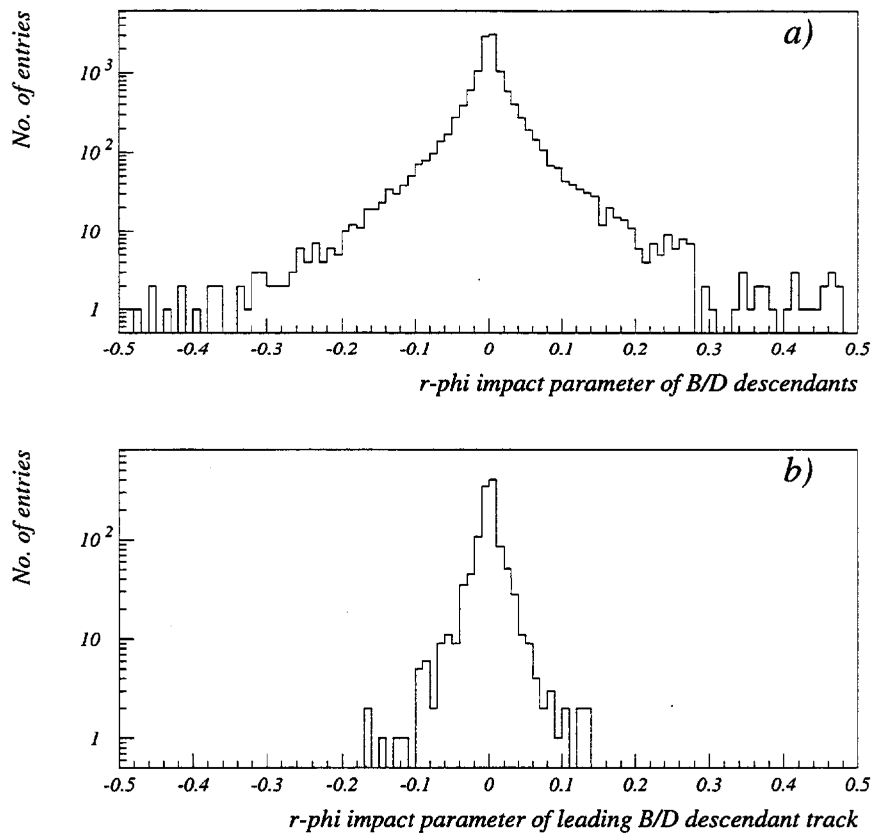


Figure 6: Impact parameter distribution of the decays products in a $t\bar{t}$ event. The top plot is for all decay partices while the bottom plot is for the leading particle.

point. If we restrict ourselves only to tracks inside a local sector then the sample will be rich with decay products of the b-quark, if it indeed was the parent of the high p_T track. The centroid of the intersection points of all tracks with the seed track direction will be a measure of the vertex point, as shown schematically in figure 7. We expect that tracks in light quark jets will average out and the centroid will be formed near the interaction region while the heavy quark jets will produce a displaced centroid. Effects of multiple coulomb scattering will smear the measuremnt somewhat but we are encouraged by a similar study [7] done for the silicon strip detector which showed promising results.

Other backgrounds to an inclusive b-quark trigger, mainly from mismeasured light quark jets and from charm jets, have been evaluated in the STT studies and have been

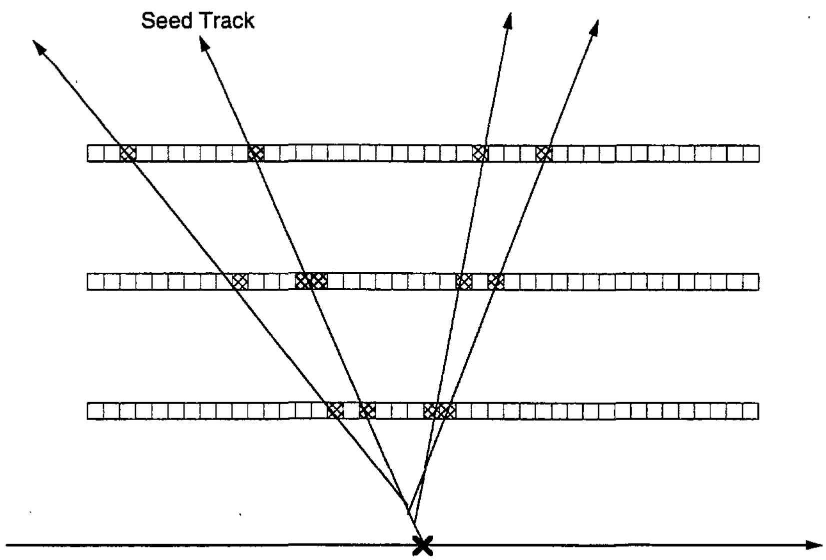


Figure 7: A schematic representation in the r-z view of a trigger tower after having found the seed track in the r-ϕ view of the pixels. The high p_T seed track and several secondary tracks are shown to form a secondary vertex.

found to be controllable. The situation only improves at the higher threshold considered here.

Various triggering schemes and electronic designs based on FPGA's and DSP's are being developed and will be the subject of a subsequent note. As will be discussed later, the feasibility of this trigger will to some extent dictate the readout architecture and hence it has to be evaluated in detail. The bare minimum requirements for the necessary readout electronics is described in section 5. Next, we present simulations of the proposed geometry and the expected rates.

4 Tracker Geometry and Rate Simulations

The pixel tracker shown in figure 1 has to be constructed using "tiles" of pixel detectors that are limited in area to about $1cm^2$ due to the yield limitations of most fabrication technologies. Figure 2 shows this construction using tiles measuring 11 mm x 9.8 mm. These dimensions are based on conservative estimates and will be described later. The figure 2 also shows a typical "logical" trigger tower. These towers are keyed to tiles in the middle layer and combined with 7 tiles each in the other two layers. This geometry provides full acceptance for all straight line tracks produced with an angle within $\pm 45^o$

for all vertices inside $\pm 22cm$ along the beamline. There is partial acceptance for vertices outside of this region.

There are two reasons for this tower geometry. First, it reduces the amount of data presented to one unit of trigger electronics and second, it greatly reduces fake backgrounds due to overlapping tracks. Once, the data have been contained within towers the trigger can operate in the r-ϕ view only. Hence, at the minimum, the pixel detectors will be required to provide only two pieces of information at L1, a chip ID and the ϕ coordinate of the hit. This information will be sufficient to construct logical towers in the trigger electronics and finding straight line tracks will be accomplished by forming simple coincidences.

The main goal of the simulations presented here is to answer questions related to data rate, dead-time, inefficiencies etc., parameters that will help in the design of the readout architecture. The plots shown have been generated using the present geometry of the silicon strip detectors planned for the run II upgrade. This geometry is similar enough to the pixel tracker that first order results can be readily obtained from existing simulation runs. Full GEANT has been employed and pile-up of variable number of interactions in a bunch crossing has been simulated.

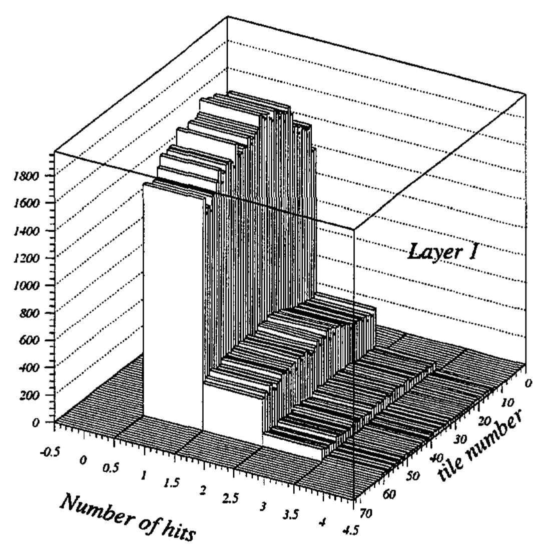


Figure 8: A lego plot of cluster occupancy per pixel tile for the inner most layer. The tiles are numbered from 13 to 60 representing z positions from -24 cm to +24 cm. Tiles with zero hits have been suppressed.

Due to the geometry of double sided silicon (50 micron ϕ strips and 150 micron z strips) a pixel size of 50x150 μm^2 is a natural choice. The estimates of hit rates will have only a weak dependence on this choice due to charge sharing among pixels. For example, 30x300 μm^2 pixels, proposed in the next section, will have a slightly higher hit rate. In order to avoid this problem, we have used "clusters" to estimate the hit rate and then scaled it by a factor of 3 to obtain the pixel hit rate. As a reference, simulations for CMS have yielded a value of 2.7 for this scaling factor.

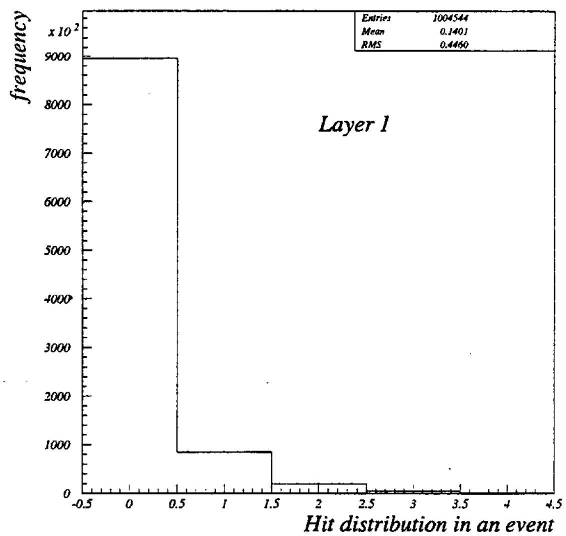


Figure 9: A histogram of cluster occupancy for the inner most layer. The mean occupany for a tile is about 0.14 per crossing.

The silicon tracker ladders were divided into 12 sections, each 1 cm along the z direction, to make "tiles". The width of these tiles is 2.2 cm, twice as wide as the proposed pixel tiles. Figure 8 shows the cluster occupancy for the innermost layer. The tiles have been binned along z into 72 bins representing 6 barrel wheels of 12 cm length each. The first layer does not have the first and the sixth wheels, hence only tile numbers 13 to 60 are plotted. Tiles with no hits in a given event have been suppressed. It can be seen that there is only a slight z dependence in the occpancy.

In figure 9, the occupancy is histogrammed after including the zero bins. From this plot we can read that the average occupancy for a tile in the inner layer is about 0.14 clusters. After using the factor of 3 scaling for charge sharing (and 1/2 for twice the area), this amounts to about 0.2 hits per crossing. For the third layer, the average turns out to

Radius	1 Int	3 Int	6 int
2.5 cm	0.15	0.3	0.6
7.5 cm	0.03	0.08	0.2

Table 2: Hit pixels per sq cm for inner and outer layers.

be about 0.15 hits per crossing.

Table 2 contains the data rate as a fuction of the number of interactions in a bunch crossing and the radial position of the detector. The rate has been averaged over $\pm 25cm$ in z. The scaling factors mentioned above have been included.

As can be seen, for the average case of 6 interactions/crossing (for luminosity levelled TeV33), the number of hit cells is less than 1 at the innermost layer. This implies that if we limit the number of transmitted hits (at L0) from each readout chip to be no more than say, 4, the resulting loss will be negligible. Figure 10 is the same as figure 9, except that the zero bin has been suppressed. As can be seen the distribution has very little population above 4 hits.

Next, we estimate the probability for a pixel unit cell to be hit twice within the L1 latency, ie, 32 bunch crossings. For the worst case of large area unit cells (assuming 50x400 μm^2) at the innermost radius, we get 0.6 hits being shared by 5,000 cells per crossing. This is a rate of $1.2x10^{-4}$ hits per cell per crossing. This implies that the probability for being hit twice within 32 crossings is about 0.4%. For the proposed size of 30x300 μm^2 this propability drops to about 0.2%.

In summary, we conclude that the pixel detectors can be used as an L1 device provided that they can transmit the digital addresses of an average (maximum) of 0.6 (4.0) unit cells per crossing. Additional information such as the pulse height can be stored in the unit cell provided we are prepared to accept a corruption of 0.2% of the data due to multiple hits. These two numbers have a major influence on the readout architecture discussed in section 6. Next, we discuss more detailed parameters of the pixel detector.

5 Pixel Detector Design

The most important design parameter that makes DØ different from other efforts at LHC is the substantially longer bunch crossing interval. Other differences include 1) finer segmentation, 2) L0 trigger pick-off and 3) acceptable deadtime due to L1 readout.

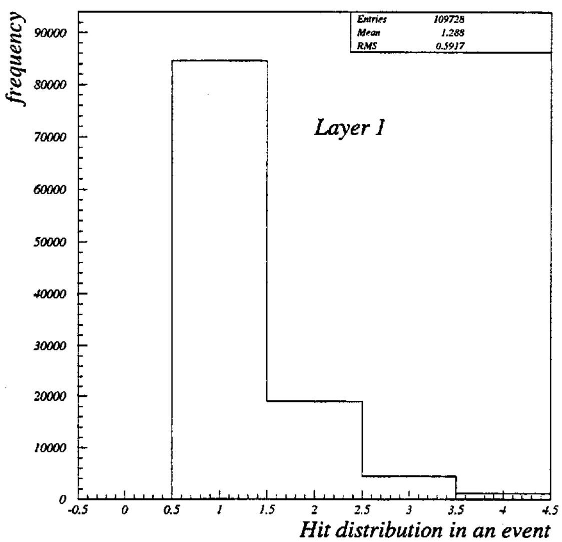


Figure 10: The cluster occupancy per tile for layer 1 where the zero bin has been suppressed. The tail above 4 hits is negligible.

We have arrived at a conceptual layout of the pixel readout chip as shown in figure 11. The chip consists of 32 columns and 256 rows. The row pitch is 30 microns and the column pitch is 300 microns. Four tiles constitute a ladder which is approximately 1.6 cm wide by 4 cm long and shares a common data bus. Below we clarify various design features that were kept in mind in order to arrive at this layout:

- A 30 micron pitch is desirable in order to match the fiber tracker momentum resolution at L1. If bump-bonding or other technical reasons render 50 microns (or higher) as the achievable pitch, we will have to correspondingly (square-root of ratios) increase the lever arm. This results in proportionately higher costs.
- Binary information from the pixels at L0 is desirable. This requires a so-called data push architecture (DPA) design [8]. An asynchronous DPA chip transfers all hits to the outside world much like a wire chamber would except here the data arrive sequentially and in digitized form. Usually, each hit results in the measurement of a 4-dimesional point and transmission of a data-packet consisting of a time-stamp, a column address and a row address. The asynchronous operation also implies that hits are not necessarily transmitted in a time-ordered sequence. Various readout designs exist (for SSC or LHC) that employ a DPA like scheme [9][8] but these were

designed for much higher bunch crossing frequencies. A chip designed for Fermilab should be able to operate *synchronously* as described below.

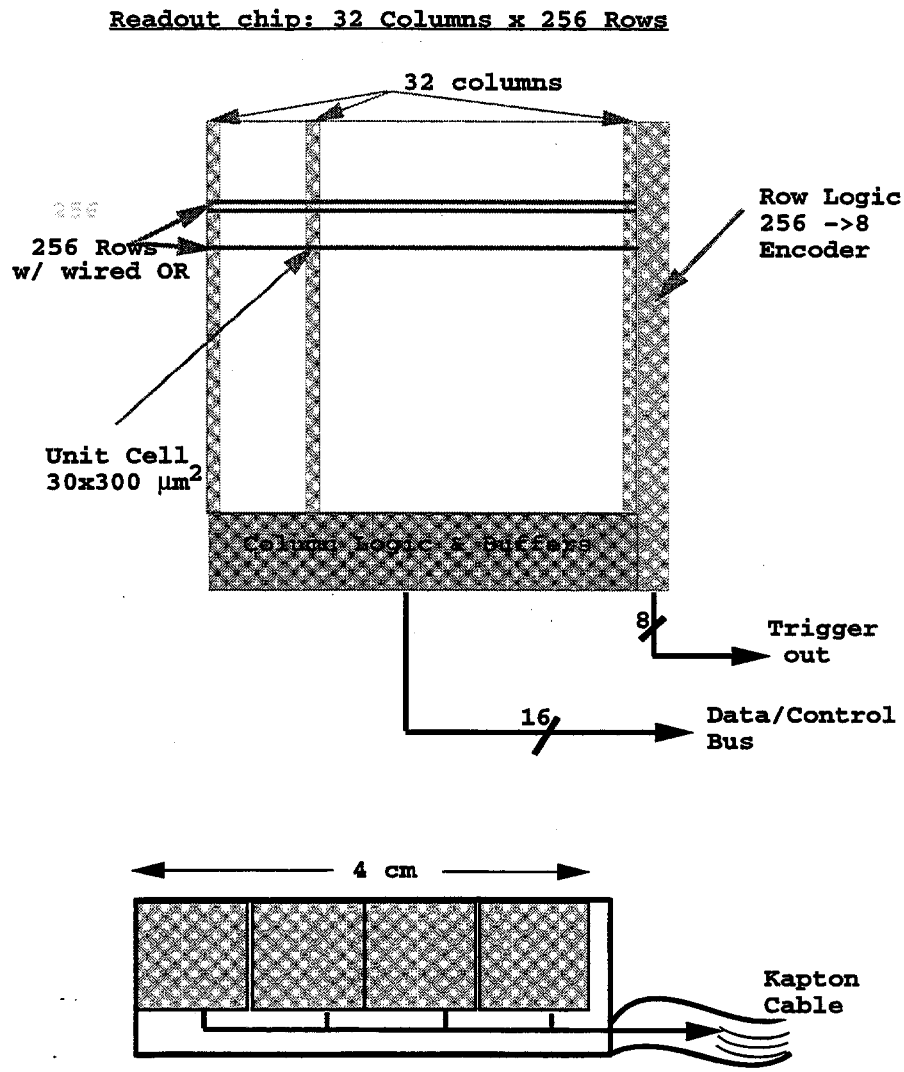


Figure 11: Conceptual design of a pixel readout chip. The architecture is column-based data-push. There is no Column OR signal but a Row OR is implemented for trigger purposes. A ladder using 4 tiles and a common data bus is also shown.

- For DØ a simplification to the DPA design would be to only transmit an OR of pixel row (ie,narrow dimension) addresses. This would reduce the L0 data rate by more than a factor of 2 primarily because of column address suppression and somewhat more because of occasional double hits in a row. The wired OR can in principle be bridged over say, 4 chips, and be as long as 4 cm. This has led us to consider a 4 cm long ladder; the exact specification will be determined based on data transmission capabilities of the bus.

- Maintaining the fully synchronous nature of the L1 trigger in DØ is essential. For a DPA design, this will result in some loss of trigger data for unusually busy events wherein we will have to truncate the list of hits. An acceptable cutoff, determined from simulations, is at a maximum of 4 hits per crossing per readout chip. Once again, a row OR will suffer much less from these truncations.

- DØ data acquisition is not dead-timeless. Both the calorimeter and tracker incur deadtime of about $5\mu s$ for every L1 trigger. For an L1 rate of $< 10kHz$, this results in no more than about 8% dead-time. Hence, unit cells in the pixel readout can be used for data storage during L1 latency, provided the readout at L1 can be performed in less than $5\mu s$. An example of the data stored in the unit cell would be its pulse height and a time-stamp (or equivalently, a pointer to a bunch crossing buffer memory location.)

- Due to limited access for services into the inner tracker, keeping the power load to a minimum is very important. A desired goal would be to keep the dissipation below 0.25 watts/cm^2. This level has been acheived by various groups designing readout chips.

- For reasons of minimizing mass, the number of cables (eg, kapton) also have to be minimized. Hence, a general rule of making all busses bi-directional (for downloading and for readout) is advisable. However, due to speed considerations, the L0 trigger path will probably have to be separate. Hence, we suggest that each readout unit compress (ie, sparsify and encode) its information into 8-bit words for transmission on a common *serial* bus during L1 readout. For now we consider a 16-bit wide bus to the end of the ladder where the conversion to a serial transmission can occur. The trigger bus, however, would be an 8-bit dedicated bus for each ladder.

- Use of fiber optics similar to that planned for the LHC would be very useful. As a rough estimate, the pixel tracker would require one kapton cable per 1.6 x 4 cm ladder as compared to the run II silicon tracker which sends out one kapton cable per 12 cm x 2.2 cm ladder. Hence, the cable plant for this pixel tracker would be about a factor of 4 bigger for each barrel. Even though the number of barrels in pixels would be less, and some reduction in number of traces is possible, kapton is a cumbersome medium and fibers are preferrable.

Keeping these points in mind, we have designed a readout architecture and generated preliminary specifications. This is described in the next section.

6 Readout Architecture

The following architecture is a blend of various designs already being developed. It is a column-based architecture adapted for the longer bunch crossing interval. The column periphery is greatly reduced because the data storage is implemented in the unit cells. The acquisition sequence is broken up into read and write cycles which do not occur simultaneously, and hence avoid interference. Furthermore, the digital and analog parts of the write cycle are also separated in time to reduce cross-talk. Below we describe the architecture. It is useful to remember that the rows are the narrow dimension and the columns are the wide dimension.

6.1 Write Cycle

The write cycle is the "live" mode for the detector and consists of the following functions:

Analog Cycle The analog block of the unit cell collects the input charge and fires a discriminator no later than T0 + 38 ns (two ticks of beam clock). This limitation on allowed time-walk, frees up 5 clock ticks for the digital cycle. Also, it is larger than the 25 ns requirement for LHC detectors and hence, it is hoped that there will be some saving in the power dissipation in the unit cell compared to those designs (time-walk, noise and power dissipation are all related specifications).

Digital Cycle 1 The presence of a discriminator "true" is recorded by the Row-periphery via a hard wired OR along the rows. The digital block of the unit cell latches a 6-bit gray-code number into a local register. This value which corresponds to a bunch crossing number between 0-31 is available to each cell over common bus lines. The number is updated at the start of the 3rd tick (38 ns) of the beam clock in order to avoid interference with the functioning of the analog block. The call also stores its analog pulse height on a local capacitor.

The "hit" cell can now be dead for the next 32 crossings. The loss due to this is minimal as shown in our rate simulations. In the rare case that the cell has a latched value from some previous crossing, it is overwritten. Meanwhile, a digital comparator compares the latched value to the current crossing number, and resets the unit cell if the numbers match, indicating that 32 crossings have elapsed. Hence, a unit cell stays disabled for 32 crossings after being hit and then resets itself.

In case an L1 trigger is received during these 32 crossings, all hit cells arm themselves for a "read" cycle. This is described later.

In summary, the digital part of the unit cell has three modes, "set", "reset" and "read". During "reset", it waits for the discriminator to fire and if so, enters the "set" mode. During "set" it checks every bunch crossing to either a) reset itself if 32 crossings have elapsed or b) look for an L1 trigger in which case it arms the token stop circuitry and enters the "read" mode. During "read" it waits for the arrival of the token to initiate readout. During both "set" and "read" the discriminator is disabled. These logical functions are performed by the unit cell between T0+38 ns and T0+57 ns (3rd tick).

Digital Cycle 2 This is the trigger cycle which is fully synchronous and occurs between T0+38 ns and T0+132 ns. During this cycle, the latched hits in the row-periphery are zero-suppressed, encoded into 8-bit addresses and transmitted off-chip. This sequence has to be especially fast so as to maximize the amount of data that can be transferred in 95 ns (10 ticks for a 106 MHz clock). Since there is no analog activity during this time, the circuitry can be made as noisy and power-hungry as necessary. The output can be on an 8-bit bus, but it is desirable to reduce the number of lines and hence multi-level encoding will be very useful. We have an ambitious goal of encoding and transferring upto 6 hits in 95 ns. Preliminary circuit designs have shown that it is quite feasible.

6.2 Read Cycle

The read cycle is the main acquisition mode during which the detector is "dead". It is initiated by the arrival of an L1 trigger. The bunch crossing clock is halted, the discriminators in the unit cells are disabled and a readout token is initiated. Each latched cell compares its value to the crossing number and stops the token if they match. After a token is stopped, the unit cell transmits its own row address and pulse height to the column periphery. The row-address is burnt-in in the silicon layout and the transfer is serial. The column-periphery mainly consists of multiplexing logic. For each row-address it attaches a column-address and sends the data packet off-chip.

The output for digital data is serial. The analog data are sent in parallel on another line. The sequence of data transmission is shown in table 3.

Since the digital data for each hit will take at least 130 ns (14 bits @ 106 MHz), the analog bus should have sufficient time to settle itself to a 5-bit value. This value is digitized off-chip, most likely in a flash ADC at the end of the ladder. Commercial rad-hard ADC's

Transfer No.	Clock Tick	Digital Bus	Analog Bus
1	1	CHIP ID	
2	2	Col Address 1	Pulse Height 1
-	9	Row Address 1	
3	16	Col Address 2	Pulse Height 2
-	23	Row Address 2	
.	.	.	
.	.	.	
n+1	14n+2	Col Address n	Pulse Height n
-	14n+9	Row Address n	
n+2	15n+2	END OF DATA	

Table 3: Data sequence from a pixel tile after an L1 trigger is received.

with a 100 ns digitization time are readily available.

At the end of a read cycle, all chips are fully reset and enter the write (or, "live") mode. At this point the entire cycle is repeated.

The implementation of such a pixel readout will require the development of a suitable readout chip. A pixel readout chip called FPIX0 has been developed at Fermilab [11]. This chip is designed specifically for 132 ns operation and has a column-based architecture. Preliminary results from testing are very promising and the important specifications related to time-walk, noise and power dissipation have been met. A new chip called FPIX1 is being designed [12]. This chip has a readout architecture that is similar to the one described above in its functionality but the implementation is quite different. Furthermore, it sends both row and column addresses for each hit. As mentioned earlier, this gives us more flexibility in the trigger algorithm but comes at the cost of having to more than double our transmission bandwidth. Efforts are underway to design a chip compatible with the needs of the DØ trigger.

7 Summary

We have shown that an inclusive b-jet sample above a moderate p_T threshold can be collected in the TeV33 running of DØ if we employ a trigger based on pixel detectors. Preliminary simulations show that the rates will be manageble. Problems due to occupancy and radiation damage are well controlled in such a tracker. A conceptual architecture for this readout and trigger has been defined.

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