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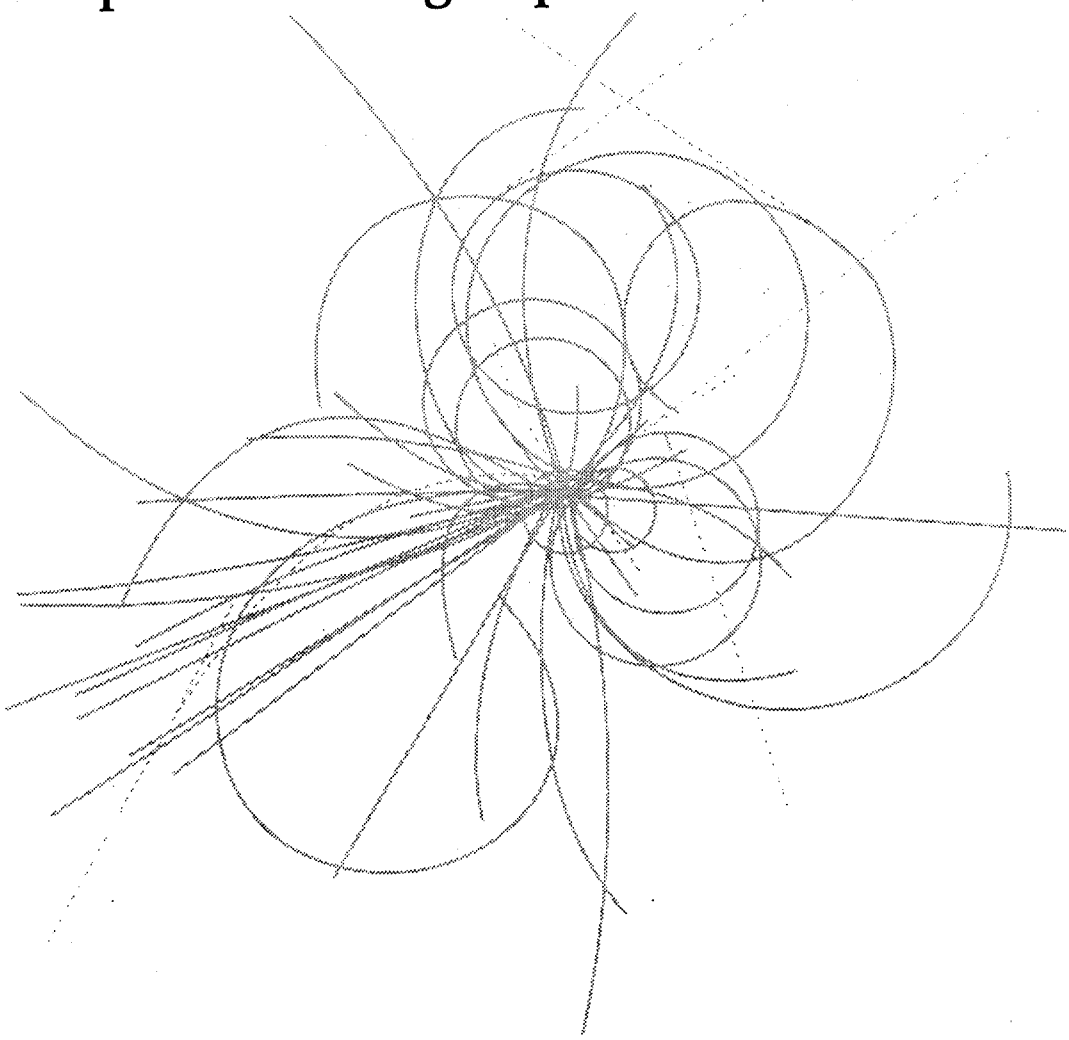
Superconducting Super Collider Laboratory



Low Energy Booster Extraction Kicker Prototype Modulator

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LOW ENERGY BOOSTER EXTRACTION KICKER PROTOTYPE MODULATOR

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Abstract

Design of the pulsed power systems required to drive the extraction kicker magnets for the low energy booster is well under way. Detailed designs of the charging power supply, pulse forming line, feed throughs, switch tube housings, drive circuits, loads, and controls will be presented, as well as SPICE analyses to verify designs.

Introduction

The low energy booster (LEB) is used to accelerate a proton beam from 1.2 GeV/c to 12 GeV/c at the Superconducting Super Collider Laboratory (SSCL). Fast kicker magnets are used to extract this beam which will be accelerated by other boosters. The nominal $\int B \cdot dL$ required for extraction is 600 G-m. The pulse width is 2.5 μs, at a PRF of 10 Hz. The rise time requirement of the field in the magnet is from 0±1% to 100±1% in 80 ns. The flat top requirement is that the integrated ΔB/B shall not exceed ±1% for the length of the pulse.

This paper will describe the design of power systems, controls, and associated hardware of the prototype modulator which will be built to drive the LEB extraction kicker magnets. Analysis of this design will also be presented.

System Design

A block diagram of the LEB extraction prototype system is shown in Fig. 1. The modulator is designed to drive two 25-Ω traveling wave kicker magnets. The charging power supply is designed to charge 103.3 nF to 40 kV. Command, resonant charging is utilized to reduce the possibility of switch tube pre-fires. The pulse forming line (PFL) consists of four parallel-connected spools of RG-220 cable. The modulator contains one main switch tube and a tail-biter tube. The tail-biter, which will only be used in the prototype, is used to provide pulse-width control and protection of the main switch tube in the event of a load short. The tubes which where selected are EEV CX1154G single gap, deuterium filled, ceramic envelope thyratrons. Similar tubes will be bought and tested from EG&G and ITT. A resistive load is used for matching and to dissipate the energy of the pulse. This load is a stack of carbon resistors mounted in a low-inductance tapered housing designed to prevent high-frequency reflections. A VXI based control system is used for system timing, to monitor various pulsed and DC signals, and to provide arc detection.

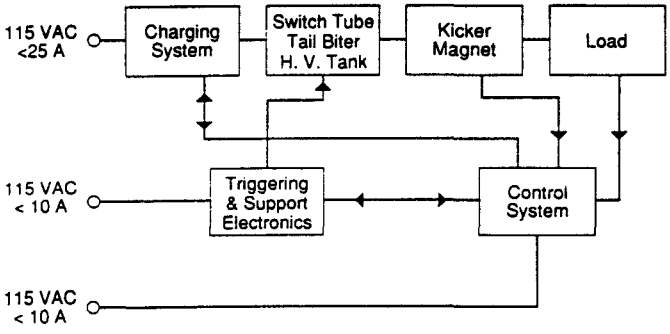

Fig. 1. Block diagram of LEB extraction modulator prototype.

Charging System Design

A schematic of the charging power supply is shown in Fig. 2. A DC, switch-mode power supply will be used as the primary power source. Several manufacturers have 300 V, 8 A, off-the-shelf power sources which will meet all of the requirements for the prototype. This supply will be operated in the constant current mode, charging the 10 mF primary capacitance. Thyristor Q_1 is used to discharge the capacitor through a high voltage step-up transformer. A current zero at the completion of charging commutates the SCR. The specifications for the transformer are a turns ratio of 1:147, a leakage inductance of 145 μH, open circuit inductance of 0.45 H, series resistance of less than 40 mΩ, core loss equivalent resistance of less than 500 Ω, and secondary capacitance to ground of less than 10 μF. All of these parameters are referred to the primary. The transformer is rated for 5 kVA. R_1 is needed to limit the current from the filter capacitor, and the cable connecting the power supply to the PFL, to less than 0.5% of the PFL discharge current in order to stay within the flat top requirements. This resistor, therefore, must be placed as close to the anode of the switch tube as possible.

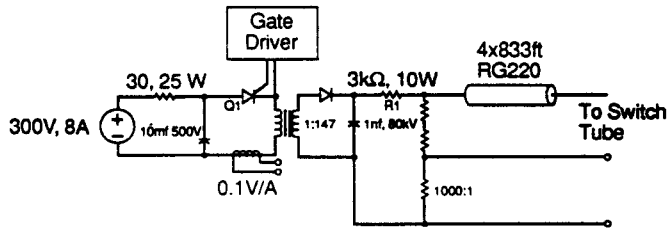

Fig. 2. Schematic of charging power supply.

SPICE analyses of this circuit are shown in Fig. 3. A modified Hu-Ki model[1] for a S15CGH12AO thyristor was used to model SCR Q_1. This analysis shows an approximately one-half sine wave primary current pulse of amplitude 580 A, and duration of 1.8 ms, to charge the PFL to 40 kV. The average current carried by the SCR is 5.88 A, while the RMS current is approximately 55 A. The I^2t of this current pulse is approximately 303 A^2s. The maximum di/dt seen by the SCR is 0.5 A/μs, and the maximum dv/dt is 0.01 V/μs. All of these values are well within the maximum allowable for the S15CGH12AO2[2].

The capacitor bank will consist of fifteen, 680 μF, 350 VDC, electrolytic capacitors. The ESR, at 120 Hz, will be specified to be less than 0.013 Ω, with a maximum ripple current greater than 40 A,

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for the array. This bank will be enclosed in a 19 inch rack mount enclosure, and connected to the SCR and transformer oil tank by #6 AWG wire in flexible conduit.

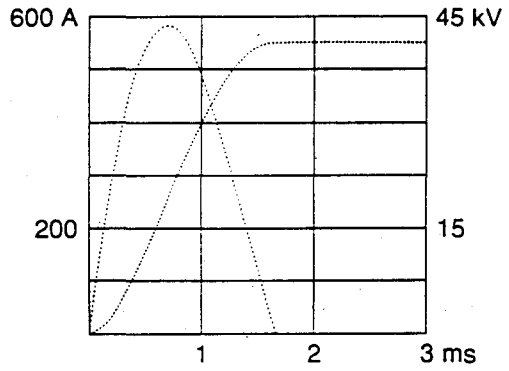

Fig. 3. SPICE analysis of charging power supply. Primary current and secondary voltage are shown.

Modulator Design

A line-type modulator design is employed where the PFL is made of four spools of RG-220 cable connected in parallel. Two switch tubes are used in this design. The main switch tube begins the pulse while the tail biter can be used to provide pulse width control and arc protection for the main tube. Dielectric and attenuation properties of the coaxial cable were considered in order to determine the suitability of using standard RG-220 cable as the PFL. The maximum RMS operating voltage for RG-220 cable is 14,000 V which constrains the cable charge time to less than 12.5 ms at 40 kV.

Several attempts were made to characterize cable attenuation which could appear as droop of the output pulse. The attenuation of coaxial cable, in dB/100 ft, at high frequencies is given by

$$\alpha = 4.34R_t/Z_0+2.78f\varepsilon^{1/2}F_p.^3$$

Here $R_t=0.1(1/d+1/D)f^{1/2}$, D is the inside diameter of the outer conductor in inches, d is the outside diameter of the inner conductor in inches, f is the frequency in MHz, ε is the relative dielectric constant of the cable, and F_p is the power factor of the dielectric. Using this equation at the fundamental pulse frequency of 400 kHz for RG-220 cable, the attenuation is 0.027653 dB/100 ft, or 0.4607 dB per cable for a two way transmission through 254 m of cable. This attenuation represents a cable "droop" of approximately 1.32%, for the PFL. This analysis assumes that most of the energy of the pulse is at 400 kHz, and that the attenuation equation above is accurate at this frequency.

A 170-m spool of RG-220 cable was connected to a variable frequency sine wave generator, and attenuation was measured for the first nine harmonics of a 2.5 μs pulse. Fourier coefficients were computed for the same harmonics, which were multiplied by the attenuation coefficients and normalized for a propagation through four 508 m parallel cables. These numbers were summed, as in a discrete convolution, to predict cable attenuation. This analysis estimates a droop of 1.4%. Both of the above analyses are based upon the propagation of a pulse through a cable. The actual application is for a PFL where some of the charge transits a very short distance and some of the charge transits the entire cable length. The attenuation measurements were also very difficult to make, and could have more measurement error than 1%.

The cable, switch, load, and connectors required to measure the droop for a 20 kV, 2.5 μs pulse are not readily available at the SSC. Two 170-m spools of RG-220 were connected in series, charged to 125 V and switched with a FET into a matched load. The results of this experiment are shown in Fig. 4. The measured droop is between 2% and 4% , however the cable junction is evident half way through the pulse and could account for 1 to 2% of the measured droop. Standard RG-220 cable seems to be a good candidate for the baseline design, even though there remains a question as to whether it will meet the flat top requirements.

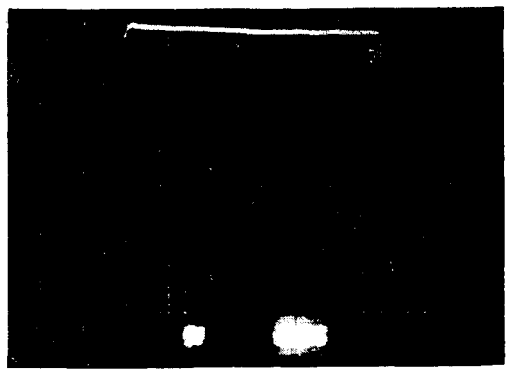

Fig. 4. PFL droop measurement. Load voltage is shown.

The 1 to 99% rise time of the kicker system $\int B\cdot dl$ is required to be less than 80 ns. The magnet has a fill time of approximately 40 ns, which leaves only 40 ns for the anode fall time of the switch tube. This results in a di/dt of about 6×10^{10} A/s. This rate of rise of current is within the limits of the EEV CX1154G thyratron. Thyratrons from EG&G and ITT will also be tested. Since the main switch tube is floating, a low-capacitance isolation transformer will be used to power the cathode and reservoir heater supplies. The voltage for both heaters will be controllable with floating variacs. The cathode heater will be rectified and filtered to reduce jitter. Pulse transformers will be used to trigger both grids, with the trigger source at ground potential. The negative grid bias supply will be powered from the isolation transformer. The tube itself will be housed in a 15.24-cm inner diameter cylindrical metal housing. This represents an impedance of approximately 28 Ω, with an electrical length of approximately 1.5 ns. The switch tube housing is shown in Fig. 5, and a block diagram of the switch and associated support electronics is shown in Fig. 6. Fig. 7 shows a SPICE simulation of the effects of the housing mismatch if all other components were ideally matched, and the anode fall time of the switch were 20 ns.

The tail biter tube is placed at the other end of the PFL, and can be used to truncate the pulse or to provide switch tube protection in the event of a load arc. The tail biter is grounded, so no isolation is needed for the support electronics. A low inductance housing is not planned for the tail biter. Both tubes will be in the same oil tank, which will be connected to the charging supply transformer tank by a single RG-220 cable.

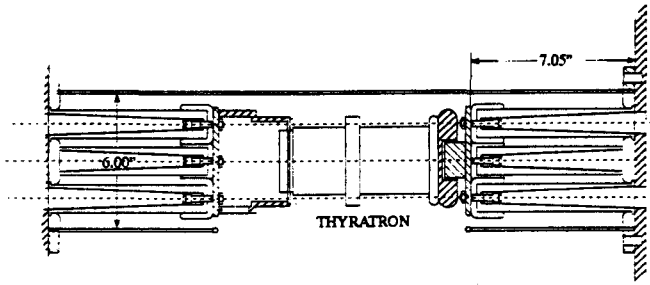

Fig. 5. Switch tube housing.

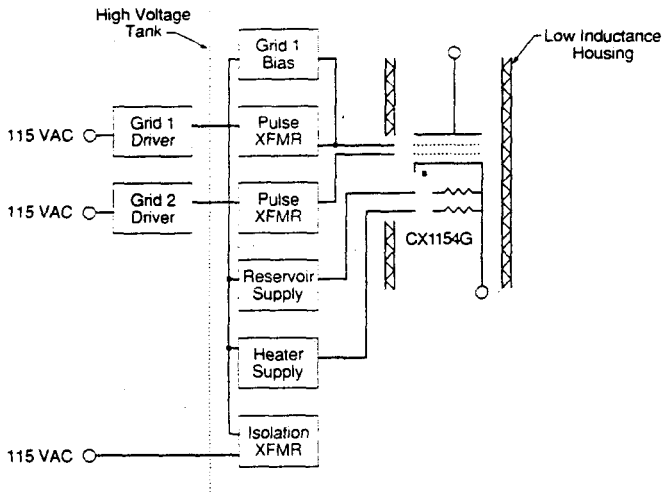

Fig. 6. Switch tube support electronics.

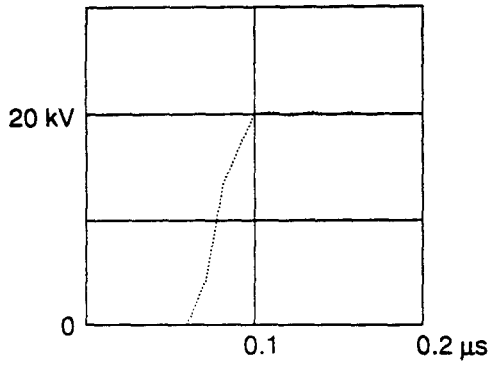

Fig. 7. SPICE analysis of effects of switch tube housing. Modulator output voltage is shown.

Load Design

A resistive load will be used to terminate the magnet to avoid reflections. This load will be constructed of fourteen, 890 mΩ, ceramic disk resistors connected in series. One 12.5 mΩ ceramic disk resistor will be added to provide for a 1000:1 voltage divider. The physical size of the resistors will be 13.97 cm O.D. by 3.81 cm I.D. by 2.54 cm thick. The resistors will be sandwiched between porous brass washers to provide electrical contact and fluid flow between the resistors for cooling. The assembly will be held in place by a plastic rod running through the middle. The rod will be threaded on the ends, with a compression spring installed at one end for holding the assembly together. The entire resistor will then be placed in a tapered housing which provides ground return and matching for high frequency pulse components. The whole assembly will be enclosed in an oil tank. An external heat exchanger will be provided to cool the oil. A drawing of the resistor assembly is shown in Fig. 8.

SPICE analysis was performed on this load to evaluate high frequency ripple during the pulse. The load was modeled by ten sections of the circuit shown in Fig. 9. The dependent source is used to model the voltage coefficient of a ceramic resistor. The inductance and capacitance values were calculated by assuming a coaxial geometry and a uniform current density in the resistor to calculating an average I.D. The length of the housing was divided into ten sections and the average O.D. of each section was used for inductance and capacitance calculations. The results of this simulation are shown in Fig. 10. This voltage would be seen at the magnet if it were perfectly matched and of zero length. All other imperfections were ignored, except that a 100 ns transmission line was assumed to connect the switch to the load. The step is caused by the voltage coefficient of the resistors, and can be eliminated if the resistors are matched at the operating voltage of the system. A system simulation was not run to determine if other non-linearities would smooth out the flat top to meet our specifications. This data does indicate that it may be necessary to place the resistive load as physically close to the magnet as possible.

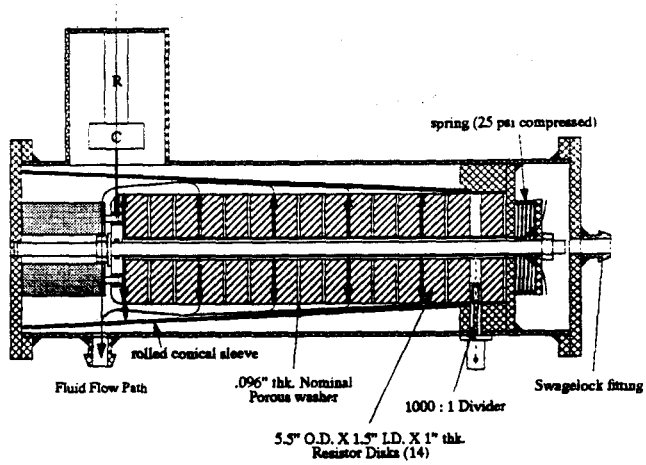

Fig. 8. Resistor assembly.

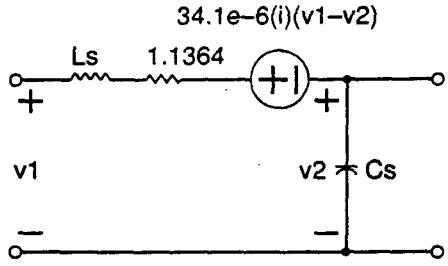

Fig. 9. SPICE model of resistor.

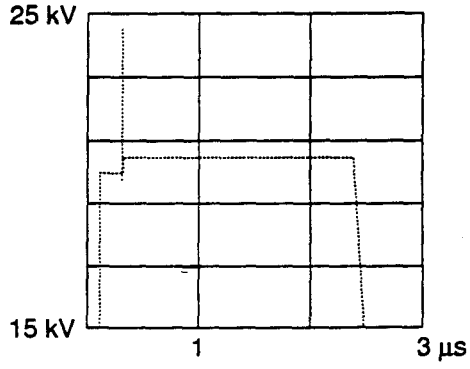

Fig. 10. SPICE analysis with effects of non-linear load. Magnet voltage is shown.

Control System Design

The control system performs four basic functions: characterization of the modulator system for commissioning, control

system timing, arc protection, and communication with the main control room. A VXI based system is being considered for its ability to handle all tasks in one chassis with a 40 Mbyte/s data throughput rate. The VXI specification also defines cooling and EMI requirements in a non-proprietary platform.

Commercially available fast digitizers, peak detectors, threshold detectors, and time interval counters will be used for system diagnostics and analysis. A-D converters will be used to read various voltages and currents in the system. D-A converters will be used to control power supplies, and monitor interlocks. Delay generators will be used to generate and route timing signals necessary maintain to system performance. An embedded controller will be used to perform the control and analysis functions. The controller will communicate with the control room via a memory-mapped reflective memory module.

A software-based feedback control system will be used to keep shot to shot modulator variation within specifications. Time averaging of the trigger to pulse delay over several shots, along with suitable adjustment of the delay generator in 1 ns steps will keep jitter within specification. Variations in switch tube drop will be compensated by adjusting the power supply voltage such that a time averaged constant amplitude voltage pulse is maintained.

Detection of arcs and misfires will be accomplished using a gated threshold detector that monitors current at strategic locations in the system. If the current exceeds a pre-programmed threshold for more than 500 ns, the detector will flag the controller and fire the tail biter. The controller then has the option of shutting the modulator down and informing the control room or continuing operation. The decision will be based upon the location and severity of the fault. The control system will have the ability to store two digitized waveforms from previous shots, as well as provide start-up and shutdown sequences for the system. The system will also have the ability to abort a synchrotron in the event of a catastrophic kicker system failure.

Conclusions

The design presented should meet all of the specifications for the LEB extraction system except possibly the ±1% flat top requirement. A lumped element PFN is under consideration if the droop of RG-220 proves unacceptable. Several types of switches where investigated before deciding upon a single gap thyratron. The main advantage of a single gap tube is there are no pre-pulses caused by multiple gaps breaking down. The use of a single gap tube places a limit of approximately 35 kV charge voltage. This voltage allows the use of standard RG-220 cable and eases feedthrough designs. Overall system design is impacted by this relatively low voltage in that more magnets are needed to meet both the $\int B \cdot dl$ and rise time requirements.

Prototype testing will focus primarily on the modulator rise time, flat top, and voltage hold-off of the system. This testing is necessary to make final selection of switch tubes, cable, feed throughs and PFNs.

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