ISBN: 978-3-95450-193-9 doi:10.18429/JACoW-ICALEPCS2017-TUPHA075

A MicroTCA BASED BEAM POSITION MONITORING SYSTEM AT CRYRING@ESR

P. Miedzik, H. Bräuning, T. Hoffmann, A. Reiter, R. Singh
GSI Helmholtzzentrum für Schwerionenforschung, Darmstadt, Germany

Abstract

At FAIR the commissioning of the re-assembled CRYRING accelerator, formerly hosted by Manne Siegbahn Laboratory Stockholm, is currently in progress. This compact low energy heavy ion synchrotron and experimental storage ring will be the main instrument for an extensive research programme [1] as well as a testing platform for the future beam instrumentation and control system concepts decided on for FAIR. Besides many other measurement systems CRYRING is equipped with 18 beam position monitors (BPM), for which a new data acquisition system (DAQ) was developed. Based on the upcoming MicroTCA form factor in combination with FPGA mezzanine card (FMC) technology the DAQ system was designed to be state-of-the-art, reliable, modular and of high performance. Testing „Open Hardware“, here the ADC FMCs and FMC carrier boards, was another intention of that concept. The DAQ layout and obstacles that had to be overcome as well as first measurements will be presented.

INTRODUCTION

The updated CRYRING accelerator [2] is presently under commissioning in the Experiment Cave B on the GSI Campus. A schematic overview over site and accelerator design is given in Fig. 1.

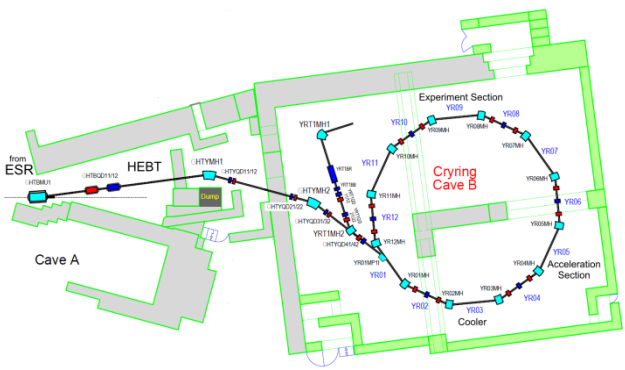

Figure 1: Scheme of CRYRING installation in Cave B.

As described in [3] the CRYRING is equipped with plenty of beam instrumentation devices to measure beam profiles, intensity, position and orbit. The latter one is based on a beam position monitor (BPM) system with 18 either horizontal or vertical oriented BPMs, which provides fundamental information for accelerator commissioning and optimization. CRYRING was delivered to GSI without BPM data acquisition electronics, so an adequate read-out had to be found. First choice would have been the Libera Technology [4], which is standard for all FAIR BPM systems. At time of that decision making the required Libera Hadron Platform B was not ready for purchase. As an alternative the very promising form factor FPGA Mezzanine Card (FMC) came up, which was well featured by CERN and DESY in the accelerator community. FMC in combination with the upcoming Micro Telecommunications Computing Architecture (µTCA) standard, which provides significant improvements with respect to data bandwidth on the backplane, redundancy and high availability compared to traditional VME solutions, was defined as being worthy to be evaluated.

INFRASTRUCTURE

Control System

The CRYRING installation at GSI is a dedicated testing machine for FAIR hard- and software developments. The control system is a CERN style FESA [5] based 3-tier architecture with a JavaFX GUI at the application level. The timing system consists of the Open Hardware (OHWR) GSI White Rabbit Timing Master and the FAIR Timing Receiver Nodes (FTRN) hosting the GSI specific event decoding firmware [6].

Acquisition Hardware

The BPM DAQ housed in a Schroff 12-slot MTCA.4 chassis combines a Concurrent Technology AM902-32 CPU with Dual PCIe x4 support on AMC ports 4-7 (FatPipe1) and 8-11 (FatPipe2) and five AMC FMC Carriers (AFC-V2). Those are equipped with 250 MSPS, 16 bit, 4 channel ADC FMC boards.

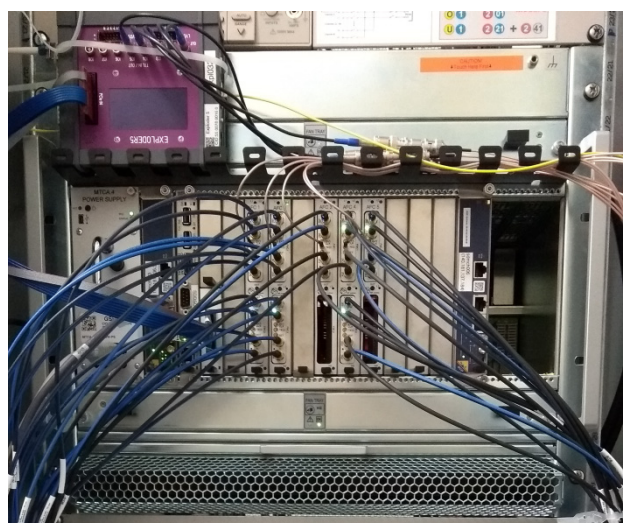

Figure 2: BPM DAQ system in µTCA form factor.

Both AFC and ADC board types were developed in cooperation between the Brazilian Synchrotron Light

ISBN: 978-3-95450-193-9 doi:10.18429/JACoW-ICALEPCS2017-TUPHA075

Source (LNLS) and the Warsaw University of Technology and were produced by the Polish company Technosystem under the CERN Open Hardware License [7]. The DAQ is triggered by an EXPLODER, the GSI White Rabbit timing receiver shown in Fig. 2 on the upper left corner, connected to MicroTCA FatPipe1 over a GSI MATPEX1a PCIe breakout board. System power is provided by one Wiener 1000W power supply. Two N.A.T. Main Carrier Hubs (MCH) had to be chosen to gain PCIe connection to MATPEX1a on FatPipe1 and AFCv2 on FatPipe2 to achieve highest possible transfer rates.

FPGA Architecture

To comply with the needs of the BPM DAQ a highly modularized FPGA framework was developed using VHDL language. It allows producing variations of final firmware with different scenarios adjusted for a particular case. Most of the components used in HDL are using either Wishbone or AXI4-Lite for management purposes. As shown in Fig. 3 they are connected together to upstream ports over Wishbone Crossbars and expose their address spaces and types over Self Describing Bus (SDB) Wishbone extensions [8] to allow automatic discovery of them.

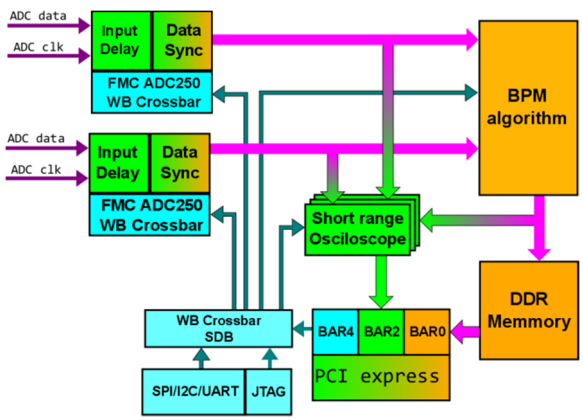

Figure 3: Example block realisation of the DAQ with data processing path enabled.

All FMC modules used in the project share the same interface which can be used in many different variants. To ease the integration process of VHDL, a FMC helper library was created and several FMC software modules, ready to use in next projects, were developed. This library creates pin assignments in a format which is understood by the synthesis tool during VHDL synthesis. Later this information is used in an implementation and bitstream creation process.

The FPGA infrastructure allows digitizing, processing and transferring data in an efficient way to the memory of the front-end controller (FEC) thanks to DMA transfers and can be reused in upcoming projects.

Enhanced Module Management Controller (eMMC)

After some IPMI instabilities between AFC and different MCHs a new implementation of eMMC [9] was designed and developed under the FreeRTOS real-time operating system kernel [10]. The eMMC supports now two architectures: ARM Cortex-M3 and AVR XMEGA and is implemented into three boards: AFC, AFCK and MATPEX1a.

BPM SYSTEM ARCHITECTURE

Figure 4 shows the schematic of the BPM system. The pick-ups are based on the linear-cut design with dimensions of 50 or 38 mm diameter to provide linearity over a large range. The pick-ups are connected to high impedance amplifiers [11] with a possibility of 40/60 dB amplification. The amplifiers contain an embedded 4 MHz filter to reduce high frequency noise. Following that, the signal is split between the ADC DAQ and a switching matrix which is connected to an oscilloscope. This allows an in-situ comparison of the BPM signals useful for commissioning and debugging of the DAQ. The BPM system also obtains an rf signal synchronized with the cavity rf.

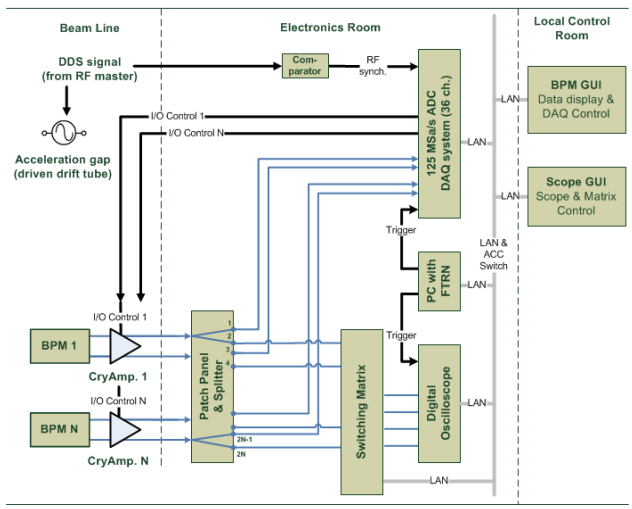

Figure 4: Schematic of the BPM signal chain and acquisition system.

There are three modes of operation envisaged for implementation in DAQ FPGA [12]. The most basic is the raw data or "scope mode" where data from each ADC channel will be displayed to a user for a selected time interval. Then, an "asynchronous mode" is foreseen, where beam positions are calculated in a user defined time window. The final mode will be the "rf synchronous mode", where beam positions synchronous to the rf cavity signal are calculated. Depending on the harmonic of the cavity, this would result in bunch-by-bunch or turn-by-turn positions. These modes of operation are planned to be incrementally implemented in the FPGA.

Signal Conditioning and Calibration

All amplifiers have been matched in the lab with the maximum gain differences below 0.03 dB, which corresponds to 0.1 mm offset. The amplifiers have an inbuilt test signal generator for verification of amplifier and ADC channel fidelity during operation. Figure 5 shows the signal flow after digitization. The ADCs are ac-coupled

ISBN: 978-3-95450-193-9 doi:10.18429/JACoW-ICALEPCS2017-TUPHA075

with the lower cut-off frequency of 20 kHz. The gain mismatch between ADC channels are measured in the lab and corrected by the gain correction register on the ADC board.

Position Algorithm

The BPM DAQ uses the Least-Square Fit of Difference signal to Sum signal to estimate the position of the beam [13]. The Least-Square Fit algorithm, see Eq. (1), has been proven as a reliable and robust estimator for linearly related signals. Further advantages are immunity to low frequency external noise or offsets to any of the electrode signals. If the difference (Δ) and sum (Σ) signals calculated from opposite plates, the position estimate $< x >$ for N samples is calculated as,

$$\frac{\langle x \rangle}{k} = \frac{N\sum_i^N(\Delta_i\Sigma_i) - (\sum_i^N \Delta_i)(\sum_i^N \Sigma_i)}{N\sum_i^N \Sigma_i^2 - (\sum_i^N \Sigma_i)^2} \quad , \qquad (1)$$

where k is the radius of the pick-up.

In the asynchronous mode, N will be provided by the user, while in the rf synchronous mode, N will be determined by the window generated by the rf signal. Figure 5 describes this process schematically.

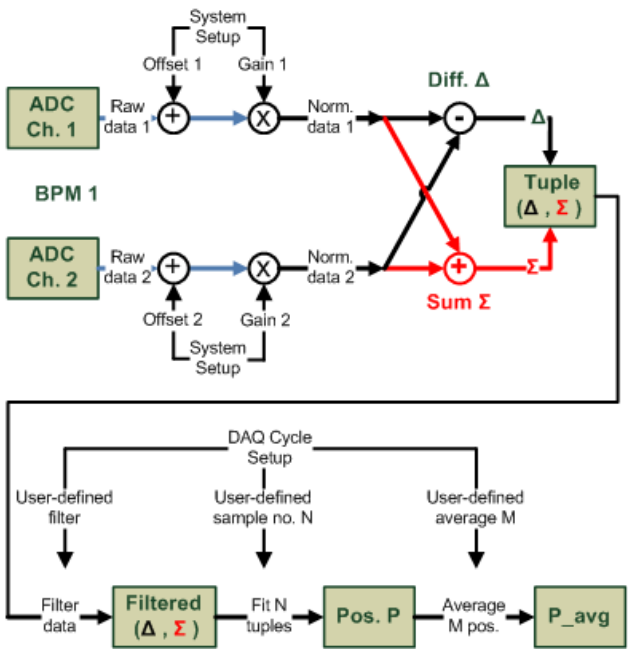

Figure 5: BPM signal flow during the digital processing in the FPGA.

HDL implementation of this algorithm is realised in multi stage pipelined architecture. In a first part of it dividend and divisor are created while in a second stage estimator is created using the High Radix division algorithm [14].

The algorithm was implemented and tested in FPGA. The result values were matching to the ones computed in PC.

MEASUREMENTS WITH BEAM

At present CRYRING is under commissioning with 300 keV/u H_2^+ beam (injection energy), which corresponds to a revolution frequency of 7.1µs. The stored current presently is of the order of 10 µA. Figure 6 shows the first BPM measurements of the described DAQ system in the "raw data" mode using a JavaFX GUI.

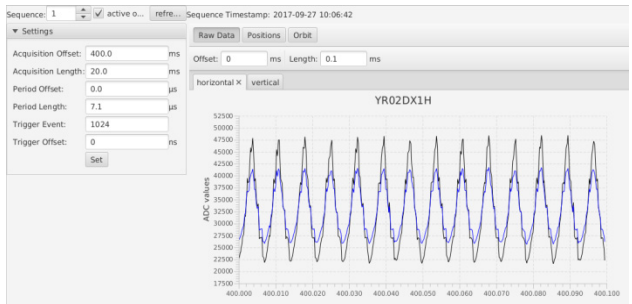

Figure 6: Real raw data BPM signal of the new DAQ system with 300 keV/u H_2^+ beam.

CONCLUSION

The decision to realize the Cryring BPM data acquisition on the base of FMC and µTCA technology was on the one hand a good base for gaining experience and learning for further FAIR developments, but on the other hand a very time consuming development and debugging phase which bound the digital engineer for almost 80% over three years. Mixing components of different vendors can work out as long these vendors test their equipment on interoperability workshops. In this specific case, the Open Hardware products delivered were comparable to an untested beta version state, showing differences already from board to board and required huge efforts on debugging and maintenance.

As the project allowed this development time, the positive output, besides a working BPM DAQ system, is the know-how gained on all stages of such a development. Many parts of the FPGA developments, such as the MMC code, can be re-used.

REFERENCES

[1] M. Lestinsky, Y. Litvinov and T. Stöhlker (Eds.), "Physics book: CRYRING@ESR", *European Physical Journal Special Topics*, Vol. 225, No. 5, September 2016.

[2] F. Herfurth *et al.*, "The Low Energy Storage Ring CRYRING@ESR", in *Proc. COOL'13*, Mürren, Switzerland, paper THPM1HA01.

[3] T. Hoffmann *et al.*, "Beam Instrumentation and Data Acquisition for CRYRING@ESR", in *Proc. ICALEPCS'15*, Melbourne, Australia, paper MOPGF153.

[4] www.i-tech.si

[5] T. Hoffmann *et al.*," FESA at FAIR – The Front-End Software Architecture", in *Proc. PAC'09*, Vancouver, BC, Canada, paper FR5REP009.

[6] D. Beck *et al.*,"The New White Rabbit Based Timing System for the FAIR Facilty", in *Proc. PCaPAC'12*, Kolkata, India, paper FRIA01.

[7] https://www.ohwr.org/

ISBN: 978-3-95450-193-9 doi:10.18429/JACoW-ICALEPCS2017-TUPHA075

[8] https://www.ohwr.org/projects/sdb/wiki

[9] https://github.com/qermit/JAMMCI

[10] http://www.freertos.org/

[11] A. Reiter, W. Kaufmann, C. Krüger, and T. Sieber, "Test of BPM Amplifiers", LOBICRYRING-2013-07, GSI internal.

[12] A. Reiter *et al.*, "The BPM system for CRYRING@ESR", LOBI-CRYRING-2015-01, GSI internal.

[13] R. Singh *et al.*, "Digital Processing of Pick-Up Signals for Position and Tune Determination", in *Proc. IBIC'15*, Melbourne, Australia, paper TUPB010.

[14] M.G. Galvez and J. Grajal, "Continuous-flow variable-length memoryless linear regression architecture", *Electronics Letters*, (49), 24, 1567-1568.