# A Trigger/Timing Logic Unit for ILC Test-beams

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*Abstract*

Detector development for the International Linear Collider (ILC) is likely to involve initial beam-tests with a triggered configuration, moving to beam-tests in a triggerless or self-triggered mode. A Trigger/Timing Logic Unit (TLU) is described which allows triggered operation, with option of smooth transition to trigger-less, data-driven mode. The unit has already been sucessfully used for a number of beam-tests.

## I. Introduction

In the early stages of sensor development, a simple easy to use trigger system is desirable, given that at beam-tests rapid installation of the device under test is often needed. Triggering on beam particles has traditionally been done using modules housed in NIM crates[2]. However, NIM crates are bulky and heavy. Moreover they are either expensive if purchased new or often in poor repair if drawn from a "loan pool". In addition it is not straightforward to expand a NIM trigger system to provide trigger time-stamping, allowing self-triggered or triggerless operation of the device under test (DUT). Modern field programmable logic allows construction of a low-cost, compact and flexible trigger unit which addresses these issues.

### A. Design Aims

An important design aim was to place few *restrictions* on the user of the TLU, whilst being as flexible as possible. The trigger unit should be as simple as possible, since ILC detectors will not be triggered. It should also be low cost, to allow widespread distribution. Ideally, each group developing detectors should be able to have at least one TLU.

### B. Operating Modes

The TLU is able provide "classic" beam-test trigger system. Incoming beam triggers are combined in a user selectable combination and passed to one or more DUT. The TLU also keeps a record of the arrival time of each trigger. Hence it can operate as time-to-digital converter for triggerless or self-triggered DUT. Both modes are active simultaneously, allowing triggered and triggerless/self-triggered DUT to be mixed in the same beam-test.

## II. Interfaces

Four $50\Omega$ terminated coaxial connectors accept NIM,TTL or photo-multiplier level pulses and receive a trigger for each particle passing through the test-beam. These four inputs are combined to form a beam-trigger. The arrival of a beam-trigger will cause a trigger to be output to active DUTs, unless one or more have indicated that they are busy. Interface to the DUT is via RJ45[1] connectors each carrying four LVDS signals. The signals from the TLU to the DUT are *trigger* and *reset*, the signals from the DUT to the TLU are *busy* and *DUT-clock*. There are six DUT connectors.

The FPGA is configured via the USB interface. Memory-mapped communication is used for setup and control. Then, block transfer is used to transfer time-stamps from the TLU to the host computer.

A photograph of the TLU front panel showing the various interfaces is shown in figure 1.

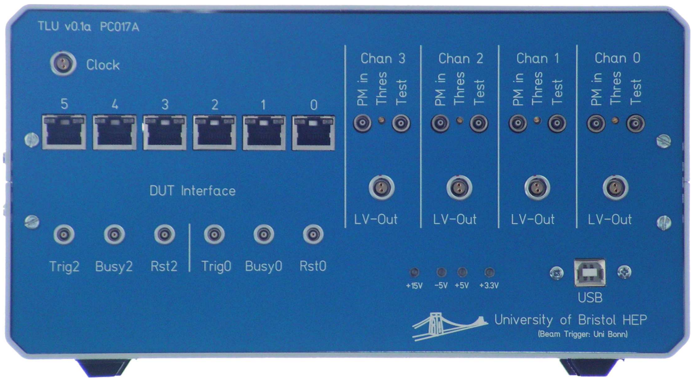

Figure 1: Front Panel of the TLU

### A. Handshake with Device Under Test

There are three handshake modes available for communication between the TLU and the DUT. The modes can be mixed, with different DUT using different handshake modes. The handshake modes are:

- **No Handshake.** The TLU asserts the *trigger* line for a fixed length of time. The *busy* line from the DUT is not monitored. In this mode the TLU acts like a simple discriminator and coincidence/veto unit.
- **Trigger/Busy Handshake.** The TLU asserts the *trigger* line connected to every DUT in the system. The TLU waits for each DUT to assert its *busy* line. When a DUT does this, the TLU de-asserts the corresponding *trigger* line and waits for the DUT to de-assert its *busy* line. The TLU does not issue any further triggers until all the DUT drop their *busy* lines. This mode is illustrated in figure 2.

- **Trigger/Busy/Trigger-Data Handshake.** This mode is similar to the Trigger/Busy handshake, but trigger information is transferred from the TLU to the DUT. When the TLU de-asserts the *trigger* line in response to the DUT asserting its *busy* line, the DUT toggles its em DUT-clock line and the TLU will clock out trigger information on the *trigger* line. Normally the trigger information is the bottom sixteen bits of the trigger counter. After the DUT is ready for new triggers and has clocked out the trigger information, it de-asserts the *busy* line.This mode is illustrated in figure 3.

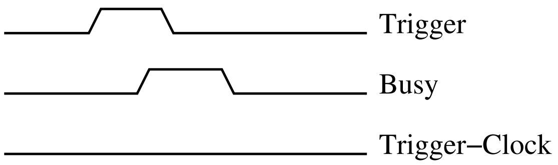

Figure 2: Simple Handshake Mode

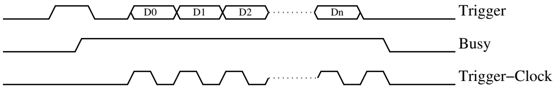

Figure 3: Trigger-Data Handshake Mode

## III. Implementation

The number of units is likely to be relatively low and the anticipated life-span of the design is modest ( $\tilde{5}$ years), which suggests the use of a COTS FPGA module coupled to a simple custom motherboard. Choosing a module that is supplied with USB interface firmware and software drivers greatly reduces the design effort needed. The FPGA module chosen[3] uses a Cypress EZ-USB FX2 microcontroller[4] to interface between a Xilinx Spartan xc3s1000 FPGA[5] and a USB2.0 port. The implementation is described in more detail elsewhere[7].

## IV. Firmware

The firmware for the FPGA was written in the VHDL. The FPGA module vendor supplied the EX-USB FX2 microcontroller firmware. The source code is available for a small fee.

Effort was taken to ensure that the FPGA firmware can be compiled using freely down-loadable synthesis tools[6] which allows TLU users to easily modify the firmware.

### A. Implementation of Asynchronous Trigger

The latency is fixed between the incoming beam-trigger and the outgoing trigger to the DUT. In order to achieve fixed latency, logic asynchronous to the system clock is used. Asynchronous logic is prone to race conditions. To mitigate these, and make the design more straight-forward, the *trigger* signal is de-asserted synchronously with the system clock. Figure 4 shows a simplified schematic of the logic used for the asynchronous-set/synchronous-clear of the trigger. The **async_trig_in** is the output of the circuitry that combines the signals from the four beam-trigger inputs. The **trig_out** signal is connected to the trigger output circuitry that drives each DUT interface. The **veto_from_fsm** signal is the "or" of the **fsm_veto** signals from all the trigger output circuits. Figure 5 shows a simplified diagram of the finite-state-machine that controls the trigger output circuit connected to each DUT. The **trigger_in** signal is from the asynchronous-set/synchronous-clear logic and **trig_out** is the signal sent to the DUT.

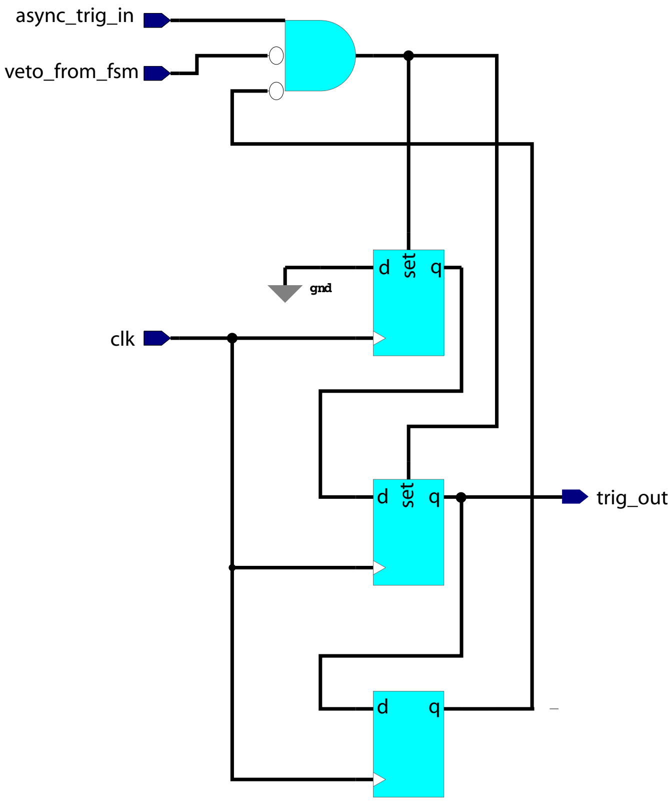

Figure 4: Asynchronous-set/Synchronous-clear Logic

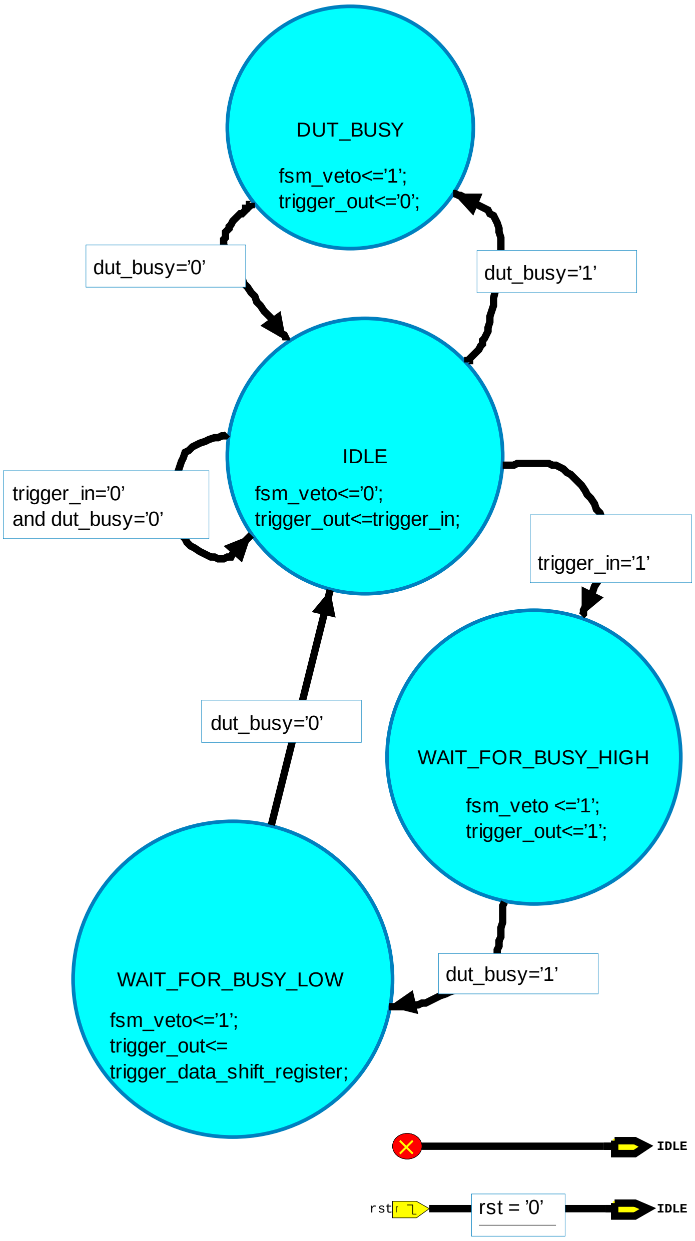

Figure 5: Finite State Machine for TLU Trigger Outputs

### B. *Trigger Latency*

With the version of the firmware in use at the time of writing, the latency between a trigger of fixed amplitude arriving at the TLU and a trigger being issued by the TLU to the DUT is $27.3 \pm 1.5\mathrm{ns}$. The error quoted is the spread between different DUT outputs and the variation anticipated over the expected temperature range. At a fixed temperature for a given DUT output the variation in latency (the timing jitter) is much smaller. The measured latency jitter is $24 \pm 5\mathrm{ps}$. The fixed-threshold discriminator used is subject to timing walk for pulses of varying amplitude. The discriminator contributes in the region of $14\mathrm{ns}$ to the total latency. With a faster discriminator and a custom FPGA layout rather than a COTS module a total latency of under $10\mathrm{ns}$ would be achievable.

### C. *Trigger Timestamping*

Currently the firmware is configured to store a 64-bit timestamp for each trigger issued. By default the time-stamp resolution is $20.83\mathrm{ns}$, which is the period of the internal crystal oscillator. However, the TLU can accept an external clock of up to $100\mathrm{MHz}$. In this case, the time-stamp resolution is the period of the external clock. The time-stamps are stored in memory inside the FPGA, limiting the number of time-stamps to 4096. However, the FPGA module used has a 8MByte of low-latency SRAM and it is planned to modify the firmware to store timestamps in this external memory. This would allow up to 512k time-stamps to be stored. Using delay-locked-loop (DLL) frequency multipliers inside the FPGA together with double-edge clocking it is possible to improve the time-stamp resolution to one-eigth of the clock period. These technique have been used in firmware designed for the CMS calorimeter trigger[8] and in the TLU will allow a time-stamp resolution of approximately $2.5\mathrm{ns}$.

## V. Conclusions

The ready availability of programmable logic devices has allowed the construction of a simple, yet flexible, trigger system for use in ILC beam-tests. The unit is lower cost, more compact and more flexible than a system constructed from traditional NIM units. The TLU was developed as part of ILC vertex-detector development, but could also be used for other beam-tests.

## References

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