

2nd generation ASICs for CALICE/EUDET calorimeters

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Abstract. Imaging calorimetry depends heavily on the development of high performance, highly integrated readout ASICs embedded inside the detector which readout the millions of foreseen channels. Suitable ASICs prototypes have been fabricated in 2006-2007 and show good preliminary performance.

1. Introduction

After several years of data taking on 10 000 channels of electromagnetic and hadronic calorimeters, the CALICE collaboration has turned to addressing the technological challenge of a highly integrated, highly granular calorimeter that can be scaled to a full size detector [1].

For this purpose, 2nd generation readout integrated chips (ASICs) are needed (the first generation ASICs are those used for the current test-beam prototype). They incorporate the digitization and the sequenced readout handling inside the ASIC on top of the previous analog signal processing so that everything can be integrated inside the detector and having only a few digital lines coming out.

The chips have been developed, starting by the Digital Hadronic calorimeter RPCs which was more urgent and simpler as it is semi-binary with a chip called HaRDROC described in section 2. This chip has allowed to validate the digital readout sequence of a set of chips daisy-chained. The second chip was SPiROC for the analog hadronic calorimeter silicon PMS

2. DHCAL technological prototype : HARDROC1 ASIC

HARDROC readout is a semi-digital readout with two thresholds (2 bits readout) which allows both good tracking and coarse energy measurement, and also integrates on chip data storage.

The 64 channels of the ASIC are made of:

- Fast low impedance preamplifier with 6bits variable gain (tuneable between 0 and 4)
- Variable shaper (50-150ns) and Track and Hold to provide a multiplexed analog charge output up to 10pC.
- Variable gain fast shaper (15ns) followed by two low offset discriminators to autotrigger down to 10 fC. The thresholds are loaded by two internal 10 bit- DACs.
- A 128 deep digital memory to store the 2*64 discriminator outputs and bunch crossing identification coded over 24 bits counter.

HARDROC1 has been fabricated in AMS SiGe 0.35 μ m technology in September 2006. It has an area of 16mm² and is packaged in CQFP240 package.

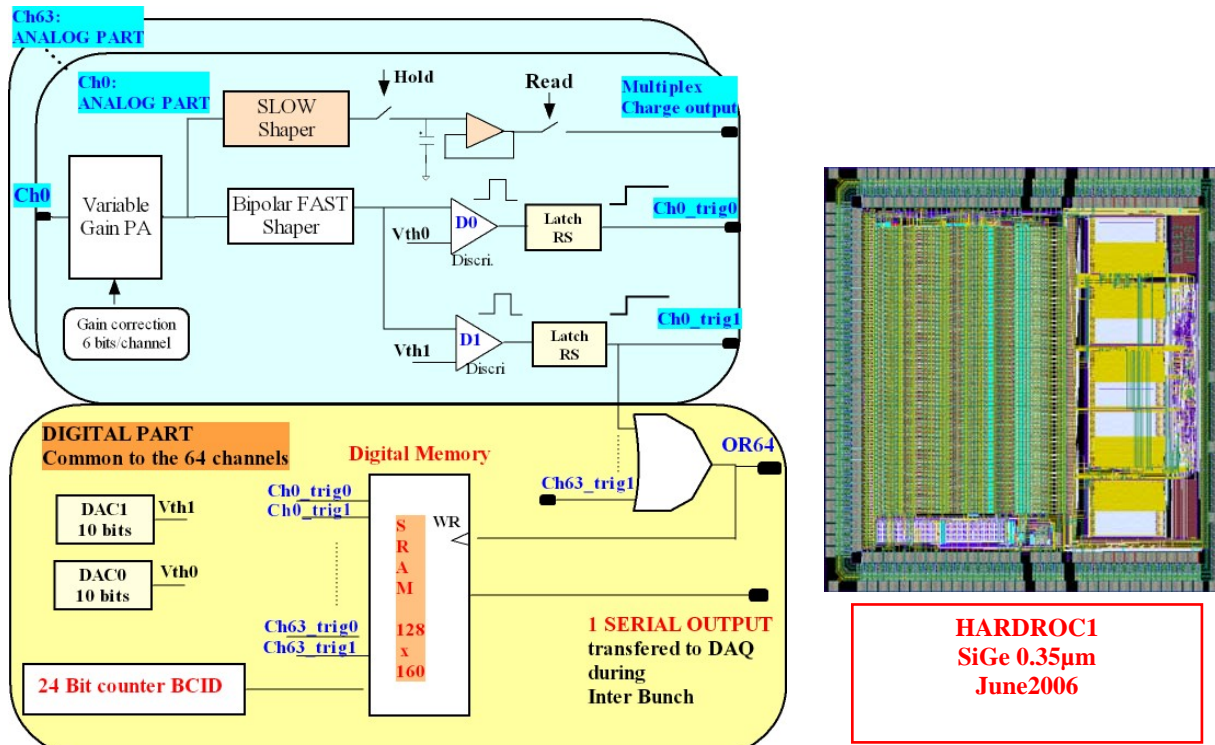


Figure 1 : synoptic view of the 64-channel HARDROC chip that reads the RPCs of the DHCAL technological prototype

2.1. Chip design

The block diagram of the ASIC is given in Figure 1. Each input signal is first amplified thanks to a variable gain current-sensitive preamplifier which exhibits low noise and low input impedance to minimise crosstalk. It allows accommodating the gain depending of the detector choice, up to a factor 4 to an accuracy of 6% with 6 bits.

The amplified current feeds then a slow shaper combined with a Sample and Hold buffer to store the charge in 2pF and provide a multiplexed charge output (5MHz) up to 10pC.

In parallel, trigger outputs are obtained via fast channels made of a fast (15 ns) shaper followed by two low offset discriminators. The discriminator thresholds are set by two internal 10 bit DACs.

Each trigger output is latched to hold the state of the response until the end of the clock cycle. The trigger1 outputs (corresponding to $V_{th1} < V_{th0}$) are OR wired to generate an internal trigger used to start the memorization of the 128 trigger outputs as well as the Bunch Crossing Identification delivered by a 24 bit counter, needed to associate hits in the DAQ to bunch crossing identification (BCID). It is also possible to capture event data using an external trigger provided from outside the chip. All the bias currents are programmed through the Slow Control and the chip is power pulsed to decrease the power consumption. 10µW/channel as targeted with a 1% beam duty cycle.

2.2. Testbench measurements

HaRDROC has been extensively measured from December 2006 to December 2007. In particular, it was the first time that the power pulsing could be tested as well as the readout scheme of the calorimeter with built-in memory, token ring and daisy chain mechanism.

The analog part, largely reused from another ASIC (MAROC worked as foreseen. The bipolar fast shaper gain is about 3.5mV/fC and its peaking time is equal to 15ns. The Slow Shaper gain is about 50 mV/pC and its peaking time can be tuned from 100ns to 150ns. The crosstalk (Fig.3) has been measured by sending 100fC in one channel and looking to the direct neighbours. This 2% crosstalk is well differentiated and located on the input.

The linearity of the two 10 bits integrated DACs used to generate the thresholds of the discriminators, has been measured and shows residuals within ± 5 mV for a 2.6V dynamic range which corresponds to an Integral Non Linearity of 0.2% (2LSB). The slope is 2.5mV per DAC unit.

The trigger sensitivity (s-curves) has been measured on the 64 channels of the chip. The quite large non uniformity between channels (± 25 %) is explained by current mirror mismatch (small transistor size to optimize speed at low current) and can be corrected using the gain tuning of the input preamp as shown in Figure 2. The s-curves also show a total noise around 1fC.

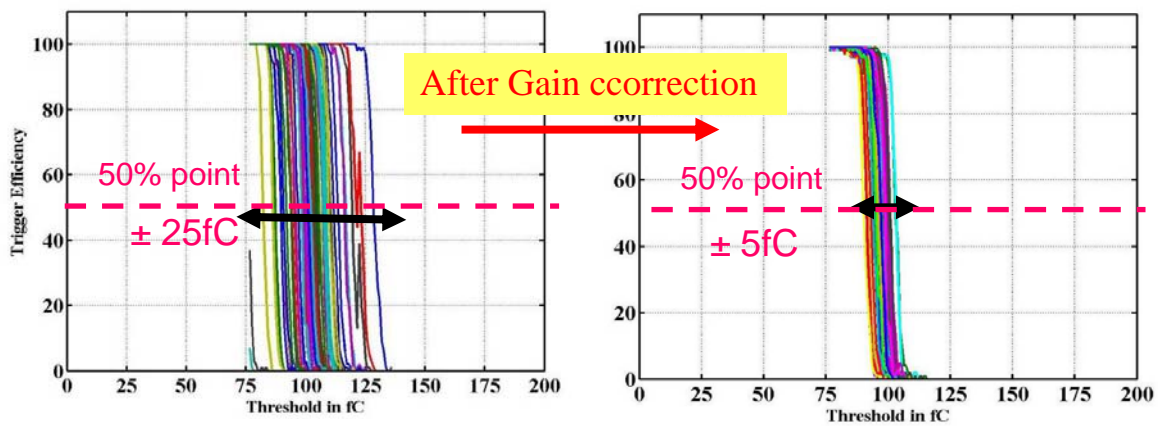


Figure 2: s-curves of the 64 channels of HARDROC1 before and after gain correction

As can be seen in Figure 3 , the dispersion between the channels is low enough to allow to bring the threshold down to 10fC. In particular, the pedestal is uniform within 1 DAC count (2.5mV or 1fC in high gain) which shows the excellent offset control obtained with this technology.

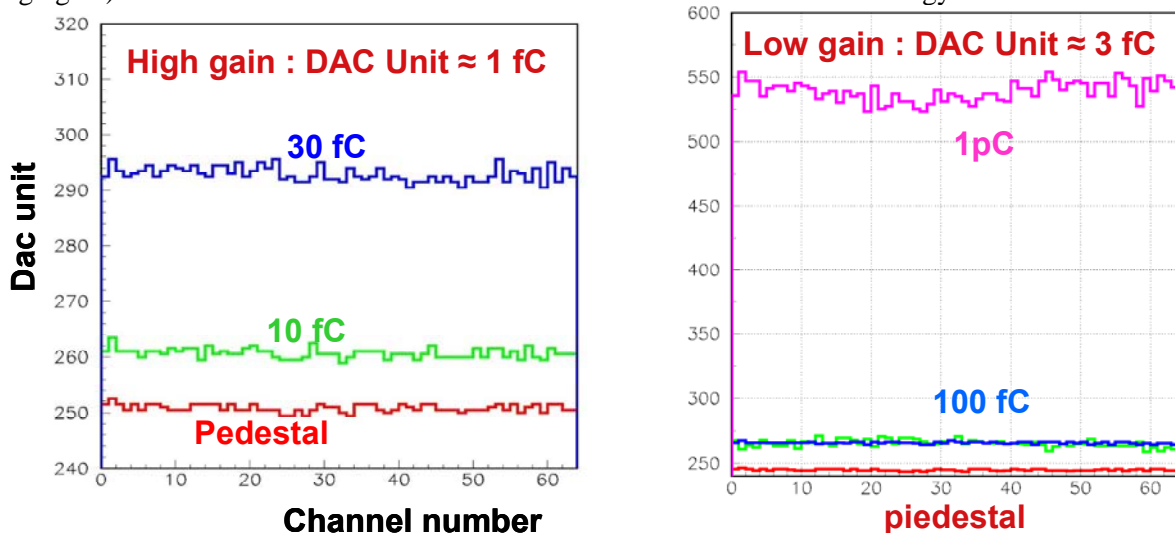


Figure 3: threshold for 50% trigger efficiency for the 64 channels

Last, but not least, the power pulsing capability has been tested on HARDROC1. There are 3 independent signals of power-on : analog, digital and DAC. Each stage can be forced on by slow control overruling the power-on pulse. As can be seen in Figure 4, it takes only 2 μ s for the analog part to be “awake” and provide a discriminator output (“trigger”) when an input charge of 100fC is

sent $2\mu\text{s}$ after the power-on signal. As could be expected, the DAC is much slower to settle (this is the reason why it had a separate power-on signal) and in it needs $25\mu\text{s}$ to reach its nominal value within a few mV.

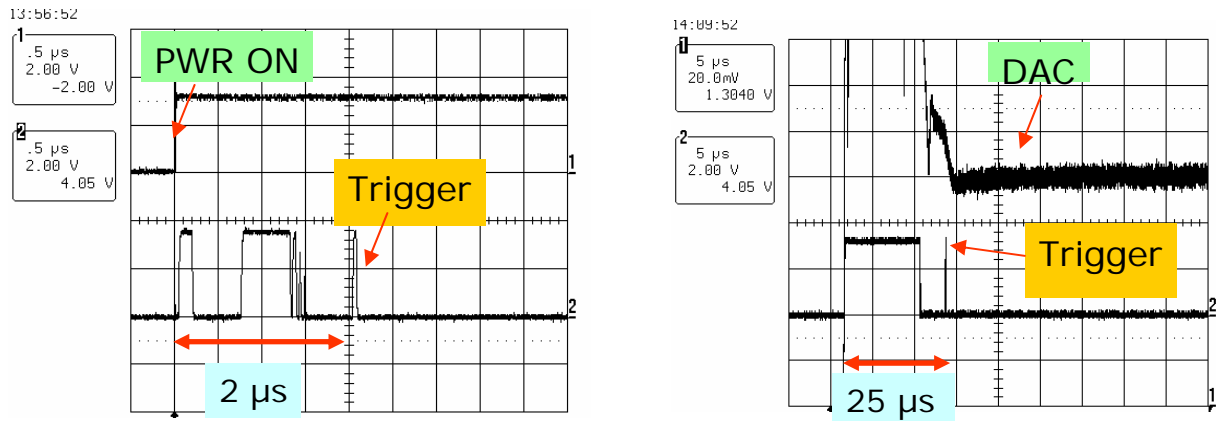


Figure 4: power-on of the analog part (left) and of the DAC (right)

2.3. HaRDROC digital part:

Because of the very high number of electronic channels foreseen in the final detector, chips will be embedded inside the detector and are designed to be daisy chained without any external circuitry, to limit to a bare minimum the number of output lines on the detector. A memory has been integrated in HARDROC to store during the bunch train the 2bits trigger outputs of each channel as well as the BCID, and this for every hit.

The data format is $128(\text{depth}) \times [2\text{ bits} \times 64\text{ ch} + 24\text{ bits (BCID)} + 8\text{ bits (header)}] = 20\text{kbits}$. There is one serial output which is transferred to the DAQ during the inter-bunch.

The auto trigger mode which is crucial for the chip functionality has been checked successfully down to 10fC . The trigger crosstalk has been measured by injecting a charge in one channel and measuring the trigger efficiency on the direct neighbours. There is no crosstalk for injected charge lower than 1.6pC , corresponding to a crosstalk value of 1%.

A PCB hosting four HARDROC chips (4X64 channels) has also been designed to study the signal connection between the different chips before extracting it through a USB device. The PCB board will be associated to both RPC and μMEGAS detectors in order to validate the whole concept through exposure first to cosmics and then to beam test at CERN.

3. AHCAL technological prototype and SPIROC

As for the ECAL and DHCAL, the AHCAL must also prove that it is scalable to large modules. There, the main issues are the integration of the electronics inside the detector with its power dissipation and readout issues (similar to the ECAL and DHCAL) and mechanical assembly of the system. Also the thickness is a very important issue, although not as critical as in the ECAL.

Once again, the ASIC is a central, critical issue of the whole detector usual coined as “no chip, no detector !”. For this purpose, a fully integrated ASIC named SPIROC (for Silicon Photomultiplier Integrated Read Out Chip) has been developed.

3.1. SPIROC ASIC architecture

The SPIROC ASIC that reads 36 SiPMs is an evolution of the FLC_SiPM used in the physics prototype. As for the ECAL, it keeps most of the analog part, adds an analog memory to record up to 16 events of a train and adds the auto-triggering capability. The digitization is brought inside the chip as well as the data handling.

The first prototype has been fabricated in june 2007 in AMS SiGe 0.35 μ m. The chip layout is shown in Figure 5, its area is 35 mm² for 36 channels and it is packaged in a CQFP240 package

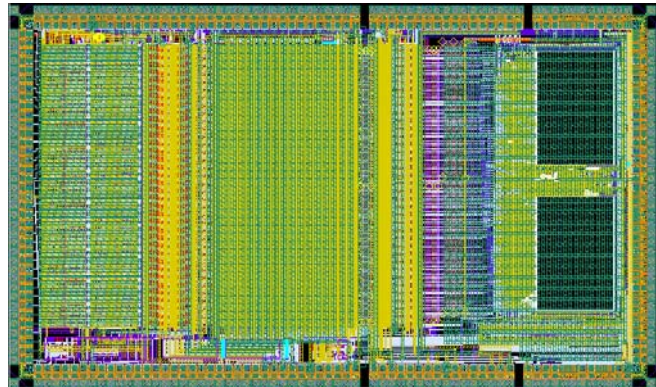


Figure 5: layout of SPIROC1

The schematic diagram of one channel is shown in Figure 6.

- The 8bit input DAC has been conserved, however its power dissipation has been brought down by 3 order of magnitude to 1 μ W/channel as it is not power pulsed. The DAC also has the particularity of being powered with 5V whereas the rest of the chip is powered with 3.5V.
- The voltage amplifier architecture with variable gain has also been kept, with a gain variable on 4 bits. However, the high gain/low gain separation splitting is now done at the preamp level by having two preamps on parallel on the input.
- The charge is measured on both gains by a “slow” shaper (50-150ns) followed by an analog memory with a depth of 16 capacitors.
- The auto-trigger is taken on the high gain path with a high-gain fast shaper followed by a low offset discriminator. All these blocks are new. The discriminator output is used to generate the hold on the 36 channels. The threshold is common to the 36 channels, given by a 10 bit DAC similar to the one from HARDROC with a subsequent 4bit fine tuning per channel.
- The discriminator output is also used to store the value of a 300ns ramp in a dedicated analog memory to provide time information with an accuracy of 1ns
- A 12bit Wilkinson ADC is used to digitize the data at the end of the acquisition period.

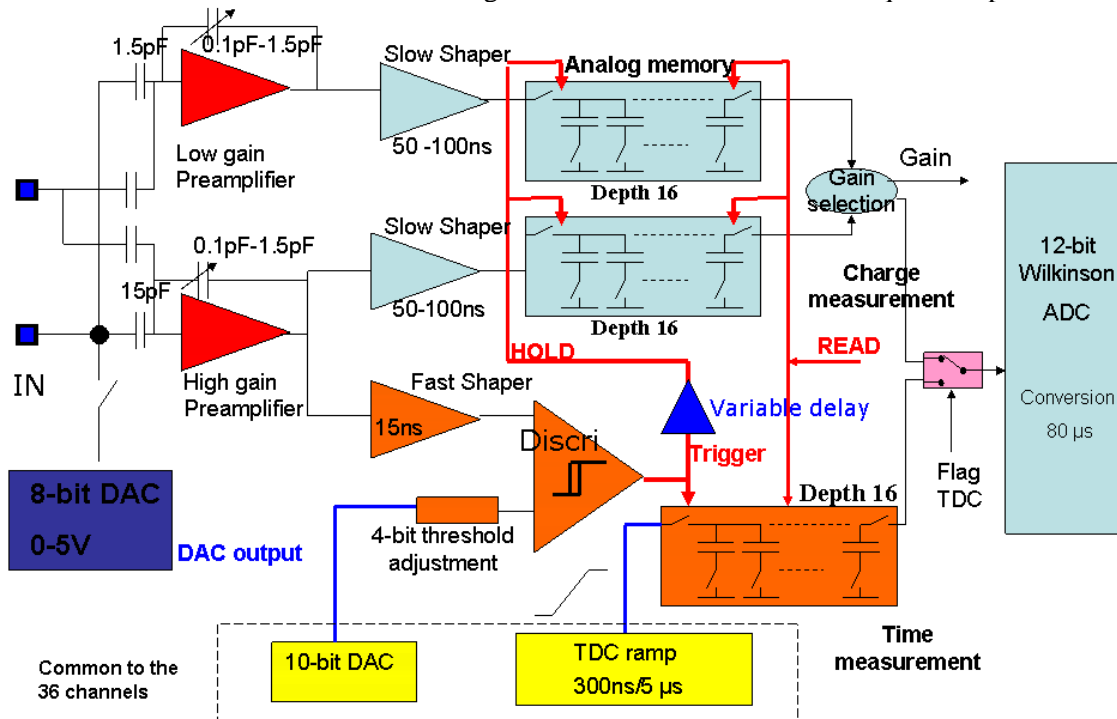


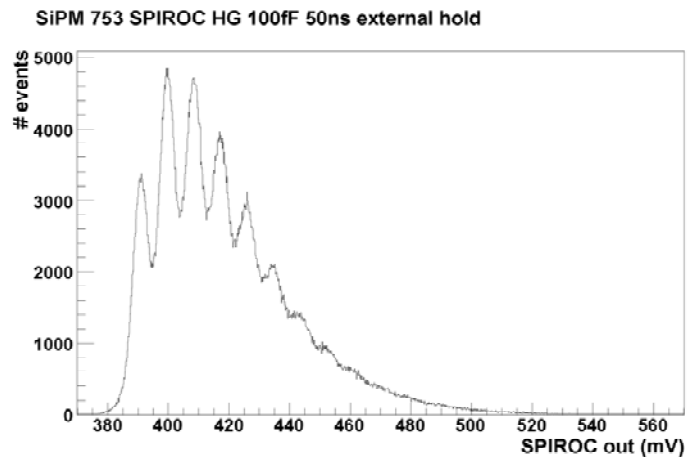
Figure 6: schematic diagram of one channel of SPIROC1

The digital part is complex as it must handle the SCA write and read pointers, the ADC conversion, the data storage in a RAM and the readout process.

3.2. measured performance

The chip has been received in October 2007 and underwent a long series of tests both in Orsay and Hamburg. The analog performance has shown good results but an inverted polarity in the ADC discriminators has unfortunately precluded any measurements with the internal ADC.

- Input DAC : the span goes from 4.5V down to 0.5V with a LSB of 20 mV. The default value is 4.5V in order to operate the SiPM at minimum over-voltage when the DAC is not loaded. The linearity is $\pm 2\%$ (5LSB), just enough for the SiPM operation but consistent with the allocated area. Also, the dispersion between channels, although not fundamental could also be improved. The power dissipation is well within the specs and the 100nA bias current to Vdd makes the chip difficult to measure without special precautions.
- Threshold and gain selection 10bit DACs behave similarly to the HARDROC.
- Charge path : the photoelectron to noise ratio of 8 allows to nicely resolve the single photoelectrons peaks
- Auto-trigger and discriminators. The ability to self-trigger on single photoelectrons or on the MIP is a new feature of SPIROC.



4. Conclusion

The first AISCs of 2nd generation for CALICE have been prototyped and tested with good performance that validated the choices made. They will go in production in first half of 2009 to equip the technological EUDET modules.

References

- [1] JC Brient : proceedings of this conference and references therein
- [2] I Laktineh : proceedings of this conference and references therein
- [3] F. Sefkow : proceedings of this conference and references therein