The ALICE pixel detector upgrade

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The ALICE pixel detector upgrade

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Abstract: The ALICE experiment at the CERN LHC is designed to study the physics of strongly interacting matter, and in particular the properties of the Quark-Gluon Plasma, using proton-proton, proton-nucleus and nucleus-nucleus collisions. The ALICE collaboration is preparing a major upgrade of the experimental apparatus to be installed during the second long LHC shutdown in the years 2019–2020. A key element of the ALICE upgrade is the new, ultra-light, high-resolution Inner Tracking System. With respect to the current detector, the new Inner Tracking System will significantly enhance the pointing resolution, the tracking efficiency at low transverse momenta, and the read-out rate capabilities. This will be obtained by seven concentric detector layers based on a Monolithic Active Pixel Sensor with a pixel pitch of about $30 \times 30\,\mu\text{m}^2$. A key feature of the new Inner Tracking System, which is optimised for high tracking accuracy at low transverse momenta, is the very low mass of the three innermost layers, which feature a material budget of 0.3% X_0 per layer. This contribution presents the design goals and layout of the upgraded ALICE Inner Tracking System, summarises the R&D activities focussing on the technical implementation of the main detector components, and the projected detector performance.

Keywords: Particle tracking detectors (Solid-state detectors); Solid state detectors

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Contents

2016 JINST 11 C12038

1 Introduction

ALICE (A Large Ion Collider Experiment) [1] is a general-purpose, heavy-ion experiment at the CERN LHC. Its main goal is to study the physics properties of the Quark-Gluon Plasma. During the Long Shutdown 2 (LS2) of the LHC in 2019/2020, ALICE will undergo a major upgrade in order to significantly enhance its physics capabilities, in particular for high precision measurements of rare processes at low transverse momenta p_{T}.

1.1 ALICE upgrade

The ALICE upgrade programme [2] during LS2 is based on the upgrade of various sub-detectors preparing them for operation at a Pb–Pb interaction rate of about 50 kHz. The study of rare probes at low p_{T} in heavy-ion collisions makes triggering inefficient due to the large combinatorial background [3]. Thus, the upgraded experimental apparatus is designed to readout all Pb–Pb interactions, accumulating events corresponding to an integrated luminosity of more than 10 nb^{-1}. This minimum-bias data sample will provide an increase in statistics by about a factor 100 with respect to the programme until LS2. The upgraded detector will provide improved vertexing and tracking capabilities at low p_{T}. In summary, the ALICE upgrade consists of the following sub-system upgrades:

- Reduction of the beam-pipe radius from 29.8 mm to 19.2 mm allowing the inner layer of the central-barrel silicon tracker to be moved closer to the interaction point.
- Two new high-resolution, high-granularity, low material budget silicon trackers:
  - Inner Tracking System (ITS) [3, 4] covering mid-pseudo-rapidity ($-1.2 < \eta < 1.2$).
  - Muon Forward Tracker (MFT) [5, 6] covering forward pseudo-rapidity ($-3.6 < \eta < -2.45$).
- The wire chambers of the Time Projection Chamber (TPC) will be replaced by GEM detectors and new readout electronics will be installed in order to allow for a continuous readout [7].

- Upgrade of the Forward Trigger Detectors (FIT) and the Zero Degree Calorimeter (ZDC) [8].
- Upgrade of the readout electronics of the Transition Radiation Detector (TRD), Time-Of-Flight (TOF) detector, PHOton Spectrometer (PHOS) and Muon Spectrometer for high rate operation [8].
- Upgrade of online and offline systems (O^2 project) [9] in order to cope with the expected data volume.

2 ALICE ITS upgrade

The main goals of the ITS upgrade are to achieve an improved reconstruction of the primary vertex as well as decay vertices originating from heavy-flavour hadrons and an improved performance for the detection of low-p_T particles. The design objectives are to improve the impact-parameter resolution by a factor of 3 and 5 in the $r\varphi$- and z-coordinate, respectively, at a p_T of 500 MeV/c [4]. Furthermore, the tracking efficiency and the p_T resolution at low p_T will improve. Additionally, the readout rate will be increased to 50 kHz in Pb–Pb and 400 kHz in pp collisions. In order to achieve this the following measures will be taken:

- The innermost detector layer will be moved closer to the interaction point from 39 mm to 23 mm.
- The material budget will be reduced down to 0.3 % X_0 per layer for the innermost layers while for the outer layers it will be about 1.0 % X_0.
- The granularity will be increased by an additional seventh layer and by shrinking the pixel size from currently 50 µm × 425 µm to about 30 µm × 30 µm.
- All layers of the upgraded ITS will be equipped with pixel sensors.

The upgraded ITS is designed such as the removal and insertion will be possible during the yearly shutdown periods for maintenance.

2.1 Layout and running environment of the upgraded ITS

The upgraded ITS, as shown in figure 1, will have seven layers. The innermost three layers form together the Inner Barrel (IB) and the middle two and outer two layers form the Outer Barrel. The radii of the layers are 23 mm, 31 mm and 39 mm and 194 mm, 247 mm, 353 mm and 405 mm, respectively. The upgraded ITS will provide a pseudo-rapidity coverage of $|\eta| < 1.22$ for 90 % of the most luminous beam interaction region. The radial positions of the layers were optimised in order to achieve the best combined performance in terms of pointing resolution, p_T resolution and tracking efficiency in Pb–Pb collisions at hit densities of about 19 cm^{-2}/event on average for minimum-bias events in the innermost layer. The detector will cover a total surface of 10.3 m^2 containing about 12.5×10^9 pixels with binary readout. The upgraded ITS will be operated at room temperature (20°C to 30°C) using water cooling. The expected radiation load at the innermost layer is expected to be 270 krad of Total Ionising Dose (TID) and 1.7×10^{12} 1 MeV n_{eq}/cm^2 of Non-Ionising Energy Loss (NIEL). In order to meet the material budget requirements, the silicon sensors will be thinned down to 50 µm and to 100 µm in the IB and OB, respectively.

2016 JINST 11 C12038

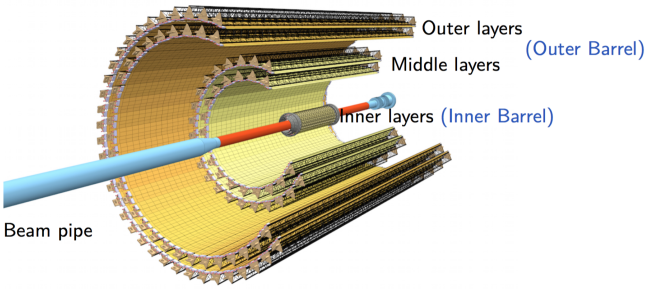

Figure 1. Layout of the upgraded ITS taken from [4].

3 ALPIDE — the pixel chip for the ALICE ITS upgrade

ALPIDE is the pixel chip development carried out for the ALICE ITS upgrade. The general requirements and current performance of the ALPIDE prototypes are outlined in table 1. The ALPIDE pixel chips are designed to fulfil the requirements of both the IB and the OB allowing the detector to be assembled using a single chip. The ALPIDE pixel chips are Monolithic Active Pixel Sensors (MAPS) manufactured using the TowerJazz 180 nm CMOS Imaging Sensor Process [10]. The front-end circuit of ALPIDE is optimised to achieve the desired granularity while maintaining a low power consumption. The event-time resolution is chosen such to enable the reconstruction of Pb–Pb interactions at the Pb–Pb interaction rate of 50 kHz.

The final pixel chip ALPIDE was submitted in spring 2016. The pixel and front-end circuit were tested in the preceding prototype called pALPIDE-3b. In figure 2, the detection efficiency and fake-hit rate measured in test beam and in the laboratory are shown in black and red, respectively, as a function of the threshold current I_{THR}. The performance before irradiation is depicted with closed squares. The detection efficiency is above the required 99 % up to I_{THR} of about 140 DAC and the fake-hit rate after masking 0.015 % of the pixels stays at the sensitivity limit for the full range. After NIEL irradiation up to the ten times nominal value of 1.7×10^{13} 1 MeV $\mathrm{n_{eq}/cm^2}$ (open circles), the detection efficiency drops below 99 % at about 120 DAC. The fake-hit rate is not influenced by NIEL irradiation. The influence of TID can be seen from the open squares. The TID irradiation leads to an effective change of charge threshold of the front-end circuitry resulting in a higher fake-hit rate at low I_{THR} and detection efficiency close to 100 % over the full range. The change of charge threshold was confirmed in S-Curve scans carried out in the laboratory and is was verified that a second parameter allows to compensate for the effective charge threshold change. As a consequence, the operational range in terms of detection efficiency and fake-hit rate is not reduced. The inherent NIEL dose of the proton irradiation to 350 krad is about 3.7×10^{12} 1 MeV $\mathrm{n_{eq}/cm^2}$.

Further measurement results are presented in [12]. A detailed description of the circuit is presented in [11].

The ALPIDE pixel chips are read out using with a global shutter in either triggered or continuous integration mode. In triggered mode, a short strobe of the order 100 ns is used to store the hits in the in-pixel memories. In continuous-integration mode, the strobe is active for the full integration window (of the order 10 µs) except for the switch over (about 100 ns) from one to the other in-pixel hit buffer.

2016 JINST 11 C12038

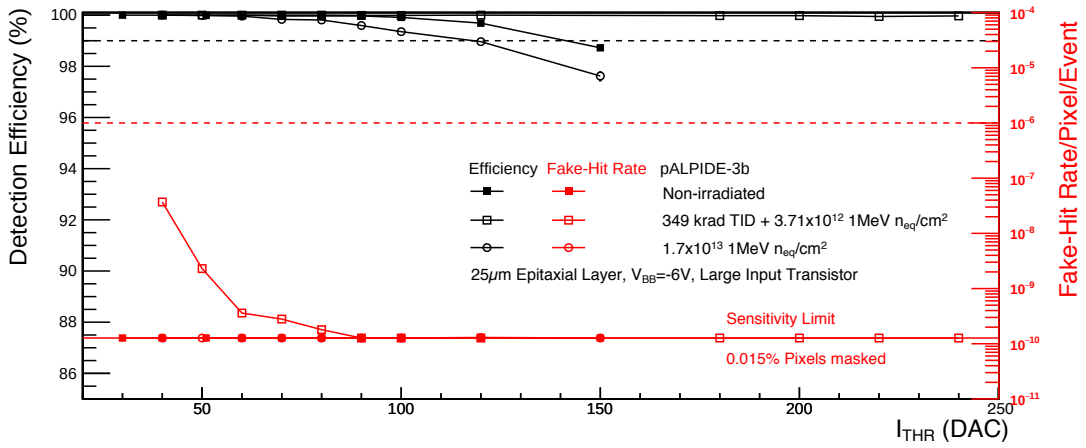

Figure 2. Detection efficiency and fake-hit rate of the pixel and front-end electronics of ALPIDE characterised with the help of pALPIDE-3b.

Table 1. General pixel-chip requirements [4] and current performance of ALPIDE prototypes [12].

Parameter	**Inner Barrel**	**Outer Barrel**	**ALPIDE**
Chip dimensions ($r\varphi \times z$, mm^2)	15×30		✓
Sensor thickness (µm)	50	100	✓
Spatial resolution (µm)	5	10	≈ 5 µm
Detection efficiency (%)	> 99		✓
Fake-hit rate (event^{-1}pixel^{-1})	$< 10^{-6}$		$\lll 10^{-6}$
Event-time resolution (µs)	< 30		< 2
Power density (mW/cm^2)	< 300	< 100	≈ 40
TID radiation hardness (krad)	270	10	✓
NIEL radiation hardness (1 MeV n$_{eq}$/cm^2)	1.7×10^{12}	1×10^{11}	✓

4 Mechanics

As mentioned above, the upgraded ITS consists of an Inner Barrel (IB) and an Outer Barrel (OB). The basic element of a layer is the stave, which consists of a carbon space frame to which the cold plate and the cooling ducts are attached. Above the cold plate a number of pixel chips, 9 for the IB and 14 for the OB, connected to a common Flexible Printed Circuit (FPC) are glued (cf. figure 3, left). The FPC consists of a polyimide with a low thermal expansion coefficient plus aluminium and copper as conductor for the IB and OB, respectively. The chip will be connected to the FPC using wire bonding to pads distributed over the entire chip surface rather than its periphery. The staves of the IB will have a length of 270 mm and a width of 15 mm. A complete IB stave weighs approximately 25 g. The staves of the middle and outer two layers of the OB will be 843 mm and 1475 mm long and weigh fully assembled 170 g and 260 g, respectively. The average material budget per layer will be 0.3% X_0 and 1.0% X_0 in the IB and OB, respectively.

2016 JINST 11 C12038

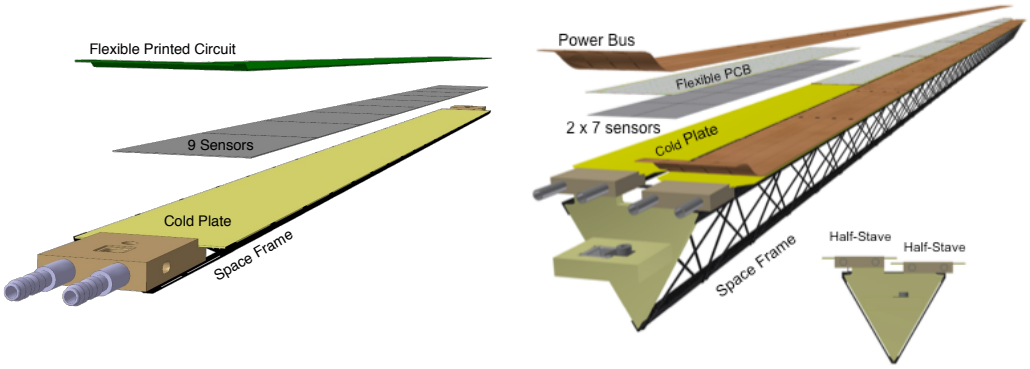

Figure 3. Exploded schematic view of an IB stave (left) and an OB stave (right).

For the OB and its wider and longer staves further segmentations are introduced (cf. figure 3, right). An OB stave consists of two half-staves. Adjacent half-staves are overlapping in order to minimise the dead area. The half-stave is further segmented into either four or seven modules of two times seven sensors for the middle and outer layers, respectively. The FPC shares the segmentation of the modules. The power bus distributes the power to the modules on the half stave.

The IB and OB space frames as well as cold plates have been successfully characterised for their mechanical strength and thermal properties [4] and first units have been produced.

5 Hybrid Integrated Circuit (HIC) prototypes

The pixel sensors together with the FPC form the Hybrid Integrated Circuit (HIC). Several HICs for the IB and OB were manufactured. In figure 4, the average threshold (left) and noise (right) of the nine chips on an IB HIC from an S-curve scan are presented. The error bars show the RMS of the distributions across the full matrix. The performance of all chips is comparable to single chips and the noise is as low as seven electrons also on the HIC. Furthermore, no systematic effects due to the presence in a module are observed. This picture is confirmed by the fake-hit rate (cf. figure 4, bottom), which is about 10^{-9} /Pixel/Event even before masking and is effectively reduced by masking a few noisy pixels. Missing points correspond to a fake-hit rate below the sensitivity limit of 4×10^{-11} /Pixel/Event.

The IB HIC was furthermore mounted on an IB stave and characterised with regard to its thermal properties. The temperature was measured in the periphery of the pixel chip where the Data Transmission Unit (DTU) is located. In figure 5 (left), the temperature change during power on and configuration is presented. The DTU is the block with the highest power density on the chip. The cooling water has a constant temperature of 18°C at the stave inlet. After 5 s, the chip is powered on and consumes 80 mW and 20 mW in the digital and analogue domain, respectively. The temperature of the central chip on the stave consequently rises by about 1°C. After 30 s, the DTU is configured and the high-speed serial link is activated, leading to another temperature increase of about 0.7°C. The overall temperature profile after activation of the DTU over the full longitudinal extension of the IB stave is shown in figure 5 (right). The temperature peaks at the positions of the DTUs, but stays within approximately a range of 2°C over the full stave.

2016 JINST 11 C12038

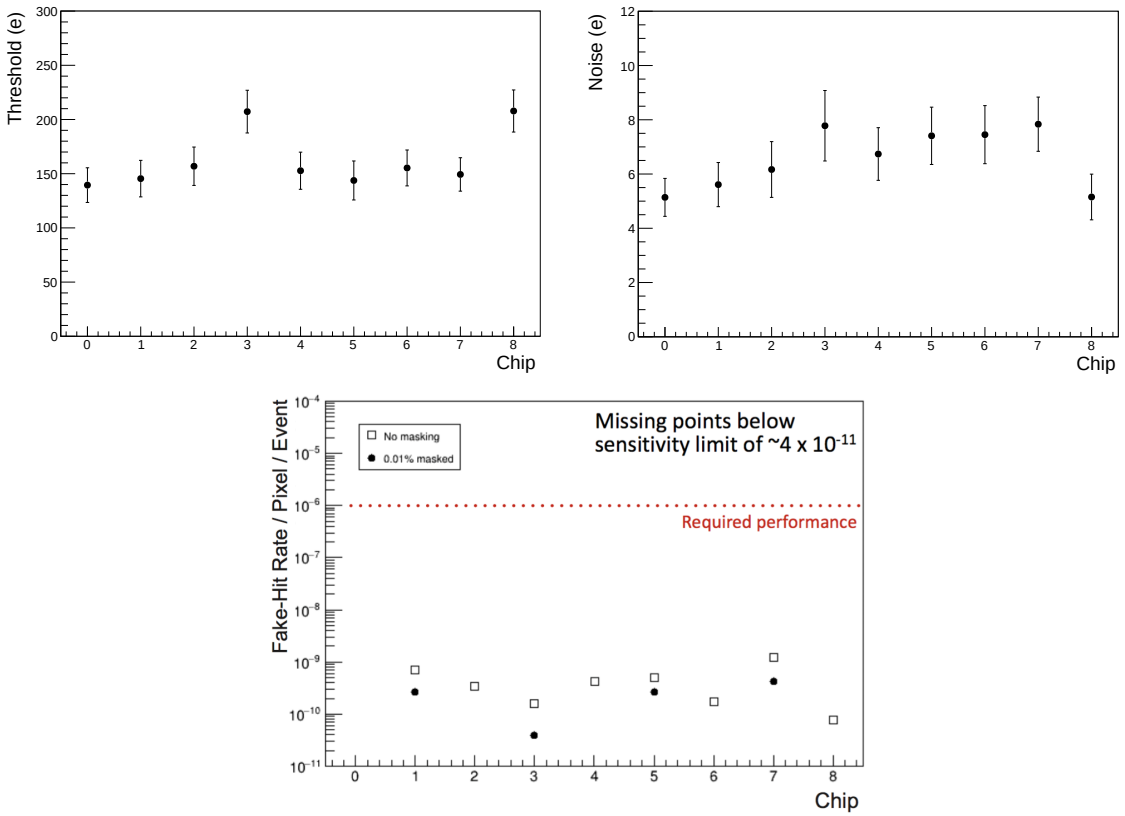

Figure 4. Threshold (left) and noise (right) from an S-curve scan as well as fake-hit rate (bottom) of the nine chips in an IB HIC.

6 Readout electronics

The global architecture of the upgraded ITS is outlined in figure 6. The readout electronics is segmented in three stages for different radiation environments. In the detector barrel, the pixel chips themselves transmit the data via copper links to the Readout Units (RUs). The RUs are located outside the detector acceptance in a moderate radiation environment of less than 10 krad of TID. The RUs receive the triggers from the Central Trigger Processor (CTP) via a GBT link [13]. The RUs ship the data to the counting rooms via GBT to the Common Readout Units (CRUs) housed in the Front-end Level Processor (FLP) computers [9]. The same data path is used to control the detector. The RU is an ITS upgrade specific development and a first prototype is currently being tested. The CRU is a common development used by several ALICE sub-detectors.

7 Summary and outlook

ALICE will replace the entire ITS by a MAPS-based, pixel-only tracker in 2020. This upgrade will significantly improve impact-parameter resolution and increase readout-rate capabilities. Moreover, a better tracking efficiency and p_{T} resolution at low p_{T} will be achieved. Within the pixel sensor R&D, large-scale prototypes were characterised and the most suitable pixel geometry and front-end electronics for the final pixel chip were selected. A first series of HICs was produced and

2016 JINST 11 C12038

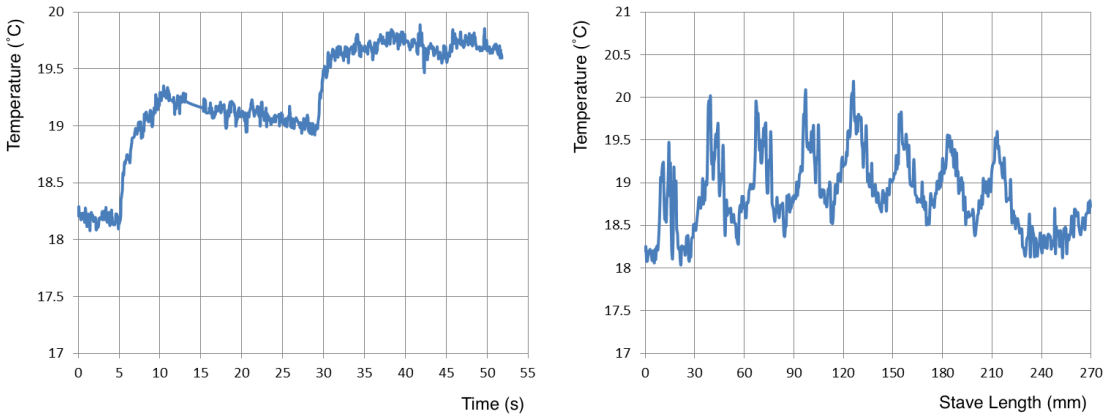

Figure 5. Temperature of measured in the pixel-chip periphery of the central chip of an IB stave during a power up (left) and across the full length the stave above the chip periphery (right).

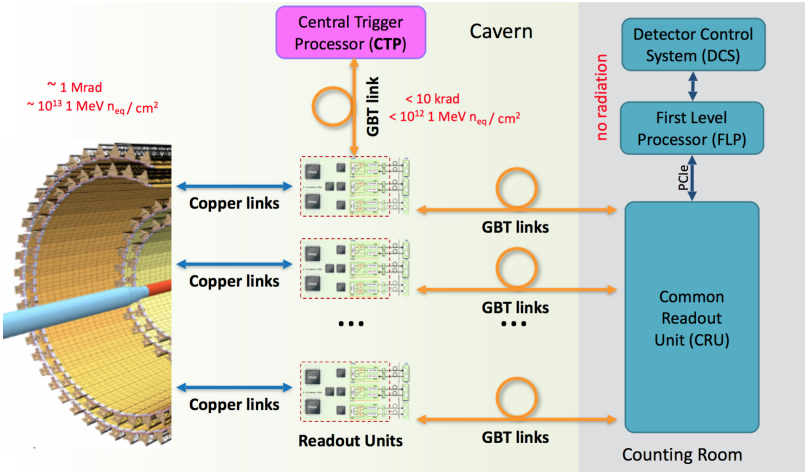

Figure 6. Global readout architecture of the upgraded ITS.

characterised. The pixel-chip prototypes showed similar performance in HICs as on single chips. In parallel, the global readout architecture was defined and the Readout Unit is being tested. With the arrival and qualification of the final pixel chip ALPIDE, the project will gradually move from the R&D phase into the production phase.

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2016 JINST 11 C12038