VON DARDEL: In the delay curves on the blackboard, did you use artificial pulses or was it a scintillation pulse from a photomultiplier?

FITCH: With phototubes, of course; with a pulser one can get infinite resolution.

VON DARDEL: The second question: Is the slope of the coincidence curve due to the pulse height variations, or is it inherent to the circuit itself?

FITCH: I do not know. I would like to say the following. As you saw, the coincidence circuit works on a cut-off in the first transistor and we are working in the low part of the leading edge of the pulse. We have found that the type 6810A photomultiplier has extremely poor characteristics in this region and this seems to cause a lot of difficulties. On the other hand, the 6810A with a curved window is very much better and the 6655 is also completely satisfactory. We have not had the privilege of trying some of the new French phototubes; presumably they are very much better still. The main objection I have to this circuit is that it utilises only a very small part of the total amount of information, and I would be very happy if someone would devise a circuit which could utilise this information.

MICHAELIS: I would like to ask two questions. First are the transistors that you used especially selected? Secondly, may one assume from the absence of measuring devices in your circuit that, in fact, the currents are not highly critical as they are in valve circuit?

FITCH: The circuit was purposely designed in order to stabilize the current. The first part of your question concerns whether we select the transistors or not. Yes, we do on arrival; we test them all, measure their β and file them accordingly, and then use them selectively in the circuit which we design.

ODIAN: Is that the d.c. β that you test, or do you test it at high frequency; does it make a difference?

FITCH: No, it does not.

LITTAUER: If you would take one of your stocks or selected β transistors and sometime later attempt to re-sort it, what kind of correlation function would you discover?

FITCH: We have not had enough experience to answer that. I can say this, that we have sorted them into the circuit and used a circuit over a considerable period of time, and were completely happy with the behaviour. This is all we were interested in. We did not take special care to make the current always constant, just to stabilize the transconductance.

A NANOSECOND COINCIDENCE CIRCUIT USING TRANSISTORS (*)

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(presented by M. Sands)

I. INTRODUCTION

Most of the experiments in progress at the Cal. Tech. 1 GeV electron synchrotron which use scintillation and Cherenkov counters require coincidence circuits with a resolving time of a few nanoseconds (**). These resolving times are required either for time-of-flight selection, or for the reduction of accidental coincidences from counters with high singles rates. Usually two-fold fast coincidences are required. More complicated coincidence combinations are obtained by the use of slower circuits operated from the outputs of several primary two-fold coincidence circuits. Until recently the fast coincidence circuits used in this laboratory have been patterned after the circuits of Wenzel[1] or that of Garwin[2].

With the advent of the Philco 2N501 transistor, which has a characteristics response time faster than the usual vacuum tubes, it became possible to consider constructing transistor coincidence circuits

(*) This work was supported in part by the U.S. Atomic Energy Commission.

(**) One nanosecond (ns) = 10^{-9} s.

with resolving times limited by the response of the scintillation counters. The lower power consumption, smaller size, and presumed greater reliability of the transistor circuits would make it possible to employ larger numbers of these circuits as is required for the growing complexity of experiments in high-energy physics. The two-fold coincidence circuit to be described was designed with these factors in view.

II. THE CIRCUIT

The configuration of the coincidence circuit is shown by the basic schematic diagram of Fig. 1. The basic configuration is one of common usage (*) and has been referred to by Wenzel[1] as a " plate addition circuit ". The input circuits, consisting of two transistors in a " long-tail-pair " serve as limiters. Negative input signals turn off fixed currents flowing in the clipping line. A pick-off diode is biased to remain non-conducting for single input signals, but to conduct on the coincidence signals. The diode current is integrated on a capacitor (1.8 k) which discharges through a pulse-shaping network into the low-impedance input of a feedback current amplifier. The output drives a terminated cable (normally 50 or 100 ohm) and is intended to operate counters or other—usually slower—coincidence circuits. The duration of the output pulse and the gain of the output amplifier can be adjusted to satisfy the needs of a particular experiment by the choice of a suitable plug-in unit which contains the elements shown within the broken line rectangle.

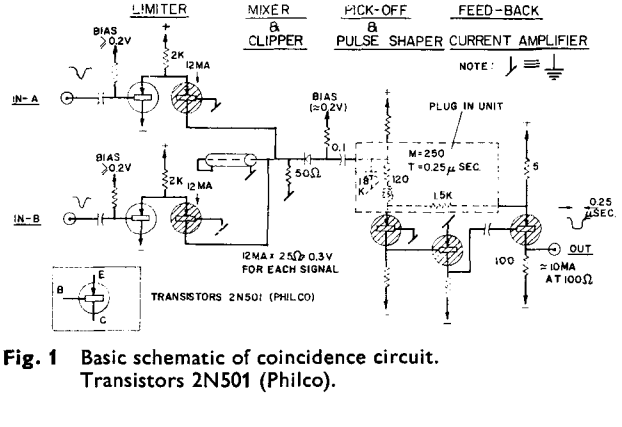

Fig. 1 Basic schematic of coincidence circuit.
Transistors 2N501 (Philco).

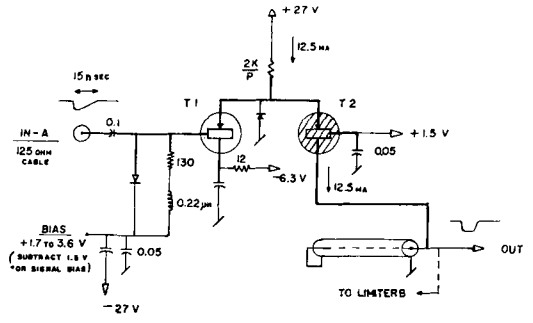

Fig. 2 Input limiter.
Heavy lines <1/2 cm long; diodes: S 570 G (transitron); transistors: 2N501 (Philco).

The input limiter

A detailed diagram of the input circuit is shown in Fig. 2. The base of the input transistor is biased 0.17 V or more positive with respect to the base of the second transistor. A current of 12 mA, determined by the emitter supply resistor flows through the second transistor. Negative input signals greater than 0.2 V will transfer the current to the input transistor reducing to zero the current flowing into the clipping line. Because of the high transconductance of the transistors, an input signal of 0.25 V is sufficient to effect this current transfer, but to obtain a rapid cut-off of the current in the second transistor, the input current must be comparable with the standing current in the transistor. For the 2N501 the basic time limitation is given by the α time-constant ($= 1/2\pi f_\alpha$) of 0.4 ns. Small signal response times are expected to be (see Appendix I) $\tau_\beta = \beta\tau_\alpha$, where β is the current gain of the transistor and is typically about 50 for these transistors. For the circuit shown, input signals of about 1 V will give input currents about equal to the standing current and can be expected to cut-off the limited current in about 1 ns.

Measurements of the response of the input limiter are shown in Fig. 3. The rise-time (10% to 90%) of the signal which appears on the clipping line is plotted as a function of the input signal amplitude for three input bias settings. (The input signals were obtained from a fast pulser, $T_R < 1$ ns, and the output was observed on an EGG oscilloscope.) The " input amplitude " is defined as that which would appear from a terminated input cable. The

(*) Fast coincidence circuits based on the addition of two limited currents on a clipping line were first described to one of us (M.S.) by Martin Deutsch in 1949.

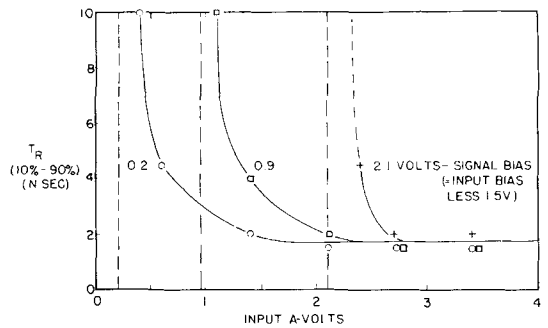

Fig. 3 Limiter rise-time vs. input amplitude.

error in the measurement of the rise-times is about 0.5 ns. The curves show the expected behavior. Signals only slightly above the signal biases (1.5 V less than the bias of the input transistor) give long output rise-times. An input amplitude one volt or more above the signal bias is required to obtain rise-times less than 2 ns. The rise-time expected for this circuit can be estimated as $2.5[\tau_\alpha^2+\tau_c^2]^{\frac{1}{2}}$ where τ_c is the time constant of the collector and stray capacitances in combination with the terminated line resistance $\tau_c \approx 15\,\text{pF} \times 25\Omega = 0.4$ ns. The expected rise-time is then 1.4 ns in good agreement with the observations.

The principal advantage of this limiter is that the circuit is normally biased in an insensitive condition. Signals much smaller than the desired ones do not disturb the quiescent current. Also, small positive overshoots from mismatching of cables will not have the undesirable effects observed when the usual pentode limiter is driven positive on the tail of a signal. It is this property of the limiter circuit which permits the use of the simple mixing arrangement adopted for this circuit. (See the discussion—particularly that associated with Fig. 2—Wenzel's report [1]).

Further advantages of the two-transistor limiter are that it provides an adjustable input threshold; that it minimizes direct capacitative coupling from the input to the clipping line; and that it presents to the input terminal an impedance which approximately terminates a 125 ohm cable for the leading edge of the input signal.

The resistor-inductor combination in the base bias circuit of the input transistor provides a low resistance path, but presents a high impedance path for the leading edge of the signal so that the whole signal current passes to the transistor. The input diode limits positive transients at the input so as to prevent breakdown of the input transistor. The diode at the common emitter junction protects the transistors against abnormally large negative input signals.

Mixer and clipper

The limited current signals from the input circuits are added linearly on a 50 ohm short-circuited clipping line. The " clipping width " is defined as twice the one-way transit time of the clipping line. Clipping widths of 3 to 10 ns are expected to be most commonly used. The choice of a 50 ohm line gives the best match of the rise-time at the mixer, due to capacitances at the collector, to the transistor response time. (See the preceding section).

Pick-off and pulse shaper

A diagram of the pick-off and pulse shaping circuit is shown in Fig. 4. A bias current of normally about 6 mA (adjustable from 0 to 13 mA) is drawn from the " Coinc. Bias " terminal. This sets a forward current of 6 mA through diode D_1 and applies, via R_3 and R_2 a back voltage bias of about 0.18 V across diode D_2. Both of these are " fast " diodes with a storage time of less than 1 ns. The combination of R_1 and D_1 has a signal resistance of 50 ohm for negative currents of 6 mA or less. Thus the 12 mA limited current from a single input operates into a terminated clipping-stub and produces clipped pulses of $(0.012)(50/2) = 0.3$ V amplitude. These pulses are too small to overcome the bias-plus-offset of diode D_2. (The " offset " of these diodes is about 0.2 V, at which forward voltage the diode current is only 0.3 mA.)

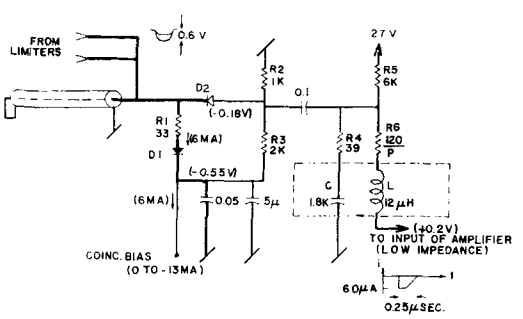

Fig. 4 Pick-off and shaper. Diodes : Q3 - 100 (Qutronic).

With coincidence signals the total limited current of 24 mA produces 0.6 V across the clipping line. During these " doubles " pulses the current in diode D_1 cuts off and 6 mA flows through diode D_2 and resistor R_4 to the capacitor C. This combination also presents an impedance of approximately 50 ohm to the clipping cable. A detailed analysis of the circuit shows that the combination D_1, R_1, D_2, R_4 presents a nearly constant resistance of 50 ohm to the clipping cable for signal currents from zero to 12 mA.

The current through D_2 on coincidences deposits a charge, of approximately 6 mA times the clipping width, onto the capacitor C. For a 6 ns clipping width the capacitor voltage rises to only about 0.02 V. The discharge of this capacitor through R_4, R_6 and L (after the coincidence) provides a shaped current pulse into the low impedance input of the output current amplifier. The shaped pulse has a duration (to half of its peak value) of $0.85\,(R_4+R_6)\,C$. The inductor L provides the shape of a " shunt compensated " pulse with critical damping. The configuration of C, R_4, R_6 and L provides a sharp leading edge to the current pulse which attains its maximum value at the end of clipped coincidence signals and decays with zero initial slope. The resistor R_5 provides an operating bias current for the following amplifier. The pulse shaping elements C and L are part of a passive plug-in sub-assembly and can be selected to give any desired output pulse duration. The values shown in Fig. 4 give a pulse duration of 0.25 μs, which was desired for operating the pulse spectrometer used for testing the coincidence circuit.

A detailed analysis of the pick-off circuit has been made assuming that the signals at the clipping stub have an exponential rise and that the diodes D_1 and D_2 are ideal rectifiers. With these assumptions the peak current of the shaped pulse is given by

$$I_{\max} = k\{t_0 - 1.4\tau - \tau \ln[1-\exp(-t_0/\tau)]\}\,, \qquad (1)$$

where t_0 is the clipping width, τ is the rise time-constant of the limited current pulse; and

$$k = \frac{I_0}{2}\,\frac{R_0}{R_0+R_4}\,\frac{0.85}{T}M \qquad (2)$$

where I_0 is the coincidence current (24 mA), R_0 is the characteristic resistance of the clipping line; T is the output pulse width (to half of peak); and M is the amplification of the current amplifier. Measurements of the output current amplitude as a function of the clipping length are given in Part IV, and agree approximately with Eq. (1).

Output amplifier

The output amplifier is designed to provide a signal amplitude suitable for operating subsequent discriminating and coincidence circuits. The amplifier diagram is given in Fig. 5. The current signal from the pulse shaping circuit of Fig. 4 is fed to the emitter of the input transistor T-5. For a step input current the emitter impedance is 50 ohm, resistive, for times $\approx T_\alpha$, but is about 4 ohm for times longer than about 6 ns (see Appendix I). (The effective input impedance of the amplifier is reduced below the above value for signals of long duration by the negative feedback). The characteristics of the pulse shaper depend only on the input impedance of the amplifier for times comparable with the duration of the output pulse. The long-time input resistance of the amplifier (<4 ohm) will thus have a negligible effect on the pulse shaper.

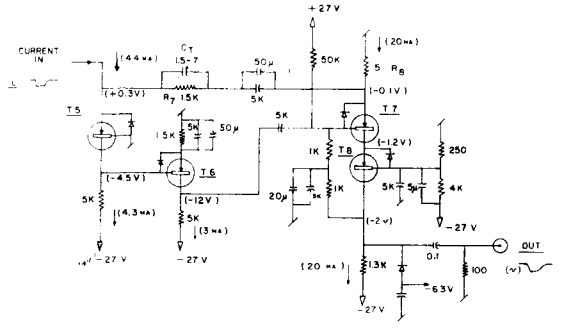

Fig. 5 Output amplifier.
Transistors: 2N501; diodes: IN 99 (all protective).

The transistor T-5 has a current gain to its collector of about 0.98. Its output current is coupled to the base of T-6 with an efficiency of 0.98. Transistors T-6 and T-7 together provide a current gain of 50^2. The overall current gain to the collector of T-8 is about 2000 when the coupling factors for the base circuits are included. A fraction of the output current, which flows through T-7 and T-8, is fed back via R_7 to the input with a return factor β of nearly $R_8/R_7 = 1/3000$. The net current gain of the amplifier

is then $300\left[1+\frac{300}{2000}\right]^{-1} = 260$ (nominally 250). There is thus a feedback factor of 7 which will stabilize the long-time amplification, but is used mainly to shorten the response-time of the amplifier. The resistors R_7 and R_8 are also contained in the plug-in unit of the pulse-shaper, as the gain and rise-time required of the amplifier depend on the pulse width selected. The gain of the amplifier is stabilized primarily by providing stabilized currents to all of the transistors. The currents are stabilized for T-5 and T-6 by the large resistances in the emitter circuits and for T-7 and T-8 by d.c. feedback to the base of T-7. The latter feedback also stabilizes the collector voltage of T-7 and T-8, as is required to ensure that the dissipation of these high-current output stages does not exceed the maximum rating of 25 mW.

The transistor T-8 serves to isolate the feedback circuit from the output, and particularly to reduce the capacitative feedback to the base of T-7 which would have a deleterious effect on the transient response of the amplifier.

The overall transient response of the amplifier is adjusted by setting C_T so as to obtain the minimum rise-time without overshoot for the output pulse. The rise-time obtained with the values shown is about 40 ns.

All the diodes shown are normally non-conducting and serve to protect the transistors against excessive voltages in the presence of abnormal transients, or at the failure of other components.

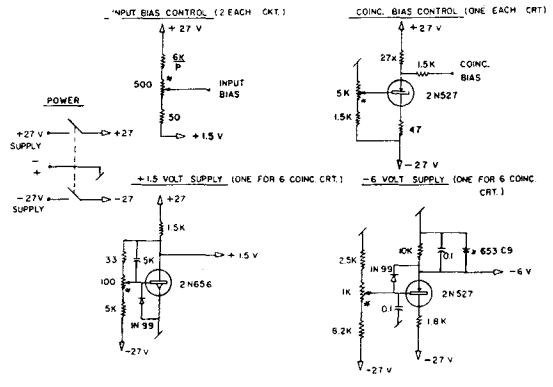

Fig. 6 Power and bias circuits.

Power and biases

The power for the coincidence circuit is obtained from two 27 V supplies, one negative grounded, one positive (Lambda LT-2095M). The auxiliary fixed voltages (+1.5 V and −6.3 V), the input bias voltages, and the coincidence bias current are derived from the primary sources by the auxiliary transistor stages shown in Fig. 6.

III. CONSTRUCTION

The coincidence circuits components shown in Figs. 2, 4, and 6 are mounted on a 20 cm by 12 cm copper plate, 1.5 mm thick in the manner of a typical computer plug-board. A circuit diagram of the coincidence board including power, or voltage, and tolerance ratings of the components is given in Fig. 7. External signal connections are made via BNC (Type 31-222) connectors mounted near the " front " end of the board, as is the connection to the clipping line. All components are mounted on ceramic terminal strips. All power and bias leads are brought to the unit via a plug-board type connector at the rear end of the board. The coincidence circuit board is shielded from external fields by copper cover plate (held by banana jacks). Photographs of the coincidence circuit board are shown in Fig. 8.

The performance of the circuit depends critically on the layout and wiring of the components, particularly those of the input, limiting, and pick-off circuits. The inductance and capacitance of all leads shown by heavy lines in Figs. 2 and 4 must be kept to a minimum. In particular, the base and emitter leads in the limiter circuit are cut to 1/2 cm and wired as directly as possible.

Six coincidence boards are mounted in a plug-board rack. The power and bias control wires are connected via the plugs to a separate control chassis which serves the 6 coincidence boards. The control chassis also has a meter and switch which permits monitoring of all the supply voltages, and the bias potentials and currents of the coincidence circuits. A rack containing 4 coincidence circuits and a control panel are shown in photographs of Fig. 9. (In one of the photographs two auxiliary boards are also shown in the plug rack.)

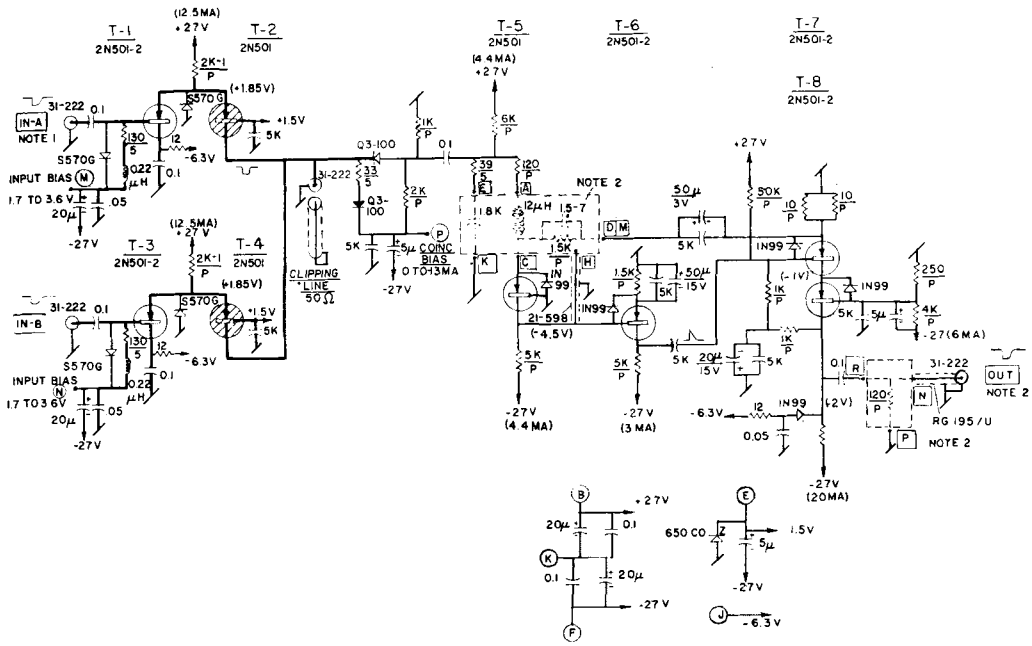

Fig. 7 Complete schematic of coincidence board.

Note 1: Approx. terminated for 125 Ω cable.

Note 2: Plug-in unit determines amplifier gain, pulse width, and output impedance. Values shown for plug-in unit Model 710B. M = 250, T = 0.25 μs, R_{out} = 100 Ω.

Note 3: 2N501-2 represents a 2N501 transistor selected to have $50<\beta<100$ at currents near 7.5 mA.

M etc.: Refer to power plug type 133-022-21-1022. (Connects to control ckt. 10-T-479.)

E etc.: Refer to plug-in unit connector type 143-015-01-1015.

—: Heavy lines must be kept short.

⊣⊢: Capacitors: 50 V ceramic; or 50 V electrolytic unless noted.

—/\/\/\—: Resistors: 12 = 1/2 watt; 6K/5 = 5% composition; 1K/P = 1% metal film.

IV. PERFORMANCE

The performance of the coincidence circuit has been measured with input signals from a pulser and with signals from scintillation counters in a particle flux.

Pulser tests

Two input signals were obtained by a "tee" from a mercury relay pulser and fed via matched 125 ohm cables and separate attenuators to the two input terminals. The signal rise-times were less than 1 ns. Measurements were made of the amplitude of the output signal current (observed on an oscilloscope) as a function of the input signal amplitudes and delays. For these measurements the input amplitude is defined as that signal amplitude which would appear if the input cable were terminated in its characteristic impedance (125 ohm). The input pulse was rectangular with a width of 10 ns. The measurements were made with a 6 ns and with a 3 ns clipping width. The latter is considered the smallest width which will give reliable operation. For all the measurements reported here the circuit was operated with the minimum input bias, with the coincidence bias set at 6.5 mA, and with the amplifier pulse width and gain at 0.25 μs and 250, respectively (as obtained with the parameters of Figs. 4,5.)

The output amplitude as a function of the input amplitude, for equal input signals, is shown in Fig. 10. In Figs. 11, 12 are shown the measurements of the output amplitude at coincidence as a function of the amplitudes of the two input signals. It is evident that the circuit will operate satisfactorily on input signals of short rise time if their amplitudes are about 0.5 to 1.5 V; the larger amplitude being required for the shorter clipping widths.

In Fig. 13 the output amplitude is shown as a function of the clipping width for equal, coincident inputs (both inputs = 3.6 V). The curve in the figure has been computed from Eq. (1) (Section II) with the

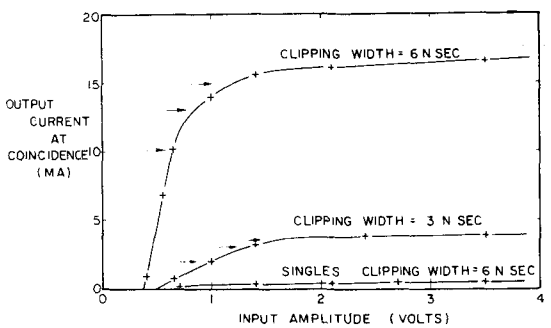

Fig. 10 Response for equal coincident inputs.

parameters k and τ adjusted to fit the curve to the observations. The values of τ and k obtained by this fit agree within 25% with values computed from the known circuit parameters.

The output amplitude as a function of the relative delay of the input signals is given in Fig. 14. The width of these curves is approximately equal to clipping width as is expected.

Counter tests

Measurements have been made of the performance of the coincidence circuit when operated by the signals from two scintillation counters. Three scintillation counters approximately 16 cm × 20 cm × 1 cm coupled by 10 cm light pipes to 6810-A photomultipliers were arranged to count the particles (mostly

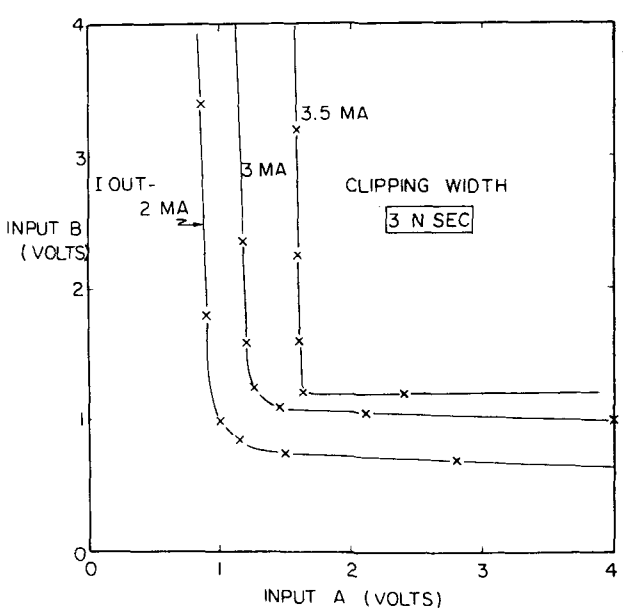

Fig. 11 Output amplitude at coincidence.

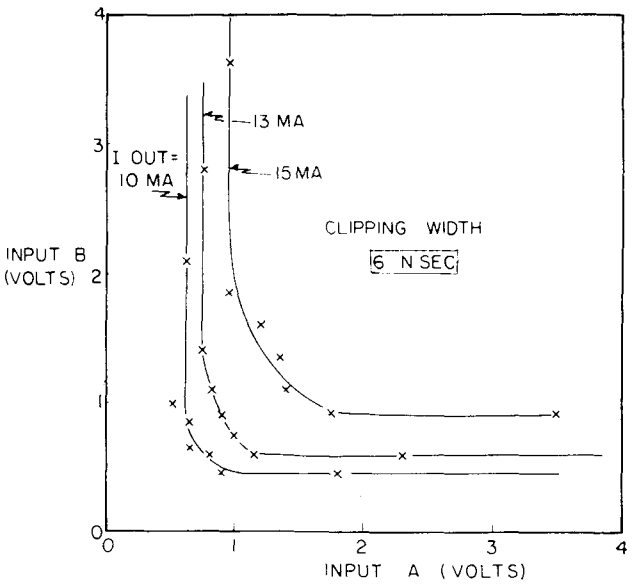

Fig. 12 Output amplitude at coincidence.

pions) from a target in the bremsstrahlung beam of the Cal. Tech. synchrotron. The first two counters of the array operated the fast coincidence circuit. The first counter was not shielded, and had a singles counting rate, during the beam pulse of about 10^6 pulses per second, (mostly electrons). The second

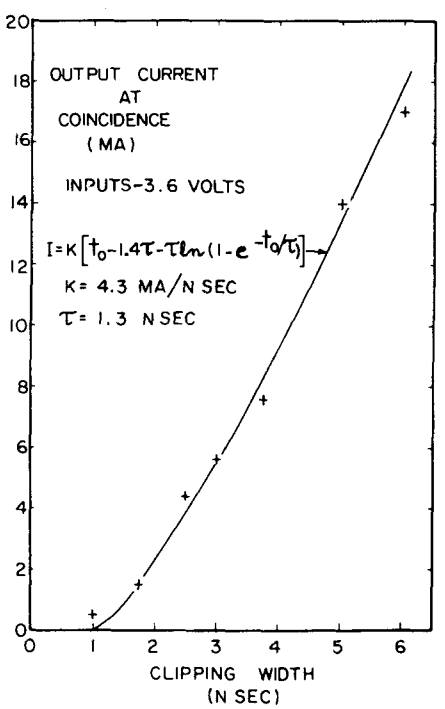

Fig. 13 Characteristics of the pick-off and pulse shaper.

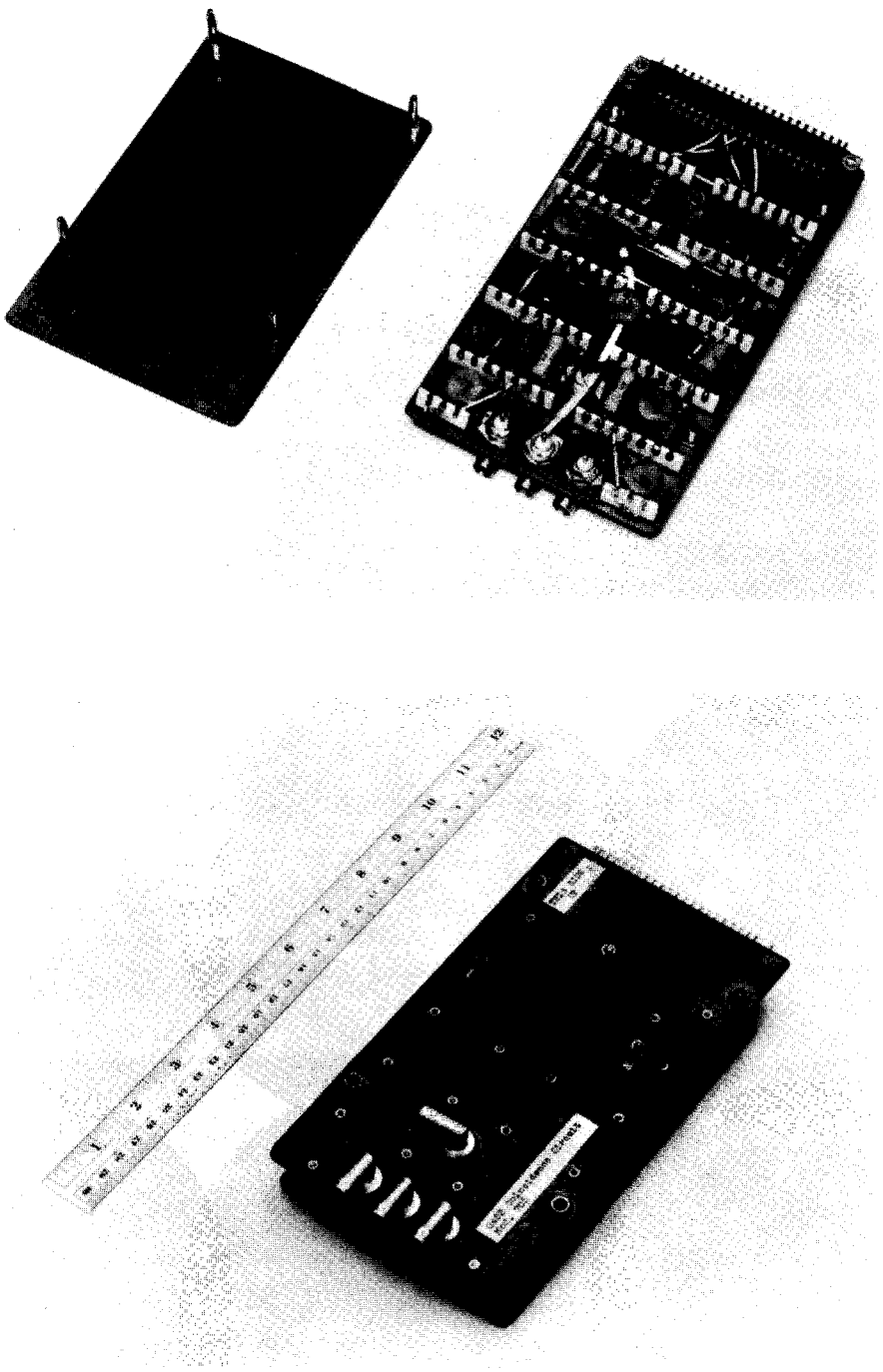

Fig. 8 Two views of coincidence board.

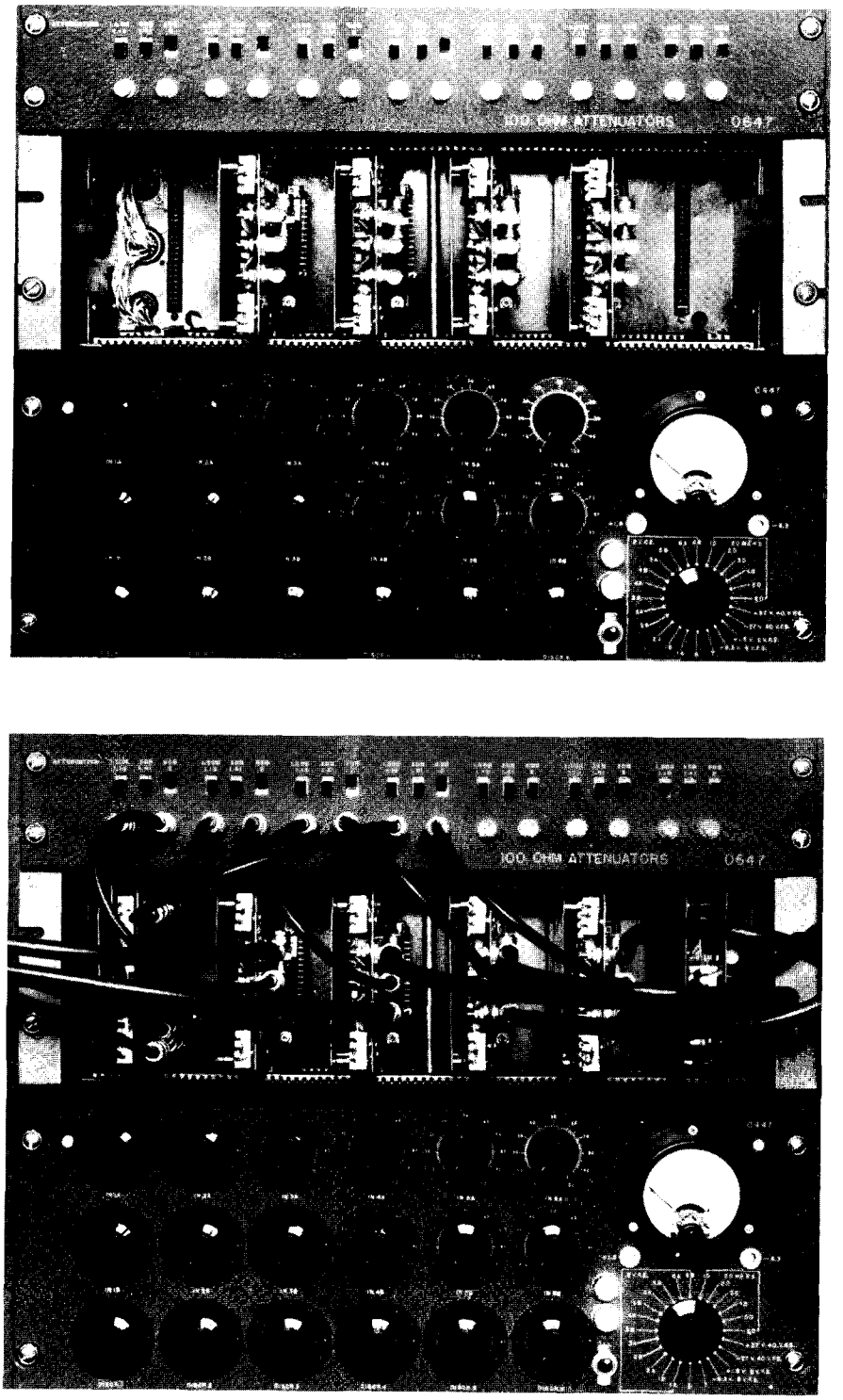

Fig. 9 Coincidence boards in plug in rack with power and control panel.

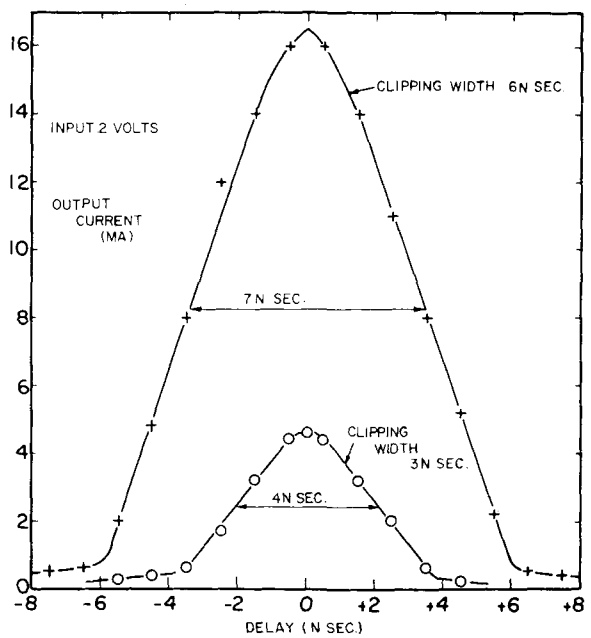

Fig. 14 Output amplitude vs. delay.

counter was separated from the first by 5 cm of lead and had a singles rate of about 10^5 pulses per second (during the beam pulse). The third counter of the array was placed behing the second counter and was completely surrounded by an additional 10 cm of lead. The output of the coincidence circuit was fed (with further amplification) to a 20 channel pulse spectrometer (kick-sorter). The third counter operated conventional 0.1 μs circuits and its output was used to gate the spectrometer so that the events which were recorded corresponded to minimum ionizing particles traversing the first two counters.

The photomultiplier tubes were operated with a total voltage of about 2.5 kV. With these voltages, the pulse height from minimum ionizing particles

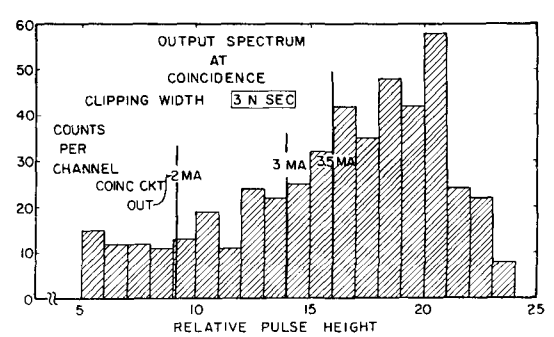

Fig. 15 Output pulse spectrum at coincidence.

was about 3 V and had a rise-time of about 4 ns when the cable was terminated at both ends with 125 ohm.

Pulse spectra obtained from the coincidence circuit, with the input cable lengths adjusted to give the maximum counting rates, are shown in Figs. 15, 16. The spectrum is quite sharp for the 6 ns clipping width, but is rather broad for the 3 ns clipping width. The cause of this pulse spread has not been certainly identified, but is presumed to be related to the rather long rise-time of the input signals.

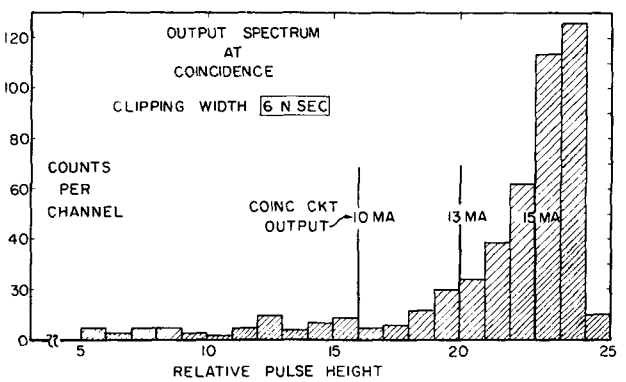

Fig. 16 Output pulse spectrum at coincidence.

The coincidence rate as a function of the relative delay of the two input signals was measured by taking pulse spectra such as those in Figs. 15, 16 with the length of cable to the two inputs adjusted to give several relative delay times between the two input signals. With each delay setting the pulse spectrum was obtained for the same integrated flux in the synchrotron beam. The results of these measurements are given by plotting the total number of output pulses larger than some particular amplitude. These amplitudes called " Output Bias " are expressed in terms of the current out of the coincidence circuit, and are indicated by the heavy lines in Figs. 15, 16.

The counting-rate vs. delay curves obtained are given in Figs. 17, 18. The curves with the intermediate output biases appear to have a flat top which would indicate a high counting efficiency, but the increase in the counting rate with decreasing bias is somewhat large. There has been no opportunity as yet to investigate the origin of the small output signals. It is felt, however, that with a 6 ns clipping time and with an output bias of 10 mA the efficiency of the circuit is probably greater than 90%. The

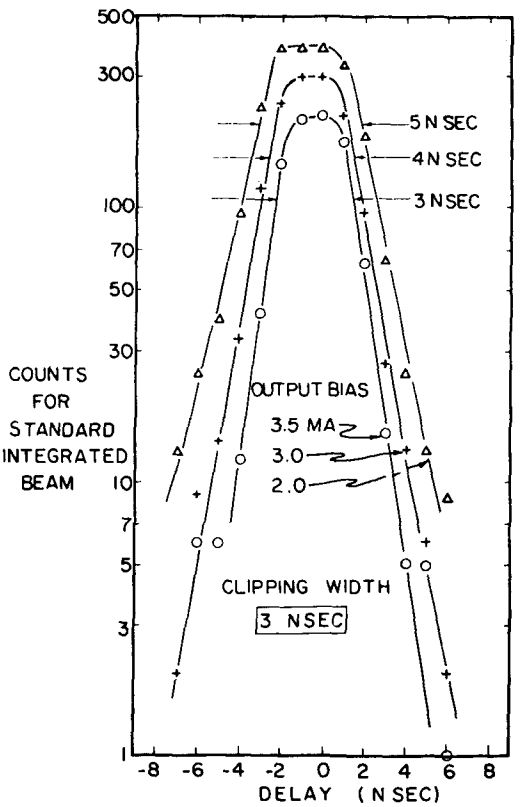

Fig. 17 Counting rate vs. delay.

maximum coincidence rate corresponds to only about 50 counts per second during the beam pulse.

The widths of the delay curves at half maximum are indicated in the figures and are close to what is expected for the clipping widths used.

The slope of the sides of the delay curves is, for the various curves, between 1 and 2 ns per decade in counting rate, and is quite acceptable for a two-fold coincidence rate of only about 100 c/s during the beam pulse (10^{-4} of the singles rate in the first counter) (*).

Stability

The only two factors which are expected to introduce variability into the operating characteristics of the coincidence circuits are the supply voltage and the temperature. The supply voltages are provided from supplies regulated to 2% and are monitored continually. The circuits have been designed to minimize the temperature dependent effects which appear primarily in the current-voltage characteristic of the base circuits of the transistors. The amplitude of the output signal at coincidence has been measured with the whole circuit at 20°C and at 40°C. At the two temperatures the output signals were the same within the 5% accuracy of the amplitude measurements.

Multiplexing

The input resistance of the coincidence circuit described here is comparable with the impedance of the input cables. It is not possible to connect more than one coincidence circuit to one photomultiplier tube (P.M.T.) without significant loss in signal amplitude (**). Yet in many experiments it is necessary to obtain several coincidence combinations from one counter. It is also often desirable to connect several counters to one coincidence input. Transistor " multiplexing " circuits have been made

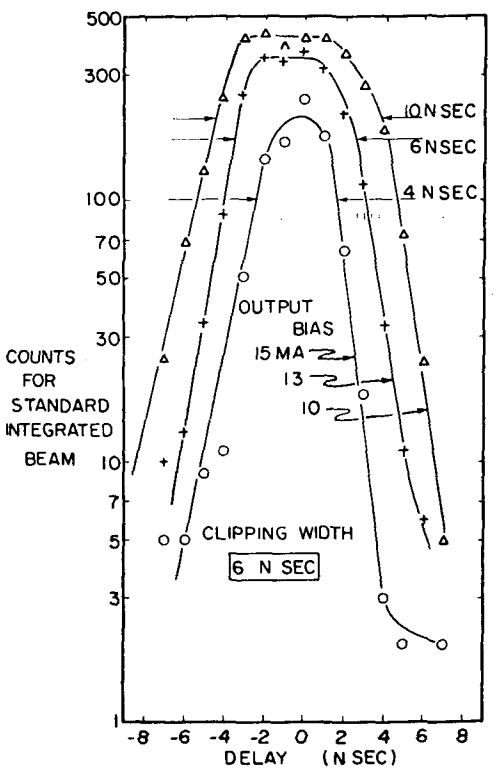

Fig. 18 Counting rate vs. delay.

(*) The somewhat steeper slopes obtained by Wenzel [1] were with 3-fold coincidences.

(**) Several input grids of vacuum tube coincidence circuits are often connected to one signal lead by connecting them as elements in a lumped component delay line.

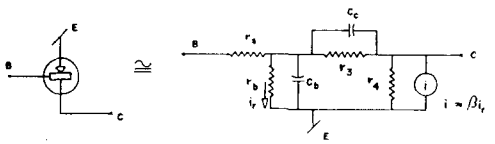

Fig. 19 Equivalent circuit of a base input stage.

$r_s \approx 50\ \Omega$ $\quad \beta \approx 50$

$r_b \approx \beta \frac{kT}{qI_e} \approx 125\ \Omega$ $\quad \tau_\alpha = \frac{1}{2\pi f_\alpha} \approx 0.4\text{n s}$

$r_b c_b \approx \tau_\beta \approx \beta\, \tau_\alpha \approx 20\text{n s}$ $\quad r_3 \approx 250\ K$

$r_4 \approx 10\ K$

$c_c \approx \frac{A}{V_c^{1/3}} \approx 5\ \text{pF}$

Note: r_b is not as usually defined in the literature.

for connecting several P.M.T.s to one coincidence input (mixing), and for connecting up to 5 circuits to one signal source (splitting).

The mixing circuit consists simply of several transistors as emitter input stages (grounded bases) with the collectors connected in parall.l to an output cable. The response time of these circuits is determined primarily by the common collector capacitance. For more than two inputs, the collectors should be connected as stages of a lumped-element line. With this arrangement the output rise-times obtained are about 1 ns.

The circuit used for coupling one P.M.T. to several coincidence circuits is shown in Fig. 21. The large signal rise-time is about 2.5 $N\tau_\alpha$ where N is the number of output channels, and is, therefore, comparable to the rise-time of the signals from a P.M.T..

Several of the coincidence circuits have been constructed and operate uniformly as described here. Five circuits have been incorporated in an experiment on pion photoproduction now in progress. Several more are being constucted to form the basis of other experiments. It is felt that the convenience, reliability, and stability of these circuits will make it feasible to perform experiments more complex than any which have been attempted before.

APPENDIX I

An approximation to the small-signal equivalent circuit of the 2N501 transistor which is convenient for fast transients is shown in Fig. 19. The large resistances r_3 and r_4 have a negligible effect on the response in low impedance circuits and are usually neglected. The resistance r_s (" base spreading resistance ") is ohmic, but the other parameters depend on the operating currents and voltages. Typical

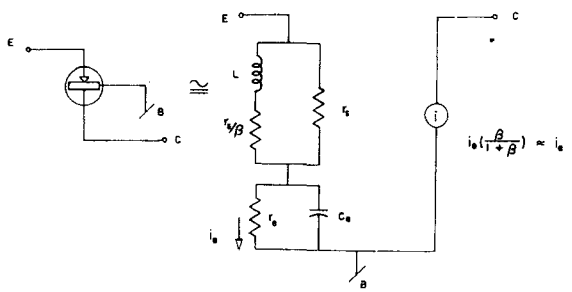

Fig. 20 Equivalent circuit of an emitter input stage.

$r_s \approx 50\ \Omega$

$r_e = r_b/\beta \approx 2\Omega$

$r_e c_c \approx \tau_\alpha$

$L/r_s = \tau_\alpha = 0.4\text{n s}$

$L/r_e \approx \frac{r_s}{r_e} \tau_\alpha \approx 6\text{n s}$

values and the nature of the principal dependencies are given in the figure. The typical values apply to an emitter current of about 10 mA and a collector voltage of a few volts. The representation shown becomes inadequate for time scales less than τ_α.

Neglecting C_c, r_3, and r_4 one can obtain the convenient equivalent circuit for a grounded base stage that is given in Fig. 20. It should be noted that although the effective input resistance for slow signals is only about 4 ohm, the input impedance for fast signals approaches r_s. The input resistance can be taken as r_e only for transients whose time scale is longer than $L/r_e \simeq 6$ ns.

It has been found convenient to select the 2N501 transistors used in certain circuits. They are sorted into groups according to whether (1) $\beta < 50$, (2) $50 < \beta < 100$, (3) $100 < \beta$. Members of the second group are designated " 2N501-2 " and are used in critical circuits to ensure predictable performance.

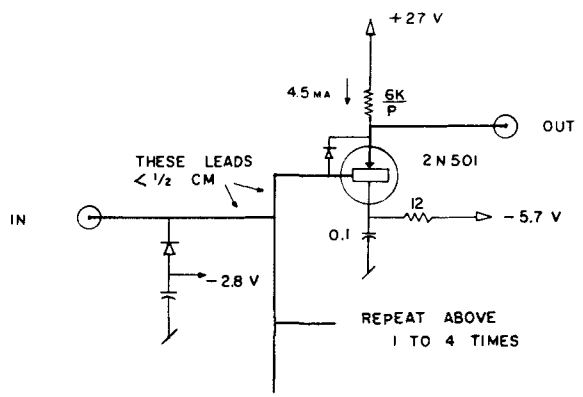

Fig. 21 Circuit for coupling one P.M.T. signal to 2 to 5 coincidence circuits.

LIST OF REFERENCES

1. Wenzel, W. A. Millimicrosecond coincidence circuit for high speed counting. UCRL (*) 8000, October 2, 1957.
2. Garwin, R. L. A fast coincidence-anticoincidence analyzer. Rev. sci. Instrum. *24*, p. 618-20, 1953.

DISCUSSION

ODIAN : I would like to know what is the particular advantage of using transistors over diodes in limiting circuits and in Rossi coincidence circuits.

SANDS : You can make circuits as fast as 4 or 5 mμs and much cheaper and smaller with transistors. I think the circuit should be faster than the ordinary diode circuits and have other desirable operating properties because of the opportunity for amplitude selection. One works on the fast leading edge of the pulse and one can particularly get rid of the overshoot problem which one observes in various diode circuits or simple limiting circuits, the overshoot from mismatched cables and pile up of small pulses and things of that sort.

LUNDBY : We have the attitude that the transistor has a much longer recovery time than a diode, so that we always proceed by putting a diode in front in the coincidence circuit and then follow it by transistors as much as you do. You would find that a pulse following about 10 ns afterwards would still have difficulties in driving the coincidence circuit. Is this not the case?

SANDS : I believe that is not the case. So long as one does not drive the transistor into saturation, that is, does not let the collector bottom, keeping always a volt or more on the collector, then the time constant characteristic of the transistor is 0.4 ns. However, you do get very long storage time effect if you let this transistor saturate. Actually, diodes are only now beginning to approach the fundamental response time which one gets with these transistors.

KANDIAH : I would like to ask a question on the subject of matching of the cable that carries the signal from the photomultiplier. Is it not true that when you are driving the transistor with a pulse whose rise-time is somewhat shorter than the t_α, particularly when you drive into the base, there is a serious mismatch for a period which is dependent on t_α and β so that it is always necessary to terminate the cable at the sending end; secondly, in order to avoid this overloading of the base emitter voltage, you put diodes in various places to stop signals exceeding a certain amount; does not this also add to the problem of reflected signals travelling back along the cable?

SANDS : I did not mention it, but one of the problems with transistor circuits is that the low input impedance poses some problems, particularly with respect to putting one signal to several circuits. However, you will find in the contribution a little discussion of that point. It is true that the input impedance is, in general, low and essentially capacitive, not of the order of τ_α but even of the order of τ_β, which is much longer. The particular circuit shown has a compensating resistor inductance combination at the input which, together with the transistors, just about terminates the 120 ohm cable, which is another reason for using transistors instead of diodes. To be conservative, we often terminate the cable at the other end too. But we have found it is not necessary, and these measurements were not made with the cable terminated at the sending end.

KANDIAH : May I add one point. The β quoted there of 50 for the 2N501, is that really typical? Our experience is that it is a good deal lower than that, a factor probably about between 5 and 10.

SANDS : Oh no. We select our transistors into three categories : β less than 50, β between 50 and 100, and β greater than 100, and we add a little number to them and specify them in our circuits—which one should be used, and I have forgotten the fraction, but a large fraction of them come out 2N501-2 which has a β between 50 and 100.

LITTAUER : I would like to confirm Sands' experience there and to point out that the 2N501 is a type of transistor whose β decreases rather rapidly as the standing current is decreased and that some laboratories are using some instruments which test β statically at low current levels; one underestimates the effect of β very severely.

SANDS : I agree.

(*) See note on reports, p. 696.