LHCb Global Timing and Monitoring of the LHC Filling Scheme

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ABSTRACT

The LHC experiments rely on a proper and stable timing for the sampling of the detector signals, and for the synchronization of the readout system. The LHC timing is distributed and received at the experiments by a system which is common to all experiments. The control and monitoring of the reception and the integration into the overall experiment control system has been developed individually by each experiment. In addition, the experiments have developed methods to monitor the LHC bunch timing based on beam pickups in order to assure the required stability of the experiment clock with respect to the bunch arrival times, and the position of the interaction region. In LHCb, this system also allows monitoring the individual bunch intensities and the filling scheme which are vital to the special random triggers used for both the online and offline determination of total luminosity and luminosity per bunch. The timing resolution is such that it also allows detecting ghost and satellite bunches down to $2*10^9$ protons in any 2.5ns RF bucket. The bunch monitoring system developed by LHCb is also used by the ALICE experiment.

This document describes the LHCb global timing, the central distribution, and the control and monitoring as well as the consequences for the operational procedures. It also presents the experience and results during the beam commissioning, during which it provided valuable information to the LHC, and the first months of LHCb data taking.

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1 Introduction

In the LHC accelerator, particles are accelerated in Radio-Frequency cavities with which a time-varying electrical field is applied. This variation is synchronous to a ~400.79MHz radio frequency clock (RF) which defines 35640 buckets along the LHC accelerator. A bucket is defined as a time interval where a bunch of particles can be found. Each bucket has a time extension of ~2.5ns. The injection of bunches of protons (or ions) is described by the filling scheme of the LHC. The minimum time interval between two consecutive bunches is defined as ~24.95ns allowing 3564 defined locations, while the maximum number of bunches of protons (or ions) allowed in the machine is 2808 per beam due to the gaps associated with the rise time of the PS/SPS/LHC injection kickers and the LHC dump kicker. A division (1:10) of the RF frequency is defined as the Bunch Clock, while a pulse at every RF bucket 1 is defined as the Orbit Clock or Orbit Revolution Pulse [1]. The clocks are re-phased to the beams in order to provide two separate and independent Bunch Clocks (BC1 & 2) as well as two separate and independent Orbit Pulses (ORB1 & 2). The beams are coarsely locked together already at injection ("cogging") to force the appropriate collision schemes at the experiment IPs, and a fine adjustment is applied during the ramp for the interaction region to be at the optimal position for the experiments.

In reality, the phases of the received clocks at the experiments are not constant, but they depend on temperature effects, beam capture effects and also inherent jitter of the clock. In addition, various operational problems during the preparation of the physics fills may lead to wrong filling schemes and ghost or satellite bunches with offset collisions which in turn may affect data quality and luminosity counting. It is therefore vital for the experiments to be able to control the timing and monitor all these parameters with high precision. The complete hardware and software framework to perform these tasks are described in this note together with the performance and the operational experience.

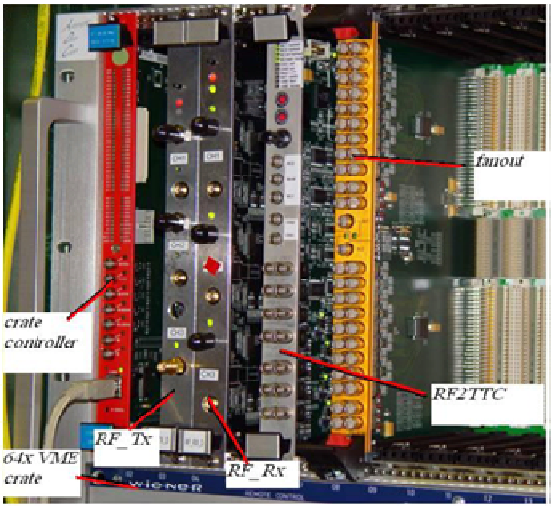

Figure 1: Picture of the Timing Crate.

2 LHC Timing Reception and Distribution at LHCb

The LHC clocks physically reach the location of the LHCb experiment via 14.1 km of fibres buried up to 1m underground. A Timing Receiver Crate, developed by the PH/ESS group with the

participation of the experiments [2], receives the clock, converts it, cleans it with narrow band quartz-based PLL circuits and fans it out to the whole LHCb Timing and Fast Control system [3].

The Timing Receiver Crate is a standard 6U VME64x compatible crate. As shown in Figure 1, it contains two so called RF_Rx modules [4] which convert the optical signals of the three Bunch and the two Orbit clocks coming from the SR4/CCC into electrical signals. A so called RF2TTC module [5] converts the clocks into ECL signals and allows performing various adjustments on each signal before making them available to the experiment timing system. The RF2TTC can also produce an internal set of clocks to drive the electronics of the experiment independently of the state of the RF system at Point 4 while there is no beam. The RF2TTC allows selecting the source for the Main Bunch Clock and the Main Orbit Clock outputs.

Finally, the two Main Clocks are fed into two dual 1:18 ECL Fan-Out modules, the first of which provides each LHCb Readout Supervisor (ODIN) with the Bunch Clock and the Orbit Clock in order to perform the readout control of the entire readout chain and the event management. As shown in Figure 2, in order to provide the readout electronics with the cleanest clock possible, the second fan-out feeds directly the Bunch Clock to the so called TTCex boards which perform the encoding of the experiment clock together with the two channels for trigger and readout control commands. The TTCex converts the multiplexed signal to optical and transmits it to the Front-End electronics and the Readout Boards. Configurable high-resolution delays in the TFC Switches allow adjusting the data channels for optimal sampling by the TTCex boards.

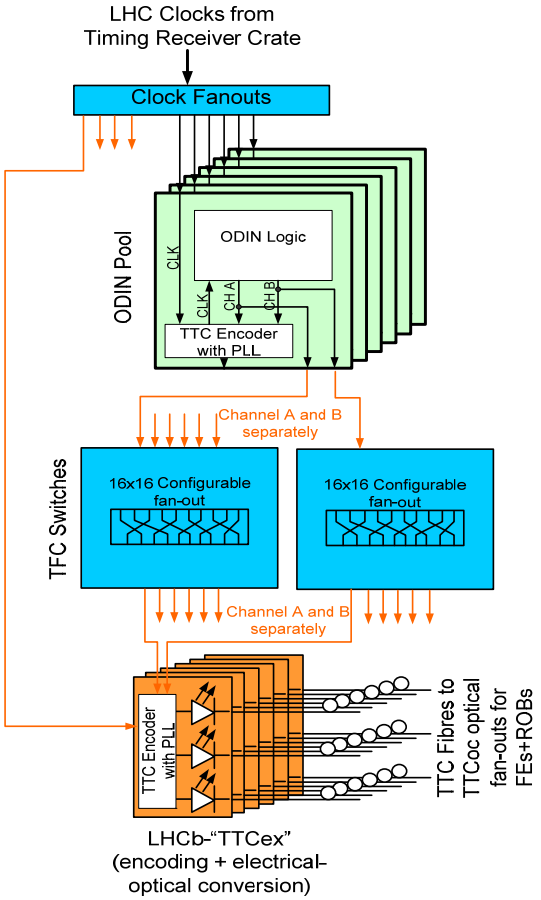

Figure 2: Layout of the distribution of timing, trigger and the readout control commands to the Front-End electronics and the Readout Boards by the LHCb Timing and Fast Control system.

A reset of the clocks and a resynchronization of the SPS and the LHC is performed at each fill before the SPS-LHC transfer of bunches, with the consequence that the clocks disappear for ~1ms. As the reset is made in the SETUP Beam Mode, LHCb switches from the internal clock to the machine clocks when the injection phase starts. There are also other cases in which the clocks are resynchronized. A precise list of the modes and the states in which the LHC machine/RF group provides stable clocks has been specified [1].

The phase of the clocks distributed to the experiments is fixed with respect to the RF clock at the RF "installation" at point 4. However, during the acceleration of the protons from the injection energy at 450 GeV to the collision energy, a slow frequency change of the clock is expected. At 7 TeV the change in the 40 MHz frequency amounts to about 86.8 Hz. The jitter of the Bunch Clocks can be as large as up to 300 ps during the ramp due to the adjustments made in order to track the rising magnetic field.

In addition to this, a drift of the clock phase is expected due to the exposure of the fibres to outdoor temperature variations. For LHCb, the expected typical drift is about 352 ps/degree of temperature, corresponding to 24.96 ps/(degree of temperature*km). This implies a typical day-night drift of ~140ps and a seasonal drift (from winter to summer considering a 20 ºC variation) of ~7 ns. In order for the LHCb sub-detectors to operate optimally with no impact on the track efficiencies and energy calibration, the phase must be maintained within a range of +/-0.5 ns.

Consequently, the LHCb requirements on the timing demands continuous monitoring of the timing reception of the clocks and the bunch arrival times in order to display timing trends and raise alarms in the LHCb control room in case of possible malfunctions. It also implies being able to fully and reliably control the timing reception in order to reconfigure the system for different purposes, and to re-optimize rapidly the global phase of LHCb. It should also feed timing status information to the LHC control room.

3 Monitoring of LHC Timing and Filling Scheme

In order to perform a precise monitoring of the timing and the bunch structure, a machine-independent system based on beam pickups has been developed. It allows monitoring at high-speed and high-precision the phase of each bunch with respect to the clock edge of the global LHCb clock, and the intensity of each bunch of the two beams.

3.1 Beam pickups

The two dedicated beam pickups (Figure 3) are part of the LHC accelerator complex and are referred to as BPTX.5L8.B1 and BPTX.5R8.B2 (Beam Pickup Timing eXperiment Left/Right of IP8 in Cell 5 on Beam 1 and Beam 2). They are installed ~150m away from the LHCb interaction point on each of the incoming beams and are based on button electrodes with a capacitive pickup. As shown in Figure 4, they produce a bipolar pulse which is a direct representation of the phase and the intensity of each bunch. The functioning of such buttons is well described in [6] and [7]. At the passage of a bunch, the positively charged bunches will cause the free-moving electrons of the metallic beam pipe to form a mirror charge on its surface. This mirror charge will follow the bunch around the accelerator giving rise to an image current, with equal magnitude but opposite sign compared to the bunch current. The image current will also travel over the circular electrode surface of the button pick-up and give rise to a signal. Since the energy of the signal captured by the pick-ups is negligible compared to the energy of the beam, this set-up can be used to monitor

the beam without influencing it. Figure 4 shows a simulation of the expected pulse shape from a single button at different intensities and Figure 5 shows the expected pulse shape for different bunch lengths for a bunch of the same intensity. In practice each BPM station consists of four button pick-ups symmetrically mounted around the beam pipe. To first order, the sum of the pulse from all four buttons is independent of the transverse position of the beam. However, as shown in Figure 5, the energy and length of the pulse change with bunch length demonstrating that the zero-crossing point is not the optimum for the phase measurement. A calibration against bunch length and bunch intensity must therefore be performed in order to achieve the optimum phase measurement.

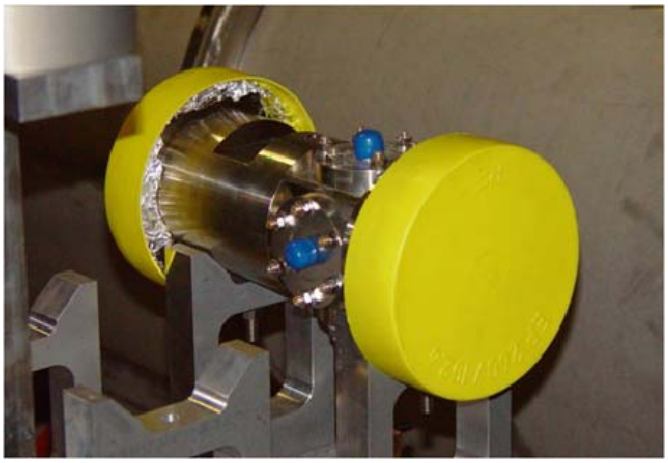

Figure 3: Picture of one of the LHCb beam pickups.

The bipolar pulse is fed via ~250/280m of Nexan ½" CMA50 coaxial cables, with a ~2dB of attenuation ratio at 80MHz per 100m and a very low signal-to-noise ratio, to a custom-made LHCb readout electronics board which measures the intensity and the phase of the beam bunch-by-bunch.

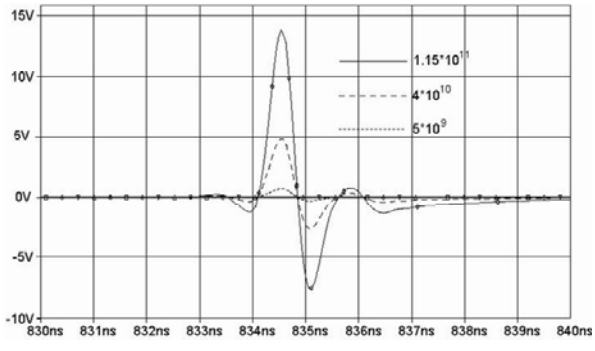

Figure 4: The pulse shape from simulation for different bunch intensities from a single button electrode.

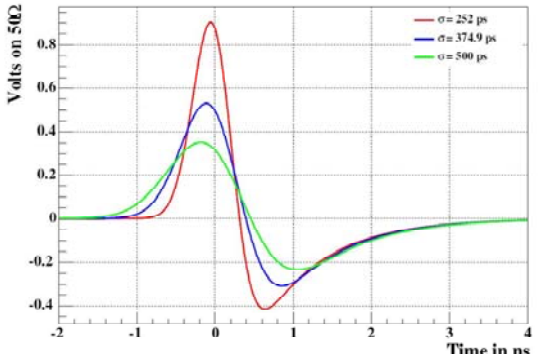

Figure 5: The pulse shape from simulation for different bunch lengths.

3.2 Beam Pickup Readout Electronics

In order to process the signal coming from the BPTXs, LHCb has developed a Beam Phase and Intensity Monitor (BPIM) readout board. The main requirements for the board are:

1. Analogue processing of the complete bipolar pulse.
2. Measure with good resolution the intensity of each circulating beam in the machine and measure the current of every single bunch.

3. Measure with very high precision the phase of the arrival time of each bunch at the LHCb interaction point with respect to the LHCb Bunch Clock edge.
4. Flexible readout control, signal processing and monitoring logic onboard.
5. Fast control interface to the LHCb Control System via Ethernet.
6. Cross check the operational information sent by the LHC (filling scheme, beam currents, beam phases) and signal anomalies.
7. 6U VME board to fit in the crate of the Timing Reception system.

The proposal of a custom-made board instead of commercial hardware (oscilloscope-based system used in ATLAS and CMS) was driven by the aim to achieve highest level of automation, precision and flexibility. The heart of the board is therefore an FPGA with more than ~8000 logical elements (ALTERA APEX 20K200E). Two 16-bit wide and 16-bit deep FIFOs assure enough memory to process data from multiple turns of the LHC. A 12-bit pipelined ADC performs digital conversion at 40 MHz of the processed analogue input signal and a 27 ps resolution TDC operating at 40 MHz provides high resolution for the measure of the bunch passages with respect to the clock edge. Moreover the board is equipped with a Credit-Card sized PC with glue logic in order to support the board busses and interface with Ethernet to the LHCb Control System.

The board has been fully developed, tested in the SPS and produced at CERN and is extensively described in [8].

3.2.1 Intensity Measurement

Figure 4 shows that the input bipolar pulse generated by the beam pick-ups is a very sharp pulse with a width of about 1.5/1.8ns and an amplitude of about 20V peak-to-peak. In order to measure the current contained in one bunch, an integration of the area of the bipolar pulse is necessary. This is achieved by a rectifier stage which inverts the positive part of the bipolar pulse, sums it up to the negative part and then integrates the pulse analogically. Very fast current amplifiers (4.58V/ns slew rate and 1.7GHz bandwidth) are used for this analogue stage. The integrated pulse is then fed to an Analogue-to-Digital Converter (AD9432BST from Analog Devices, 105 MHz MSPS max, pipelined) which outputs a 12-bit value at 40 MHz to the main FPGA onboard for processing.

The integrator is then reset every 25ns in order to be ready to integrate the next bunch and introduces a dead-time of ~3 ns. This allows reading out full orbit intensity measurements as a function of the bunch crossing.

The intensity data is also output continuously through an 8-bit general purpose output on the front panel which allows interfacing it to the LHCb Readout Supervisor ODIN for storage in the ODIN data bank with each event at 40 MHz.

3.2.2 Phase Measurement

As mentioned above, the aim of the phase measurement chain is to produce a digital value that represents the phase of each bunch sampled by the BPTXs with respect to the LHCb Bunch Clock of the LHC. This measurement on the two beams also allows monitoring the difference in bunch arrival time of beam 1 and beam 2, the so-called ΔT, in order to guarantee the proper fine-cogging of LHC and thus well-positioned bunch crossings longitudinally at the IPs.

As shown in Figure 5, ideally, a threshold corresponding to a fraction of the input pulse corresponds to the stable sampling point for the phase measurement. However, due to the extreme pulse characteristics a simplified adjustable “constant-level crossing” method is used. For this purpose, the timing measurement employs two Digital-to-Analogue Converters to define two threshold levels for a comparator:

1. A threshold which defines the presence of a pulse associated to real beam and allows noise suppression.
2. A constant-level threshold that defines the sampling point on the falling edge of the positive half of the bipolar pulse.

The two thresholds are fed to a high performance comparator (MAX9601EUP, dual ECS/PECL 500 ps, Ultra-High-Speed Comparator by Maxim) which compares the level of the input pulse with the threshold levels. A validation pulse is then produced using high-speed flip-flops and is fed to the Time-to-Digital Converter together with the pulse generated from the clock edge which is used to restart the internal TDC counter.

The TDC used is the ultra performing TDC-GPX produced by ACAM [9]. The datasheet specifies a TDC resolution of about 27 ps with a 28-bit time counter corresponding to a time range of 40 μs.

3.2.3 Clock distribution

The clock distribution throughout the whole board is crucial since it affects the measurement of the phase. To minimize the uncertainties related to the measurements, the clock is distributed differentially from a single clock driver/fan-out to the entire board. The board is equipped with an ECL input for the Bunch Clock and an ECL input for the Orbit Clock.

Three programmable cascaded delay chips assure enough margins to shift the phase of the clock in the board by a maximum amount of 30 ns, covering the whole extension of a bunch clock. This allows adjusting the optimal signal integration and ADC sampling.

3.2.4 Firmware

The firmware is written in VHDL and contains mainly the functions for the beam monitoring. An overview of the data flow and the functional blocks are shown in Figure 6. The main blocks are:

- TDC controller and ADC controller
- FIFOs controller
- Clock delay controller
- Thresholds controller
- I/O interfaces.
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The heart is the effective Digital Signal Processing block which continues to evolve with new implementations to satisfy requests for additional functionality, in particular with respect to the information fed back to the LHC.

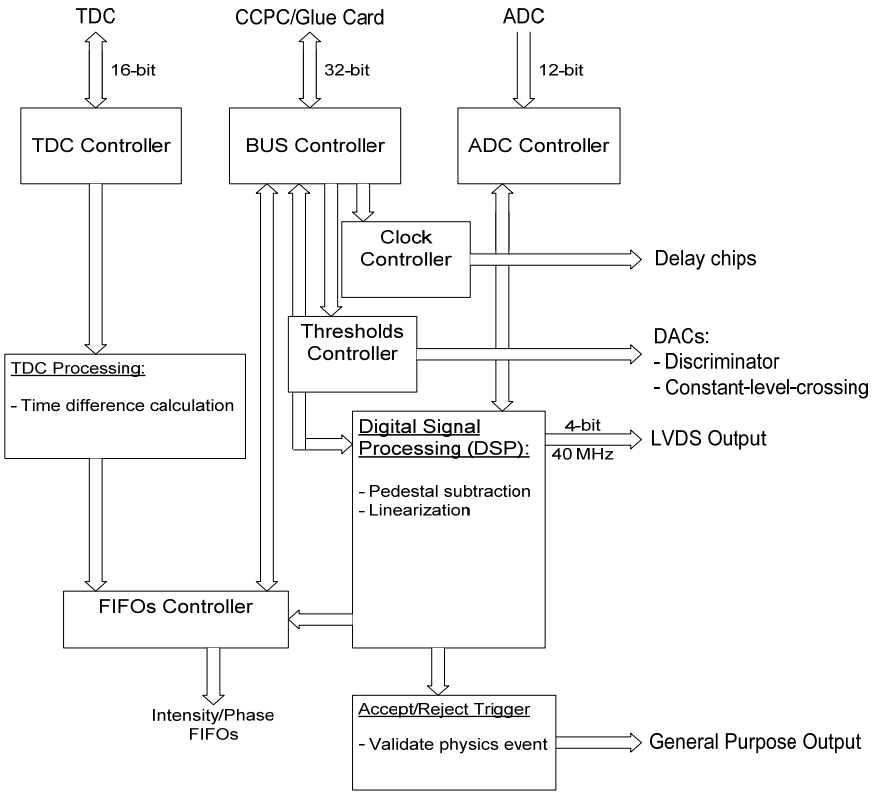

Figure 6: Overview of the data flow and functional blocks in the BPIM firmware.

4 Control and Monitoring

4.1 Control System Architecture

Figure 7 shows the architecture of the control and monitoring system for the Timing Receiver electronics and the Beam Phase and Intensity Monitor. The control system is built with PVSS [10] running on a UPS fed power redundant Linux PC and is an integral part of the LHCb Experiment Control System. The control and monitoring of the Timing Reception electronics is controlled and monitored via the VME bus by a crate controller based on the CAEN V1718 VME-USB bridge [11]. A VME/USB server performs the hardware accesses to the Timing Receiver electronics and communicates with the PVSS system using DIM [12].

The control interface on the Beam Phase and Intensity Monitor readout boards is based on a Credit Card-sized PC[13] with Ethernet running a strip-down version of Linux and which performs the access to the board resources via the PCI bus converted to native hardware busses by glue logic[14]. A server based on the same generic protocol on top of DIM allows the PVSS system to configure and monitor the electronics.

The general software architecture and communication protocol of this system is the same as that for the LHCb Timing and Fast Control and is described in details in [15]. The system also allows generic subscription to monitoring information for continuous archiving and permanent display in the control room.

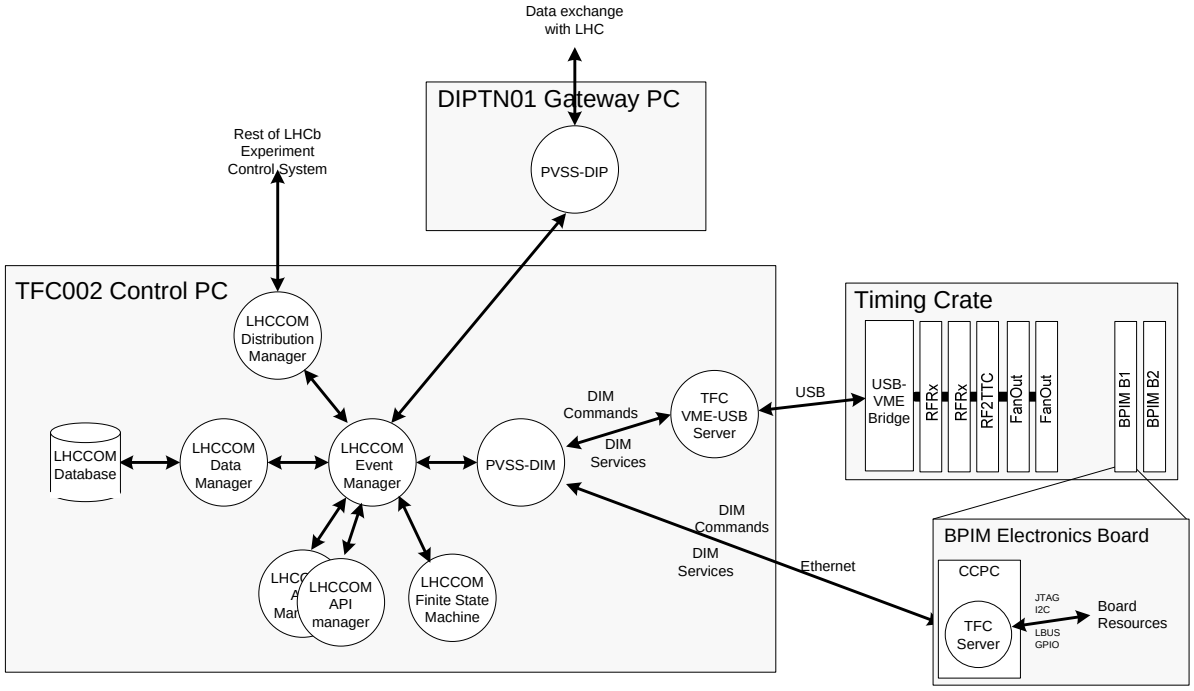

Figure 7: Architecture of the control system for the timing reception and timing monitoring.

The system is part of the LHCb Finite State Machine framework allowing easy control and transmission of states and alarms to the overall LHCb Control System and the LHCb Alarm screen. Also all important monitoring parameters are logged in an online Experiment Condition Archive together with all other running conditions such as LHC machine and beam parameters, luminosities, rates, backgrounds, and running performance.

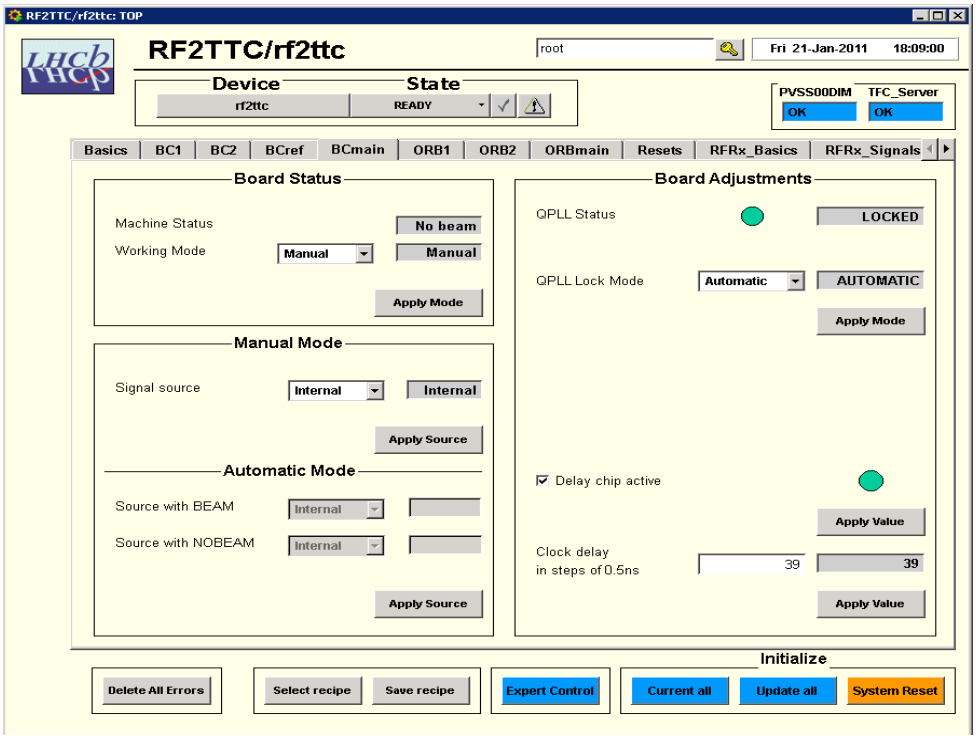

Figure 8: An example of an expert control panel for the Timing Receiver electronics.

4.2 High-level Control and Monitoring

Figure 8 shows an example of the control panels of the RF2TTC which allows configuring the whole Timing Receiver system and fine adjusting the global clock phase of LHCb, as well as selecting the source of the clocks. Normally these panels are operated by experts only.

The monitoring data retrieved from the Timing Receiver and the BPIM is processed and displayed in the LHCb control room on a dedicated screen (Figure 9).

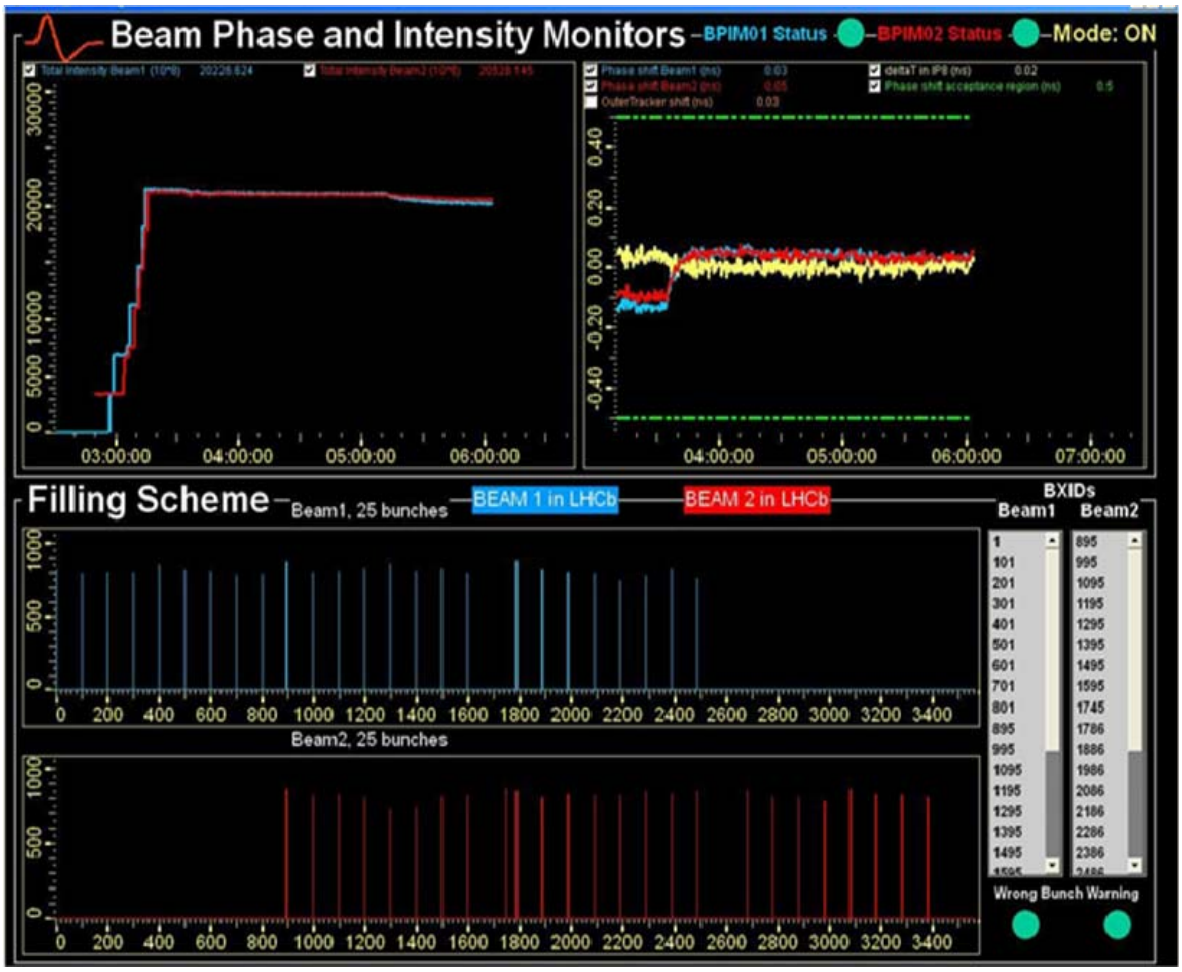

Figure 9: Screen shot of the LHCb timing display in the Control Room. The top left square trends the intensity measurement of both beams (beam 1 in blue, beam 2 in red). The steps are the increase of intensity at each injection of a batch of four bunches. The top right square trends the phase measurement for beam 1 (blue), beam 2 (red) and the so called ΔT. The increase in phase is due to the ramp of the beams from 450 GeV to 3.5 TeV. The two bottom squares plot the filling scheme for each beam with a complete list of the Bunch Identifiers in the machine. Also, a "Wrong Bunch Warning" flag signals to the LHCb control room if the measured filling scheme in the machine does not correspond to the expected scheme as received from the LHC.

The main operational parameters which are monitored by the LHCb shifters are:

1 – *Bunch-by-bunch currents*: Each bunch intensity is measured continuously at 40 MHz. This monitors the LHC filling scheme, which is used in the LHCb Readout Supervisor to flag the events with the crossing type (empty, beam 1 only, beam 2 only, beam1 on beam2) and in order to

count triggers in different types of crossings for online luminosity purposes. It is also used in ODIN to produce calibration triggers and the special random triggers which are used to determine the luminosity precisely offline. If the filling scheme does not match the scheme which is received directly from the LHC during the injection phase, it is signalled by a "Wrong Bucket Flag" to both the LHCb control room and to the LHC control room. Also, the sum of each of the measured bunch intensities is displayed as the total current for each beam. This information is made available to ODIN via a direct hardware connection in order to insert the information in the ODIN data bank per event.

2 – *Bunch-by-bunch phases with respect to clock edge*: Each bunch arrival time at the LHCb Interaction Point is compared to the rising edge of the global LHCb clock. In April 2010, during the first month of running with LHC circulating beams at 3.5TeV, a calibration of the phases were performed in order to define two offsets for the clock phases associated with beam 1 and beam 2. These offsets are used to calculate a "zero-phase reference", which gives a quantitative indication of the shift of the timing with respect to the LHCb ideal sampling phase. The LHCb global timing is then re-adjusted in between fills via the RF2TTC board to compensate for any shift described in Chapter 3.2. An averaged value of the "zero-phase shift" for beam 1 is archived in the LHCb Conditions Database and is used in the offline reconstruction for correcting the Outer Tracker T0 of the drift time.

3 –*IP time offset (called ΔT):* By measuring the relative phase of each bunch with respect to the clock edge, it is possible to get the difference in arrival time of the two beams at the IP, which in the case of head-on collision is equivalent to a displacement of the centre of the luminous region along the beam line by $\Delta T*c/2$. This information is fed back to the LHC control room and is used by the RF system for fine cogging purposes, i.e. in order to tune the RF phases of the beams to centre the IPs in the experiments.

5 Performance of the Monitoring with first LHC beam

The BPIM system was developed and the prototype tested in the SPS in 2007 and results are extensively described in [8].

5.1 Commissioning with first LHC beams at 3.5 TeV

The commissioning of the full system has been performed during the first month of operation at the LHC with beams at 3.5 TeV, between the 30th March and the 7th of May 2010. During this period the phase of the beams with respect to the clock edge as measured by the BPIMs-BPTX were compared to the drift time in the LHCb Outer Tracker detector and to three stations of the LHCb Muon detector. Figure 10 shows the trend over the considered period, where outliers due to calibration runs are removed and where the measurements were normalized to the initial phase at the 30th March. On 7th of May, the global LHCb clock was shifted back by 2.5ns in order to re-centre the sampling point of the detector.

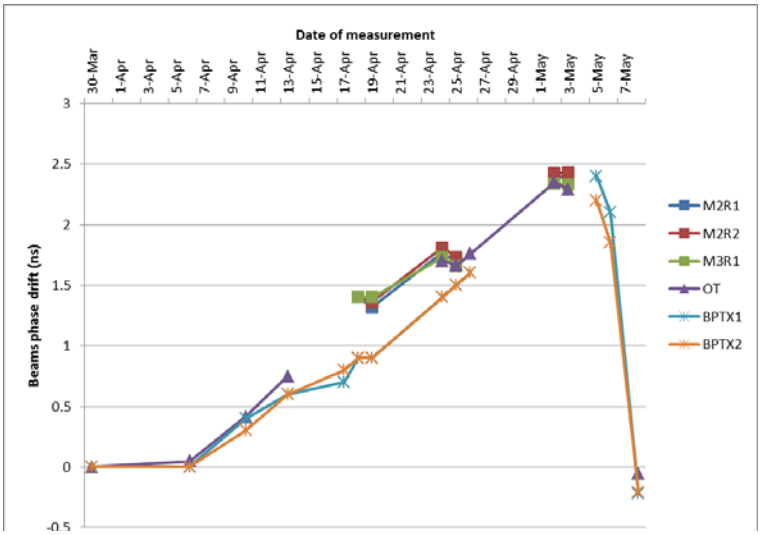

Figure 10: Trend of the clock phase drift as measured by the BPIM, the LHCb Outer Tracker and the Muon Chambers.

5.2 Intensity Calibration

In order to calibrate the intensity measurement and correct for any non-linearity, measurements were first performed with only the BPIM readout board in the lab using a very fast signal generator. The input pulse generated by the signal generator had the same shape as the pulse generated by the BPTX during the passage of the beam, and the phase of the pulse was set up in order to perform the integration of the pulse in the exact same conditions as during normal beam operations. A calibration curve of the area of the pulse measured in V*ns using an oscilloscope, was plotted against the raw ADC values and fitted, as shown in Figure 11. The fit was made with a third-order polynomial.

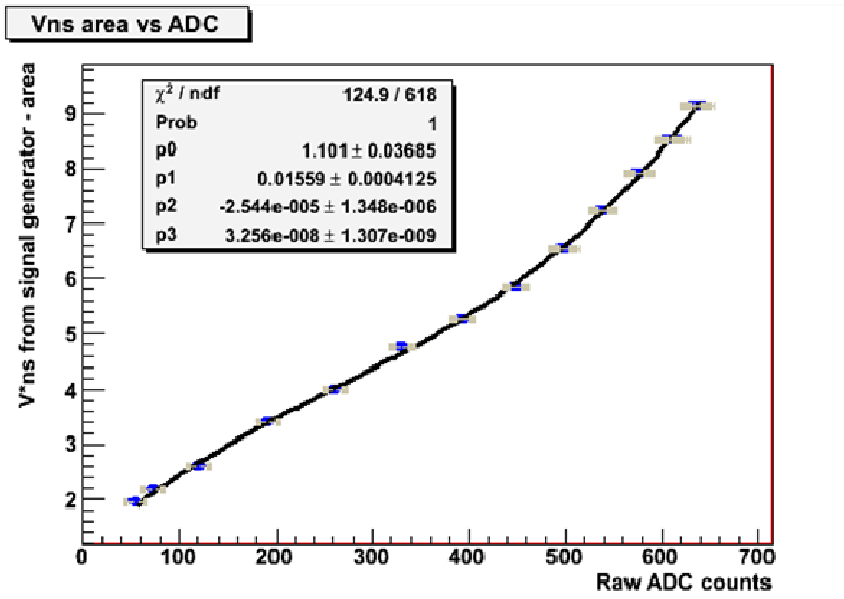

Figure 11: Calibration curve of the integrator circuit and ADC performed with a signal generator.

Also, a fudge factor was determined in order to convert the corrected ADC counts to a proper measurement of the bunch and beam intensities expressed in protons per bunch. This was performed in Fill 1250 by comparing with the LHC Direct Current Bunch Current Transformers which provide continuous measurements of the total beam intensities. Figure 12 shows the intensities measured by the DCBCT for beam 1 and beam 2 as a function of the BPIM ADC counts. The plots were fitted with the calibration curve of the integrator circuit in order to obtain the global conversion factor to intensity. The dynamic range of the ADC results in an intrinsic resolution of $1.8*10^8$ protons-per-bunch/ADC count for BPIM1 and $3.5*10^8$ ppb/ADC count for BPIM2. As the baseline subtraction is about 20 ADC counts, the minimum intensity which can be measured by the BPIM is about $4*10^9$ protons-per-bunch (ppb) for beam 1 and about $6*10^9$ ppb for beam 2.

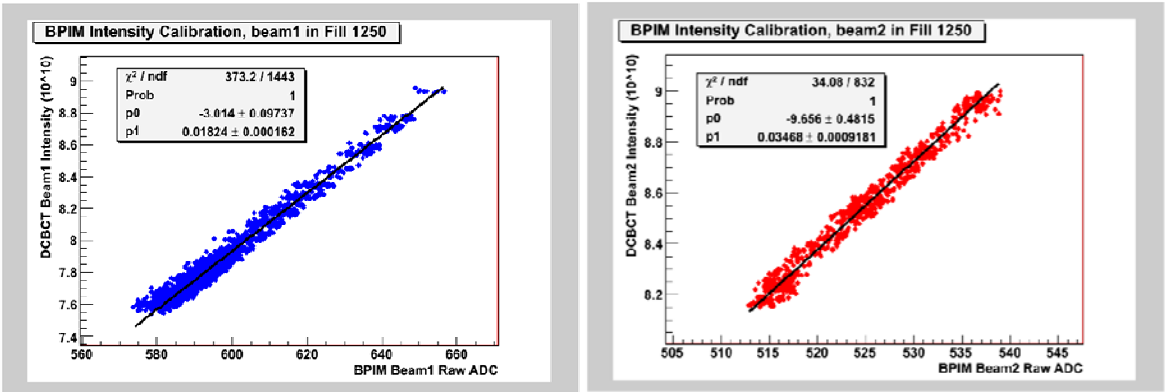

Figure 12: Determination of the global conversion factors for the intensity measurements of beam 1 and beam 2 using the calibration curve of the integrator circuit.

It should be noted that the understanding and calibration of the DCBCT evolved during 2010 and that the calibration work will continue. Nevertheless, in order to get an indication of the error on intensity measurement, Figure 12 also shows the spread of the measurements around the fitted values. The error is therefore about $1.6*10^7$ ppb for beam 1 and $9.2*10^7$ ppb for beam 2.

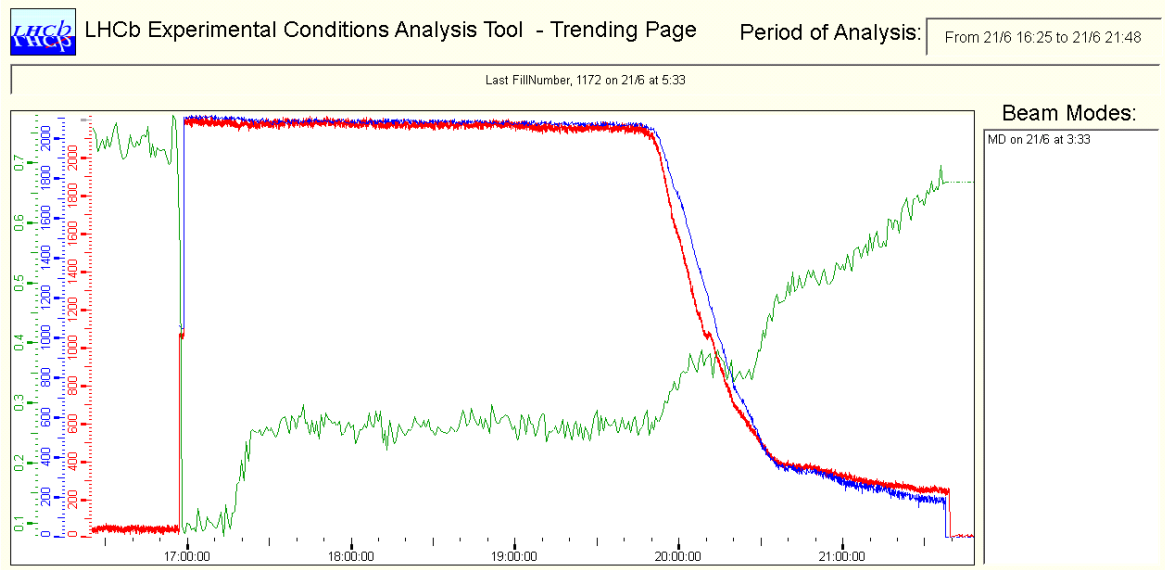

Figure 13: Trend of the intensity measurement during a scraping test by the LHC from 10^{11} protons per bunch down to $2.2*10^{10}$. From top to bottom: Beam 1 intensity as measured by the LHC DCBCT (red). Beam 1 intensity as measured by the LHCb BPIM (blue). Beam 1 phase with respect to clock edge as measured by the LHCb BPIM (green).

During Fill 1172, the LHC machine performed a test in which beam 1, containing two bunches, was scraped from a high intensity of about $1.1*10^{11}$ protons per bunch to a low intensity of about $2.2*10^{10}$ protons per bunch. Figure 13 shows the trends of the raw intensity values. This provided an opportunity to check the linearity correction over a wide range of intensities and check the assumption that the energy of the bipolar pulse of the BPTX pickups is directly proportional to the bunch intensity.

The intensity conversion function obtained from the data in Figure 11 and Figure 12 was used to correct the data obtained with the BPIMs during the scraping test, and check how well the correction apply to the BPIM data. In Figure 14, the intensity measurement from the LHCb BPIM for beam 1 is plotted against the intensity measurement from the LHC DCBCT. The corrected data with the conversion function are also compared to the non-corrected data, i.e. the raw BPIM data from the scraping test. The corrected data are finally fitted with a linear function to show how that the slope is almost unitary and the offset is almost zero. This confirms that the calibration curve can be used to correct real data and obtain a linear relation between the LHC measurement and the LHCb measurement.

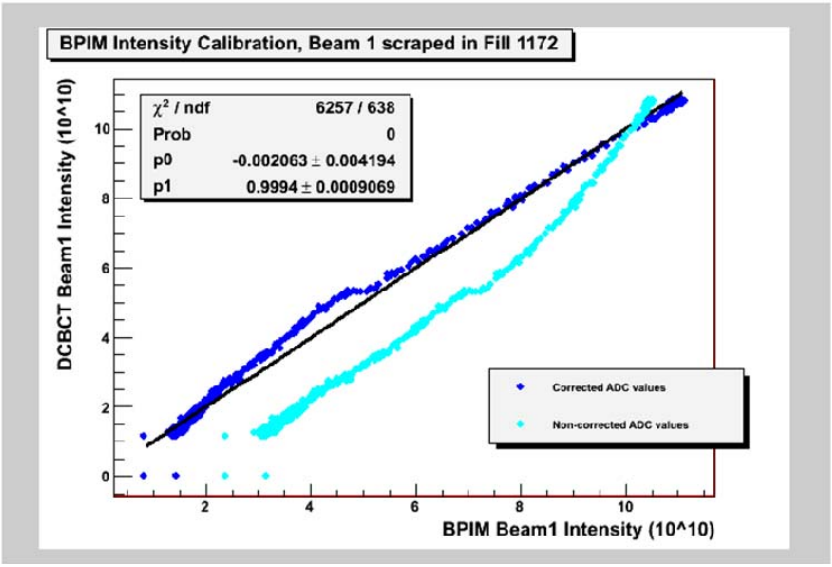

Figure 14: The corrected data (dark blue) with the calibration curve are compared to a linear fit and to the non-corrected data (light blue). Some non-linearity is still present. This is largely due to other beam effects during the scraping test.

It is however important to note that even though the calibration curve applied to data improves drastically the intensity relation, some non-linearity is still clearly visible. Also a jump is present during which the DCBCTs detected no change in intensity while the BPIMs did. To a large extent these effects are attributed to a change in the bunch shape and to de-bunching which takes place during the beam scraping. The effect of changes in bunch length on the pick-up signal is shown in Figure 5. An effect is also visible in the phase measurements at this point.

5.3 Phase Resolution

In order to evaluate the resolution of the phase measurement, Fill 1233 was selected since it had no strong changes in the bunch intensities and temperature variations were small. It lasted for more than 15 hours during which LHCb recorded 65 nb^{-1}. Figure 15 shows the phase

measurements for beam 1 and beam 2, and the ΔT trend for the entire fill. The phase shift due to the daily temperature drift is very visible and will be analyzed more in detail in Chapter 5.4.

The data sample was stripped down to the period between 11am (start of STABLE BEAM period) and 5 pm during which the temperature was reasonably stable and little drift was observed. The data was fitted with a linear function in order to eliminate the small drift and produce the distribution of the spread of the measured phases. Figures 16 and 17 show the distribution for the phases of beam 1, beam 2 and the ΔT.

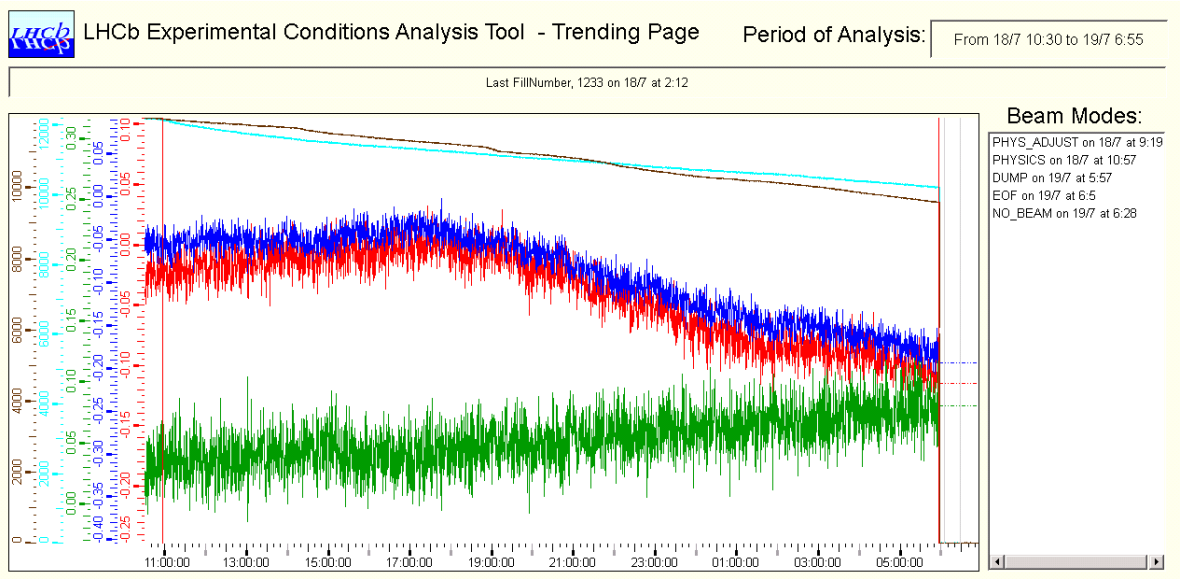

Figure 15: Trends of the clock phases and the difference in arrival time between beam 1 and beam 2. From top to bottom: Beam 1 intensity as measured by the LHC DCBCT (light blue). Beam 2 intensity as measured by the LHC DCBCT (brown). Beam 1 phase with respect to clock edge as measured by the BPIM (blue). Beam 2 phase with respect to clock edge as measured by BPIM (red). ΔT as calculated from the phase measurements (green).

Each of the three distributions agrees with a Gaussian distribution and the RMS of the distribution is about 12 ps-13 ps for both beam 1 and beam 2 phases, which becomes 17 ps for the ΔT measurement. The ΔT measurement also takes into account cable adjustments in order to give a precise quantitative measurement of the shift in time at the collision point.

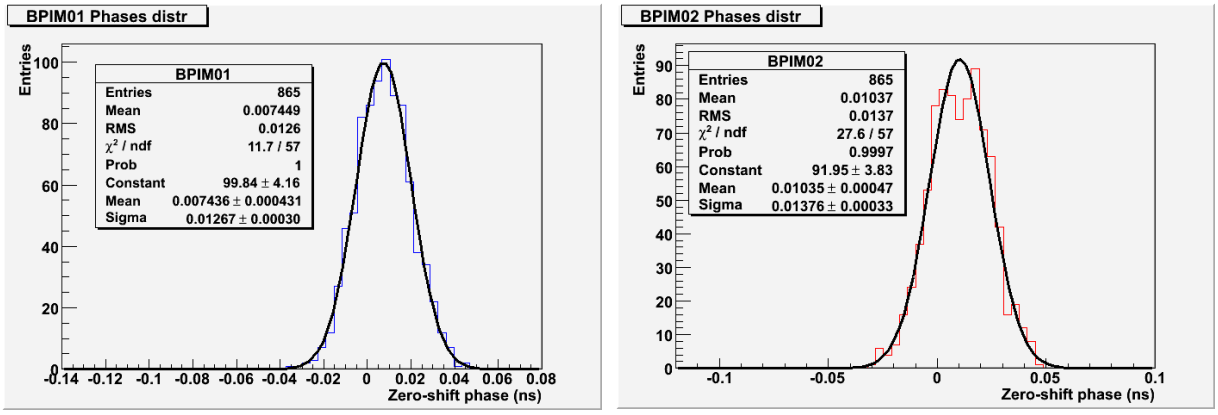

Figure 16: Distributions of the spread of the measured phases for beam 1 (left) and beam 2 (right).

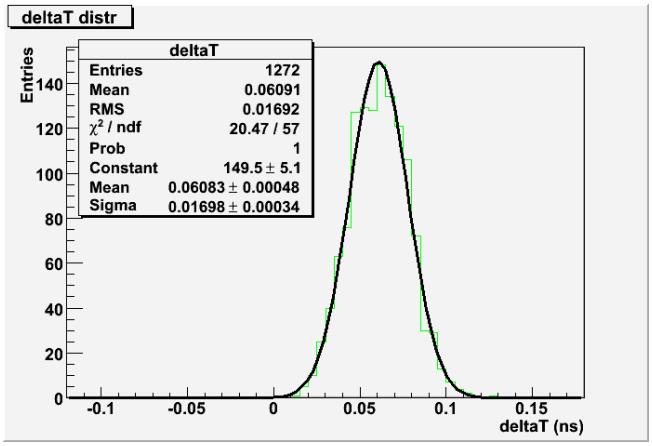

Figure 17: Distributions of the spread of ΔT.

5.4 Phase Shift due to Temperature Drifts

As mentioned in Chapter 3.2, the phase of the bunch with respect to the clock edge varies with the outdoor temperature. Fill 1222 allowed quantifying the drift as it lasted for more than 11 h and there was a strong temperature change in the morning. The calculated ΔT was stable and no particular beam losses were observed meaning that the shift was entirely due to temperature drifts. Figure 18 shows the comparison between the measured zero-shift phases and the temperature during the STABLE BEAMS period. The temperature went from 20 °C to about 28 °C in 5 hours and the phases shifted by about 100 ps during the same interval.

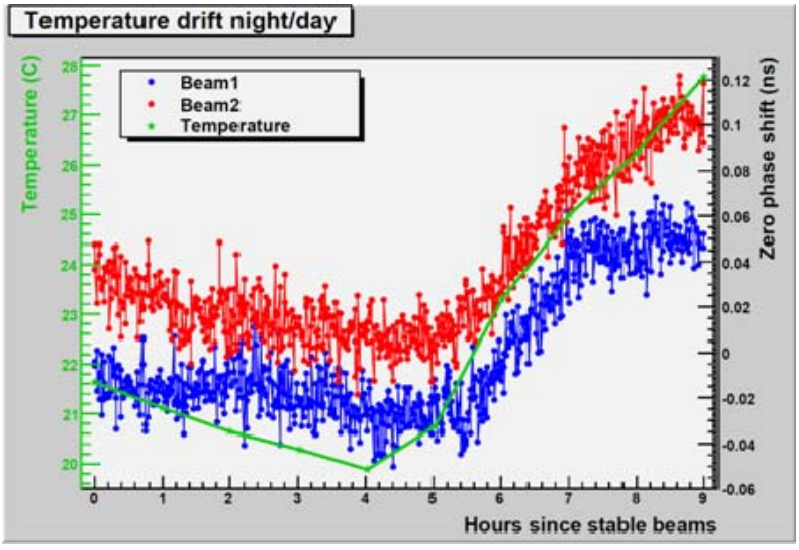

Figure 18: Trend plot comparing the zero-phase shifts of beam 1 (blue), beam2 (red) and temperature (green). The temperature changed by about 8°C in 5 hours and the zero-shift phases varied by about 100ps. This means that the clock edge was late by 100 ps with respect to the arrival time of each bunch of each beam at the end of fill with respect to the beginning of fill.

Figure 19 shows the zero-phase shift and the temperature drift over a period of about 90 days from the beginning of May to mid-July. During this period the global LHCb timing has been shifted seven times, each of them by 0.5 ns in order to compensate against the timing drift. The zero-

phase shifted by a total amount or 4 ns, while the average temperature went from 10°C to about 25°C. This corresponds to a shift of about 260 ps/deg over the 13 km of fibres that connects LHCb to the LHC global clock distribution system.

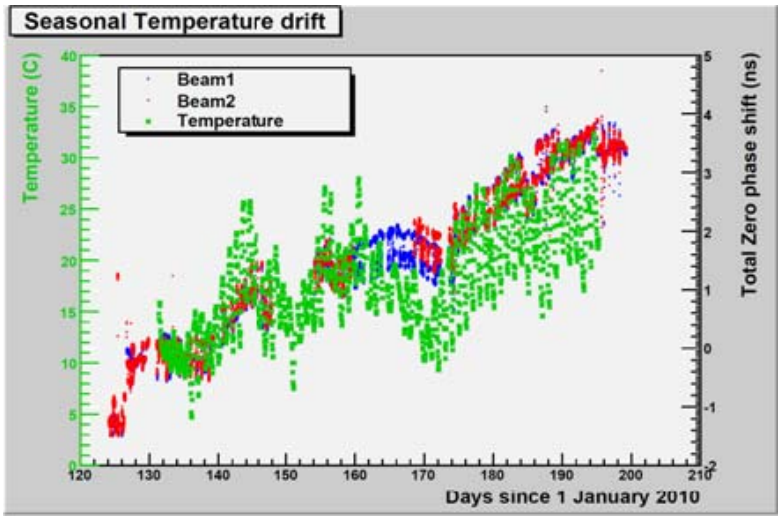

Figure 19: Temperature (green) and phase drifts during a period of 3 months.

5.5 RF Cogging, RF Fine Adjustment and LHC Vistar

During the first period of operation at 7 TeV collision energy, the BPIM system was contributing to the work of adjusting the LHC RF system to provide the experiments with the best possible collision point. The BPIM system is also continuously monitoring the coarse phase (bucket filling scheme) and the fine phase of each bunch in each beam. Together with the luminous region size and position and the wrong bucket flag, the timing information is fed back to the LHC via a common data exchange mechanism and is displayed in the LHC Control Room and on the Web via the *LHC Vistar pages* (Figure 20). These values may be used real-time by the LHC machine operators to tune the collision point in each of the four experiments and is used to have a rapid feedback on possible mis-configuration of the accelerator.

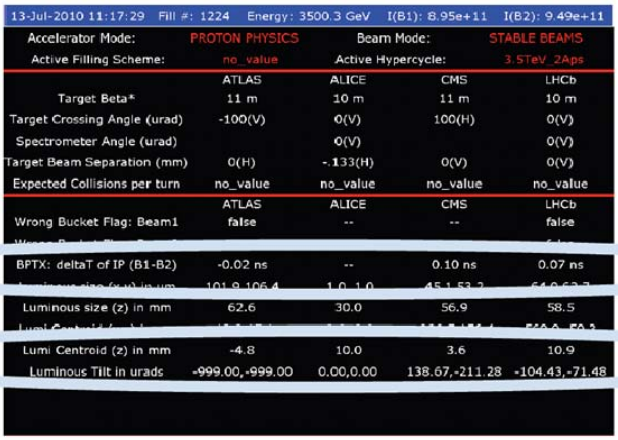

Figure 20: The LHC Configuration Vistar page in the LHC Control Room and on the Web.

6 Conclusion

LHCb has developed, installed and commissioned an advanced system for the global timing of the LHCb experiment. The system includes a timing receiver crate which receives, converts and cleans the global LHCb clock, and two dedicated beam pickups for monitoring the intensity and arrival time with respect to the LHCb global clock of each bunch. A custom-made Beam Phase and Intensity Monitor electronics board with both analogue and digital circuitry has been developed for the readout and digital processing logic. This board is able to measure the intensity of each bunch continuously at 40 MHz. It is also able to measure the phase of each bunch with a single measurement resolution of about 30ps. Of particular importance for the determination of the online and offline luminosity, the system is also providing LHCb with complete monitoring of the LHC filling scheme.

The system has been fully operational since the LHC pilot run in 2009 and has proven to be highly reliable.

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