SLAC-TN-72-14
M. Fishman
September 1972

# INSTRUCTION MANUAL
# FOR THE SLAC TYPE 114-119 SCALER READ-IN TRANSFER BUFFER

## 1. Introduction

Off-line computation can generally be used to subtract the number of detected invalid events from an accumulated count. However, when the additional data required to test the acceptability of a count becomes large, it may be desirable to discard an invalid count before it is accumulated. The low duty cycle of the SLAC machine allows one to use a serial-in, serial-out transfer buffer for controlling the count transfer to an accumulating counter.

The serial-in, serial-out buffer system consists of two modules: namely the EG&G 110/N Pre-Scaler and the SLAC 114-119 Module. The buffer contains the following basic units:

1. A 2-decade high-speed scaler containing:
   a. the EG&G S110/N decade scaler
   b. a decade scaler containing a level shifting amplifier and an I.C. decade counter.
2. A gated pulse generator containing:
   a. a transfer command amplifier
   b. a pulse-standardizing one-shot
   c. a set-reset flip-flop
   d. a gated ring one-shot pair
   e. an output amplifier.
3. A "slow" 2-decade scaler and associated inverting amplifiers.
4. An identity gate.
5. Reset level-shifting amplifiers.
6. A voltage regulator.

A block diagram of the buffer system is shown in Fig. 1.

A reset pulse is applied to the system prior to the beam pulse. During the beam pulse, the fact scaler accumulates a count, and external hardware determines whether or not the count is meaningful. If the count is to be accumulated, a transfer command is applied to the 114-119 module. The transfer command starts the gated pulse generator which transmits pulses both to an external accumulating scaler and to the slow scaler. When identity is achieved between the count in the high-speed scaler and the count in the slow scaler, the identity gate sends a stop-pulse to the gated pulse generator. Consequently, the number of pulses transmitted to the accumulating scaler is the same as that originally stored in the high-speed scaler.

## 2. Circuit Description

### 2.1. The 2-Decade High-Speed Scaler

NIM-standard fast logic event pulses are accepted at the input of the EG&G S110/N decade scaler whose characteristics are described in the following data sheet (see page 4).

The system is reset prior to a beam pulse. A reset pulse from the reset amplifier described in Section 2.5 is applied to terminal 12 of the S110/N Digital I/O Connector. Event pulses are then applied to the S110/N scaler. Overflow carry pulses are transmitted to the input of the second decade located in the SLAC 114-119 module.

The second decade of the high-speed scaler accepts input pulses across resistor R1 as shown in Figs. 2 and 3. Transistors Q-1 and Q-2 are part of a conventional differential input stage which presents a 50 ohm input impedance to the carry signal from the first decade. The non-inverted output of the differential pair is inverted by transistor Q-3 and applied to the input of an integrated circuit decade scaler in IC 31. The output of transistor Q-4 is a positive pulse for TTL logic. Current sinking is provided by resistor R12.

### 2.2. Gated Pulse Generator

A NIM-standard logic level pulse whose duration is equal or greater than 20 nanoseconds is applied at the base of transistor Q-4 across resistor R7. Transistors Q-4 and Q-5 are part of a differential pair and Q-6 functions as an inverting amplifier. The transfer command amplifier is identical to the carry amplifier described in Section 2.1.

The output of the carry amplifier is a positive pulse which is applied to pin 10 of IC 41, an integrated circuit one-shot. The DCL 8162 used for IC 41 is an ac coupled device which triggers on the trailing edge of the carry pulse.

The output of IC 41 is connected to the set input of a flip-flop consisting of two interconnected NOR gates in IC 42. The reset input is obtained from the identity gate described in Section 2.4. The Q output from pin 10 of IC 42 is applied to pin 2 of a NOR-gate in IC 42 when the flip-flop is set. The positive-going pulse at pin 1 of IC 42 is inverted and applied to the input of one-shot IC 52. The trailing edge of the signal from pin 4 of IC 2 triggers one-shot IC 51. One-shot IC 51 feeds back a pulse to pin 3 of IC 42 which permits pulses to be transmitted around the ring until the flip-flop is reset. The output pulses from pin 4 of IC 52 are applied to the input of the slow scaler at pin 8 of IC 13. In addition the output pulses from IC 52 are amplified and reshaped by the output amplifier.

The output amplifier of the gated generator is built around transistors Q-7, Q-8, and Q-9. Signal is applied to the base of Q-9 through R17 which acts as a protective resistor. The emitter of transistor Q-9 is held at approximately + 1.3 volts. Thus Q-9 acts as a discriminator of TTL logic level pulses from IC 52. The output of Q-9 is applied to one side of a differential amplifier containing Q-7 and Q-8. The base of transistor Q-8 is held at - 3.9 volts. Catching diodes CR1 and CR2 are connected between the bases of Q-7 and Q-8 to limit the voltage swing.

2.3. Slow Scaler and Associated Inverters

Pulses from IC 52 are applied to the input of the slow scaler at pin 8 of IC 13. The carry output from pin 12 of IC 13 is applied to the input of IC 43. Integrated circuits IC 13 and IC 43 are binary coded decimal counters type DCL 8280. The outputs of IC 13 are applied to 4 inverters in IC 23. Similarly the outputs of IC 43 are applied to 4 inverters in IC 33. The outputs of the inverters in turn are applied to the identity gate.

2.4. Identity Gate

Let the 1, 2, 4, and 8 outputs of the high-speed scaler be designated by A, B, C, and D respectively. Similarly let the inverted outputs of the slow scaler be designated by $\bar{a}$, $\bar{b}$, $\bar{c}$, and $\bar{d}$ respectively. Applying corresponding pairs of inputs to a NAND gate, one observes that identity holds only when $(A\bar{a} + B\bar{b} + C\bar{c} + D\bar{d})$ = FALSE.

The identity gate consists of IC 22 and IC 32 connected in a wired "OR" configuration. Resistor R19 functions as a pullup resistor. When all gate inputs are false, a plus pulse appears at the reset input of the control flip-flop in the gated oscillator at pin 12 of IC 42.

2.5. Reset Amplifiers

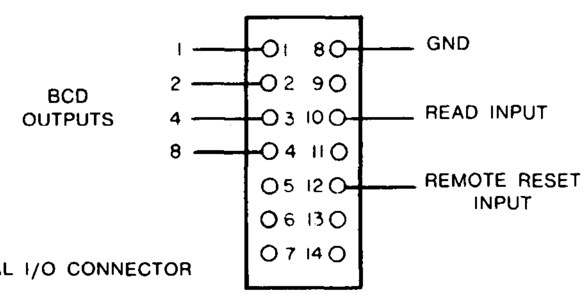
Reset pulses are applied to clear both the high-speed and slow scalers prior to a beam pulse. The reset pulse input may be distributed either through the NIM-bin or through external BNC inputs. Input pulses are OR-ed through CR11 and CR12. Nominal 3-volt reset pulses are inverted by Q-11 and applied to integrated circuit scalers IC 31, IC 13, and IC 43. The output of transistor Q-11 is re-inverted and reshaped by Q-12. The plus-going pulse is transmitted to the S110/N remote reset input.

## 2.6. Voltage Regulator

Since the SLAC 114-119 has modest current requirements for driving the IC's, a regulator is used to obtain a voltage of 5.6 V from the standard + 12-volt NIM supply. Transistor Q-10 acts as a simple emitter follower whose base-emitter voltage drop is compensated for by the diode drop across CR9. Consequently the output voltage at the emitter of Q-10 is approximately equal to 5.6 volts, the drop across Zener diode CR10. The integrated circuits are supplied through one of three dropping diodes to nominal voltages of Vcc = 5 volts.

## SPECIFICATIONS

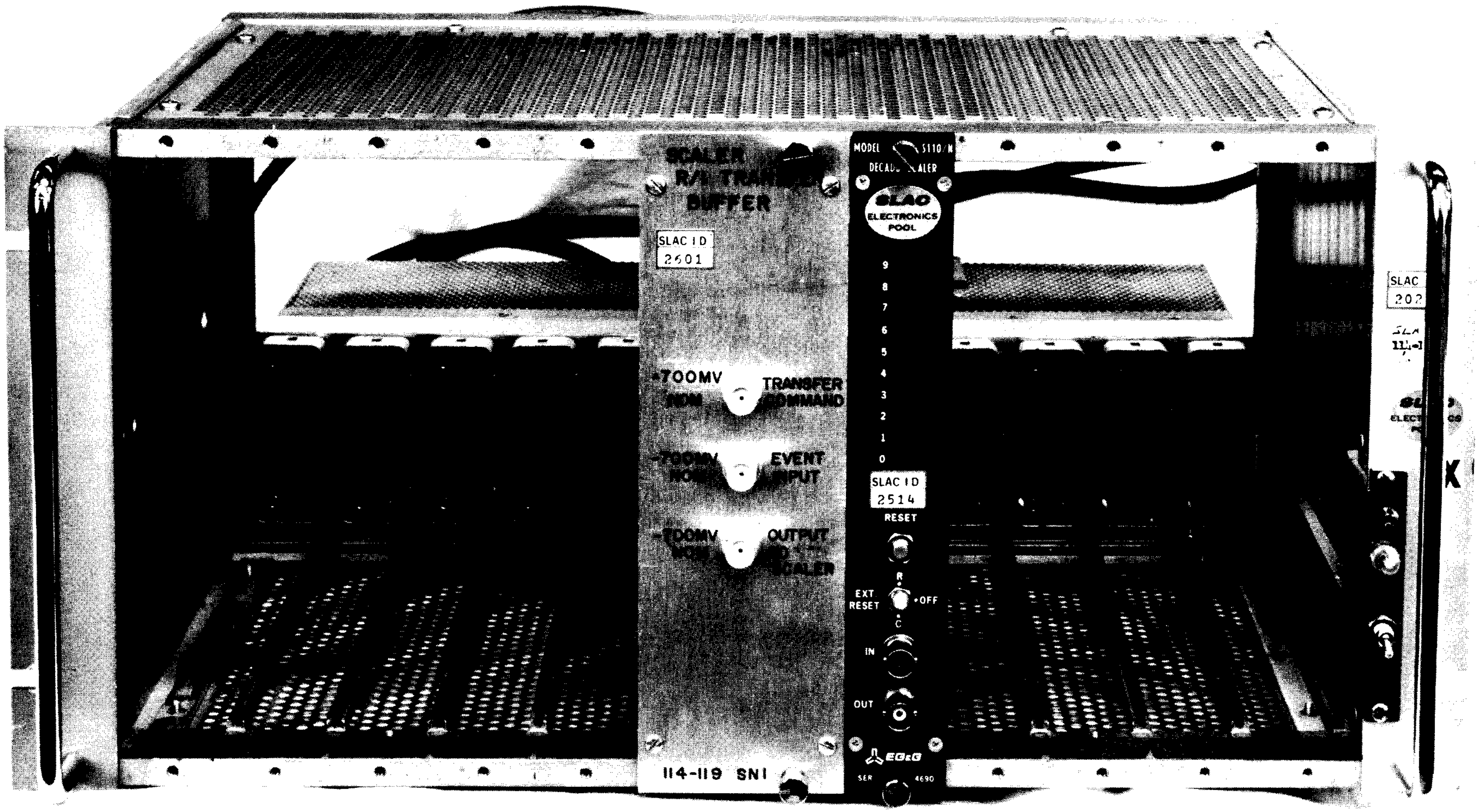
| | |
|---|---|
| INPUT: | 50-ohm termination with reflections less than 10% peak from −10 V, 1 nsec step input. Breakdown limits: ±5 V dc; ±10 V, 100 nsec pulses of duty factor less than 10%; ±100 V transients. Input offset less than ±50 mV. |
| THRESHOLD: | Typically −400 mV. Temperature coefficient typically 2 mV/°C. |
| SPEED: | Greater than 200 MHz CW; pulse pair resolution less than 4 nsec; both measured with NIM-standard fast logic signals. |
| CARRY OUTPUT: | NIM-standard fast logic signals, for 50 ohm termination. Width typically 20 nsec FWHM. Width may be increased by changing internal capacitor; carry output has maximum 50% duty factor. |
| RESET INPUT: | ZERO level 0 ±1.5 V; ONE level +3 V to +20 V or −4 V to −20 V. Minimum reset input ±3 V, 100 nsec width FWHM. Input impedance, 2K. Internal reset timer duration 2 usec maximum. |
| READ INPUT: | For NIM-standard slow logic signals. ZERO level 0 ±1.5 V; ONE level +3 to +20 V. Minimum input +3 V, 0.25 usec FWHM. |
| DIGITAL OUTPUTS: | NIM-standard slow logic signal outputs for data transmission. ZERO level 0 to +300 mV. ONE level +24 V from source impedance of 3.6K (6.6 mA short circuit; +24 V open circuit). NIM-standard slow logic signal levels are generated into load impedances from 0.5K to 3.6K. The four output lines are supplied with 1248 coding, which may be changed to 122'4 coding. |
| DIGITAL I/O CONNECTOR: | Amphenol 57-40140, which requires an Amphenol 57-30140 cable plug. |
| POWER REQUIREMENTS: | +24 V, 155 mA.<br>+12 V, 64 mA.<br>−12 V, 70 mA.<br>−24 V, 162 mA. |
| PANEL COLOR: | Blue. |



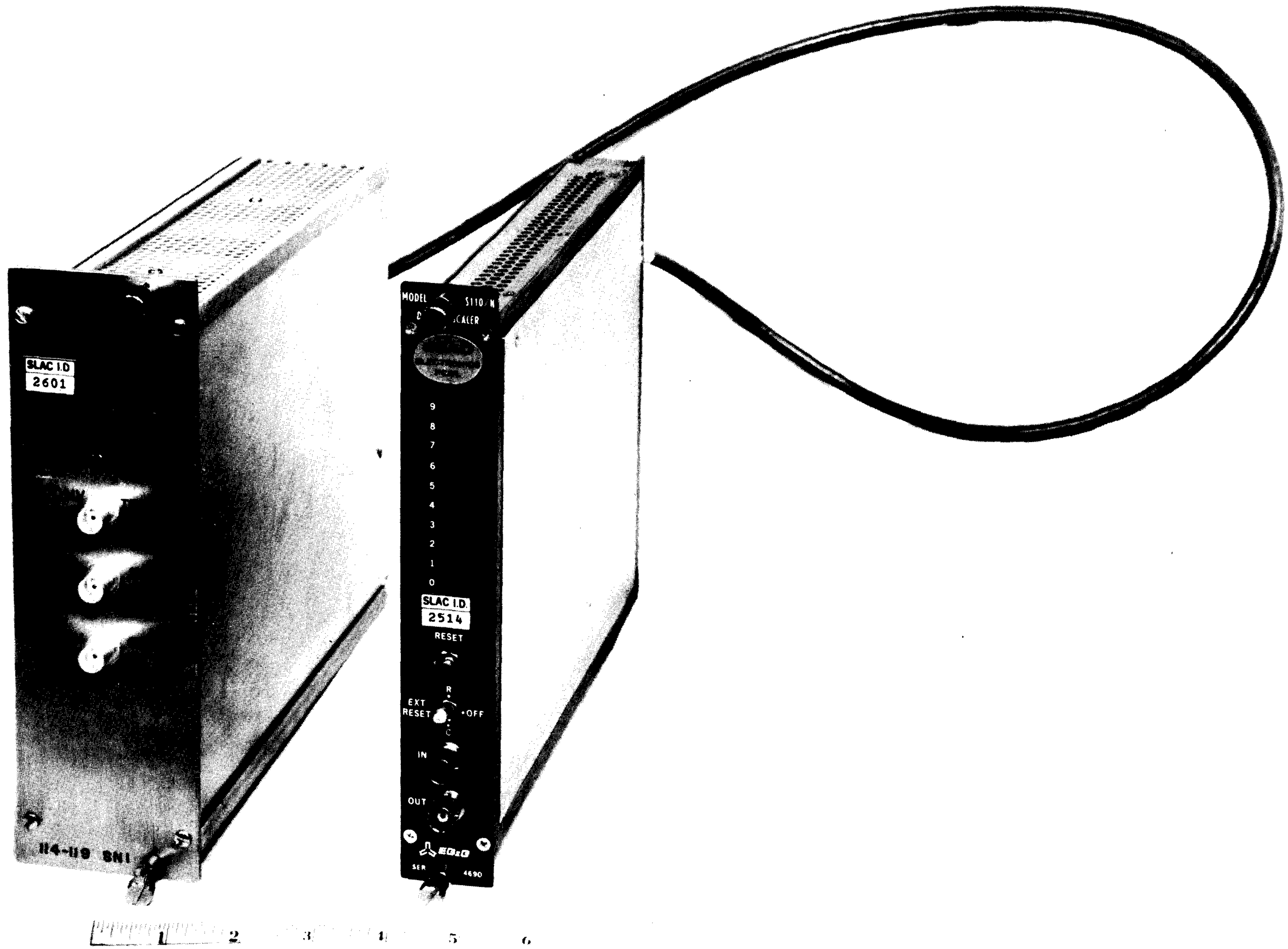

S110/N DIGITAL I/O CONNECTOR

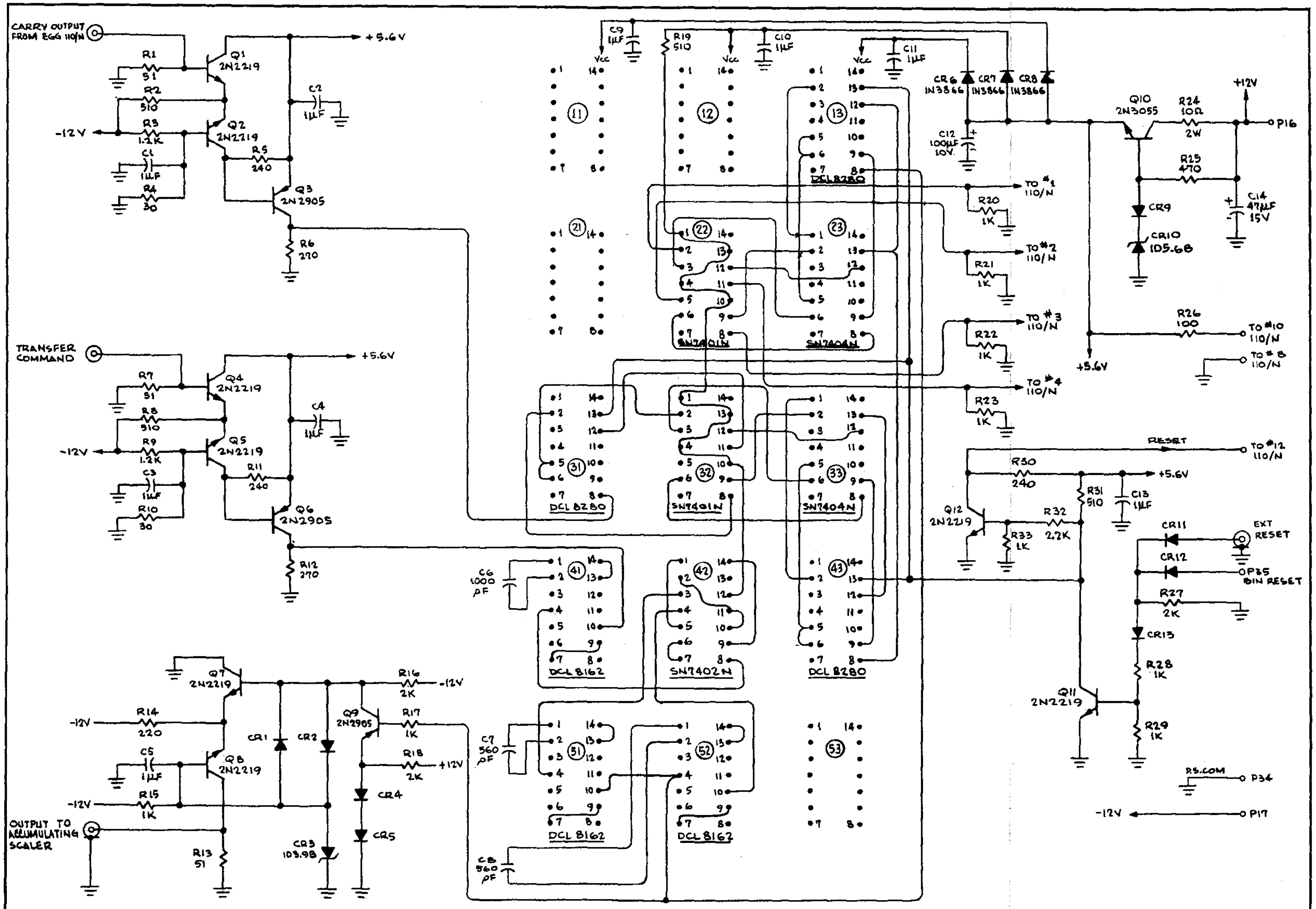
**EG&G INC.** NUCLEAR INSTRUMENTATION DIVISION, 35 CONGRESS STREET, SALEM, MASS. 01970
TEL: 617-745-3200 TWX: 710-347-6741 CABLES: EGGINC-SALEM
PRINTED IN USA 5-68 FORM N1085

VIEW OF SLAC 114-119 BUFFER SYSTEM INSTALLATION IN STANDARD NIM-BIN.



SIDE-BY-SIDE VIEW OF SLAC 114-119 MODULE, EG&G S110/N SCALER, AND INTERCONNECTING CABLE.






NOTE:
1. FAIRCHILD µGA901659X MAY BE SUBSTITUTED FOR SN 7404N

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WIRING DIAGRAM
SCALER READ-IN
TRANSFER BUFFER

WD 114-119-00-R0 C

FIGURE 3

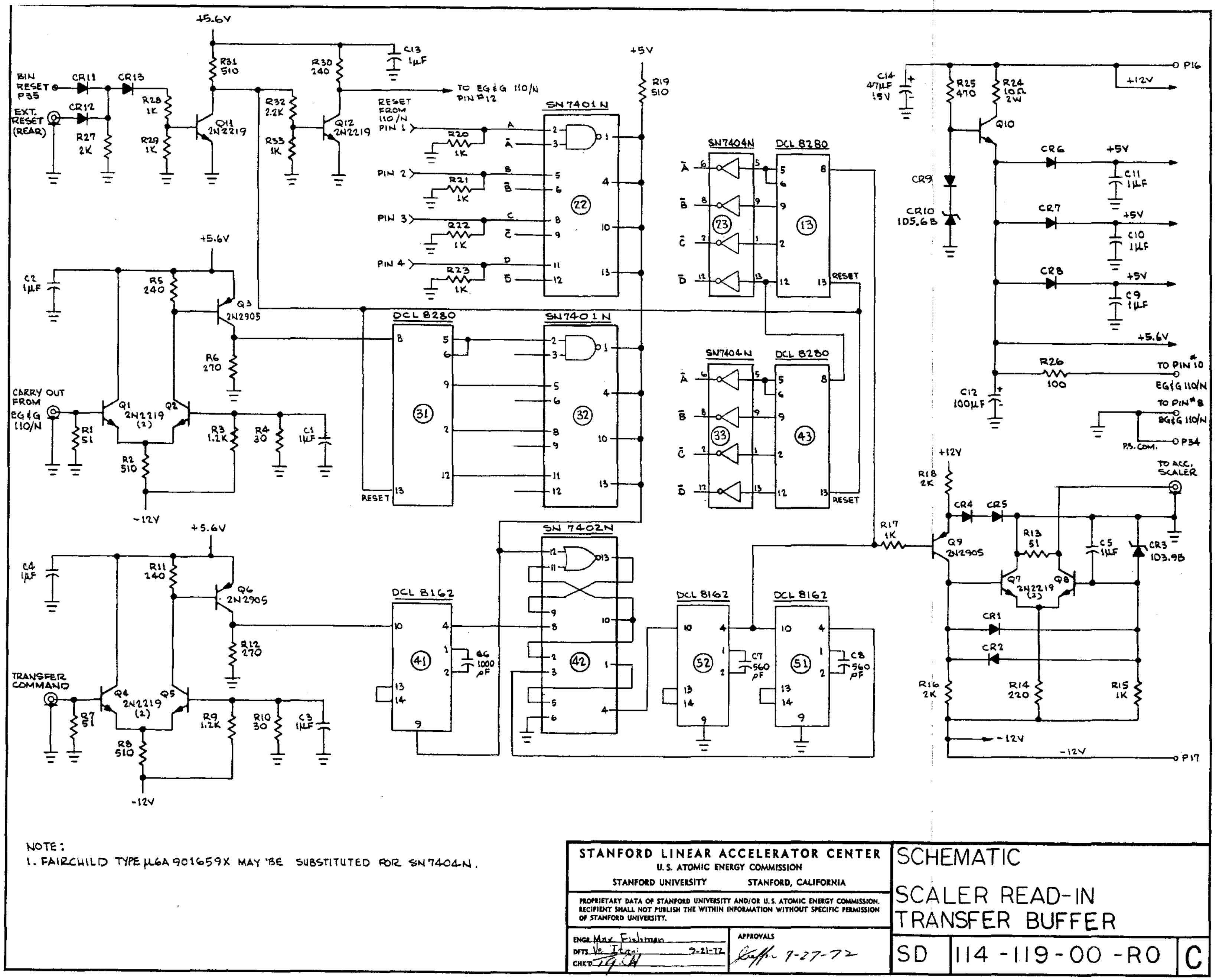
NOTE:
1. FAIRCHILD TYPE μL6A 901659X MAY BE SUBSTITUTED FOR SN7404N.
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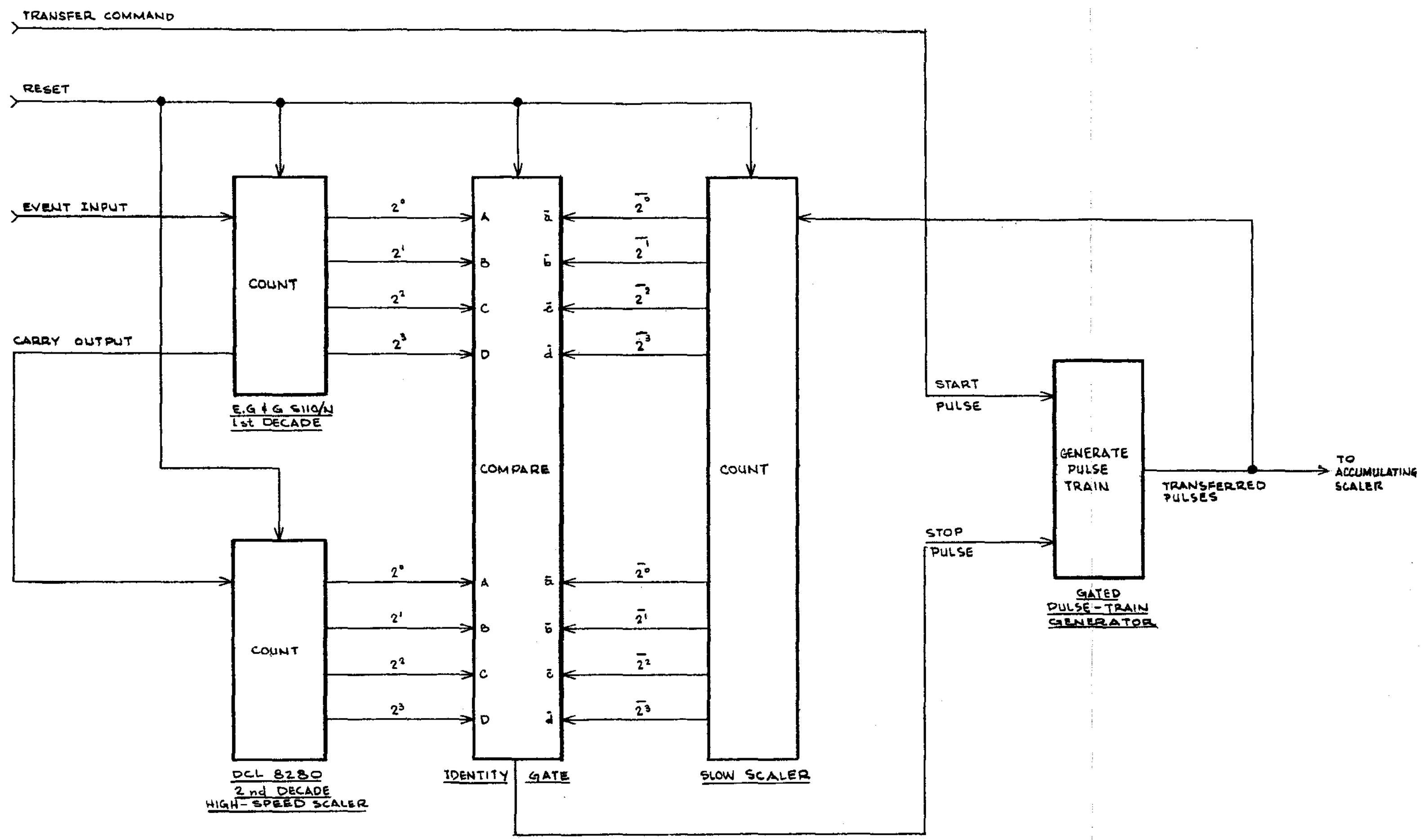
FIGURE 2

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BLOCK DIAGRAM
SCALER READ-IN TRANSFER BUFFER

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