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A Clock and Data Recovery Circuit for the ATLAS/CMS HL-LHC Pixel Front End Chip in 65 nm CMOS Technology

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A Clock-Data Recovery circuit has been developed to be integrated in the RD53B front end chip for the HL-LHC upgrade of the ATLAS/CMS pixel detector. The 160 Mb/s input data stream is recovered and used to synthesize all the necessary clock signals including the 1.28 GHz clock that drives the high speed output link. Robust locking is guaranteed by starting up in Phase-Locked Loop mode and afterwards automatically switching to Clock-Data Recovery operation, while the circuit has been optimized for low jitter. Full characterization was performed with the aid of a dedicated test chip. Less than 60 ps p-p jitter was measured while the circuit remains fully functional and locking is reliably achieved after a total ionizing dose of 600 Mrad.

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1. Introduction

In order to address the stringent requirements of the high luminosity LHC (HL-LHC) ATLAS and CMS pixel trackers, the RD53 collaboration [1] was formed to develop a new readout front end integrated circuit (IC). The RD53 chip data link, shown in Fig. 1, must support multi-Gb/s capacity to cope with the expected hit rates up to 3 GHz/cm^2. One of it's most critical components is the Clock-Data Recovery (CDR) circuit. It provides all the necessary clock signals by phase-locking a voltage controlled oscillator (VCO) to the transitions of the 160 Mb/s input command data stream. Therefore, reliable locking is essential for the full chip operation and correct start-up must be guaranteed. The high speed 1.28 GHz VCO clock is used by the serializer that feeds the output data to four 1.28 Gb/s lanes driven by a current mode logic (CML) stage with pre-emphasis [2]. To ensure high quality data transmission that is compatible with the low-power GBT (lpGBT) [3] communications IC, the CDR is required to achieve low jitter performance. The input jitter is comprised of the lpBGT output jitter, which is expected to be less than 5 ps rms, plus the inter-symbol interference caused by the low mass cable. The output downlink jitter budget, which also includes the cable effects, is equal to 200 ps p-p. Due to the high radiation levels of the HL-LHC, the CDR circuit should be able to withstand up to 500 Mrad of total ionizing dose (TID) and be tolerant to single event effects (SEE).

A CDR block has been designed in 65 nm CMOS technology to adhere to these specifications. It was integrated in the RD53A demonstrator chip [4] that has been successfully fabricated and characterized. Due to the clock-gating phase detector that was used, locking after start-up was discovered to not always be successful. Furthermore, it would be preferable to further optimize the jitter performance. To address these shortcomings, a new version of the CDR circuit has been designed for the RD53B [5] chip that is currently under development. To assess the suitability of the RD53B CDR, a dedicated test chip has been developed and characterized.

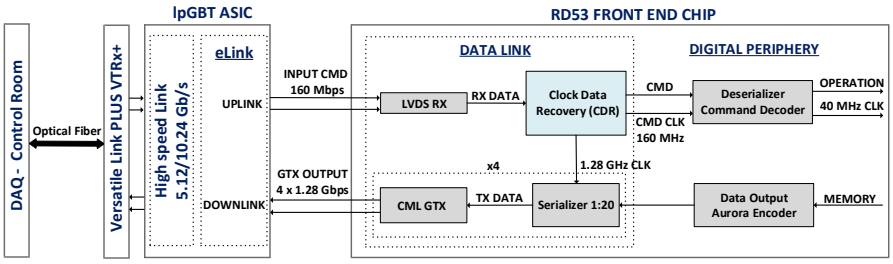

Figure 1: Data link configuration of the HL-LHC Phase-II upgrade ATLAS/CMS pixel detectors

2. Circuit Description

The RD53B CDR block diagram is depicted in Fig. 2. To achieve reliable phase-locking, the circuit starts up in phase-locked loop (PLL) mode using a standard phase frequency detector (PFD), while the 160 Mb/s training pattern of 010101... is provided at the input. Sufficient time is allowed until the VCO frequency is stable and equal to the nominal value of 1.28 Gb/s. The PLL mode duration is predefined by a counter and is equal to approximately 500 μs. Afterwards, the

CDR mode is automatically activated and commands can be sent through the input data stream. The CDR loop is based on a bang-bang Alexander phase detector (PD) [6] aided by a rotational frequency detector [7] with pull-in range equal to 25% of the data rate.

A behavioral model was developed in Verilog in order to accelerate the closed loop simulation. Each block was individually simulated and optimized using SPICE and the extracted properties were imported into the model in order to tune the loop parameters for minimum jitter. To enhance tolerance to radiation effects, transistor geometries larger than the minimum size have been used and increased biasing currents are applied to sensitive blocks such as the VCO. Validation by simulation has been carried out using radiation models developed by the RD53 collaboration. Triple modular redundancy (TMR) was used in the design of the divider and counter in order to reduce susceptibility to SEE effects.

The charge-pump (CP) consists of a standard drain-switching configuration with current steering and a unity gain buffer to limit spurious signals caused by charge sharing during the switching phase. The CP current is configurable and it's nominal value is set to 1 μA. The filter is comprised of a 300 pF metal-oxide-metal (MOM) capacitor and a configurable resistor from 50 Ω to 1 kΩ. The VCO is based on a 3-stage differential ring oscillator architecture followed by a differential to single-ended converter. Cross-coupled loads are used in the delay cell design to improve performance. Four VCO gain values are available to be selected from, while the nominal gain is equal to 1.5 GHz/V. By optimizing the transistor dimensions and increasing the biasing current, the VCO cycle jitter (J_c) has been reduced by a factor of two compared to the RD53A CDR and is equal to 400 fs. The divider is based on a synchronous configuration to reduce it's jitter contribution.

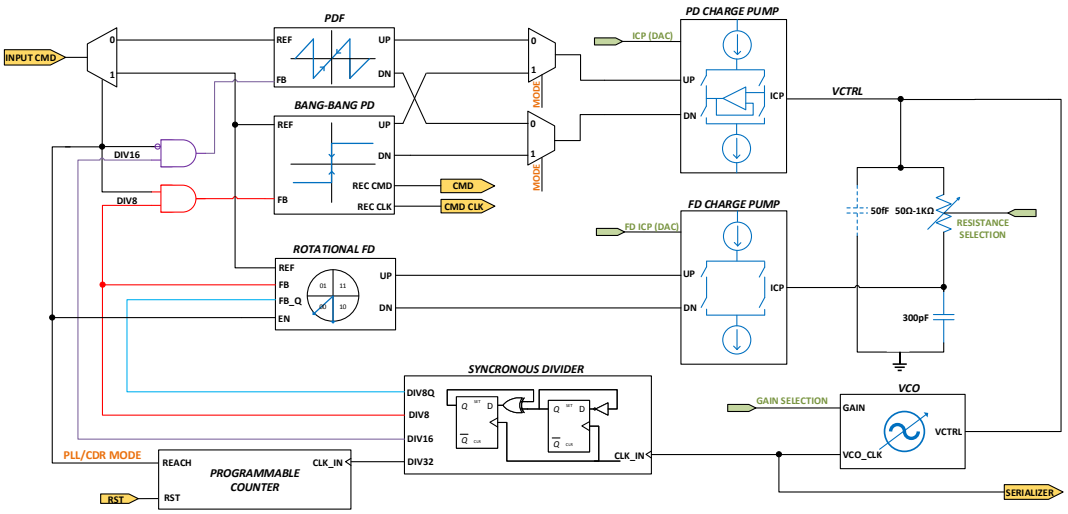

Figure 2: Architecture of the RD53B CDR circuit

3. CDR Test Chip

A test chip was developed as platform to characterize the CDR performance. The necessary supporting blocks were imported from the RD53 chip library with the goal of having a similar environment after integration in RD53B. Low voltage differential signaling (LVDS) is used for the

command input and the recovered command and clock output signals. Gigabit CML drivers [2] are used for the serialized output and the VCO clock. The serializer input data can be provided by an included pseudo random binary sequence (PRBS) generator. The biasing currents as well as the CP current are configured by 10-bit digital to analog converters (DAC). An SPI interface with TMR registers is used to control the chip settings. The RD53A CDR is also included for comparison.

4. Measurement Results

The test setup is based on the BDAQ53 data acquisition system [8]. The input command can be provided by BDAQ53 directly or by an external signal generator. The VCO tuning curve is shown in Fig. 3a. The measurement result matches the simulation and the small deviation is attributed to temperature. The CDR power consumption at the nominal voltage of 1.2 V was measured equal to 7 mW, which also agrees with the expected value.

4.1 Locking Reliability and Jitter Performance

To assess the locking reliability at start-up, the CDR was power-cycled 100 times for different power supply voltages. The training pattern was provided for 1 s, and afterwards a command stream was sent. The VCO frequency was monitored and the recovered command was validated. The filter capacitor was then discharged for the next cycle. Locking was found to be 100% successful down to 0.9 V power supply voltage.

The jitter performance of the CDR was evaluated using a setup wired with 1 m long SMA cables. A PRBS5 input command stream with 5 ps rms jitter was provided and the chip was configured to output serialized PRBS15 data at 1.28 Gb/s rate. The measured eye diagram is depicted in Fig. 3b. The output jitter is equal to 6.7 ps rms and 57 ps p-p for a representative large sample of 250k edges. To validate the CDR model, the jitter spectrum analysis of the VCO clock is shown in Fig. 3c. Good accuracy can be observed, while the difference in the region below 1 MHz is attributed to distortion introduced by the LVDS receiver and the rest of the input path. The CDR bandwidth is tuned to approximately 5 MHz to minimize the total jitter.

4.2 X-ray Irradiation and Total Ionizing Dose Effects

The CDR test chip was irradiated with X-rays at the University of Bonn up to a total TID of 600 Mrad. The X-ray tube that contains a tungsten cathode was biased at 40 kV and a thin aluminium filter was used to harden the spectrum. The chip temperature was kept constant at -14°C. Start-up locking was 100% successful down to 1 V power supply voltage and the total jitter (TJ) p-p was increased by 13%. The difference is mainly due to duty cycle distortion (DCD) introduced in the test chip output path. Apart from this minor performance degradation the circuit remains fully functional after 600 Mrad TID.

5. Conclusions

A CDR circuit was designed for the RD53B ATLAS/CMS phase-II upgrade readout chip. Substantial improvements in reliability and performance were achieved compared to the RD53A version of the CDR. Locking is robust and the link quality is enhanced by reducing the jitter by three times. The circuit is fully functional after 600 Mrad TID without significant loss in performance.

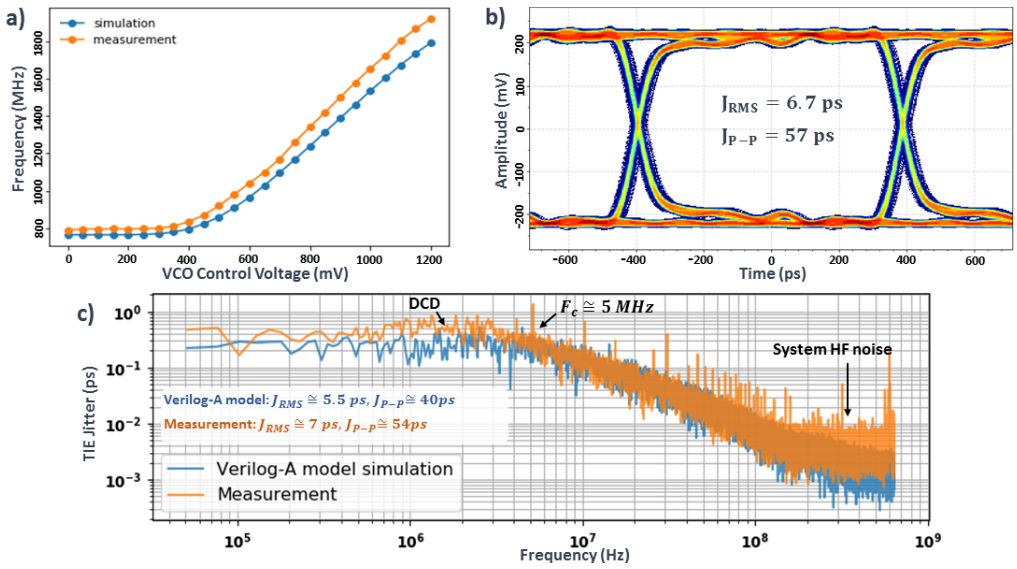

Figure 3: a) VCO tuning curve b) Eye diagram and time interval error (TIE) jitter of PRBS15 data output using PRBS5 command input with 5 ps rms jitter c) VCO clock jitter power spectrum

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