

A DATA-ACQUISITION SYSTEM FOR A
LARGE WIRE CHAMBER SPECTROMETER*

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1. INTRODUCTION

A large wire chamber spectrometer has been constructed at SLAC for the study of neutral K-meson decays. We will describe herein the construction and performance of the wire chambers and high voltage pulsing system, the capacitor-diode readout system, and the data acquisition system for gathering the wire chamber data and digitized information pertaining to the time and pulse height of a large array of scintillation counters which are used in the trigger logic.

Our choice of wire chamber design and readout system was dictated largely by two factors: the need for a large acceptance and the requirement of high multitrack efficiency. The first experiments to be done using the spectrometer involve high statistics studies of the charge asymmetry and Dalitz plot in the decay $K_L \rightarrow \pi^\pm \mu^\mp \nu$ and of the Dalitz plot in the decay $K_L \rightarrow \pi^+ \pi^- \pi^0$. Both experiments require a large and relatively uniform detection efficiency. A large magnet was therefore necessary, as were very large wire chambers placed in the fringing field of the magnet. Rather than attempt to operate magnetostrictive or ferrite core readout systems in the field, a novel readout system was conceived which is inherently insensitive to magnetic fields and which has unlimited multitrack capability. The scheme, which will be described in more detail below, consists of connecting each readout wire to a 5 nF capacitor and then interrogating the capacitor through a diode network to see if it has been charged by the spark. This idea evolved from an earlier scheme in which a FET was used as the interrogation gate. The diode network was found to be more reliable, and in addition, a very convenient packaging method was devised, which greatly simplified fabrication and servicing of the readout system.

Our second requirement, high multitrack efficiency, is necessitated by SLAC's poor duty cycle (.06%). Since the delay between the detection of an event and application of high voltage to the chambers is a significant fraction of

the beam pulse width ($1.6\mu\text{sec}$) it is difficult to effectively employ large clearing fields. Therefore an average trigger may contain several extraneous tracks in addition to the tracks from the desired event. Missing sparks make the separation of event tracks from background tracks difficult, and therefore great emphasis was placed on achieving high multitrack efficiency in the wire chamber and readout systems. This was accomplished in the following manner:

1. Each chamber consists of two planes of parallel wires, one for the application of high voltage, the other for readout.
2. Pairs of wires on the high voltage plane are fed from the high voltage bus through a $470\ \Omega$ resistor, thus limiting the current in an individual spark.
3. The high voltage pulse is applied to the chambers by discharging delay lines through a hydrogen thyatron.

This technique has resulted in a system whose efficiency is $> 98\%$ independent of the number of sparks up to at least 8 sparks/chamber/event.

2. CONSTRUCTION AND PERFORMANCE

2.1 Mechanical Construction

The spectrometer consists of two arrays of wire chambers, each with ten planes, and a large magnet (2.5m x 1m x 1m gap). Each group of chambers consists of four x-coordinate planes, four y-coordinate planes and two slanted planes, termed u and v, for ambiguity resolution in multitrack events. The dimensions of the chambers are listed in Table 1. Figure 1 is a plan view of the spectrometer.

Each of the 20 chambers consists of two planes of parallel stretched wires with separated functions, either high voltage or readout. The gap between planes is 1 cm, and the wire spacing in a plane is 1 mm. Parallel wire chambers

eliminate the pulse propagation problems inherent in crossed wire chambers, resulting in a high and uniform efficiency, even for our large $1.8 \times 2.4 \text{ m}^2$ chambers.

Three methods of mounting the wires were considered: woven screening, mylar backed wire, and stretched wire. Woven screening was rejected because of the close control needed to obtain the necessary wire positioning accuracy and the difficulty of obtaining wire screening with easily solderable wires. Glueing the wires to a mylar backing was considered unsatisfactory because of problems arising from the sensitivity of the gap width to fluctuations in gas pressure, and spurious sparking problems encountered during early tests. We chose the stretched wire technique and have developed a system which provides the rigid frame structure necessary to maintain wire tension, yet enables the gaps to be assembled close together. A large winding machine (capable of handling 4 frames of up to $3 \times 3 \text{ m}^2$ in size) was used.

We have also simplified the manufacture of the relatively large number of chambers by using a modular form of construction (see Fig. 2). Consider, the example, the square $1.2 \times 1.2 \text{ m}^2$ chambers (see Fig. 3). There are two groups of these, each group giving x, y, x, y readout, or 8 gaps in all. Each group of 4 gaps is made of 5 modules clamped together with 1 cm thick lucite window frames and "O"-rings as gas seals between them. Each module consists of $2.5 \times 10 \text{ cm}^2$ A1 bars welded together, with fiberglass epoxy boards (G-10) glued to both sides. After glueing, the outside surfaces of the G-10 were ground flat. The 0.1 mm (dia.) Be-Cu wires were wound on the winding machine at about 230 g tension; the modules were then mounted on the machine where the wires were glued (after alignment) to the G-10 surfaces. In order to maintain wire tension after glueing, the modules were pre-stressed by applying a single

load (about 70% of the total force exerted by the wires) at the midpoint of the module. After the wires were glued, this load was removed.

In the case of the $1.2 \times 1.2 \text{ m}^2$ chambers, ten identical modules were constructed. After the wires were glued in place, they were optically measured. The measurements are referred to tooling balls which are mounted on the extreme corners of the module mounting lugs where they may be sighted after assembly. The modules were then selected, those having the best wire positioning accuracy being used for readout, the others for high voltage. The wire planes on each side of a module are perpendicular to each other, one plane being half of an x readout gap, the other plane half of the adjacent y readout gap. However, they both serve the same function, i. e. , HV and readout planes are not "mixed" on the same module.

The HV wires are soldered in pairs to a printed circuit strip board; each pair of wires is connected through a 470Ω resistor to a HV bus. Breakdown along the edges perpendicular to the wires is prevented by a mylar strip extending about 2 cm into the chamber. To minimize optically induced spurious sparking, sheets of black paper have been installed in the center of each module.

The readout wires are soldered individually to the traces of "fanout" PC boards. Soldering was chosen because of its reliability. These fanout boards are mounted on the backs of the two rows of connectors into which the readout boards are inserted. The use of connectors enables easy and quick interchange of readout electronic cards. A sheet metal enclosure provides electromagnetic shielding for the readout boards and their associated cabling.

The gas employed is 90% neon, 10% helium, bubbled through 1-propanol at 55°C at 30 c. c. per hour. A standard LRL-Berkeley design gas cart controls the gas flow. The propanol is necessary to avoid spurious sparking and edge breakdown.

2.2 High Voltage Pulsing System

The high voltage pulse is applied by discharging a group of 50Ω charging cables through a hydrogen thyatron. Cable length was chosen to give a 200 nsec long pulse at the chambers. The number of cables per chamber was such that there was one charging cable for approximately $.4 \text{ m}^2$ of chamber area. One 50Ω termination per cable was provided at the chamber high voltage bus bar. Each termination was in series with a $.01 \mu\text{f}$ capacitor, to allow the use of a D.C. clearing field. Fine adjustments of the amplitude of the high voltage pulse on each chamber was accomplished by using additional terminating resistors at the HV bus. One thyatron (either EGG HY12 or ITT F103) could accommodate up to 10 charging cables. Thus all ten rear chambers were driven by individual thyatron unit. Triggering of the thyatron is by means of an avalanche transistor amplifier, which transforms a standard fast NIM pulse into a 400V positive pulse at the control grid of the thyatron. Output delay with respect to the trigger pulse is about 100 nsec. The rise time of the HV pulse was 12-15 nsec into a resistive load, and about 40-50 nsec into the capacitive chamber load.

The charging cables, fed from a 200 mA high voltage supply, were isolated via 100 k resistors, resulting in a charging time constant of about 10 msec. The event rate was thus limited to about 30 per second, consistent with the time required for interrogation of the wire chambers, data acquisition and software dead-time.

2.3 Tests of Chamber and Readout System Performance

A number of on-line tests have been devised to monitor the performance of the wire chambers and the readout system. These tests greatly facilitate the maintenance of the system in good order and were vital to the initial efforts in installing and debugging the hardware.

Histograms generated on-line are a primary source of information on system performance. Among these histograms are the following:

1. Number of sparks per event per chamber
2. Distribution of spark widths in each chamber
3. In any one chamber, the number of sparks per readout board. This, for example allows rapid tracking down of edge breakdown, should it occur.
4. In any one chamber, the number of sparks per "sense line", i. e. in channel one, the sum of all hits on wire 1 on each board in the chamber, etc. This allows one to immediately find comparator failures.

Another very useful type of information is provided by the "Wire Scan". This test, for reasons of memory limitations, divides the 30,000 wires into eight groups. After a given number of events, every wire in a group should have been struck at least once. At the conclusion of a scan, which takes on the order of thirty minutes, the locations of any wires which have not read out are typed, and the program moves on to the next group. Should the wire not read out again on the next scan of that group, it is flagged as bad, which indicates a broken wire, missing wire or bad capacitor-diode readout element.

An on-line generated computer display of selected events (Fig. 4) is also valuable in monitoring system performance. This display allows the experimenter to quickly verify that all spark chambers are performing normally and that the expected correlations between the scintillation trigger counters and tracks in the chambers exist.

2.4 Wire Chamber and Readout System Performance

Data on the wire chamber efficiency are presented in Figs. 5 and 6. Figure 5 shows the spark chamber efficiency as a function of power supply high voltage.

Data are plotted for the smallest ($1.2 \times 1.2 \text{ m}^2$) and largest ($1.8 \times 2.4 \text{ m}^2$) chambers. The terminating resistors on each chamber are trimmed to effect maximum overlap of the plateau regions of all twenty chambers. "Event tracks" are those associated with scintillation counters which have been latched in the event, and are therefore about 500 nsec old.

The multitrack efficiency for a typical chamber is shown in Fig. 6. As our trigger requirement specifies two particles in the front chambers and at least one in the rear, the additional tracks are associated with other particles which did not satisfy the trigger, but which passed through the chambers during the same beam burst. Some of these may then be as much as $2 \mu\text{sec}$ old when the chamber is fired. This is the predominant reason for the slight falloff in efficiency as the number of tracks increases. Another contributing factor is that the number of possible tracks found by the track fitting program increases as n^3 , and without the counter latch constraint, some of these may not be tracks at all. Nonetheless, the multitrack efficiency is seen to be excellent.

The number of capacitor-diode units which are set by a spark is a function of the chamber high voltage, as can be seen in Fig. 7. At low voltages, there may be as many as 12-15% single wire hits, and presumably some sparks do not set any wires, although this has not been disentangled from chamber inefficiency. The system is run such that the number of wires set per event is between 2 and 3. Further increase in voltage results in a rapid increase in the number of very wide sparks.

The spatial resolution of the chambers was 0.3 mm. This is the rms deviation of a spark in a given chamber from the least square fit of a four-spark track. Variation from chamber to chamber is approximately 10%.

3. ORGANIZATION OF DATA ACQUISITION

The major components of the data processing system are: (i) Capacitor-diode circuits to store the spark charge; these include read, sense, clear, test and address decoding circuits, (ii) A reformatting digital circuit that presents an 18-bit word containing information on spark location and width to a PDP-9 computer, (iii) Logic circuits that accept computer instructions and translate them into hardware operations required for the control of the spark chamber data acquisition process, (iv) A 512 position multiplexer for data acquisition from scalers, ADC's, time-of-flight measurements, and run identification parameters that are required for the complete reconstruction of an event, and (v) A 256 position multiplexer for PM voltage setting and reading, and for dynamic control of a variety of experimental equipment via the PDP-9 program.

3.1 Capacitor-diode Readout Circuit

Figure 8 shows a capacitor-diode (C-D) readout circuit. Two identical circuits are mounted on a ceramic substrate 6.0 cm x 1.2 cm^{*}. The hybrid circuit uses deposition resistors, capacitor chips and hermetically sealed diodes (Fairchild 1N3064 in a D035 package) for low leakage currents. Thirty-two such circuits are mounted on a PC board to serve 64 wires (see Figs. 9 and 10). Each PC board is organized to control two words of 32 bits (wires) each; the first group will be referred to as an 'EVEN' word, the other as 'ODD'. Thus each hybrid circuit contains the readout for one bit (wire) each of an 'EVEN' and 'ODD' 32-bit word.

Operation of the circuit will be described referring to Figs. 8 and 9. A six-bit address code and IC's A1, A2 (Fig. 9) select the board to be interrogated.

* Manufactured by CENTRALAB, 900 E. Keefe Ave., Milwaukee, Wisconsin 53201.

After the address transients have passed, the 7th bit, a READ signal, is applied to interrogate 32 capacitors. The amplified READ signal is +24 volts in amplitude and $1\mu\text{s}$ in duration. When C has been charged due to a spark, a signal of $\leq 1\mu\text{s}$ duration will appear at the SENSE terminal of the respective C-D element. Otherwise, the READ current will raise the capacitor potential from its quiescent value of -1.4 volts to -0.4 volts due to the time constant $R1 \cdot C$. Bit $\bar{7}$ will be referred to as READ EVEN, while bit 7 is the READ ODD signal. C is cleared via D1, the same terminal acting also as a positive clamp for occasional high spark pulses. A negative clamp diode, D4, prevents asymmetrical rectification at C, in case of ringing following a spark. TEST signals are applied via the READ terminals; they differ from the READ signals in their duration, ($\approx 15\mu\text{s}$), which is sufficient to charge C (Test procedures are described in sec. 3.2.1). The number of PC boards per chamber ranges from 18 for a $1.2 \times 1.2 \text{ m}^2$ chamber to 36 for a $1.8 \times 2.4 \text{ m}^2$ chamber. The total system utilizes 476 readout cards corresponding to 30,464 wires. Bits of like binary weight are hardwire OR'ed on a 32-conductor cable common to 4 planes. Each bit line is then terminated in 200 ohms and applied to a comparator (N5711A) that acts as a discriminator and standardizes the output to logic (TTL) levels.

3.2 Spark Chamber Data Acquisition System, Fig. 11

The major elements of this system are:

- (i) A 5-bit "plane counter" that selects the plane from which data are to be taken next. It is loaded into the computer as the plane ID word and is identified through $\text{MSB}=1$.
- (ii) A 7-bit "board address" counter that selects the group of 32 data bits within a plane. Six bits are utilized for board selection, decoding being effected on each readout board. The seventh bit is delayed to allow transients of address

selection to decay, and is transmitted over two wires. These read the 32 bits of the ODD and EVEN words, respectively.

(iii) A 5-bit 'wire address' counter. This counter is gated on when non-zero data are present in the 32-bit shift register and encodes the 32 shift position into a 5-bit word. The state of the counter corresponds to the last bit of the encoded spark position.

(iv) A 5-bit 'spark width' counter showing the number of adjacent wires on which a spark has developed. The 5-bits for 'width' encoding are required for self-testing only (see sec. 3.2.1) since the most probable width for actual sparks is 2-3 wires.

(v) A logic circuit that tests whether the interrogated word contains non-zero information and whether one or more sparks (adjacent 1's) are contained in one word. The logic circuit also includes a gated clock, delay circuits and a 32-bit shift register.

Items (ii) through (v) represent the 'formatting logic' that accepts information from 32 wires and delivers an 18-bit word containing the location of the spark and its width. MSB=0 signifies that the word contains data, as distinct from the plane ID word, in which MSB=1. The spark location in any given plane is equal to the wire spacing times the quantity

$$\text{BOARD ADDRESS} + \text{WIRE ADDRESS} - \frac{\text{WIDTH}-1}{2}$$

Note that the bit position of the 'board address' effectively multiplies that quantity by 2^5 .

Acquisition and processing of data proceeds as follows (see Fig. 11). An event is recognized by the fast selection logic and triggers 16 thyratron generators, each applying a pulse of ~ 4.0 KV to the chamber planes. The EVENT pulse (a) generates a signal to inhibit the fast logic, (b) increments the 'run number' counter,

and (c) presets the DMA word counter and address register to 1001_8 . The PLANE ID word is loaded into the DMA, followed by data words from plane No. 1. A circuit in the formatting logic tests each word and increments the board address counter if there is no spark information. Otherwise, the 2.5 MHz clock is gated on and the shift register is actuated to encode the wire position and the spark width.

The end of a plane is recognized by a logical AND (PLANE NO.) \wedge (LAST BOARD+1). This signal increments the plane number counter and loads that number into the DMA. Examination and formatting of data words proceeds as before. The last word in the spark chamber system produces an END-OF-CHAMBER signal which initiates acquisition of counter data (see sec. 3.3). The chamber of 30K wires is read in ≈ 5 msec.

3.2.1 Testing Features

In a system of the magnitude described here it is mandatory to have self-test features. These are initiated under computer control with the help of a peripheral device described in sec. 3.4. Two tests are routinely performed:

(a) Test for '1'. In this test one applies a $\approx 15\mu s$ READ pulse to charge all capacitors of a selected plane. After a selectable delay (up to 22 msec), the readout logic is actuated as in a regular event. If no failures are present all 32-bit words are 1.....1. The encoding of wire position and spark width therefore result in an all-zero word in the respective counters. A failure of one or more bits will be interpreted by the formatting logic as 2 or more sparks. Locations of failures are thus directly obtained from the data. It is now obvious why the width counter was designed to have a 5-bit capacity.

(b) Test for '0'. This is actuated through the command 'SIMULATE EVENT'. Ideally all capacitors should be discharged. Any failures in the capacitor-diode

elements, the fanouts, cables, etc., will show up as invalid event words and are easily recognizable on a TTY print out.

The program steps sequentially to test all the planes for either mode of failure. A TTY print out (Fig. 12) provides either a summary of failures or information on plane number and wire location where a failure has been recorded.

3.3 Counter Data Acquisition System, (Fig. 13)

Collection of data from more than 200 modules is initiated from the END-OF-CHAMBER signal. The counter data acquisition logic incorporates a 9-bit counter to generate address codes for chassis and module selection. Five bits are reserved for chassis selection, which is accomplished through switches in the chassis control module. The same module encodes the remaining four bits for data module selection, and provides an OR function on data bus lines of like binary weight ('wire OR'ed').

Each module thus addressed is first examined for content; only non-zero data are loaded into the DMA. After the last module has been examined, an END-OF-EVENT signal is generated that inserts the DMA word count in location 1000_8 of the PDP-9 memory. Thus the block of data in the DMA contains information on the block size, facilitating internal memory transfers that are required for DMA-memory buffering.

An API request is made on (END-OF-EVENT) \vee (OVERFLOW), directing the program to a trap address for software processing. New events are inhibited until the DMA memory contents have been transferred to a buffer location.

Fig. 14 shows a flowchart of the hardware operations described in the foregoing section.

3.4 Peripheral Device for Control of Experiment

The peripheral device, Fig. 15 has the capacity to control 256 locations in the experiment. The 18 bits of the computer are utilized as follows: 8 bits for

address selection; 6 bits for function, data or sub-address; 2-bits for DATA ON/OFF and 2 bits for DVM ON/OFF, where a READ operation is required.

Thus the 256 channel peripheral device has the capacity (a) to set data, logic levels, pulses, etc. via computer control and (b) to "read" the results of the former settings using a DVM in a 'READ' operation. The channels are utilized as follows:

(i) Voltage setting for 144 photomultipliers that are used for trigger selection and particle identification. This subsystem has a capacity to control 192 PM's with a resolution of 15 volts and a total range of 795 volts, nominal. Selection of the desired PM is done via an 8-bit address code, the voltage is set via the 6-bit data code followed by a DATA ON or DATA OFF signal, as appropriate. The set voltage is read on a DVM, the same information also being loaded into the computer memory. A background program executes periodic checks to verify correctness of voltage settings and thus releases the experimenter from the tedium of attending to many PM's.

(ii) Checkout of time-of-flight channels. The time-of-flight channels are tested with light emitting diodes that are powered from a HV generator with a rise time of 0.5 nsec. The mercury relay of the HV generator is turned on via a suitable code from the peripheral device; a group of PM's is similarly selected, using coaxial relays. Histograms of number of counts versus a fixed delay are then obtained on ADC's that convert time into a train of pulses with a resolution of <100 psec/count. The time delay is then changed using a NIM level generated by the peripheral device and applied to a 3-input majority logic circuit set to respond to a 2-fold coincidence. The histograms thus obtained check whether all channels function properly and also calibrate the time-of-flight system.

(iii) NIM levels, and pulses for running and testing of the spark chamber under computer control, as discussed in sec. 3.2.

(iv) Storage scope control and a variety of other control function that are done either through relay closures or NIM level or pulse sources.

The experimental apparatus described in this section utilizes a good fraction of 10^6 components. In its first runs covering two experiments ($K_L^0 \rightarrow \pi\mu\nu$ and $K_L^0 \rightarrow \pi^+\pi^-\pi^0$) some 10^7 events were accumulated with negligible loss of experimental time due to component failure. Loss of a capacitor-diode element affects the particular wire only and is ignored without adverse effects.

TABLE 1

DIMENSIONS OF WIRE CHAMBERS

Upstream Chambers	x	$1.2 \times 1.2 \text{ m}^2$
	y	$1.2 \times 1.2 \text{ m}^2$
	u, v	$1.5 \times 1.5 \text{ m}^2$
Downstream Chambers	x	$1.2 \times 2.4 \text{ m}^2$
	y	$1.2 \times 2.4 \text{ m}^2$
	u, v	$1.8 \times 2.4 \text{ m}^2$

FIGURE CAPTIONS

1. Plan view of spectrometer.
2. Spark chamber assembly (exploded view).
3. Photograph of $1.2 \times 1.2 \text{ m}^2$ module assembly.
4. Sample event as displayed on on-line storage scope. u, v planes not displayed. Titles and dark areas do not appear on display.
5. Chamber efficiency as a function of applied high voltage.
6. Multitrack efficiency.
7. Number of wires per spark, as a function of applied high voltage.
8. Capacitor-diode (C-D) readout. Basic circuit serving one wire.
9. Circuit diagram including C-D elements, drive, address decode and test circuitry serving 2×32 -bit words.
10. PC board of circuitry of Fig. 9.
11. Spark chamber data acquisition system using C-D readout.
12. Sample test printout. (P = plane number, B = board number).
13. Counter data acquisition system. Simplified block diagram.
14. Flowchart of hardware data acquisition system (Block diagram Fig. 11 and 13.)
15. 256-channel peripheral device for programmed transfer I/O transactions to control experiment.

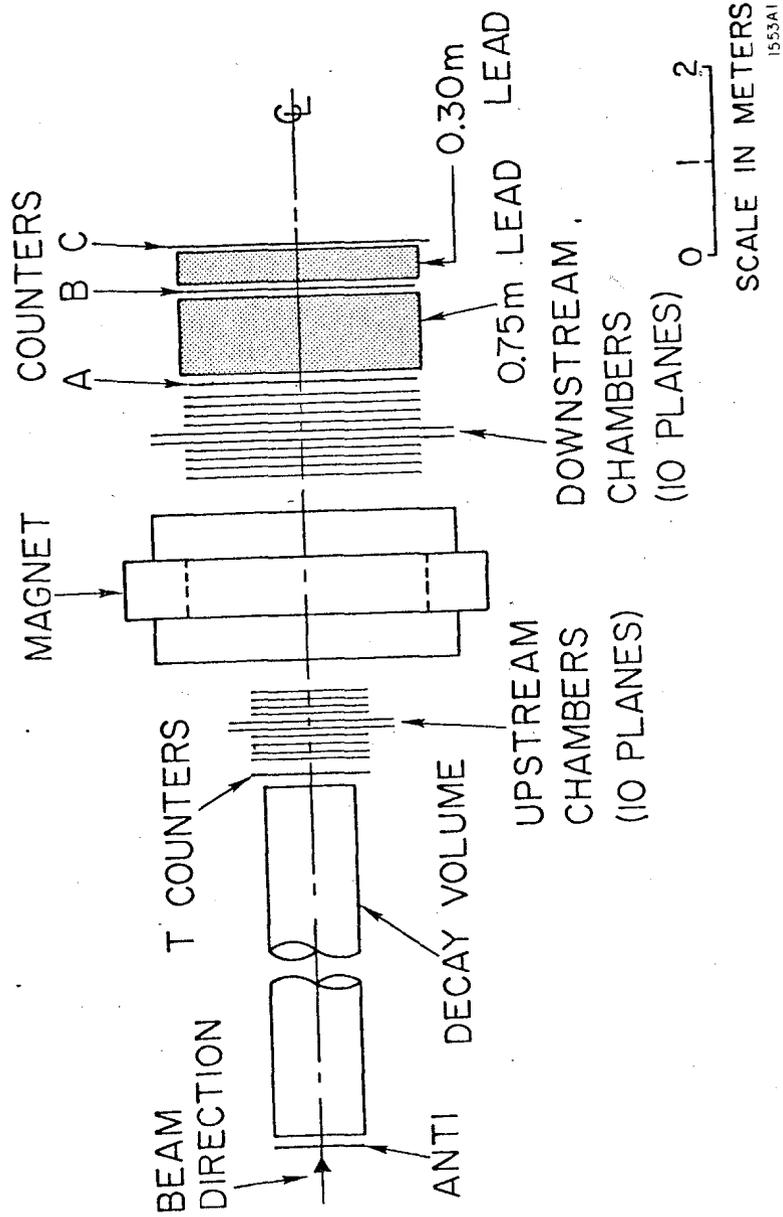


Fig. 1

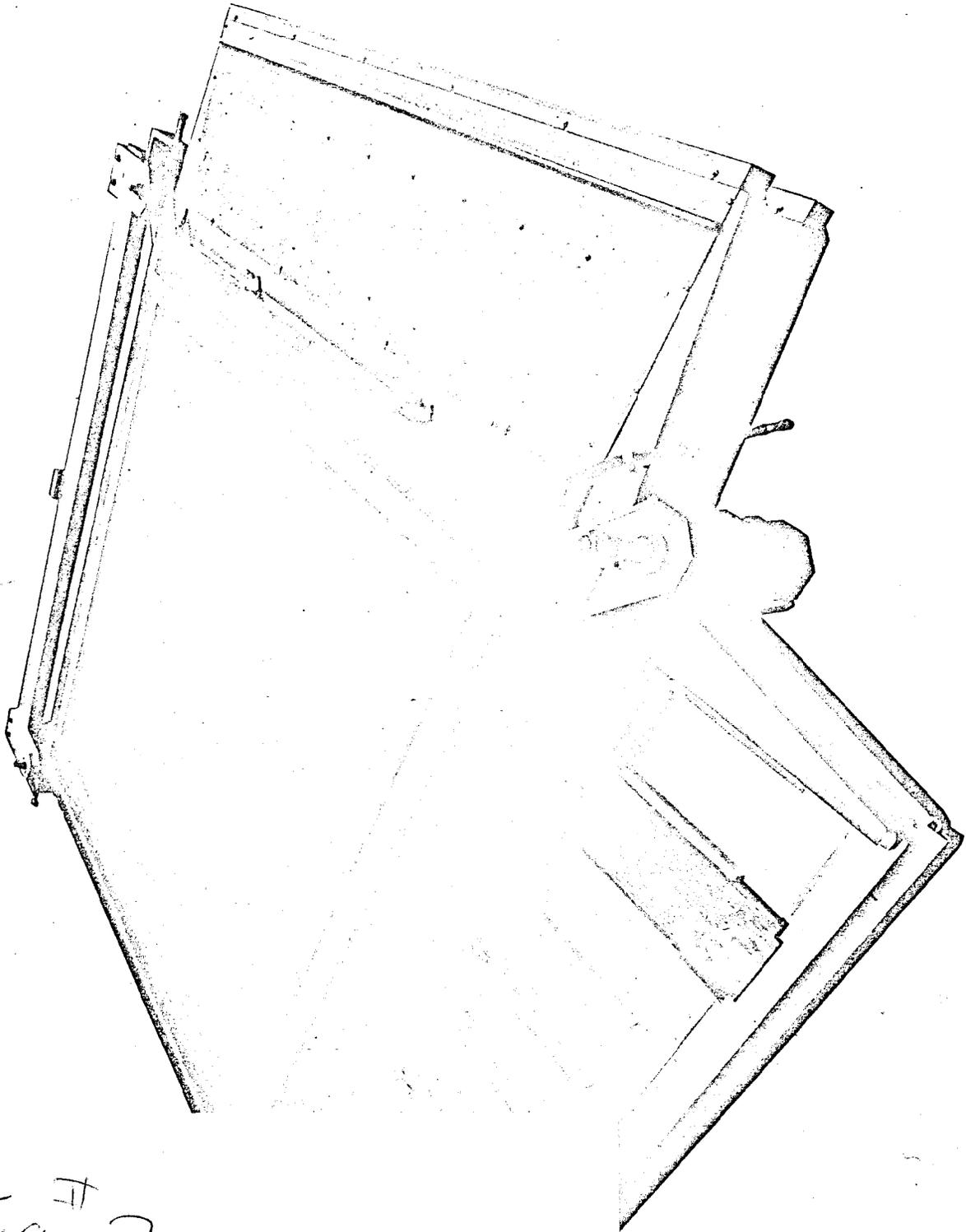


Fig. 3

FIG[#] 2

Lucas[#] 1553A4

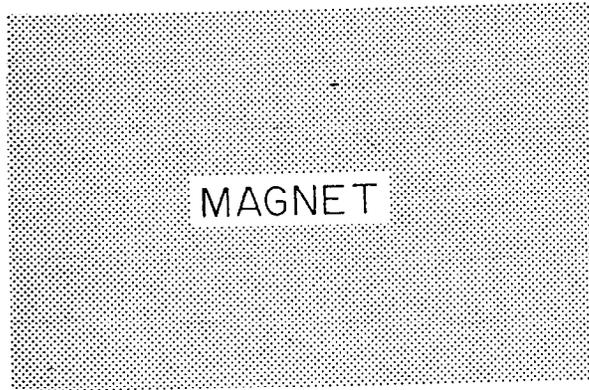
BEAM DIRECTION



T COUNTERS

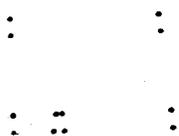


UPSTREAM
CHAMBERS



MAGNET

DOWNSTREAM
CHAMBERS



A COUNTERS



LEAD

B COUNTERS



LEAD

C COUNTERS

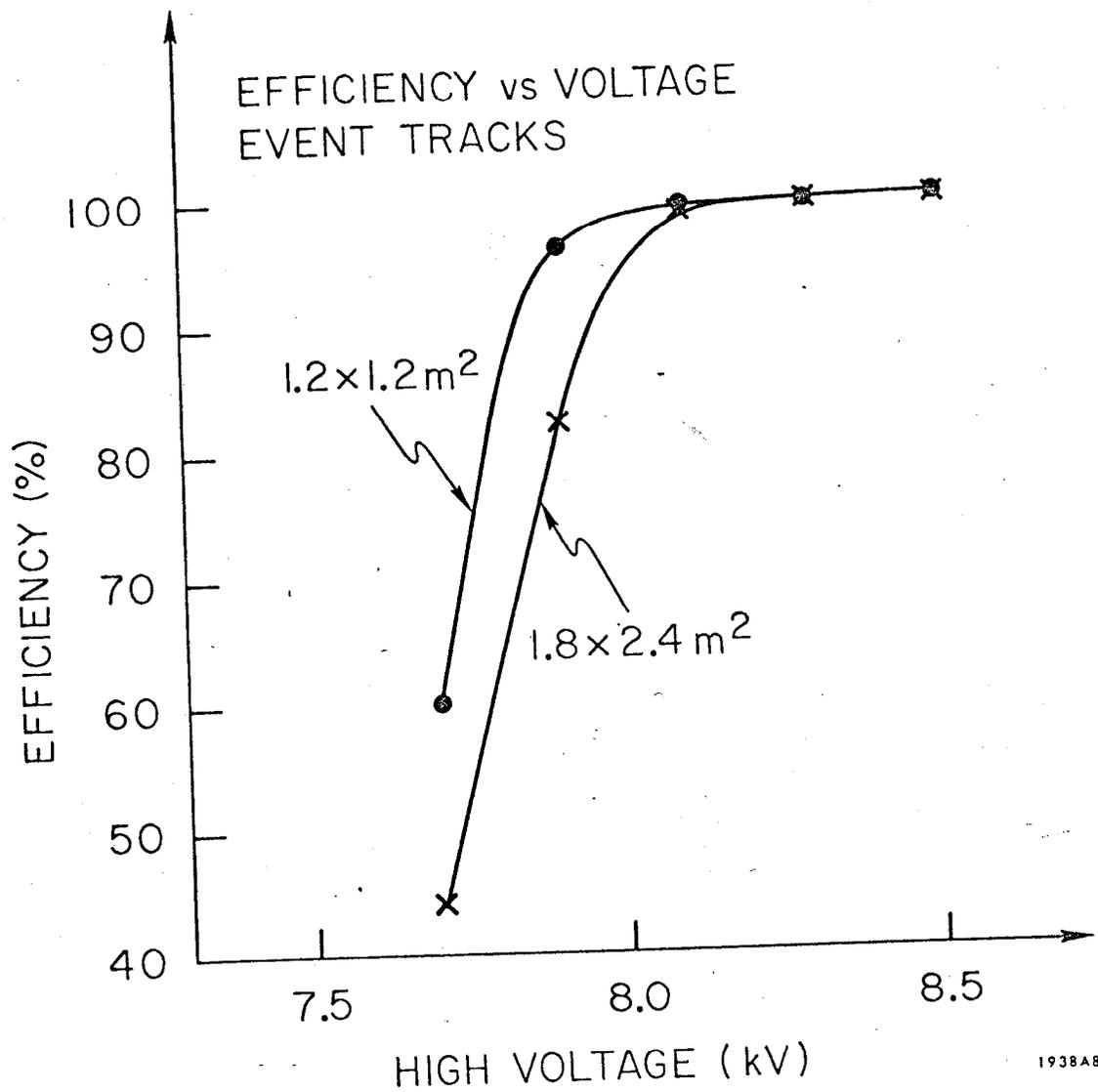


ELEVATION

PLAN VIEW

1938813

Fig. 4



1938A8

Fig. 5

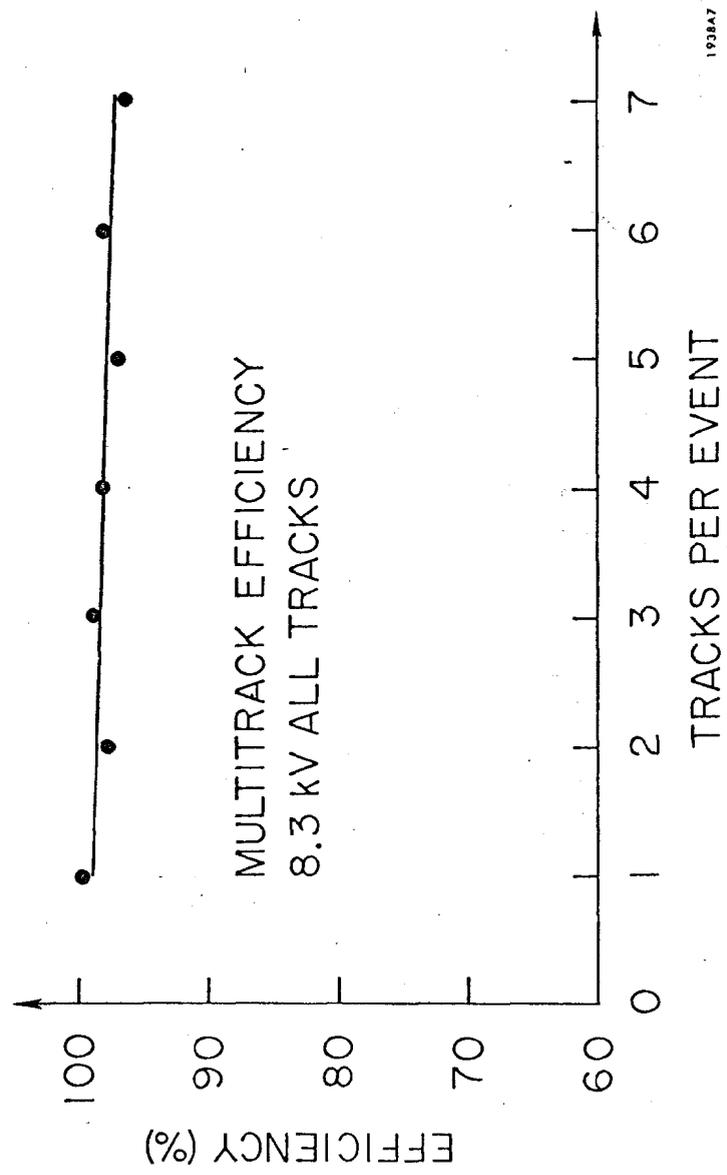


Fig. 6

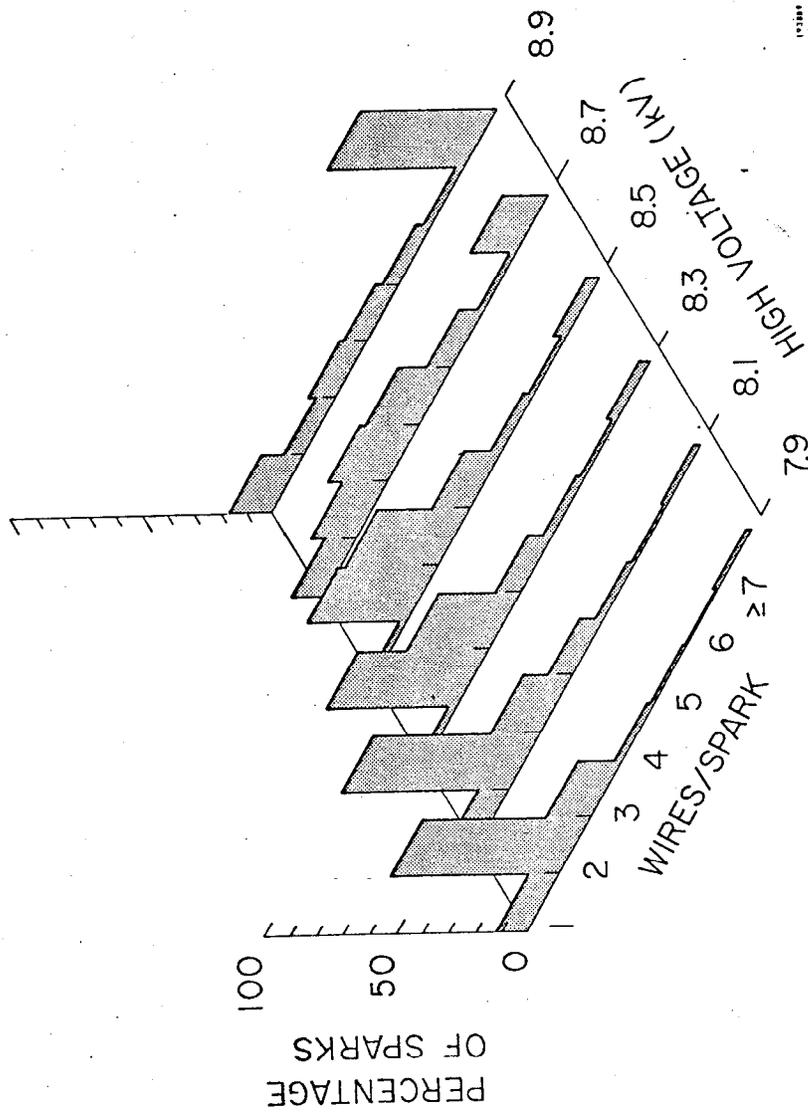
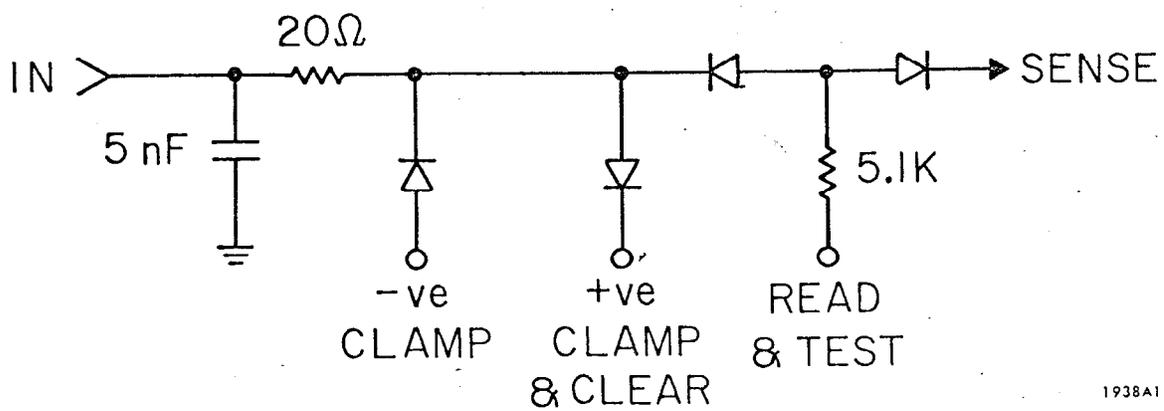


Fig. 7



1938A1

Fig. 8

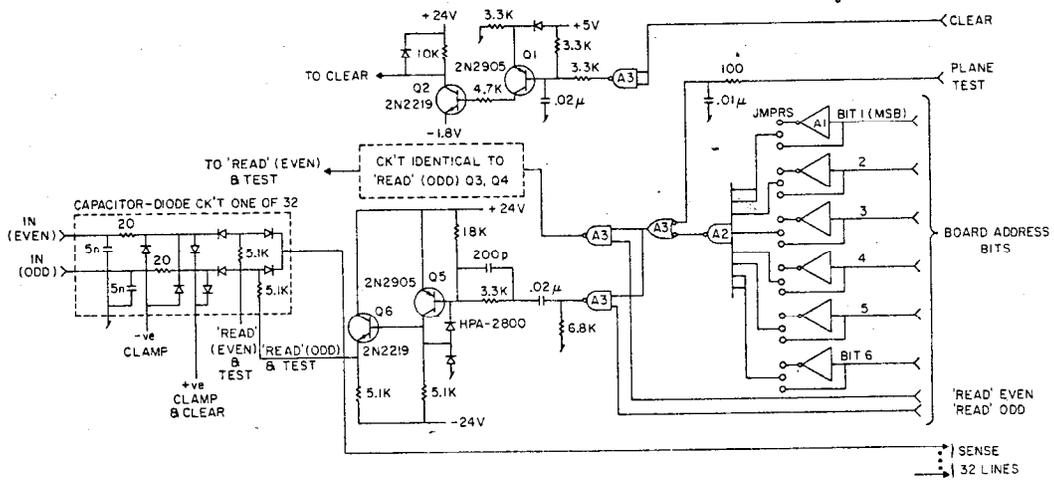
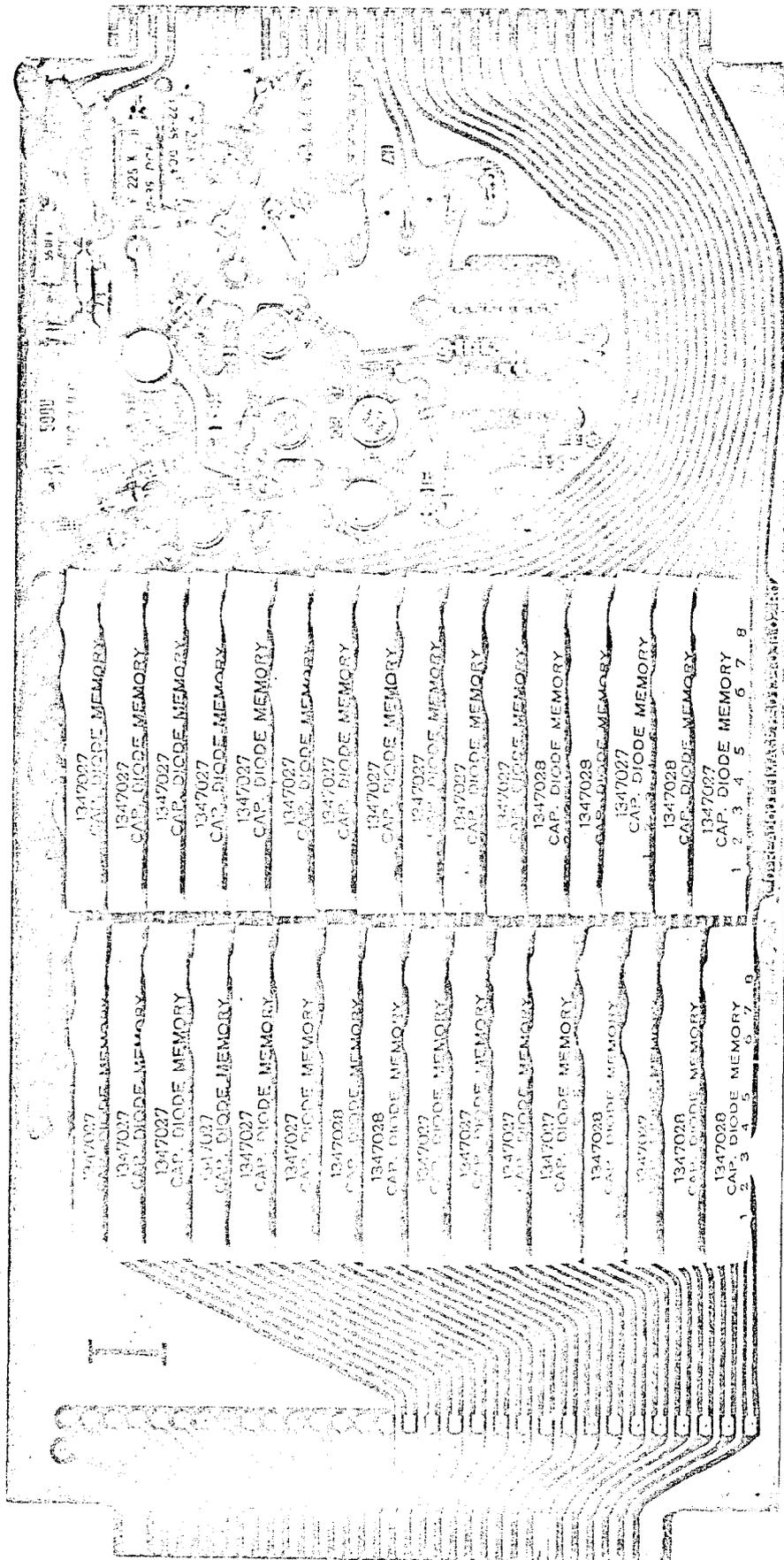


Fig. 9



1938A12

Fig. 10

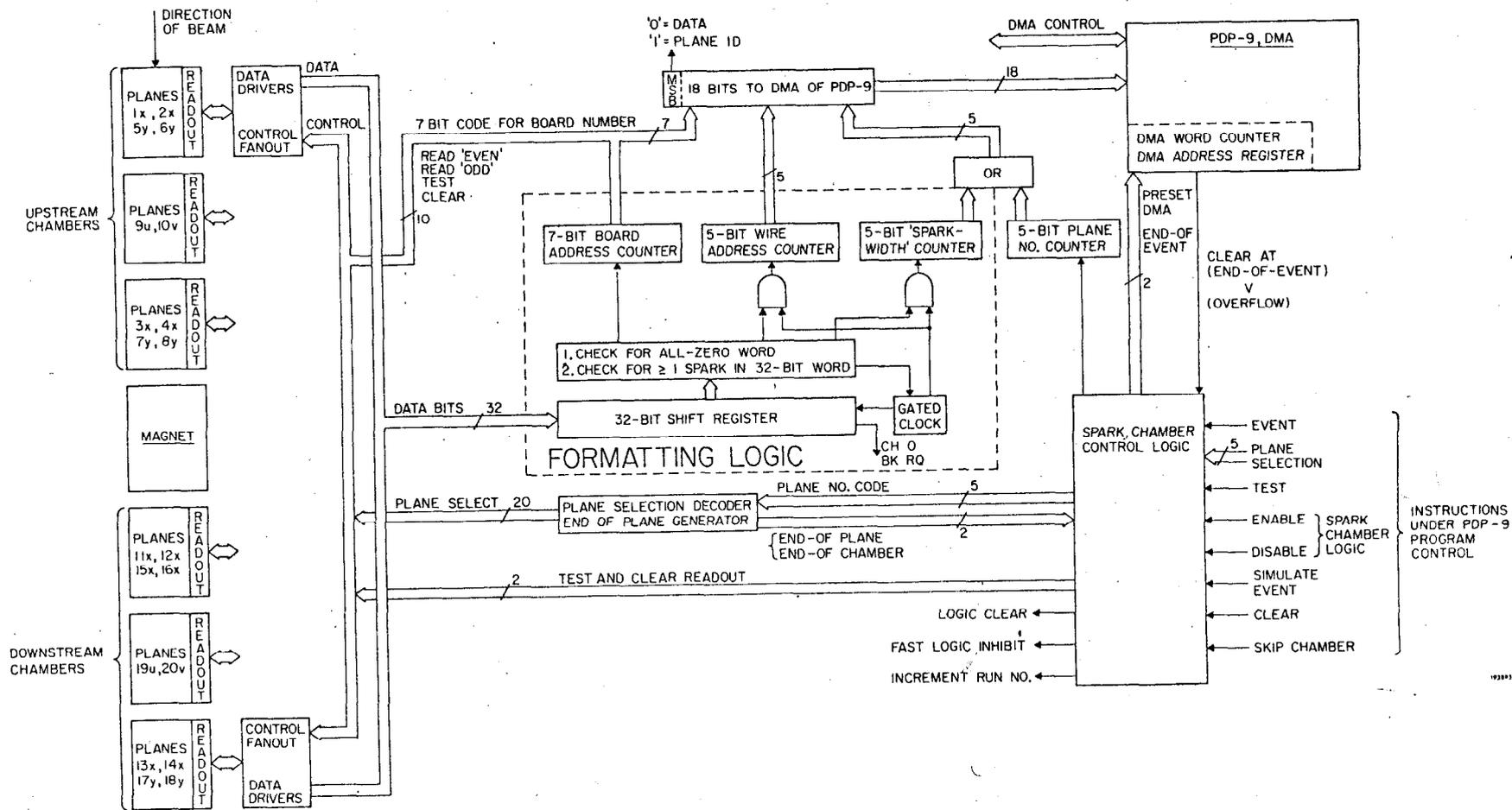


Fig. 11

< DO NOT NOW >

BEGIN READOUT TEST

P B WIRES

20 59 11111111 11111111 10011111 11111101
001 ON ERRORS

11 70 00001000 00000000 00000000 00000000
19 14 00000000 00000000 00000000 00001000
002 OFF ERRORS

1938A14

Fig. 12

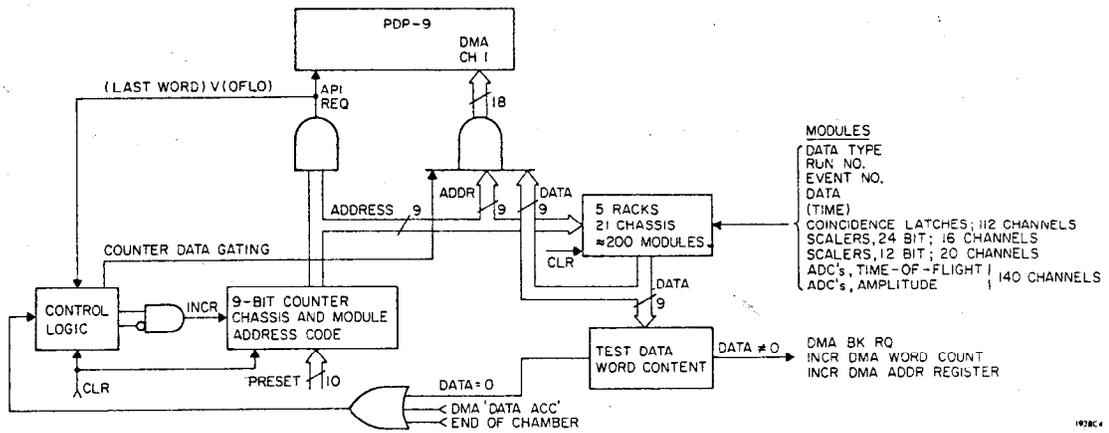


Fig. 13

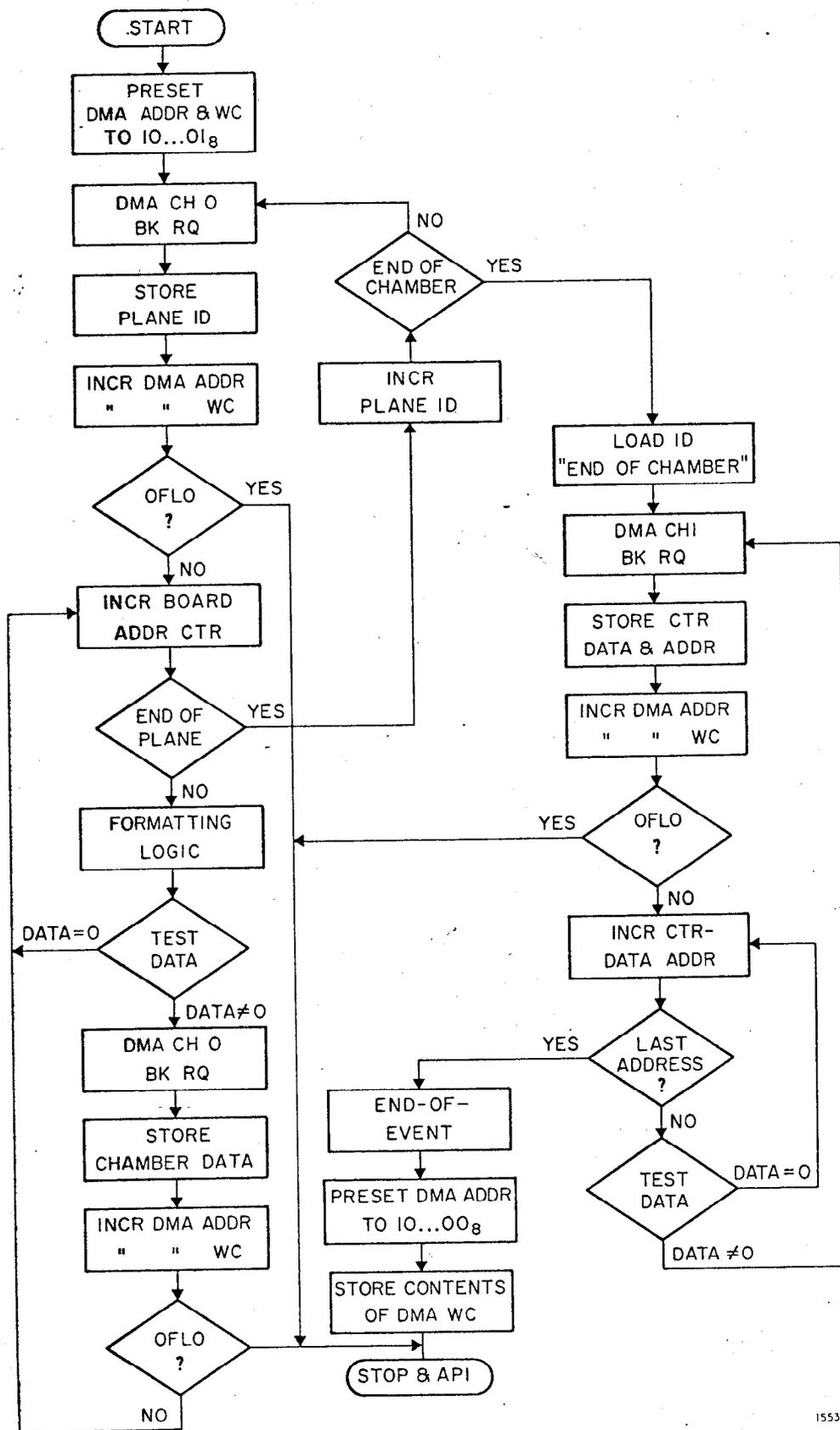


Fig. 14

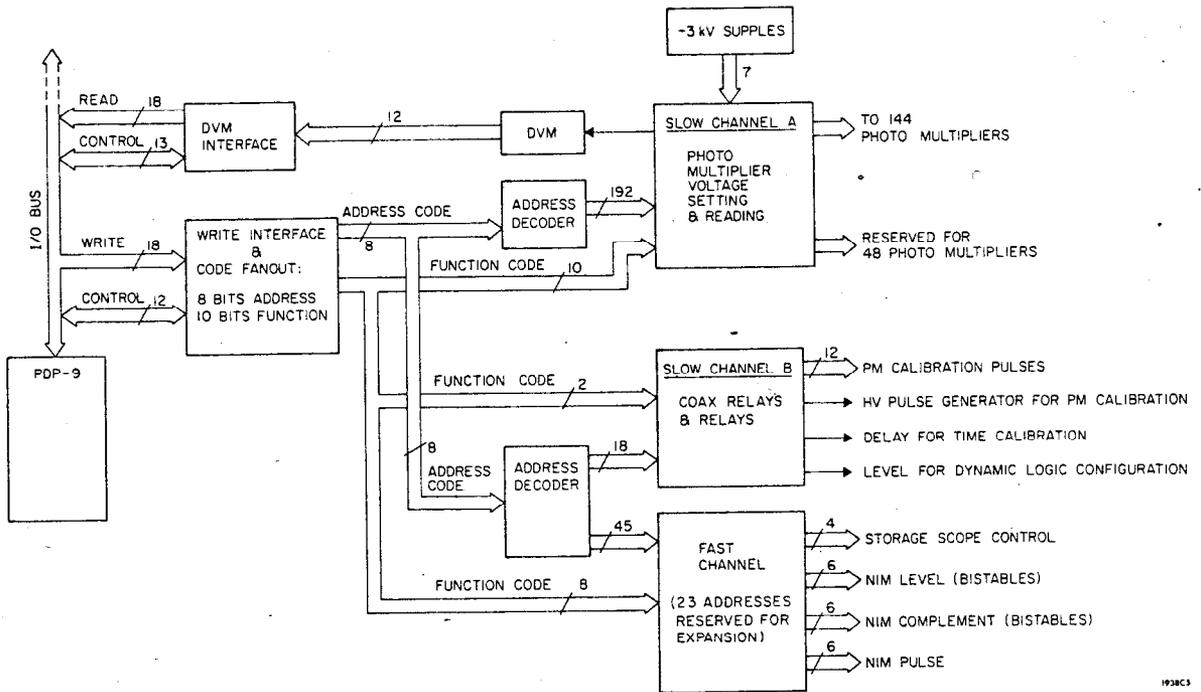


Fig. 15