

Performances of typical high energy physics applications in flash-based field-programmable gate array under gamma irradiation

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Performances of typical high energy physics applications in flash-based field-programmable gate array under gamma irradiation

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ABSTRACT: Recent field-programmable gate arrays (FPGAs) based on flash memories offer a high radiation tolerance. We discuss potential applications of the Microsemi IGLOO2 FPGAs in high energy experiments. We implement a 24 channel time-to-digital converter with a time binning of 0.78 ns and evaluate the performance. Differential and integral non-linearity is measured to be far below the time binning. The time resolution obtained is approximately 0.25 ns. The FPGA was exposed to gamma rays with a total ionizing dose of 300 Gy. The function of the configuration memory is monitored and the degradation of the performance on the ring oscillator and high-speed transceiver is measured. The errors during firmware download and verification of downloaded firmware have been observed at 110–120 Gy and 80–90 Gy, respectively. The functionality of the ring oscillator and high-speed transceiver remains up to about 200 Gy.

KEYWORDS: Front-end electronics for detector readout; Radiation damage to electronic components; Radiation-hard electronics

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1 Introduction

Field-programmable gate arrays (FPGAs) are widely used in the experiments of high energy physics. FPGAs based on flash memories could have high radiation tolerance with respect to the FPGAs based on static random access memories. This extends the potential applications of the FPGAs. In this study, the flash-based IGLOO2 FPGA manufactured by Microsemi [1] is focused on. Examples of the experiments of high energy physics include the ATLAS experiment [2]. IGLOO2 FPGA has relatively high tolerance against single event effects [3]. Therefore we focused on total ionizing dose. The irradiation level at the monitored drift tube (MDT) chambers at the ATLAS detector is estimated to be 2–20 Gy in 10 years of LHC operation [4]. A 24 channel time-to-digital converter (TDC) with time binning of 0.78 ns, which has the same binning and number of channels as in the current MDT system, is implemented and tested. The radiation tolerance of the IGLOO2 FPGA against total irradiation dose is evaluated. The reprogrammability of the configuration memory, the current-voltage characteristic of the ring oscillator, and the high speed transceiver under gamma ray irradiation up to 300 Gy are investigated.

2 Demonstration of the TDC

2.1 Schematic of the TDC

Figure 1 shows a schematic of the TDC, which has been developed with Xilinx Kintex-7 FPGA [5]. The internal clocks of 320 MHz and 160 MHz synchronized with a 40 MHz reference clock are

generated with a phase-locked loop circuit provided in the FPGA. In this design, a multisampling scheme based on quad phase clocks with the frequency of 320 MHz is employed to achieve the time binning of $1/(320 \text{ MHz} \times 4) = 0.78 \text{ nsec}$. Time measurement is provided in a time window of 6.25 nsec and transferred with 160 MHz clock. The dynamic range of $(1/160 \text{ MHz}) \times 2^{14} = 100 \mu\text{sec}$ is fulfilled by adding the information of 14 bit counter running with 160 MHz clock.

The performance of the time measurement could generally be affected by the variation of the delays between different signal paths in the core of the TDC. The locations of the D flip flops in the core of the TDC are placed near the input ports to minimize the difference between signal path lengths. The signal path difference obtained from a simulation corresponds approximately to 0.2 nsec.

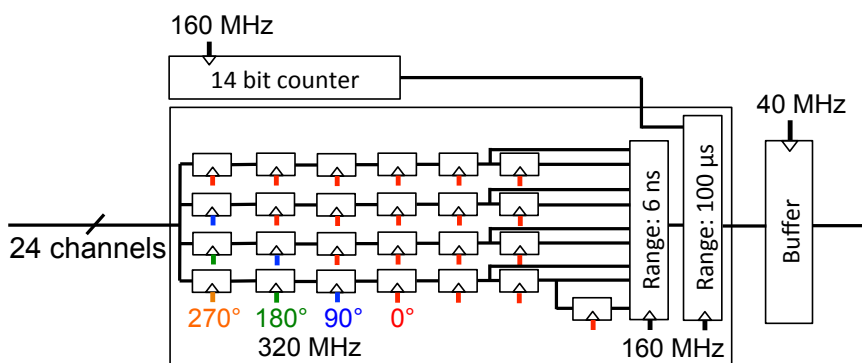


Figure 1. A schematic of the demonstrator of the TDC.

2.2 Demonstrator and test setup

Figure 2 shows a picture of the evaluation kit (M2GL-EVAL-KIT) used for the evaluation of the TDC performance. The performance is evaluated for all of 24 channels. The reference clock and the signals are provided from a pulse generator (Agilent 81150A [6]). The standard deviation of

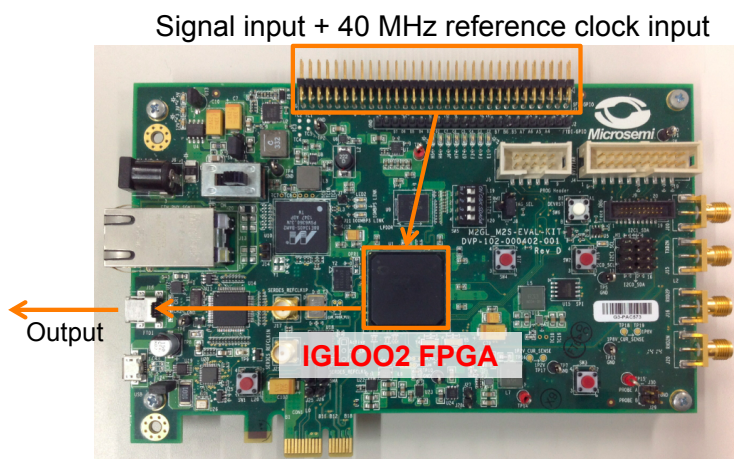


Figure 2. A demonstrator used for the TDC performance evaluation.

the time difference between the two leading edges of the pulses is measured to be 30 psec. The data output from the TDC is read out with the UART protocol.

2.3 Performance evaluation

The differential nonlinearity (DNL) and the integral nonlinearity (INL) have been measured. The DNL is defined for each bin as

$$\text{DNL}_i = \frac{T_i - T_{\text{BIN}}}{T_{\text{BIN}}}, \quad (2.1)$$

where T_{BIN} is the ideal time binning and T_i is the time difference between the specific bins i and $i + 1$. For the measurement of DNL, the output from the core of the TDC is read out for the time difference of the leading edges between the signal clock and the reference clock. By scanning the time difference between signal and reference clocks, the width of a typical bin can be focused on. The scan is performed with a step size of 25 psec. The result of the measurement of the DNL for channel 1 is shown in figure 3. The measured DNL is less than half of the unity. The nonlinearity is dominated by the length difference between signal paths in the FPGA. Similar results are obtained for all 24 channels.

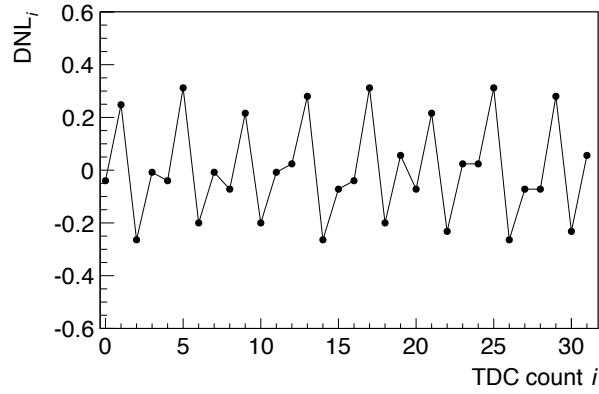


Figure 3. Result of the measurement of DNL.

The INL is parameterized in this study by

$$\text{INL} = \frac{\langle T_{\text{measured}} \rangle - T_{\text{input}}}{T_{\text{BIN}}}, \quad (2.2)$$

where T_{input} is the time difference between the leading edges of input signal clocks and $\langle T_{\text{measured}} \rangle$ is the mean of the time difference measured by the TDC. The result of the measurement of the INL for channel 1 is shown in figure 4. The measured INL is consistent with zero up to 100 μsec . Similar results are obtained for all 24 channels.

The time resolution is evaluated by taking the data with various time difference between the leading edges of the input signal clocks. The standard deviation of the difference between the measured and input time difference is taken. The time difference is scanned from 200 ns to 100 μs . Figure 5 shows the distribution of the difference between measured time and ideal time for channel 1. Neither overflow nor underflow is found. The obtained standard deviation is 0.35 ns. The time

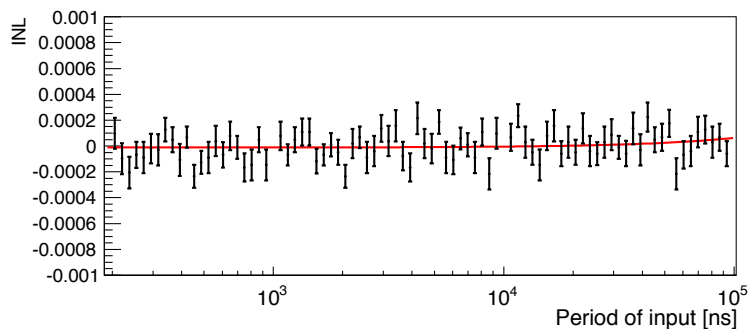


Figure 4. Results of the measurement of INL. The red line shows the result of a linear fit by $\text{INL} = AT_{\text{ideal}} + B$. Parameters A and B are obtained to be $(-1.0 \pm 1.7) \times 10^{-10}$ /ns and $(-0.3 \pm 5.0) \times 10^{-6}$, respectively.

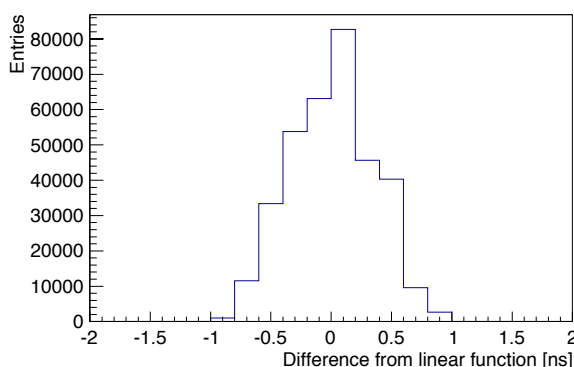


Figure 5. The distribution of difference between measured time and ideal time.

resolution for the signal edge measurement has been estimated to be 0.25 ns. Similar results are obtained for all 24 channels.

3 Gamma ray irradiation test

3.1 Irradiation test board and setup

Figure 6 shows a board developed for the irradiation tests of the IGLOO2 FPGA (M2GL010T-1FGG484). The board has SMA connectors for high-speed transceiver (SERDES) and general purpose input and output ports. Gamma rays have been irradiated at the Cobalt-60 irradiation facility at Nagoya University. The irradiation rate is 0.1–1 Gy/min.

3.2 Irradiation test result

3.2.1 Test results for configuration memory

Two boards have been irradiated with a step size of 10 Gy for the evaluation of the tolerance of the configuration memory. The commands of READ ID CODE (extraction of the identifier of the FPGA), PROGRAM (firmware download) and VERIFY (verification of the downloaded firmware) are examined from the Microsemi Libero SoC Design Suite [7, 8]. Errors on VERIFY have been

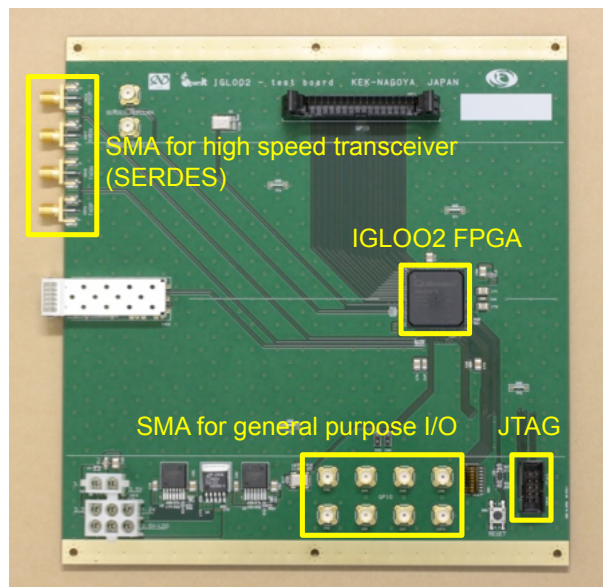


Figure 6. Irradiation test board.

observed with the irradiation level of 80–90 Gy depending on the boards. Errors on PROGRAM have been observed with the irradiation level of 110–120 Gy.

3.2.2 Test results for ring oscillator

The change in the current-voltage characteristic of metal-oxide-semiconductor field-effect transistor (MOSFET) due to the irradiation dose could affect the TDC performance. Since the oscillation of the ring oscillator is sensitive to the current-voltage characteristic of MOSFET [9], we have tested the ring oscillator. Other two boards have been irradiated with a step size of 10 Gy. The ring oscillator consists of 501 NAND gates, where the output of each NAND gate is connected to the two inputs of another NAND gate. The firmware utilizes 4% of the lookup tables as 501 NAND gates. The oscillation period and the power consumption have been measured. To evaluate the tolerance beyond the limit of firmware download, the firmware download is performed only at the beginning of the irradiation test. Figure 7(a) shows the relation between the period and the irradiation level, and figure 7(b) shows the relation between the power consumption and the irradiation level. The resulting change in the oscillation period ($\pm 1\%$ level) indicates no significant effect on the TDC performance with irradiation level of up to 200 Gy. The power consumption of the ring oscillator remained almost unchanged with irradiation level of up to 200 Gy. The oscillation stops after an irradiation dose of about 200 Gy.

3.2.3 Test results for high speed transceiver

Other two boards have been irradiated with a step size of 100 Gy for the evaluation of the tolerance of SERDES. Pseudo-random data has been transmitted and looped back with the coaxial cable. Data transfer rates of 2 Gbps and 4 Gbps are tested. The bit error rate (BER) has been measured. This firmware utilizes 15% of lookup tables, 10% of D flip flops, 50% of clock resources, and 100% of SERDES blocks. The worst slack path timing is 1.7 ns. To evaluate the tolerance beyond the

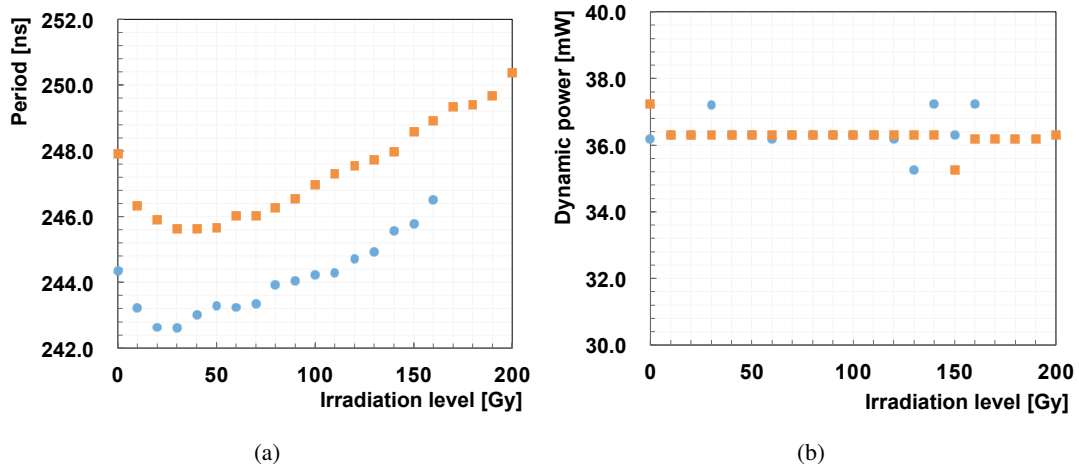


Figure 7. Results of the measurement of the period (a) and the dynamic power consumption (b) for the ring oscillator based on 501 NAND gates. The orange and blue plots correspond to the boards 1 and 2, respectively.

limit of the firmware download, the firmware download is performed only at the beginning of the irradiation test. Table 1 shows the measured BER for each irradiation level and data transfer rate. No data is sent or received after the irradiation of 200 Gy.

Table 1. Measured BER for SERDES depending on the irradiation dose.

Total Dose [Gy]	BER for 2 Gbps	BER for 4 Gbps
0	$< 8 \times 10^{-13}$	$< 4 \times 10^{-13}$
100	$< 8 \times 10^{-13}$	$< 4 \times 10^{-13}$
200	Not functional	Not functional

3.2.4 Recovery of the functions

In total eight boards are irradiated to an irradiation level of 92–300 Gy depending on the boards. After the irradiation, the four boards with the irradiation of 92–120 Gy had errors in PROGRAM, while the other boards with the irradiation of 160–300 Gy had errors in READ ID CODE. Two boards which have the errors in READ ID CODE were put in the thermostat chamber ESPEC SH-641 [10], and the temperature was kept to be 75°C for the investigation of recovery, while heating is not considered for the actual application for MDT. Recovery has been observed for the two boards.

Figure 8 summarizes the results of the function recovery. The function of PROGRAM are recovered in a few hours for the irradiation level of 100 Gy. The time needed for the recovery seems to correlate with the total irradiation level. The function of READ ID CODE and implemented firmware were recovered by annealing in the high-temperature environment of 75°C. Implemented firmware, i.e. ring oscillator and SERDES, was also recovered at the same time of the recovery of the function of READ ID CODE.

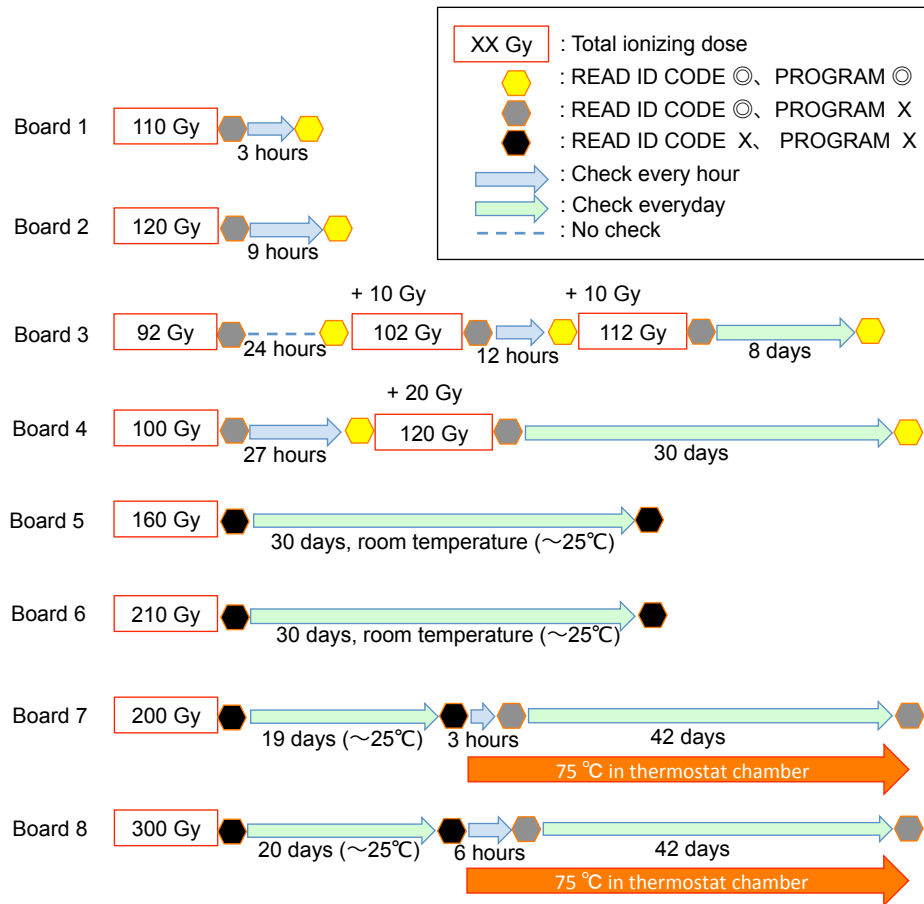


Figure 8. Summary of the recovery for the irradiated boards.

4 Conclusion

In conclusion, we examine the performance of the flash-based Microsemi IGLOO2 FPGA. We implement a 24 channel time-to-digital converter with a time binning of 0.78 ns. The differential nonlinearity and integrated nonlinearity are measured to be small. The time resolution obtained is approximately 0.25 ns. The radiation tolerance against total ionizing dose is studied with the gamma ray irradiation of a few hundred Gy. Firmware download is observed to be impossible after irradiation of about 100 Gy. The downloaded NAND ring oscillator and SERDES seem to survive up to a higher irradiation level of 100–200 Gy. This study provides useful information on the use of IGLOO2 FPGA in high energy physics experiments.

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