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Parametrization of the radiation induced leakage current increase of NMOS transistors

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ABSTRACT: The increase of the leakage current of NMOS transistors during exposure to ionizing radiation is known and well studied. Radiation hardness by design techniques have been developed to mitigate this effect and have been successfully used. More recent developments in smaller feature size technologies do not make use of these techniques due to their drawbacks in terms of logic density and requirement of dedicated libraries. During operation the resulting increase of the supply current is a serious challenge and needs to be considered during the system design.

A simple parametrization of the leakage current of NMOS transistors as a function of total ionizing dose is presented. The parametrization uses a transistor transfer characteristics of the parasitic transistor along the shallow trench isolation to describe the leakage current of the nominal transistor. Together with a parametrization of the number of positive charges trapped in the silicon dioxide and number of activated interface traps in the silicon to silicon dioxide interface the leakage current results as a function of the exposure time to ionizing radiation. This function is fitted to data of the leakage current of single transistors as well as to data of the supply current of full ASICs.

KEYWORDS: Radiation damage to detector materials (solid state); Radiation damage to electronic components; Radiation-hard detectors; Radiation-hard electronics

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1 Introduction

The radiation induced leakage current and the threshold voltage shift of NMOS transistors are well known and intensively studied challenges for the design of radiation hard application specific integrated circuits (ASIC).

Hardness by design (HBD) techniques [1, 2] have been developed and extensively used in the circuit design in the 0.25 μm technology node for the LHC experiments [3]. The HBD techniques consist mainly in the use of enclosed gate transistors to mitigate the source to drain leakage current along the shallow trench isolation (STI) and guard ring structures surrounding the transistors to avoid leakage current between neighboring structures. The use of this technique requires an increased area as well as custom libraries. With the transition to the 0.13 μm technology node, the amplitude of the leakage current increase decreases by three orders of magnitude, with the result that the HBD techniques are needed in sensitive nodes of the design only for radiation hard designs [4]. However, while the chip is operational, the increase of the leakage current of NMOS transistors results in a significant increase of the supply current. A generic parametrization of the leakage current as a function of the total ionizing dose (TID) of single NMOS transistors is presented in this paper. The resulting function is fitted to published data of a diversity of technologies in use or under investigation for use in extremely radiation intense environments. As demonstrated in this paper, this parametrization can be used as well to model the supply current shift with TID on full ASICs and to predict the current to be expected during operation of the ASICs as a function of the temperature and the dose rate, once the parameters of the parametrization are measured.

2 Parametrization of the leakage current

This model describes the leakage current increase of linear NMOS transistors independent of technology details. The increase of the leakage current as a function of total ionizing dose has been reported for a large number of technologies. It originates from *parasitic transistor channels* along the STI, in which the transistor is embedded as indicated in figure 1.

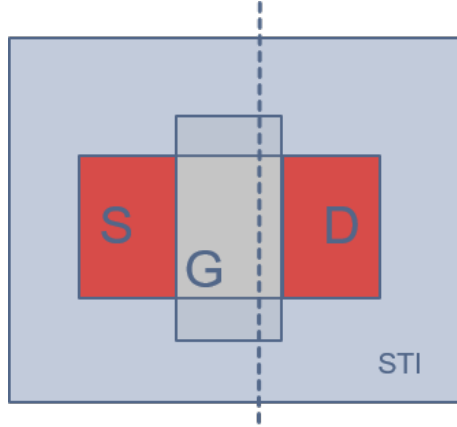


Figure 1. Top View of a linear transistor. The source (S), gate (G), and drain (D) as well as the shallow trench isolation (STI) are indicated. The dashed line shows the place of the cross section in figure 2.

With a positive space charge appearing in the STI due to ionizing radiation, an inversion layer is created along the STI, which results in leakage current paths from source to drain [4]. This is indicated in the cross section in figure 2.



Figure 2. Cross section of a transistor along the line indicated in figure 1. The channel of the parasitic transistor along the STI is indicated in yellow.

These leakage current paths can be described as the channels of two parasitic transistors. As can be seen in figure 3, each parasitic transistor has a layout analogue to a linear transistor with the only difference, that the electric field opening the transistor channel originates from the positive space charge in the STI instead of from the potential at the gate. The space charge in the STI is always positive and therefore in PMOS transistors this transistor channel is closed by the radiation induced space charge. Thus the leakage current increase is only observed in NMOS transistors.

This analogue layout motivates to describe the leakage current increase due to the parasitic device using the *transfer characteristics* of the parasitic transistor.

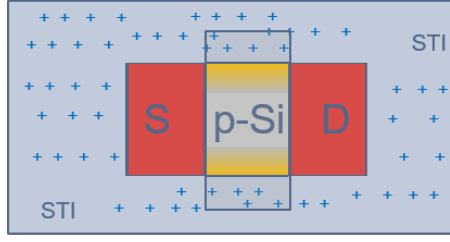


Figure 3. Top view of the two parasitic transistors below the gate. The channels of the parasitic transistors along the STI are indicated in yellow.

2.1 Transfer characteristics of the parasitic transistor

The transfer characteristics (drain current as a function of the gate to source voltage) of transistors operated in saturation can be simplified by

$$\begin{aligned} I_D &\approx 0 & \text{for } V_G < V_{\text{thr}} \\ I_D &\approx K' \cdot (V_G - V_{\text{thr}})^2 & \text{for } V_G \geq V_{\text{thr}} \end{aligned} \quad (2.1)$$

where sub-threshold leakage current is neglected. The sub-threshold leakage current of the parasitic transistor is negligible, because it is orders of magnitude smaller than the sub-threshold leakage current of the regular transistor.

I_D is the drain to source current, V_G is the gate to source voltage, and V_{thr} the threshold voltage. K' is the proportionality constant containing the widths, lengths, oxide capacitance, and the mobility of the minority charge carriers in the channel of the transistor, etc. In the parasitic transistor (which is responsible for the leakage current) the electric field originates from the effective space charge. Assuming an electric field in the silicon proportional to the effective space charge, the gate voltage of the parasitic transistor is in this model replaced by the *effective number of charges* N_{eff} . Similarly, the threshold voltage is expressed by the *threshold number of charges* N_{thr} . The transfer characteristics of the parasitic transistor are then given by

$$\begin{aligned} I_D^{\text{par}} &= 0 & \text{for } N_{\text{eff}} < N_{\text{thr}} \\ I_D^{\text{par}} &= K \cdot (N_{\text{eff}} - N_{\text{thr}})^2 & \text{for } N_{\text{eff}} \geq N_{\text{thr}} \end{aligned}$$

and thus the leakage current of the regular transistor I_{leak} is given by

$$I_{\text{leak}} = I_{\text{leak}}^0 \quad \text{for } N_{\text{eff}} < N_{\text{thr}} \quad (2.2)$$

and by

$$I_{\text{leak}} = I_{\text{leak}}^0 + K \cdot (N_{\text{eff}} - N_{\text{thr}})^2 \quad \text{for } N_{\text{eff}} \geq N_{\text{thr}} \quad (2.3)$$

with I_{leak}^0 the preirradiation leakage current of the regular transistor. N_{thr} is constant in time (and therefore accumulated dose) and temperature. With these assumptions a parametrization of the number of effective charge carriers N_{eff} describes the leakage current shift in NMOS transistors.

2.2 Processes of charge generation

A combination of four processes results in the effective space charge in the STI. First, due to ionization of the atoms, the incident radiation generates free electron hole pairs in the silicon dioxide of the STI [5, 6]. Some of these pairs recombine quickly, but the mobility of the electrons is between six and twelve orders of magnitude larger than the mobility of the holes, depending on the temperature and the electrical field [7–10]. Therefore many electrons are quickly removed from the STI, while the left over holes move slowly in the silicon dioxide by hopping transport [5]. Sites with missing oxide atoms in the amorphous silicon dioxide result in energy levels above the valence band and thus electrically neutral deep hole traps [5]. These traps are distributed in the STI volume, and their concentration is largely influenced by the manufacturing of the STI, and thus it is technology dependent. During the movement some holes get trapped in these sites and a space charge is built. The holes have a certain probability to get detrapped by thermal energy. The lifetime τ_{ox} of the holes in the traps depends on the energy level of the traps, and of the temperature.

Holes which are not trapped in the silicon dioxide can move to the silicon to silicon dioxide interface. At this interface are incomplete or dangling atomic bonds due to the abrupt transition from amorphous to crystalline material. The dangling bonds manifest themselves as energy levels in the band-gap, and thus they trap mainly electrons or holes, depending on the Fermi-level of the silicon [5]. This trapping of electrons in the case of NMOS transistors (p-type silicon) and holes in the case of PMOS transistors (n-type silicon) degrades the transistor performance, and therefore usually the dangling bonds are deactivated by the manufacturer using hydrogen. The radiation induced free holes can react with the hydrogen and the dangling bonds get re-activated [5]. In this case they are commonly called radiation induced *interface traps*.

In the case of NMOS transistors the activation of the interface traps results in a negative space charge, while the trapping of holes in the STI results in a positive charge [4]. The electric fields compensate each other, so that the effective number of charges N_{eff} :

$$N_{\text{eff}} = N_{\text{ox}} - N_{\text{if}} \quad (2.4)$$

becomes relevant, with N_{ox} the number of trapped holes in the STI, and N_{if} the number of electrons trapped at the interface. The parametrization of these two numbers during and after ionizing radiation is explained in the following.

2.2.1 Parametrization of the number of positive charges trapped in the STI

During exposure to ionizing radiation with a constant dose rate D the number of holes getting trapped in the STI volume is proportional to the exposure time t with a proportionality constant $k_{\text{ox}}D$, where k_{ox} describes how many holes are trapped per dose unit. At the same time, the trapped holes have a life-time τ_{ox} in the traps, until they are free again and can move out of the STI. Therefore, the number of holes trapped in the STI is defined by the differential equation

$$\frac{d}{dt}N_{\text{ox}}(t) = k_{\text{ox}}D - \frac{1}{\tau_{\text{ox}}}N_{\text{ox}}(t) \quad (2.5)$$

which is solved by

$$N_{\text{ox}}(t) = k_{\text{ox}}D \cdot \tau_{\text{ox}} \cdot \left(1 - e^{-\frac{t}{\tau_{\text{ox}}}}\right). \quad (2.6)$$

If the irradiation stops after an exposure time t_1 , only the second term of equation (2.5) stays and results in an exponential decrease of the number of holes trapped in the STI, which is usually called annealing. This decrease can be described by

$$N_{\text{ox}}(t) = N_{\text{trap}} + (N_{\text{ox}}(t_1) - N_{\text{trap}}) \cdot e^{-\frac{t-t_1}{\tau_{\text{ox}}}} \quad (2.7)$$

where N_{trap} describes the number of holes captured in traps of the oxide which are too deep for detrapping at the given temperature.

2.2.2 Parametrization of the number of activated interface traps

The number of activated interface traps follows a very similar behavior, as motivated here. The holes travelling to the silicon to silicon dioxide interface and activating the radiation induced interface traps are generated again with a constant rate $k_{\text{if}}D$. k_{if} describes here the number of holes available to activate interface traps per dose unit. The number of interface traps that can be activated by the radiation is technology dependent and it is limited. Therefore the probability that the holes activate new interface traps decreases with time exponentially. This can be described equivalently using the analogue equation

$$N_{\text{if}}(t) = k_{\text{if}}D \cdot \tau_{\text{if}} \cdot \left(1 - e^{-\frac{t}{\tau_{\text{if}}}}\right). \quad (2.8)$$

The needed temperature to anneal the interface traps is known to be well above room temperature and even more above the operational temperature of the ASICs. It is technology dependent and in the range of 100 °C to 300 °C. Therefore, the annealing of the interface traps is negligible for the presented parametrization.

2.3 Summary of the parametrization

The complete formula for the leakage current during irradiation is therefore given by

$$I_{\text{leak}} = I_{\text{leak}}^0 \quad (2.9)$$

for

$$k_{\text{ox}}D \cdot \tau_{\text{ox}} \cdot \left(1 - e^{-\frac{t}{\tau_{\text{ox}}}}\right) - k_{\text{if}}D \cdot \tau_{\text{if}} \cdot \left(1 - e^{-\frac{t}{\tau_{\text{if}}}}\right) < N_{\text{thr}}$$

and by

$$I_{\text{leak}} = I_{\text{leak}}^0 + K \cdot \left[k_{\text{ox}}D \cdot \tau_{\text{ox}} \cdot \left(1 - e^{-\frac{t}{\tau_{\text{ox}}}}\right) - k_{\text{if}}D \cdot \tau_{\text{if}} \cdot \left(1 - e^{-\frac{t}{\tau_{\text{if}}}}\right) - N_{\text{thr}} \right]^2 \quad (2.10)$$

for

$$k_{\text{ox}}D \cdot \tau_{\text{ox}} \cdot \left(1 - e^{-\frac{t}{\tau_{\text{ox}}}}\right) - k_{\text{if}}D \cdot \tau_{\text{if}} \cdot \left(1 - e^{-\frac{t}{\tau_{\text{if}}}}\right) \geq N_{\text{thr}}.$$

During the periods with no incident ionizing radiation (dose rate $D = 0$) N_{ox} is similarly replaced by equation (2.7), and the number of activated interface traps N_{if} stays constant because they do not anneal at the considered temperature range.

Figure 4 presents the resulting leakage current increase as a function of time during an exposure to ionizing radiation with a constant dose rate. The exponential decrease step in the far right of

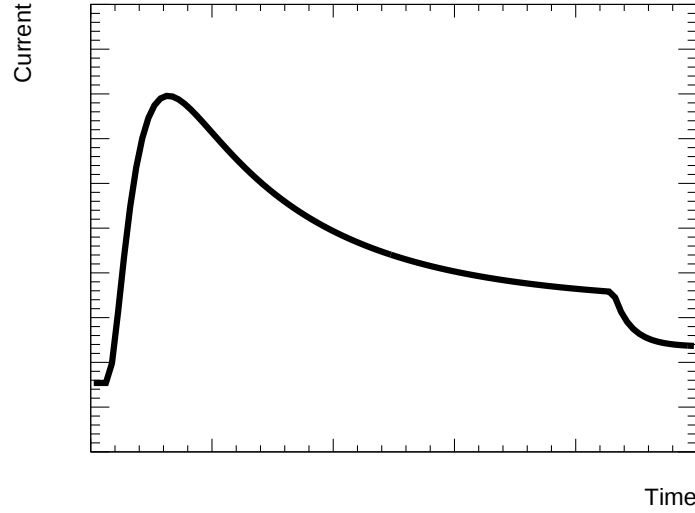


Figure 4. Plot of the leakage current parametrization as a function of the time, including the abrupt switch-off of the ionizing radiation, resulting in the exponential decrease.

the plot illustrates the annealing behavior when the radiation is switched-off. For many studies the leakage current is given as a function of the TID. The parametrization can be expressed during periods of constant intensity exposure using $TID = D \cdot t$.

The temperature dependency of the parameters is not explicitly included here. The generation of the positive space charge depends on the temperature. This can be modelled sufficiently well with a temperature dependent de-trapping probability, and neglecting the temperature dependence of the electron and hole mobility and generation [7, 11]. Then only τ_{ox} depends directly on the temperature. The generation of the interface traps is also expected to be a function of the temperature, but it is not well known. A dedicated measurement campaign is ongoing to provide the data that are needed for the extraction of the temperature dependence of these terms. As these data are not yet available, here the parametrization is used to describe the measured leakage current increase at a given temperature.

For the design of an ASIC using linear NMOS transistors affected by the described leakage current increase, three quantities are of major interest: the time (at a given dose rate) or the total dose at which the maximum occurs, the current at the maximum I_{max} or the maximum current increase $\Delta I_{max} = I_{max} - I_{leak}^0$, and the saturation current increase $\Delta I_{sat} = I_{sat} - I_{leak}^0$ after very long exposure. The time of the maximum can be obtained calculating the derivative of equation (2.10) and setting it to zero. The solution to this equation can not be solved analytically, and therefore it needs to be obtained numerically. The maximum current is then obtained from equation (2.10). The saturation current can be calculated easily from equation (2.10) using

$$\Delta I_{sat} = \lim_{t \rightarrow \infty} I_{leak} = K \cdot \left[k_{ox} D \cdot \tau_{ox} - k_{if} D \cdot \tau_{if} - N_{thr} \right]^2. \quad (2.11)$$

These three quantities can be extracted similarly for the supply current of a full ASIC. Then they are of major interest for the design of a system that uses the ASICs in an irradiation environment, as they need to be known to define several key design parameter of the system.

In the following two sections this parametrization is first fit to measured data of single NMOS transistors. Then the same function is used to describe the supply current shift of the ATLAS IBL pixel readout chip FE-I4 [12] as an example of the consequence of the leakage current shift for the ASIC operation in radiation intense environments. This is an example for the power of this parametrization to predict the ASIC supply current increase once the basic parameters are known for the given technology.

3 Fit to single transistor data

Equations (2.9) and (2.10) are used to describe the leakage current shift of single NMOS transistors produced in a 180nm silicon on insulator (SOI) process [13] by XFAB. The data have been published previously in [14] and [15]. The device was irradiated up to 700 Mrad at a dose rate D of 8 Mrad h⁻¹ and at a temperature of $\sim 25^\circ\text{C}$. The device leakage current is measured here as the source to drain current when the gate bias is equal to the drain potential ($V_{GS} = 0\text{ V}$). V_{DS} was 1.8 V (saturation mode) during the measurement. V_{BS} was as well 0 V. Because the proportionality factor K appears in the parametrization only in products with the other parameters, K was fixed to a value of $1 \times 10^{-19}\text{ A}$ per effective charge carrier. The threshold charge N_{thr} , the time constants τ_{ox} and τ_{if} , as well as the proportionality constants k_{ox} and k_{if} are free fit parameters. The measured data (black dots) and the interpolating function (green line) are shown in figure 5 to 7 and demonstrate the good agreement of data and parametrization on single transistor level.

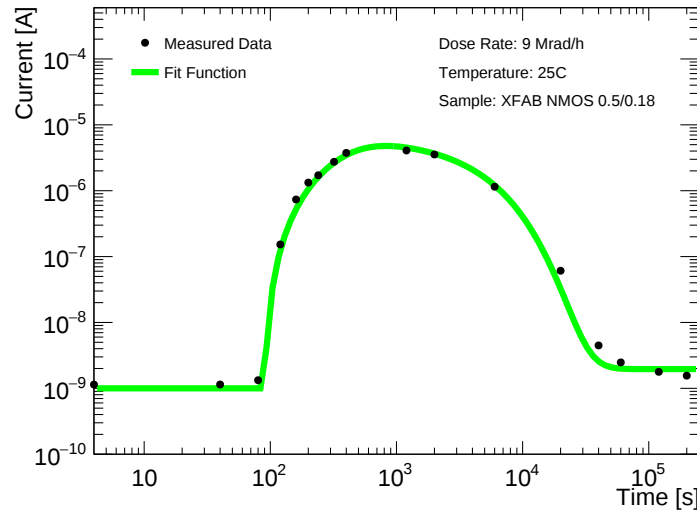


Figure 5. Fit of the leakage current parametrization as a function of the time to the leakage current measurement of a single NMOS transistor (width $0.5\ \mu\text{m}$, length $0.18\ \mu\text{m}$). A logarithmic y-axis is used to render the data to fit function agreement throughout the leakage current increase of four orders of magnitude.

Table 1 lists the coefficients of the parametrization after the fit to the data of the three single transistors. The given uncertainties are the fit parameter uncertainties as provided from the fit. The maximum current, the TID of the maximum current, and the saturation current after very long exposure are extracted from the model as described in section 2.3 and shown in table 2.

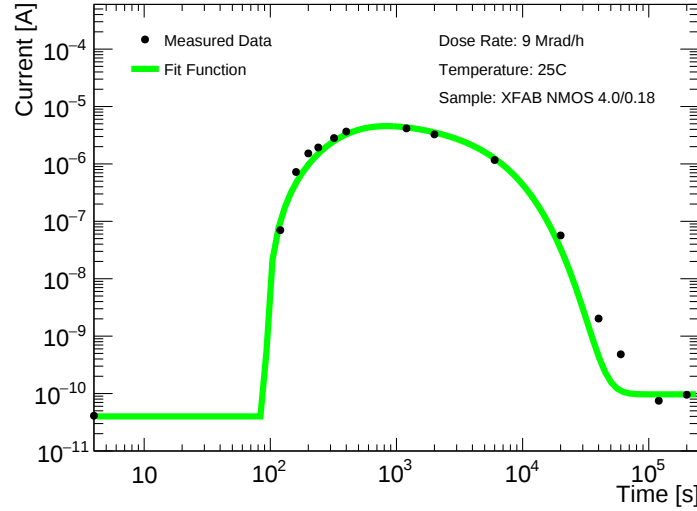


Figure 6. Fit of the leakage current parametrization as a function of the time to the leakage current measurement of a single NMOS transistor (width $4.0\ \mu\text{m}$, length $0.18\ \mu\text{m}$).

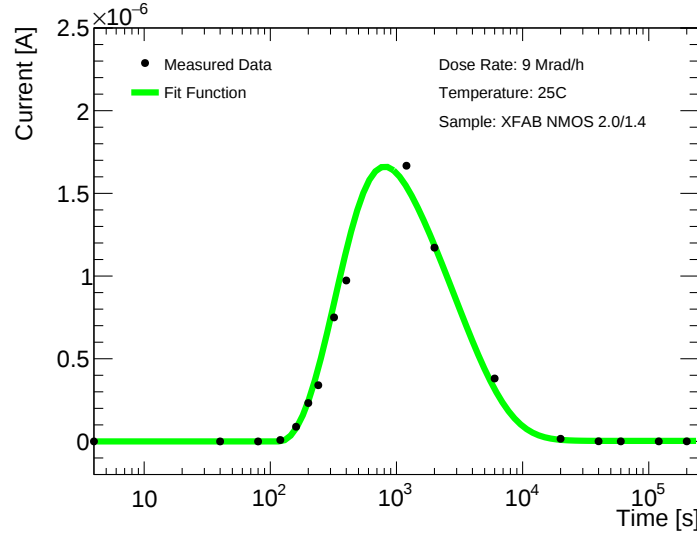


Figure 7. Fit of the leakage current parametrization as a function of the time to the leakage current measurement of a single NMOS transistor (width $2.0\ \mu\text{m}$, length $1.4\ \mu\text{m}$). A linear y-axis is used to illustrate the description of the data by the fit function at the peak values.

4 Fit to full ASIC supply current shift

ASICs composed of a large number of linear NMOS transistors can show a significant supply current shift when operated under ionizing radiation. This supply current shift is a serious challenge for the ASIC operation and impacts the design of the system, because the services need to be able to cope with this shift. The amplitude of the increase depends on the environmental conditions, such as dose rate and temperature. An intense investigation program is currently carried out on ATLAS FE-I4 readout chips. The ASIC, produced in IBM 130 nm technology, is composed of about 80 million transistors, and HBD techniques are not used for the large majority of the transistors. The ASIC is

Table 1. Coefficients of the model after the fit of function 2.9 and 2.10 to the data of linear transistors in XFAB 0.18 μm SOI technology.

$W[\mu\text{m}]/[L\mu\text{m}]$	N_{thr}
0.5/0.18	$1.579 \times 10^6 \pm 190$
4.0/0.18	$1.607 \times 10^6 \pm 213$
2.0/1.4	$1.402 \times 10^6 \pm 65$

$[W\mu\text{m}]/L[\mu\text{m}]$	$\tau_{\text{ox}}[\text{s}]$	$k_{\text{ox}}[\text{rad}^{-1}]$
0.5 / 0.18	200 ± 0.25	$9.02 \pm 3 \times 10^{-4}$
4.0 / 0.18	199 ± 0.38	$8.97 \pm 5 \times 10^{-4}$
2.0 / 1.4	196 ± 0.11	$6.50 \pm 5 \times 10^{-4}$

$[W\mu\text{m}]/[L\mu\text{m}]$	$\tau_{\text{if}}[\text{s}]$	$k_{\text{if}}[\text{rad}^{-1}]$
0.5 / 0.18	7060 ± 31	$0.164 \pm 3 \times 10^{-7}$
4.0 / 0.18	7602 ± 60	$0.149 \pm 4 \times 10^{-7}$
2.0 / 1.4	5610 ± 5	$0.122 \pm 2 \times 10^{-7}$

Table 2. Key quantities extracted from the model after the fit of function 2.9 and 2.10 to the measured leakage current increase of linear transistors in XFAB 0.18 μm SOI technology.

$[W\mu\text{m}]/[L\mu\text{m}]$	$TID_{\text{max}}[\text{Mrad}]$
0.5 / 0.18	2.06
4.0 / 0.18	2.09
2.0 / 1.4	2.02

$[W\mu\text{m}]/[L\mu\text{m}]$	$\Delta I_{\text{max}}[\text{A}]$	$\Delta I_{\text{sat}}[\text{A}]$
0.5 / 0.18	4.8×10^{-6}	1.5×10^{-10}
4.0 / 0.18	4.6×10^{-6}	6.4×10^{-9}
2.0 / 1.4	1.7×10^{-6}	2.1×10^{-11}

operated under controlled environmental conditions while being exposed to X-ray radiation. The supply voltage for the large majority of transistors is the digital supply voltage, which was set to 1.2 V (analog supply voltage 1.4 V), and the ASIC is kept active running calibration procedures. The supply current is measured as a function of the exposure time. This measurement is carried out for various dose rates and temperatures. Some preliminary results are public [16] and used here to demonstrate the ability of the parametrization to describe the supply current shift of full ASICs.

Figure 8 shows the fit to the supply current of the ASIC as a function of the exposure time using 120 krad h^{-1} dose rate at 38°C . The same parameters as in section 3 are free during the fit, while K is fixed now to $1 \times 10^{-12} \text{ A}$ per effective charge in order to account for that the supply current is the convolution of the leakage current of about several ten millions of transistors. Additionally, the pre-irradiation supply current is added as offset. At the time $t_1 = 215\,500 \text{ s}$ a TID of 7.2 Mrad is reached and the irradiation was switched-off and the annealing as described in equation (2.7) is shown. The parameters are fit to the time interval 0 to t_1 only. For the annealing the same parameters are used, especially the same time constant τ_{ox} . This reflects that the annealing is caused by the same process as the saturation of the number of positive charges trapped in the oxide during irradiation.

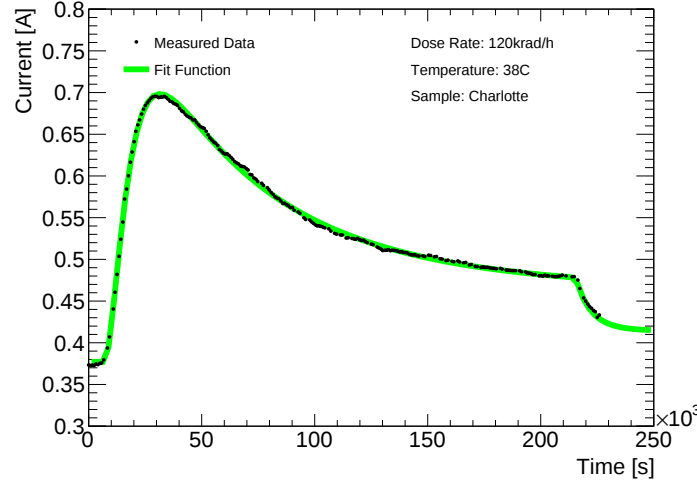


Figure 8. Fit of the leakage current parametrization as a function of the time to the supply current measurement of an ATLAS FE-I4 readout-chip. At a the time $t_1 = 215\,500\text{ s}$ (TID = 7.2 Mrad) the dose rate is switched-off, and the annealing starts.

Figure 9 shows the same fit to data taken at different temperature (15 °C). A slightly higher amplitude of the increase is observed, as expected due to the longer lifetime τ_{ox} of the positive charges in the traps.

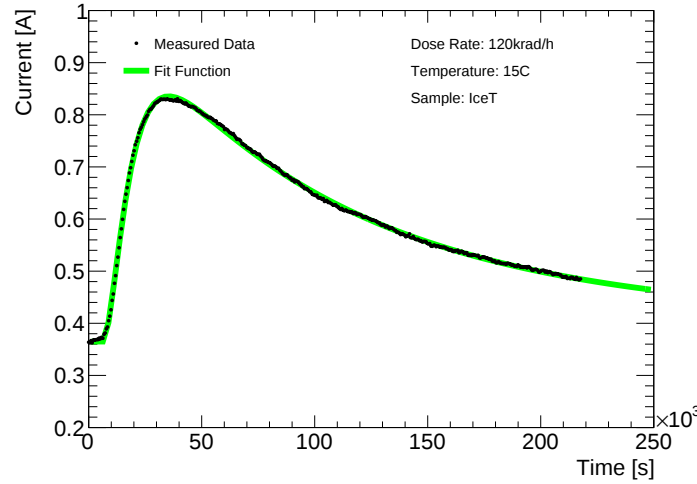


Figure 9. Fit of the leakage current parametrization as a function of the time to the supply current measurement of an ATLAS FE-I4 readout-chip.

The data shown in figure 10 are taken again at 15 °C, but using a higher dose rate of 420 krad h^{-1} . The current maximum is significantly higher due to the larger dose rate.

Table 3 provides the extracted coefficients after the fit to the measured supply current of the FE-I4 readout-chip. The given uncertainties are the fit parameter uncertainties given by the fit. The large uncertainty of τ_{if} for the sample irradiated at a dose rate of 420 krad is a consequence of the measurement of the first part of the peak only. The data after long exposure, which are important for the extraction of τ_{if} , are not measured on this sample. Table 4 shows the extracted key quantities current increase as extracted from the model.

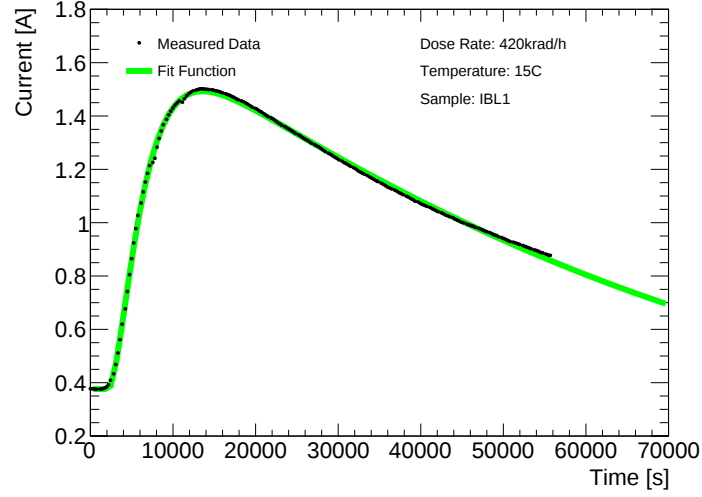


Figure 10. Fit of the leakage current parametrization as a function of the time to the supply current measurement of an ATLAS FE-I4 readout-chip.

Table 3. Coefficients of the model after the fit of function 2.9 and 2.10 to the supply current increase of a full integrated circuit.

$T[^\circ\text{C}]/D [\text{krad h}^{-1}]$	N_{thr}
38 / 120	$354 \times 10^3 \pm 52 \times 10^3$
15 / 120	$310 \times 10^3 \pm 9 \times 10^3$
15 / 420	$437 \times 10^3 \pm 0.3 \times 10^3$

$T[^\circ\text{C}]/D [\text{krad h}^{-1}]$	$\tau_{\text{ox}}[\text{s}]$	$k_{\text{ox}}[\text{rad}^{-1}]$
38 / 120	8055 ± 139	2.37 ± 0.09
15 / 120	8770 ± 67	2.13 ± 0.03
15 / 420	3062 ± 1.5	8.66 ± 0.01

$T[^\circ\text{C}]/D [\text{krad h}^{-1}]$	$\tau_{\text{if}}[\text{s}]$	$k_{\text{if}}[\text{rad}^{-1}]$
38 / 120	$71\,540 \pm 1347$	0.074 ± 0.002
15 / 120	$158\,038 \pm 2521$	0.047 ± 0.001
15 / 420	$3 \times 10^6 \pm 2 \times 10^7$	0.103 ± 0.001

The exact dependencies of the fit parameters and of the extracted quantities from the temperature and from the dose rate are currently under investigation. The good agreement between the parametrization and the data demonstrate the capability of the proposed model to predict the supply current increase during operation in radiation environment, once the basic parameters have been measured for the ASIC in the laboratory.

5 Conclusions

The presented parametrization of the leakage current of NMOS transistors uses simplified transfer characteristics of the *parasitic* source to drain transistor along the STI. The function resulting from

Table 4. Key quantities extracted from the model after the fit of function 2.9 and 2.10 to the supply current increase of a full integrated circuit.

$T[^\circ\text{C}]/D$	krad h^{-1}	$TID_{\text{max}}[\text{Mrad}]$
38 / 120		1.05
15 / 120		1.18
15 / 420		0.45

$T[^\circ\text{C}]/D$	krad h^{-1}	$\Delta I_{\text{max}}[\text{A}]$	$\Delta I_{\text{sat}}[\text{A}]$
38 / 120		0.321	0.111
15 / 120		0.470	0.111
15 / 420		1.117	0.111

the proposed parametrization is in good agreement with measured data. Therefore, the gate potential of the radiation induced parasitic transistors can be described by the effective number of charges. Similarly, the threshold voltage of the radiation induced parasitic transistors can be described by the threshold charge. Together with the concentration of the charges parametrized as a function of the exposure time, the proposed model describes the observed leakage current increase of linear transistors.

Furthermore, the parametrization can directly be used to predict the supply current increase of full ASICs in radiation environment, when HBD techniques are not used for the majority of transistors, once the parameters are known as a function of dose rate and temperature.

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