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The CERN NA62 experiment: Trigger and Data Acquisition

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The main goal of the NA62 experiment at CERN is to measure the Branching Ratio (BR) of the ultra-rare decay of a charged kaon into a charged pion and two neutrinos ($K^+ \to \pi^+ \nu\overline{\nu}$). The experiment aims to collect about 100 events in two years of data taking and to test the Standard Model of Particle Physics (SM), using a secondary hadron beam obtained by the SPS accelerator. The key issues for the Trigger and Data Acquisition system (TDAQ) are readout uniformity of sub-detectors, scalability, efficient online selection and lossless high-rate readout. The TDCB and the TEL62 boards are the common blocks of the fully digital TDAQ and they will be used for several sub-detectors in this high-flux rare decay experiment. TDCBs measure hit times for sub-detectors, TEL62s process and store them in a buffer, extracting only those requested by the trigger system, which merges trigger primitives also produced by TEL62s. The complete dataflow and firmware organization are described.

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1. The NA62 experiment

1.1 introduction

The NA62 experiment is located in the CERN North Area SPS extraction site and it aims at measuring the Branching Ratio of the ultra-rare FCNC kaon decay $K^+ \to \pi^+ \nu\overline{\nu}$ collecting about 100 events in two years of data taking [1]. This decay, with its neutral partner $K_L \to \pi^0 \nu\overline{\nu}$, is a very useful process to study flavour physics and to obtain a stringent test of the Standard Model; the Branching Ratio of these decays can be computed with high precision [2],$BR(K^+ \to \pi^+ \nu\overline{\nu})(SM) = (7.81^{+0.80}_{-0.71} \pm 0.29) \times 10^{-11}$ where the uncertainty is dominated by the current precision of the CKM mixing matrix input parameters.

The strong suppression of the SM contributions and the remarkable theoretical precision of the SM rate make this decay a powerful probe for possible new physics, complementary to direct searches at the LHC and potentially sensitive to much higher energy scales. The combination of the Branching Ratio of these two decays ($K^+ \to \pi^+ \nu\overline{\nu}$ and $K^0 \to \pi^0 \nu\overline{\nu}$) allows to determine the β angle of the Unitarity Triangle from K decays only and, in this way, to have a powerful test on Standard Model.

The most accurate measurement of this decay, $BR(K^+ \to \pi^+ \nu\overline{\nu}) = 17.3^{+11.5}_{-10.5} \times 10^{-11}$, was obtained by the E787 experiment and its upgrade E949 at BNL (from 1995 to 2002) which collected seven events [3]. NA62 aims to improving the measurement of this Branching Ratio reaching a precision of at least 10%: the experiment is currently in its final installation phase, with the first commissioning run scheduled for fall 2014.

Assuming a signal acceptance of about 10% and a branching ratio of the order of 10^{-10}, 10^{13} kaon decays are required. To achieve the signal over background ratio of 10/1 a rejection factor of 10^{12} is needed, coming both from particle vetoing and particle identification, and from kinematics, together with the possibility to measure efficiencies and background suppression factors directly from data.

1.2 NA62 Experimental Setup

NA62 will use the SPS 400 GeV/c proton beam from the SPS in order to produce K^+ decaying in-flight.

The total beam rate at the end of the beam line is of the order of 750 MHz but kaons are about 6% of the flux. Downstream detectors aren't affected by this large flux because the undecayed particles remain inside the beam pipe; the integrated rate over these detectors is of the order of 10 MHz.

The downstream detectors start about 100 m after the beryllium target and are distributed along 170 m longitudinally; the fiducial region for decays extends from 100 m to 165 m after the target. Detectors have an approximate azimuthal symmetry around the beam axis, with an inner hole to let the high flux of undecayed particles pass through without hitting the downstream detectors.

The NA62 experimental setup [4], shown in figure 1, consists of these detectors:

- The *Cerenkov Differential counter with Achromatic Ring focus* (CEDAR) is used to identify K^+ in the beam. It has a time resolution of about 100 ps to tag the kaon time.

- The Gigatracker (GTK) is composed by three silicon pixel stations placed in vacuum, with transverse (x and y) dimensions which cover the beam area, and is used to measure particles direction and momentum before they enter the decay region. The GTK has to cope with the full beam intensity of about 750 MHz and must provide a time resolution of the order 200 ps to avoid a wrong matching of a beam particle to the reconstructed decay downstream, and a resulting error in the calculation of the missing mass. Between the stations, 4 magnetic dipoles make an achromatic spectrometer for any momentum: the momentum resolution is 0.2%, and the angular resolution for the particle direction is about 15 μrad.
- The CHarged ANTIcounter (CHANTI) is a set of scintillator rings that follow the last GTK station used as a veto for charged particles before they enter the decay region.
- A system of photon veto detectors covering a polar angle from 0 to about 50 mrad polar angle with respect to the beam direction using 12 large annular vetos (LAV) made of lead glass crystals with attached photomultipliers (PMT) and covering an angle from 8.5 to 50 mrad, a liquid krypton electromagnetic calorimeter (LKr) for angles between 1 and 8.5 mrad, an intermediate calorimeter (IRC), made of alternating layers of lead and scintillators (shashlik), to cover the ring around the beam and a small angle calorimeter (SAC) placed at the end of the beam line after a sweeping magnet and using the same shashlik technology.
- A magnetic spectrometer (STRAW) made of four straw tube chambers inside the vacuum tank is used to measure the position of the decay vertex, the direction and momentum of the charged secondary particle. The reason to operate in vacuum is to minimize the multiple scattering. The dipole magnet from the earlier NA48 experiment is located after the second chamber and provides a 270 MeV/c kick in the horizontal plane, for track momentum determination. In the center of each chamber it's present a region without straw to let the beam particles pass undisturbed.
- The Ring Imaging Cerenkov (RICH) is designed to distinguish π and μ in the momentum range between 15 and 35 GeV/c and to measure direction and velocity of such particles. This detector is 17 m long, filled with Neon at atmospheric pressure and equipped with 2000 photomultipliers and has an inner beam pipe to avoid beam interactions with the gas. The timing resolution is of the order of 100 ps.
- The Charged Hodoscope (CHOD) is placed after the RICH to reduce the inefficiency in photon detection due to conversion or photo-nuclear interactions inside the material of the RICH, moreover it is used for trigger purposes.
- A system of muon vetoes composed of two iron-scintillator hadronic calorimeters (MUV1 and MUV2), and a plane of fast scintillators (MUV3) placed after an iron wall, gives additional power in muon vetoing and a fast trigger information.

2. The Trigger and Data Acquisition system

The intense beam flux of the experiment requires a high performance trigger and data acquisition (TDAQ) system, which must minimise dead time and random veto, and maximise the effi-

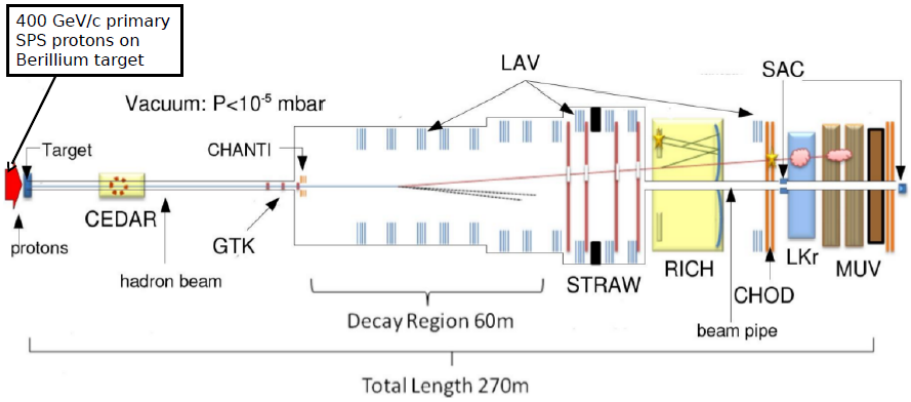

Figure 1: Longitudinal view of the NA62 experimental setup.

ciency in data collection at high rates; indeed it is an important issue to have a very low undetected DAQ inefficiency, below 10^{-8}. The low inefficiency, joined with a kinematics rejection factor $O(10^4)$, allows to achieve a background rejection of 10^{12} essential to obtain a signal to background ratio $S/B \simeq 10$. NA62 has a unified trigger and data acquisition system: trigger is integrated inside the DAQ system allowing to have a better control of the trigger, that use the same data available at readout, and a higher flexibility.

The timing of the experiment is provided by the Timing, Trigger and Control (TTC) system used in LHC experiments [5], its 40 MHz clock is the common reference for all time measurements. The time scale is defined by a 32-bit timestamp, with 25 ns LSB, that covers the duration of an entire accelerator spill, plus 8 bit of fine time with 100 ps LSB.

The NA62 trigger system is composed of 3 levels that must reduce the event rate from 10 MHz to some kHz. The rates and the number of channels of the experiment (12 sub-detectors, about 80000 channels, 25 GB/s of raw data) have driven the choice of NA62 for a hardware lowest-level trigger (called L0); after the L0 trigger, the sub-detectors transfer the data to a farm of PCs, where the software trigger levels L1 and L2 are implemented. The L1 is based on the information computed by each complete sub-system. The L2 uses an assembled and partially reconstructed event with the possibility to use correlations between different sub-detectors. A schematic view of NA62 trigger hierarchy can be seen in figure 2.

The L0 will be implemented in the common TEL62 board (see section 2.1) and will be used to reduce total rate to below 1 MHz using information coming from fast detectors: the charged hodoscope (CHOD) and the RICH as positive elements, the muon veto (MUV) and the photon vetoes (LKr, LAV) as negative ones. It will also be possible to implement secondary triggers for control samples and different physics goals, such as the search for other rare or forbidden decays of the K^+ and the π^0. Data from all sub-detectors will be stored in buffers during L0 trigger evaluation, for a time up to the defined maximum L0 trigger latency of 1 ms. The unusually long latency was chosen to possibly allow complex operations, even using GPUs. The L1 algorithms will check data quality conditions and then require simple correlations between conditions computed by single sub-detectors, reducing the rate under 100 KHz. In case of positive L1 decision, a complete event reconstruction at L2 will be done. Then all data satisfying the L2 trigger condition will be finally

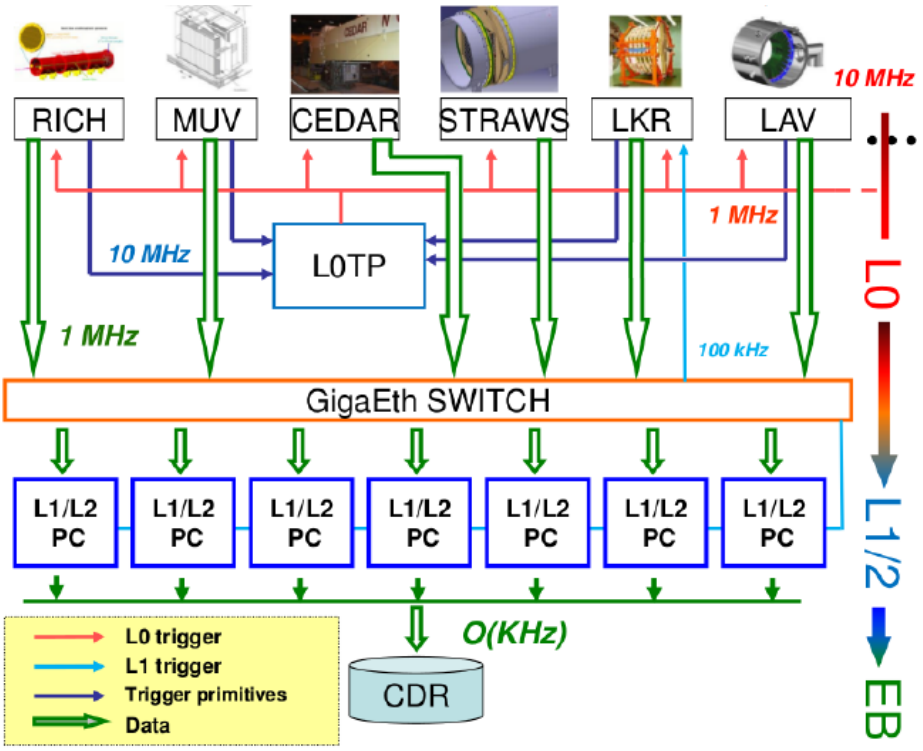

Figure 2: Schematic view of NA62 TDAQ system

logged to tape with a rate of about 10 KHz.

2.1 The TEL62 Board

The TEL62 board (see figure 3) is the common FPGA-based motherboard for trigger generation and data acquisition of the NA62 experiment. It has been developed at INFN Pisa, and represents a major upgrade of the TELL1 board designed by EPFL Lausanne for the LHCb experiment at CERN [6]. The overall architecture of the TEL62 is similar to the TELL1's, but the board is based on much more powerful and modern devices, resulting in 8 times the computing power, about 20 times the buffer memory and an improved connectivity.

The board is a 9U Eurocard standard and the printed circuit is made of 16 layers, with all lines controlled in impedance (50 ohm). Special care has been used for the routing of the clock tree, to avoid signal jitter.

The board is composed of the following parts:

- 4 PP-FPGAs (Altera Stratix III FPGAs EP3SL200F1152) each one to pre-process and to handle the data from one digitizing mezzanine daughter-card like TDCB (see section 2.2); the daughter-card, such as the TDCB, is connected through a 200-pin connector (4 X 32 bit at 40 MHz data buses). Each PP-FPGA is also connected to a 2-GByte DDR2 memory buffer (64 bit at 640 MHz);

- 1 central SL-FPGA (Altera Stratix III FPGA EP3SL200F1152), connected to all the PPs through two independent 32 bit buses at 160 MHz (5 Gb/s per PP) for data and trigger flow,

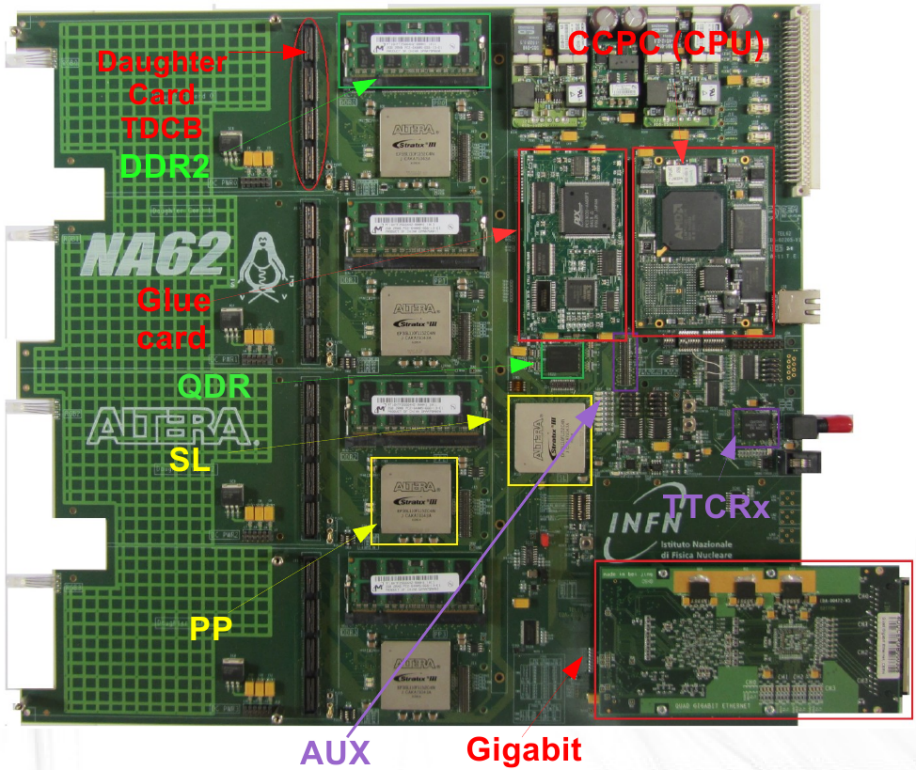

Figure 3: TEL62 motherboard.

and connected also to the output mezzanine GbE; a 1Mb QDR RAM is used as temporary buffer;

- 1 custom Quad-GbE mezzanine as output board (same as on the TELL1), equipped with 4 X 1 Gbit Ethernet channels, used to connect the TEL62 to the L0 Trigger Processor (L0TP), to other TEL62s in daisy chain, or to send the main data flow to the PC farm;
- a commercial Credit-Card PC (CCPC) and a custom interface card (Glue), identical to those on the TELL1 board, are two mezzanine cards used to handle the slow control of the board. The Glue card is connected to the CCPC through a PCI bus and it uses three communication protocols distributed to all devices and connectors: JTAG, I2C (mainly used for slow communication with TDCB daughter-cards), and ECS (a parallel bus to access FPGA internal registers);
- an auxiliary connector (AUX) meant to be used for custom interconnection of TEL62 boards (2 independent 16 bit buses);
- clock and L0 trigger are distributed through a standard optical TTC link, a CERN-developed optical time-multiplexed connection which distributes the main 40 MHz clock with trigger and timing signals encoded in it; a TTCrx chip is used to decode this information([7]).

The data coming from the 4 TDCs of each daughter-card are collected and merged into one single buffer by the corresponding PP, for each 6.4 µs long data frame. Merged data is triplicated in

Figure 4: TDCB.

different streams to feed three parts of the firmware: one for monitoring purposes, one for trigger primitives generation, one for data storage inside the DDR2 buffer. The SL sends to each PP the timestamped trigger requests, and as a consequence the data corresponding to a programmable number of 25 ns time slots around the trigger time are extracted from the DDR2 and transferred to the SL. The PP also continuously sends the generated sub-detector primitives to the SL. The SL firmware merges the data coming from the 4 PPs for each L0 request to build an event fragment and stores it into the temporary QDR buffer. Event fragments are read and assembled into a multiple-event packet in UDP format and then sent through the GbE to the PC farm. A similar part of the firmware handles, merges and transmits the trigger primitive information coming from the PPs through the GbE to the L0TP.

2.2 The TDC Board

The TDC board (TDCB, see figure 4) is a custom 10-layer daughter-card for the TEL62 developed in Pisa for the high resolution time and time-over-threshold measurements. Up to 4 TDCBs can be housed on a TEL62, each one connected through the 200-pin connector. The board includes 4 High Performance Time to Digital Converter (HPTDC) developed at CERN, each one giving 19 bit leading time and time over threshold measurements with 98 ps LSB for 32 LVDS input channels, thus allow the readout of 512 LVDS input channels per motherboard.

In standard configuration the TDCs produce two 32 bit-long words for each LVDS signal in each channel, one word for the time of the leading edge of the pulse and one for its trailing edge. The data are then buffered before being read periodically by the on-board TDCC-FPGA (1 Altera Cyclone III FPGA EP3C120F780), which adds a time-stamp and a counter to the data stream and addresses it to the TEL62.

Several other features are implemented in the TDCB firmware, including a TDC data simulator for testing purposes, the possibility of triggering front-end board calibration signals through an output line and the controller for two on-board 1 MB SRAM memories usable for monitoring or online processing.

A QPLL (the clock jitter reduction is under 40 ps) is included to avoid compromising the time resolution of the measurements.

2.3 The L0 Trigger Distribution

TEL62 produces L0 trigger primitives at firmware level directly from data and if certain logical conditions are fulfilled, the primitive is sent to the central L0 Trigger Processor.

The L0 Trigger Processor (L0TP) merges in time the information from all the trigger primitives arriving from several subdetectors and sends trigger decisions back. L0 triggers are dispatched to sub-detectors by the L0TP through the TTC system.

Two options for the for the L0 Trigger Processor are being developed: one implementation is fully FPGA-based while the other is a FPGA-PC hybrid.

L0TP sends the triggers to LTU (Local Trigger Unit), a slightly modified version of the ALICE LTU [8] developed in Birmingham, which act as transparent dispatchers of L0 triggers to the TTCex modules, built by CERN PH/ESE, which encode the clock and trigger signals onto optical fibres and send them to the TTCrx of the TEL62 using up to 10 optical outputs. LTU also receives CHOKE and ERROR backpressure signals from detectors and propagates them to the L0 Trigger Processor.

2.4 Other System

The LKr calorimeter, the GTK and the STRAW Tracker developed three special digitising and readout systems.

The readout system of the liquid Krypton Calorimeter (LKr) is based on the Calorimeter Readout Module (CREAM), a VME 6U board able to digitise 32 LKr channels at 40 MHz using four 8-channel, 14-bit ADCs. 432 such boards will be needed to readout the 13248 calorimeter cells. After the signal digitisation, samples are stored in a circular buffer built inside a DDR3 module, waiting the L0TP signal. Upon its reception through a custom VME backplane, data is moved to the L0 buffer, also built in the DDR3 module, where it waits for a L1 signal, since due to the high data rate, this detector is only readout at the reduced L1 trigger rate. When such signal is received, the corresponding data is sent to the PC farm as UDP packets. The module also computes digital sums of 4x4 channels for trigger purposes: two such sums are sent by each CREAM every 25 ns to a system based on 36 TEL62 and custom interface mezzanine boards, where LKr L0 trigger primitives, based on energy deposits and cluster identification, are generated.

The Gigatracker system is composed by 54K TDC pixel channels silicon detectors disposed over 3 stations. The readout, for each station, is composed by 10 Giga Tracker AISCs (GTK-ASIC) whose output data flows continuously toward the GTK off-detector readout (GTK-RO) cards. These cards provide temporary data storage until the L0 trigger decision, upon which the GTK-RO cards extract trigger matched data from the on-board memory buffers and transmit the data to the sub-detector PCs through Gigabit Ethernet links. The GTK-RO design is actually made of two decked units: the mother board, hosting the main functional blocks, and a daughter card featuring TTC interface block and various timing functions necessary to the operation of the connected ASIC chips.

The STRAW Tracker front-end electronics is based on CARIOCA chip [9], installed on a custom board (COVER) that is also part of the gas manifold. The signals from straw tubes are collected on one end by means of a flexible circuit, which hosts high voltage resistors and decoupling capacitors. The Straw Readout board (SRB), a custom 9U VME board, provides the control and data flow for 16 COVERs.

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