A Fast and Simple Trigger for High Energy Cosmics

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Abstract

A massive parallel trigger system for efficient data reduction and event recognition is under design for the 14400 channels of the AUGER fluorescence detector. The trigger is combined with a cost-effective control and readout by PCI devices. The first level trigger includes a count-rate dependent trigger-threshold and suppresses Cerenkov pulses, and the second level trigger will identify straight tracks of cosmics in the AUGER fluorescence detector. Configurable FPGAs are used to enable parallel processing and yields a cheap high-speed data handling solution. Furthermore, the use of one PCI-board type for the readout allows a very cost-effective solution for the overall system. By digital pulse-shape recognition more than 90 % of the Cerenkov pulses will be suppressed. Due to fast hardware event-pattern recognition of three adjacent pixels within the detector we expect an excellent noise reduction of about $3 \cdot 10^5$.

1. INTRODUCTION

We are developing a trigger-system for the Fluorescence Detector (FD) proposed for the PIERRE AUGER Project [1]. The FD works in correlation with the Cerenkov ground detector array [4] to be installed. The FD identifies unambiguously the energy of cosmics with energies more than 10^{18} eV and the source(s) of emission by the angular distribution of these events. The detector is looking with three eyes for the fluorescence light produced by cosmic particles in the night sky. Three eyes are necessary to allow 3-dimensional reconstruction of tracks. An eye consists of a pixel camera with 4800 photomultipliers (PMT). Each pixel covers a cone of 1.5 degrees in the sky. Straight tracks of cosmics have to be identified in the presence of a high level of background noise (200 Hz) for each pixel, starlight and Cerenkov events. The actual design consists of 100 PMTs per sub-mirror, four sub-mirrors per mirror system and 12 mirror systems per eye (see fig. 1). For the identification and reconstruction of cosmics with very high energy a continuous film of the signals at each PMT has to be taken with a minimum digitization rate of 10 MHz.

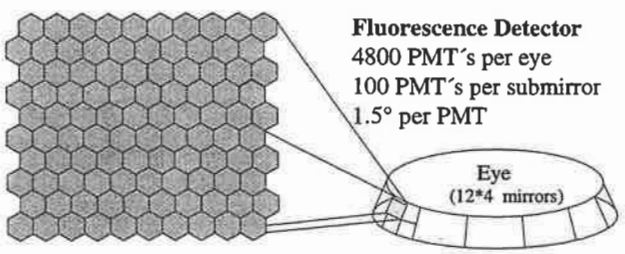

Figure 1: Schematic view of one eye of the fluorescence detector

Because of the overall involved number of readout channels the system costs and power consumption are important factors for the design. Low power consumption will be implemented as far as possible by using 3.3 V technology. At the same time low power consumption spares money for active cooling and helps to keep temperatures of components as low as possible, necessary for an experiment with a long lifespan (= 20 years). On the other hand the symmetry of the system facilitates low costs. The number of different boards to be developed is low. The main task for the trigger is fast data reduction and therein minimizing the amount of necessary buffer storage and readout speed.

2. SYSTEM CONCEPTS

This paper concentrates on the optimization of the system under cost constraints while a former paper [5] concentrates on the methods to suppress background. The costs of the electronics for the AUGER fluorescence detector will be mainly influenced by four factors:

1. physically necessary dynamic range of the ADC-system,
2. trigger and necessary memory buffer to guarantee data integrity,
3. gain control by high voltage at PMTs or with programmable gain at preamplifiers, and
4. readout system.

These topics will be discussed in the following sections.

2.1 Dynamic Range of Fluorescence Signals

The high dynamic range of the fluorescence signals (10^4 to 10^5 or 14 to 16 bit) and on the other hand the necessary low relative resolution of 6 to 7 bits lead to two 10 or 12 bit ADCs or three 8 bit ADCs as the most economic solution for the digitization. An amplifier with a non-linear characteristic would be another smart solution. But the necessary precise calibration and temperature stabilisation is a difficult problem in the rough, non-temperature stable environment of FD electronics. Digital solutions with ADCs delivering constant relative resolution (5 bit mantissa and 3 bit exponent) are under test for CMS [2], but have an unacceptable high power consumption (1.3 W/channel) and insufficient number of bits for our application. We chose two 12 bit ADCs.

2.2 *Optimum Buffer Memory Size*

The necessary size of the buffer memory, the speed of the readout, and the quality of the trigger are strongly correlated. For a positive trigger of each contributing PMT a film of 100 µs with time slices of 100ns resolution has to be taken. The trigger rate for each PMT will be limited to 100 - 200 Hz after first level trigger. By optimization of the trigger (see next chapter) the size of the buffer memory was limited to eight 1k*16bit ring buffers. An organisation of this buffer in one dual port memory of 8 pages with a 1k*16bit page size will give also a space optimized solution. A faster SRAM of the same size but used at both slopes of the 10MHz system clock will give a space and cost-effective solution for this problem.

2.3 *Gain Control of Each PMT Channel*

The gain of each PMT channel may be controlled by the high voltage at the PMT or by a digitally adjustable gain at the preamplifier. A multiplying DAC or a programmable amplifier is today state-of-the-art and may be cheaper than an individual programmable high voltage supply. We will study this line in the design. Furthermore a low gain PMT with only 6 or fewer dynodes has a lower gain spread than a multi-dynode PMT at the same gain, because the tube with a lower number of dynodes has to be driven nearer to saturation. That gives in addition a good single electron resolution.

Also the lifetime of the PMTs in such a large dark current environment is an important limitation for the design. Conservative estimates of the lifetime of PMTs are given by a maximum drawn charge in the range of 300 – 1000 C [3]. With a low gain tube, gain 1 – $5 \cdot 10^4$ we won't reach ageing limits within 20 years, the possible lifetime of the AUGER experiment. For a background of 3 pe/100ns, gain $5 \cdot 10^4$, 20 years of operation, only at night time (at 1/3 of the day) the collected charge will be of the order of 50 C. That gives enough safety, even if we include stars of 2nd order of magnitude in the sight of the PMTs. We would get an additional factor of 2.65 higher charge collection, safely within the range of 300 C.

Following this simple overall concept we may use a very cheap collective HV-systems for each mirror system.

2.4 *Selection of Readout System*

Due to the geometrical organisation of the detector, see fig. 1, one data concentrator is necessary in each of the mirror systems. To obtain a good price-performance ratio we select a simple industry PC. In our conception a single industry PC controls one mirror system consisting of 4 sub-mirrors with 4 • 100 PMTs guaranteeing a profitable and flexible control design (< 1000$). This PC

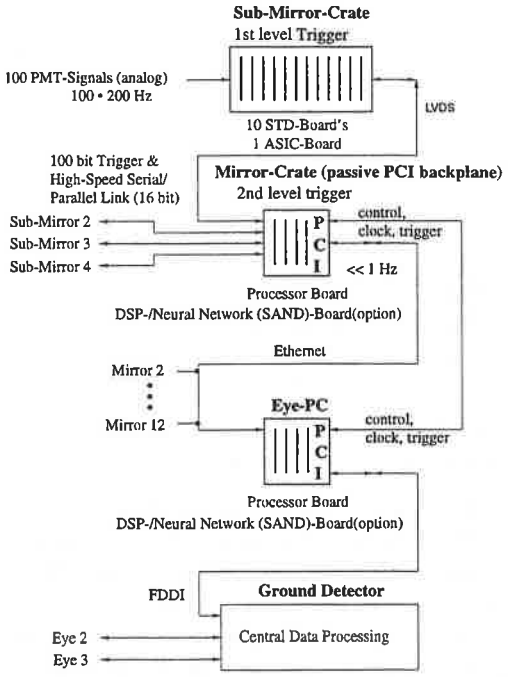

Figure 2: Readout scheme for FD of AUGER.

is connected via PCI bus to a passive PCI back plane with the locally installed sub-mirror electronics, designed for 100 PMTs as shown in fig. 2 and 3. The front-end system is a proprietary 6U Euroboard system. The mirror systems are not equipped with a disk to guarantee better long term stability, but contain 256 Mbyte of memory to allow comfortable operation and to provide sufficient buffer space. The CPUs are equipped with passive cooling instead of fan units to yield a longer mean time between failures.

With the developed trigger the data rate per eye will be lower than 1 Mbit/s. Due to this fact it is sufficient to

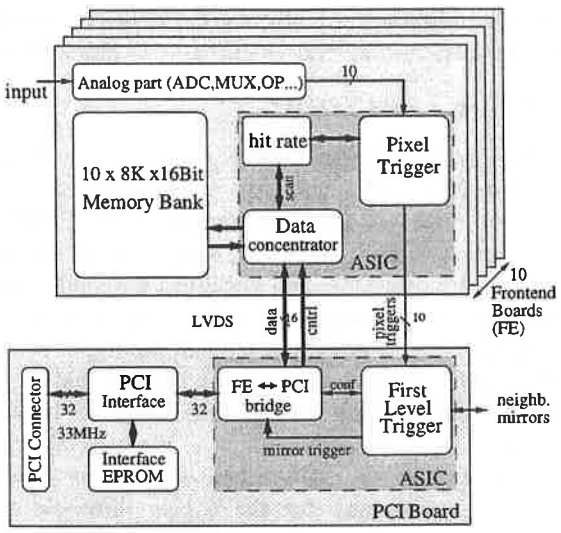

Figure 3: Structure of 1st and 2nd level trigger boards.

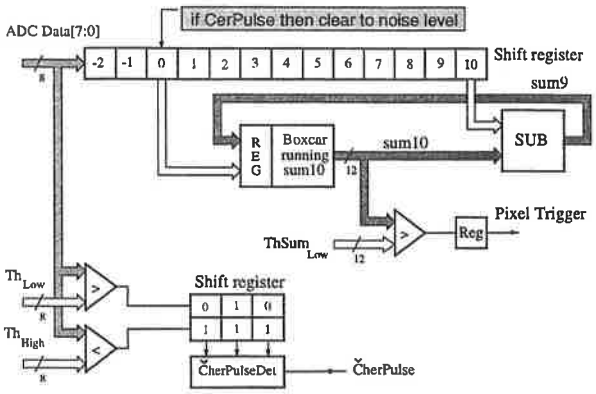

Figure 4: 1st level trigger: boxcar running sum and Cerenkov pattern recognition.

connect the PCs of one eye by Ethernet. The mirror client PCs boot from the eye server, which is equipped with a disk system. The operating system will be LINUX because of its fast context switching speed and low costs. Currently a PC system with two clients is under test to learn the software problems and the performance of the overall system. For the connection to central computing of the ground detector a mono mode fibre FDDI has to be provided because of the long distance (≥ 20 km). Furthermore, the triggers of the eyes have to be correlated with the trigger of the ground detector at the central computing station.

If the Cerenkov suppression is not sufficient, we leave a free PCI-slots on the mirror level to install a very fast neural network board [6], which is capable to handle our size of input patterns of 400 pixels, as given by the mirror size. The board is equipped with four SAND/1-chips and has a processing power of $8 \cdot 10^8$ connections per second.

3. TRIGGER

In the following we describe the front-end electronics and the first- and second-level trigger in more detail.

3.1 First Level Trigger

Ten channels of PMTs are digitized and pre-processed on one front-end board. By integrating the 1st level trigger of these ten channels into one single FPGA (field programmable gate array) we have reduced the amount of analogue electronic and improved the modularity and flexibility of the design. This FPGA contains the digital integration and Cerenkov detection, see fig. 4. After a 10 MHz ADC on each photomultiplier channel a sliding boxcar running sum for 10 time slices is inserted to improve the noise performance of the adaptable trigger threshold. Due to the tenfold digital summation the signal to noise ratio for the trigger threshold can be improved by a factor $\sqrt{10}$ without losses in the time resolution given by the 100ns conversion time of the ADC's. The chosen Altera FPGA has enough free space left for reprogramming to a larger integration time (eg. 2 μs) to improve signal noise ratio further if it is necessary.

The threshold ThSum in fig. 4 is controlled by the trigger rate. The trigger rate is prescaled on the same FPGA in a hit-rate counter and then readout and accumulated via PCI in the mirror PC. For larger deviations from the standard value (100-200Hz) the PC will correct the threshold to avoid insensitivity or high noise rates.

Parallel to the integrator a finite-state-machine (FSM) rejects fast Cerenkov pulses with 90 to 95 % probability. Cerenkov pulses are recognized by their short duration and high charge in one 100 ns trigger slice. This signature results in most cases in a 010 trigger pattern at consecutive time slices discriminated with sufficient high digital thresholds, see fig. 4. If a Cerenkov pulse is detected, the ADC data will be cleared to the actual value of the noise level. Due to this provision the sum-energy trigger is corrected. Two additional registers (-2,-1) in the sum-energy pipeline correct for the time delay of this decision.

Together with some bookkeeping and control electronics 2400 logic cells or 14 k equivalent gates on an Altera FPGA were used to install the described algorithms for ten PMTs.

3.2 Second Level Trigger

The pixel trigger generated by the sub-mirror electronic is processed in the second level trigger. The event detection combines a geometrical and a timing criterion, which have to be fulfilled by an air shower. All criteria are integrated into an FPGA hardware present for each sub-mirror system (100 PMTs) once.

A shower at a maximum distance of about 20 km should trigger 3 PMTs at least, what is defined as a minimum event. Due to the continuous tracks of the cosmics three adjacent hits of PMTs in succession are taken as geometrical criterion. To guarantee overlap the signals are extended by approximately 3 μs (see fig. 5) and by the coincidence of a neighbouring PMT avoiding unnecessary signal extensions – enlarging the probability for noise triggers. This trigger function is a completely

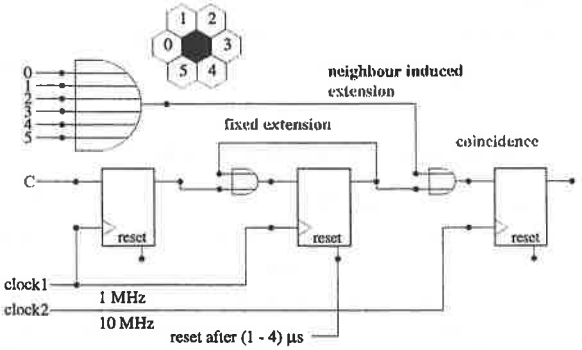

Figure 5: Neighbourhood coincidence for each pixel.

local task and can be executed in parallel on the FPGA yielding together with the following geometrical scan a delay of 1 µs only.

Our trigger concept is based on areas of 9 pixel (3 • 3) pixels. A look-up table (LUT, see fig. 6), for economic realization and maximum flexibility implemented into the internal FPGA-RAM does the event detection within this minimum area. In a scan one sub-mirror is covered by all possible arrangements of

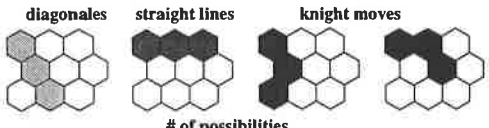

Figure 6: Geometrical allowed pattern for 2nd level trigger. In case of 10*10 the number of possibilities includes hits on boundaries to neighbouring mirrors. Not geometrically bounded triple coincidences give $3.7 \cdot 10^5$ possibilities.

these minimum areas. We have realized the scan by 10 LUTs implemented into the internal FPGA-RAM scanning in each step 10 minimum areas in parallel, see fig. 7. Therefore we need 9 steps to evaluate the whole mirror and the adjacent PMTs from the neighbour mirrors. This scan is a compromise between fast event detection and an optimized hardware. Using this principle we calculated an excellent noise reduction of

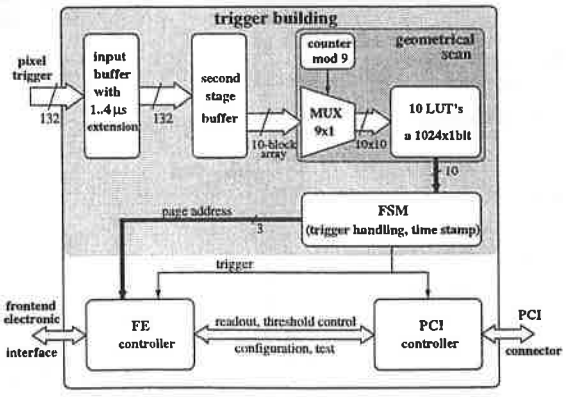

Figure 7: 2nd level trigger scheme.

about $3 \cdot 10^5$ by the hardware.

The time criterion rejects all events, which have duration of more than 60 µs. This function is realized with a finite state machine implemented into the FPGA, too. In addition the FSM determines the end of a trigger and controls the data control for saving the valid events. Furthermore the FSM generates all read and write addresses for the dual port memories and the time stamp for each detected event.

Both designs – the first-level and the second-level triggers – are described using the hardware description language VHDL and both designs are automatically synthesized. Working with state of the art design tools we are easily able to adapt to changing evaluation parameters in the future.

4. CONCLUSION

We have presented the concept for an efficient trigger system for the Pierre Auger fluorescence detector. The hybrid system design is based on configurable and programmable hardware for the first-level and second-level trigger and software for the higher-level triggers. Using a modular structure an efficient data management is possible reducing memory requirements. In addition the number of different boards is minimized. All aspects of our system concept reduce on the one hand the logistic problems for maintenance and bring down on the other hand the system costs. Moreover these hardware based triggers yield an excellent noise reduction and allow a flexible event detection. The actual FPGA trigger designs are finished and synthesized.

At the moment we are preparing a first prototype system to evaluate our concept presented in figure 2. The boards for the second-level trigger with the PCI interface to the diskless PCI computer are under design. A prototype experiment at Gran Sasso end 1999 will evaluate the presented designs. The massive parallel trigger concepts and simple PCI structure and overall cheap system solution may be also of some stimulation for other projects.

5. REFERENCES

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