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Architecture of the SPS Beam and Extraction Interlock Systems

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Abstract

For the machine start-up in 2007, the SPS must deliver beams for fixed target experiments, to the LHC and for the neutrino beam to Gran Sasso with the highest possible efficiency. Fast changes of the SPS cycle will be required, which has many implications for the SPS control system. In particular the existing software and hardware interlock systems that protect the SPS machine against beam induced damage due to failures must be upgraded. This report presents the requirements and architecture of the new hardware interlock systems.

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1 Introduction

The SPS is a cycling machine with a typical elementary cycle length of 14 to 25 seconds. The SPS cycle, which is referred to as the super-cycle of the machine, is split into one or more elementary cycles that are used to deliver different types of beams. Presently the SPS is delivering slow extracted beams for Fixed Target experiments (FT) and MD beams of various kinds, although mainly in preparation for the LHC. Super-cycle changes are slow, they require typically 1 hour, and are therefore made rarely. In the future the SPS will have to deliver fast extracted beams for the LHC [1] and for the CNGS experiment [2]. This comes in addition to the usual FT and MD beams. Figure 1 gives an overview of the planned SPS machine in 2007. To operate efficiently, the control system of the SPS will be modified to allow fast Super-cycles changes (within 1 or 2 cycles). Since the high intensity and high brightness proton beams can cause damage to the machine components in case of failures, a fail-safe hardware interlock system is required to protect the SPS. The presently used hardware interlock system was designed in the 1980's and is not designed to handle the fast cycle changes planned in the near future.

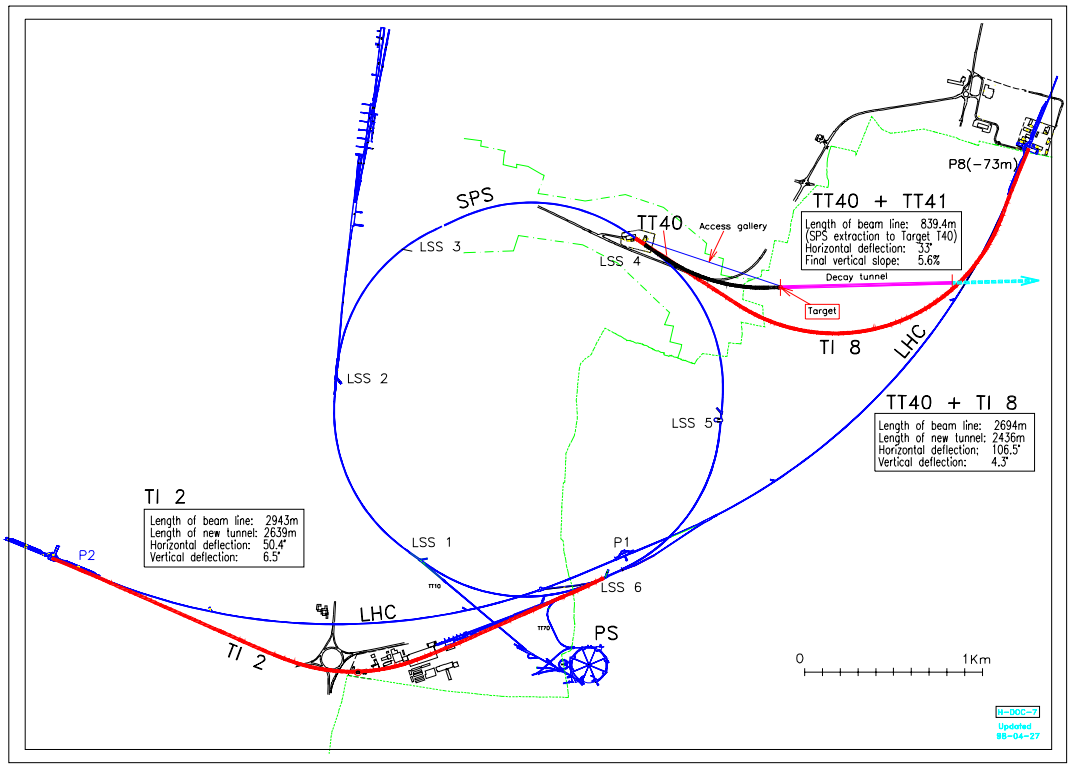

Figure 1 : Overview of the SPS complex with the new transfers lines TT40, TT41, TI8 (extraction from LSS4) and TI2 (extraction from LSS6) [LSS = Long Straight Section].

This document first describes briefly the hardware and software interlock systems that are presently used to protect the SPS. After this introduction, the new fast extractions will be briefly described. The objectives and requirements for the hardware interlock system will be given. The architecture of a new hardware interlock system is proposed. Possibilities to share developments in common with the future LHC interlock system [3] are explored. Finally a list of existing and future interlocks will be described and discussed.

This document reflects the state of the interlock system design at the time of writing. Future developments and requirements may impact on design and architecture of the systems, in which case this document will be amended.

2 The Present SPS Interlock System

2.1 SPS Beam Dump and Emergency Interlock Systems

The SPS internal beam dump system [4,5] consists of the fast dump kicker magnets MKDH and MKDV and the dump blocks TIDH and TIDV. The 3 MKDH magnets provide a damped half-sine horizontal sweep with a rise-time of ~25 μs [6]. The 2 MKDV magnets provide a vertical deflection with a rise-time of 250-300 ns. The combination of horizontal and vertical deflections is used to distribute the dumped beam on the surface of the dump blocks to limit temperature excursions. For beam energies of up to 100 GeV the beams are dumped on the TIDH block, for higher energies the beams are deposited on the TIDV. Energy tracking of the kicker voltages must be performed through each cycle. The system is installed in BA1 and LSS1 and a layout of the system in LSS1 is shown in section 13, Appendix B. The Emergency Interlock System provides the interface between the beam dump system and its clients.

The SPS beam dump can be triggered in two fundamentally different ways. First, a beam dump can be programmed in advance at a given moment in the SPS cycle. In that case the dump is triggered by a timing event and the kick is synchronized to the particle free gap in the beam. Synchronization of the beam dump with the beam gap is performed using a revolution frequency signal. For example, the 'end of cycle dump trigger', which must always be present, is programmed at a fixed time at the end of the beam cycle. The absence of this timing event triggers an internal interlock of the beam dump (channel 2 in crate 1, see below). A beam dump can also be triggered by an interlock signal generated by one of the Emergency Interlock System clients. Such a dump is always asynchronous, i.e. not synchronized to the beam gap, leading to beam losses around LSS1 where the TIDV block constitutes the physical aperture of the machine in the vertical plane. The main reason not to synchronize an emergency dump is the reliability of the trigger generation for the dump. The synchronization will be implemented in the coming years to reduce the amount of beam that is sprayed in LSS1.

The interface between clients and Emergency Interlock System is based on current loops. On the emergency system side, the current is detected by opto-couplers to avoid galvanic coupling. The hardware interlocks generated by equipment systems distributed over the SPS ring arrive in 3 crates installed in BA1. The input signals to those crates are listed in Table 1. All interlock channels of crate 2 are automatically reset at the end

of each elementary cycle to avoid down time from faults due to beam transients. The reset will only be effective if the client has re-enabled the signal on his side. After 3 automatic resets, a manual reset by the operator is required. This reset procedure prevents blocking all beams when an interlock has occurred on a given cycle. The summary output of crate 3 is sent over a cable to the PS control room to prevent further beam extraction from the PS towards the SPS.

Table 1 : Input channels to the present SPS Emergency Interlock system (for all 3 system crates installed in BA1)

Crate No.	Channel No.	Interlock signal	Comment
1	1	Beam dump internal fault	Kicker vacuum, LOCAL control, etc
1	2	Beam dump no trigger	Absence of end of cycle dump.
1	3	Summary Ba6	Extraction interlock summary from BA6
1	4	Energy tracking	
1	7	Beam tracking	Tracking with respect to beam presence and synchronization.
2	1	SSIS (SPS Software Interlock System)	
2	2	Beam position > 30 mm	
2	3	Beam losses LSS1	Injection beam losses
2	4	Beam losses LSS2 and TT20	North extraction losses
2	5	Beam losses LSS6 and TT60	West extraction losses
2	6	RF	
2	7	Beam losses ring and BCT	Ring beam losses and fast current losses during the energy ramp.
3	2	Vacuum	
3	3	Main power supplies	Main magnets (dipoles, quadrupoles and sextupoles) status
3	4	MPS fast Chain	Fast interlock on 18 kV disturbances.

Operators have the possibility to disable (de-activate) any input channels to the emergency dump system. Such an action is automatically triggers a beam stop by the software interlock system, discussed in section 2.3. To re-establish the beam with a disabled hardware interlock channel, the operator must also disable the software interlock condition associated to a disabled hardware interlock channel. This second software interlock layer provides a protection against accidental disabling of a channel. The user interface of the SPS Emergency Interlock system in the control room is shown in Figure 2. The emergency system experts also have the possibility to protect the interlock channels from being disabled by an operator.

One emergency system crate is installed near the proton injection kicker MKP in BA1. A summary of all emergency beam dump channels is send to this crate. In the presence of an emergency interlock, injection into the SPS ring is prevented by a 50 μs delay of the injection pre-pulse, and the beam is sent to the TBSJ dump block. A reset of the beam dump system also resets the injection kicker interlock, thus re-enabling injection.

The General Machine Timing of the SPS is not used by the Emergency Interlock System itself, except to reset the interlocks in crate 2 for the sub-sequent cycles, but it is handled internally by the beam loss system to define thresholds and other parameters.

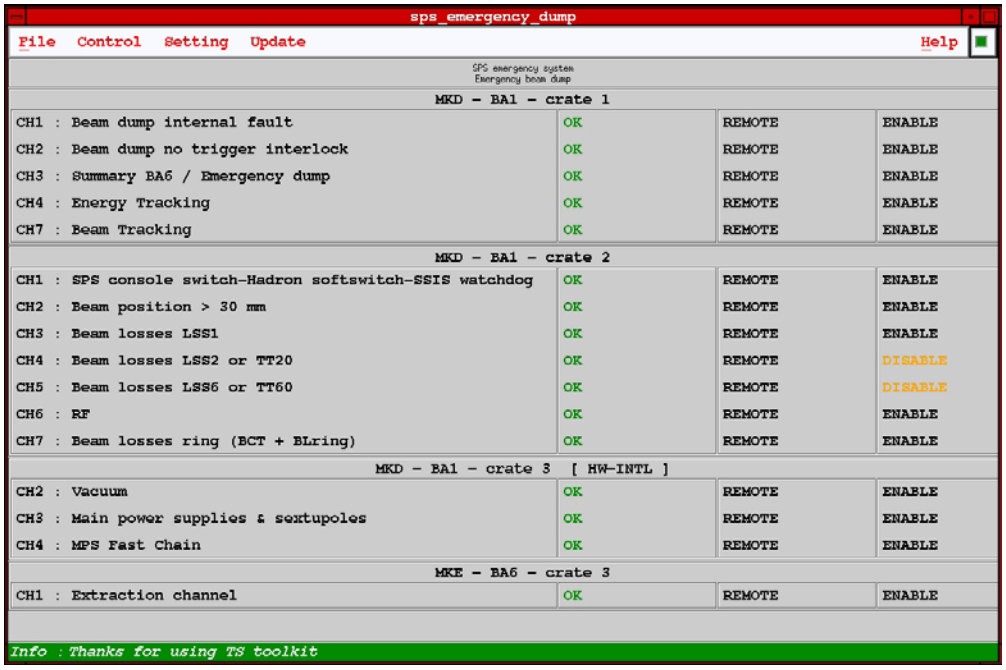

Figure 2 : User interface of the SPS Emergency Interlock System in the control room with the list of presently available interlock channels. The "remote" flag indicates that a channel can be disabled by the operator. In this example channels 4 and 5 have been disabled by the operator.

2.2 The SPS extraction interlock system

Since the end of the high intensity neutrino physics programme, the extraction interlock system has been deactivated. The hardware components of that system were identical to the Emergency Interlock System.

During the high intensity neutrino physics programme with 2 fast-slow extractions of over 10^{13} protons/extraction, the extraction interlock system could inhibit the fast slow extraction in case of faults on the septa (in particular sparks occurring in the electrostatic septa just before extraction), on the neutrino target (temperature, position) or when the currents of critical elements in the transfer line where out of tolerance. The 'C-link' software system was responsible for the surveillance of the Mugef system, with reference settings and tolerances independent of the functions send to the power converters controlled by the Mugef crates.

2.3 The SPS Software Interlock System

The SPS Software Interlock System (SSIS) is a flexible software package that provides an additional protection layer on top of the SPS emergency beam dump system. The SSIS performs a software surveillance of the SPS machine and generates beam stop requests associated to a given beam type. Three output signals are generated by the SSIS namely SPS-Hadron-Ready (for the main beam segment), SPS-Leptons-Ready, SPS-MD-

Ready (for the MD beam segment). The state of the tree signals is visualized by LEDs in PCR.

For each sampling interval defined by the monitoring rate, the SSIS verifies a predefined set of equipment. Tests are made according to a monitoring logic defined by :

- the name of the equipment,
- the desired state,
- an optional protection,
- the actions to be taken if the state is not correct (send alarm, stop beam...),
- the SPS mode for which this test is effective.

The tests are organised in elementary test groups, each test group being associated to a logical channel. Each logical channel is associated to a beam type (lepton, hadron, or MD) and a selected equipment group (state, setting…) and can be enabled or disabled individually. If an elementary test fails, the SSIS can request a beam stop or just raise an alarm depending on the severity of the failure. When the SSIS is not able to perform an equipment check during a monitoring interval, only an alarm is generated. Due to delays in equipment access, the SSIS is not able to perform all tests within one super-cycle.

For each of the three beam types, the SSIS deactivates the associated output signal if at least one active channel has received a beam stop request. The SSIS also generates alarms when a logical channel (enable or disable) has received a beam stop request or when a channel is disabled.

The SSIS output channels are connected over a hardwired link to the PS control room to stop beam ejection and to the Emergency Interlock System to request a beam dump and inhibit the injection kicker when a software interlock is present. The PS operator has the possibility to bypass this veto. The SPS operators can set a switch to by-pass the complete SSIS.

A new software interlock system will be developed in parallel to the new SPS control system. This new software system is expected to have higher performance (speed) and must be able to handle the fast cycle changes foreseen in the future. The analysis of this system is outside the scope of the document. We will assume here that either SSIS or its successor will complement the future hardware interlock system by providing an additional and extended protection and surveillance layer and the associated diagnostics.

3 SPS Beams

In 2006/2007 the SPS will deliver beams to fixed target experiments in the North Area, to the CNGS experiment and to the two LHC rings. Resonant (slow) extraction is used for the fixed targets beams that are extracted in Long Straight Section 2 (LSS2). Two new fast extractions will be used for the LHC and CNGS beams in LSS4 and LSS6. These fast extractions are the main motivations to design a new hardware interlock system for the SPS. Some details on those extractions and the corresponding beams are given in this section.

3.1 SPS cycles for LHC and CNGS

Fixed target beams are injected at 14 GeV/c and accelerated in 3 seconds to 400-450 GeV/c. A third order resonant extraction is used to produce a ~5 second long spill at top energy. The length of a typical proton fixed target cycle is ~12 seconds, including the

ramp down of the magnetic field at the end of the cycle. For ion operation both energy and cycle length may vary, but the spill length does not change significantly.

The LHC beam is injected at 26 GeV/c and accelerated to 450 GeV/c [1]. The length of the standard cycle is 21.8 seconds. The injection plateau is 10.8 seconds long since up to 4 injections of 72 bunches must be accommodated, the injections being separated by 3.6 seconds. The length of the 450 GeV/c flat top is ~1 second.

The CNGS beam is injected at 14 GeV/c and accelerated to 400 GeV/c, with an expected cycle length of 6 seconds. Injection plateau and energy ramp are similar to the fixed target cycle. The two injections are separated by 1.2 seconds. The length of the flat top at 400 GeV/c is only ~ 100 ms, the two extractions being separated by 50 ms. The 400 GeV/c flat top of the presently foreseen CNGS cycle may however be too short for certain interlocks, in particular those concerning power converters with tight tolerances.

Examples for LHC and CNGS cycles are shown in Figure 3.

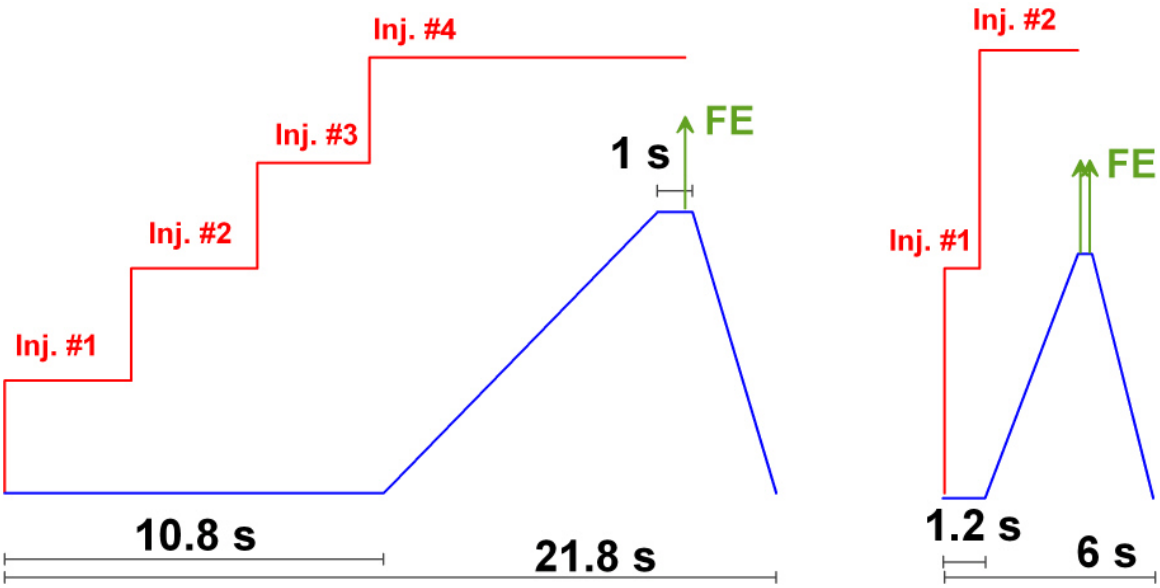

Figure 3 : Examples for LHC (left) and CNGS (right) beam cycles in the SPS. The blue line represents the beam momentum (respectively the magnetic field), while read lines indicate the total beam intensity.

3.2 Extraction from LSS4

Extraction of the beams to the CNGS target and to LHC ring 2 will take place in LSS4. After extraction both beams will travel in the common TT40 line over ~ 100 m. A string of 8 dipole magnets (MBSG410) acts as a switch to deflect the extracted beam either to the TT41 line towards the CNGS target or to the TI8 line towards LHC ring 2. A current of ~ 3600 A is required to switch the beam to TT41. For a vanishing current, there is no deflection and the beams travel to TI8 (see Figure 1). A particular feature of the TT41 and TI8 lines is the shared power converter for the dipoles of the 2 lines. An electronic (or mechanical) switch will be used for the selection of the line to be powered. To switch from one line to the other, the current must be reduced to ~ 0 A. Interlocking of the switch status is clearly of prime importance.

Two movable TED beam dumps [7] are installed in the lines, one at the end of TT40 and a second at the end of TI8 before the first injection elements into the LHC. No dump is installed in the TT41 line, this role being held by the neutrino target T40 that is itself interlocked (temperature…). Both dump blocks are able to absorb the full intensity LHC and CNGS beams.

The extraction elements include:

- 4 orbit bumpers in each plane,
- the MKE kicker (5 independent magnets) [8],
- the MSE magnetic septum.

Since the CNGS beam is composed of 2 batches that are extracted at an interval of 50 ms, the kickers in LSS4 are equipped with a 'clipper switch' to provide a fast decay-time of the kicker pulse (some tens of ns).

With the clipper switch the extraction (discharge of the Pulse Forming Networks/PFNs) can be aborted in case of an erratic firing of one of the MKE kickers within 0.5 to 1 μs. For the LHC beam the average deflection of each kicker at the MSE septum is ~ 9 mm. In the event of a kicker mis-firing the beam will pass close to the TPSG inside the SPS vacuum chamber. Depending on the mechanical tolerances and on the exact beam sizes, some beam could touch the TPSG. The beam oscillation of 8 mm that propagates around the SPS ring is within the aperture in the horizontal plane (~ 25 mm). If one kicker is missing, the beam will hit the TPSG.

The bumped beam position is measured and surveyed by a special large aperture beam position monitor (BPCE) in lattice position 418, corresponding to the maximum amplitude of the bumped beam.

The timing sequence of the fast extraction is given approximately by the following event sequence, as seen from the extraction kicker system, the time referring to the moment of extraction:

Step 1	**-1000 ms**	The extraction warning event arrives.
Step 2	**-20 to -50 ms**	The interlock system enables the extraction.
Step 3	**-15 ms**	The PFNs are charged.
Step 4	**-20 μs**	The fast pre-pulse trigger signal arrives.
Step 5	**0**	The MKE kicker pulses.

Whenever the extraction enable signal is cleared before the actual extraction (i.e. after step 2 and before step 5), the beam must be dumped immediately, since this may indicate an erratic firing of one of the kicker magnets.

The list of interlocked elements and measurements includes:

- The SPS ring orbit bumper currents.
- The SPS ring bumped beam position.
- The SPS extraction kicker (synchronization, energy tracking…).
- The extraction septum MSE.
- All TT40, TT41 and TI8 power converters and magnets, with loose tolerances on the orbit corrector magnets (to be refined as more experience is gained with the lines).
- The beam trajectories and the beam losses in TT40, TT41 and TI8 (possibly surveyed by software interlock, except for TT41 where beam losses occurring during the first extraction must be used to prevent the second extraction).

Interlocks signals associated to the 3 lines must be carefully decoupled, in particular between TI8 and CNGS, to avoid crossed interlocks that would prevent extracting the LHC beams when the CNGS beams is stopped by an interlock in TT41 (or vice-versa). In addition to this list, the quality of the beams (total intensity, intensity spread amongst bunches, emittance…) must also be controlled before extraction, in particular for the LHC.

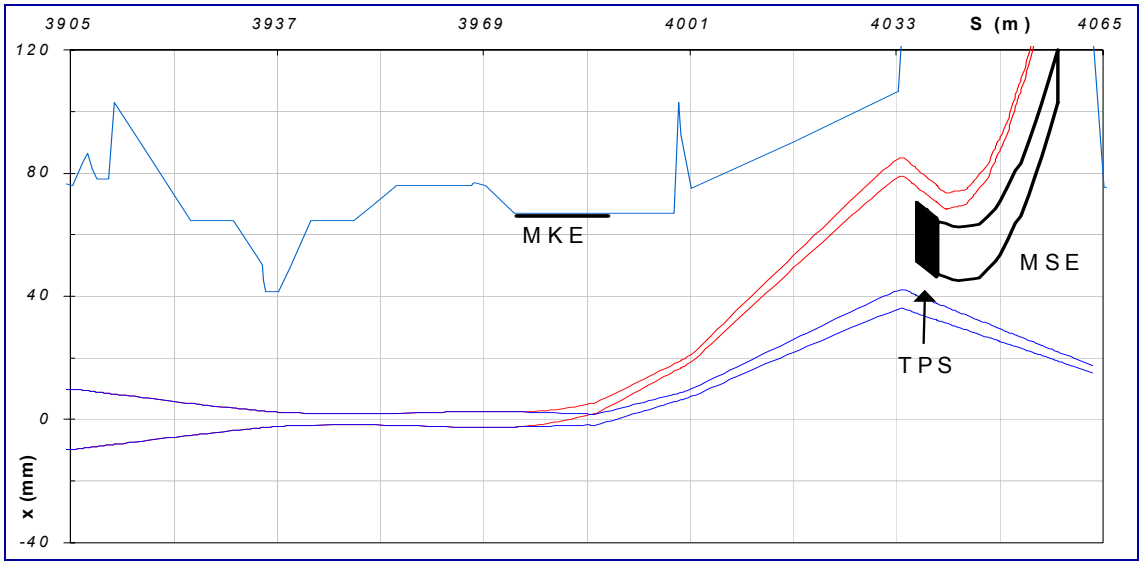

Figure 4: Extraction channel layout for the horizontal plane in LSS4. The circulating beam (blue) is bumped horizontally close to the septum using 4 horizontal bumper magnets and kicked into the extraction channel by the MKE kicker magnet (red trace).

3.3 Extraction from LSS6

The layout of the fast extraction in LSS6 is not yet finalized because the decision to shutdown the West Area for fixed target beams was only taken mid-2002. The general concept of the extraction will be identical to the fast extraction in LSS4, except that it will only be used for LHC beams, which simplifies layouts and interlock handling. A noticeable difference for the extraction kicker system is the absence of clipper switches for fast discharges [8]. The layout and the powering scheme of the TI2 transfer line are similar to TI8.

3.4 Extraction from LSS2

Beams for fixed target experiments in the North Area will continue to be slow extracted from LSS2. The extraction elements include:

- 4 orbit bumpers in each plane,
- the MST and MSE magnetic septa,
- the ZS electrostatic septa.

Any interlock that arises during the slow extraction must immediately trigger a beam dump.

Presently the power converter settings of the TT20 transfer lines are not surveyed.

4 Architecture of the SPS Interlock System

4.1 Objectives and overall architecture of the interlock system

The objectives of the SPS hardware interlock system are:

- **Protection of the SPS machine**: in case of failures the beam must be dumped and the extractions must be aborted (slow extractions) or prevented (fast extractions).
- **Fault diagnostics**: for each beam dump or extraction abort, the system must provide the necessary information to identify the initial failure.
- **Efficiency optimisation**: unnecessary aborts or beam dumps must be prevented. Unnecessary downtime due to latched interlocks must be minimized.
- **Compatibility with multi-cycling**: the interlock system (and its clients) must not limit the SPS as a multi-cycling machine. Interlock conditions must be adapted automatically from one cycle to the next. For the interlock system itself this implies that interlock inputs must be activated or de-activated (masked) based on information distributed by the General Machine Timing system. Handling of the machine timing events must be reliable and fail-safe [9].
- **Fast detection, reaction and propagation times**: the internal delays of the interlock system for signal propagation, evaluation of the interlock conditions… should not exceed 1 SPS turn.

The SPS hardware interlock system is split into three inter-connected systems :

- **The Beam Interlock System** protects the SPS ring and requests a beam dump if an unsafe situation is detected. This system replaces the SPS Emergency Interlock System which presently interfaces the beam dump system with its clients.
- **The Extraction Interlock System** protects the extraction lines to the LHC, the CNGS target and the experimental areas. Whenever a failure is detected, it prevents the extraction (or aborts a slow extraction) and requests a beam dump. The extraction interlock system is sub-divided into 3 sub-systems responsible for the LSS2, LSS4 and LSS6 extractions.
- **The Software Interlock System** provides further protection by a software surveillance of a large number of SPS equipment (settings, states…). This interlock system can prevent beam injection and request a beam dump when abnormal conditions are detected.

The following principles are used as guidelines for the architecture of the SPS interlock system:

- Within the interlock system itself, handling of machine timing, which is unavoidable in the context of a multi-cycling machine, is concentrated in a few elements.
- The system should be as similar as possible to the LHC machine protection system to avoid duplicated effort. The requirements for the LHC Beam Interlock Controller (BIC) and the SPS interlock modules are very similar [3].
- The system should be distributed and modular.

The proposed architecture is based on a system with two basic components, corresponding to two interlock modules. The final implementation the modules might be

identical, except that some functionality, related to the use of the machine timing, is not activated in all interlock modules.

4.2 Generic Architecture of the Interlock Modules

The sub-components of a generic interlock controller module are shown schematically in Figure 5. Each interlock module is composed of

- An input interface for the client signals (1),
- A logical matrix and its associated monitoring (2),
- A switch to open / close an interlock loop and to generate one or more local output signals (3),
- An receiver / transmitter for an interlock loop (4),
- A General Machine Timing receiver (5).

To obtain a modular system where elements can be connected in series, the local output signal should follow the same standard as the input interface signals.

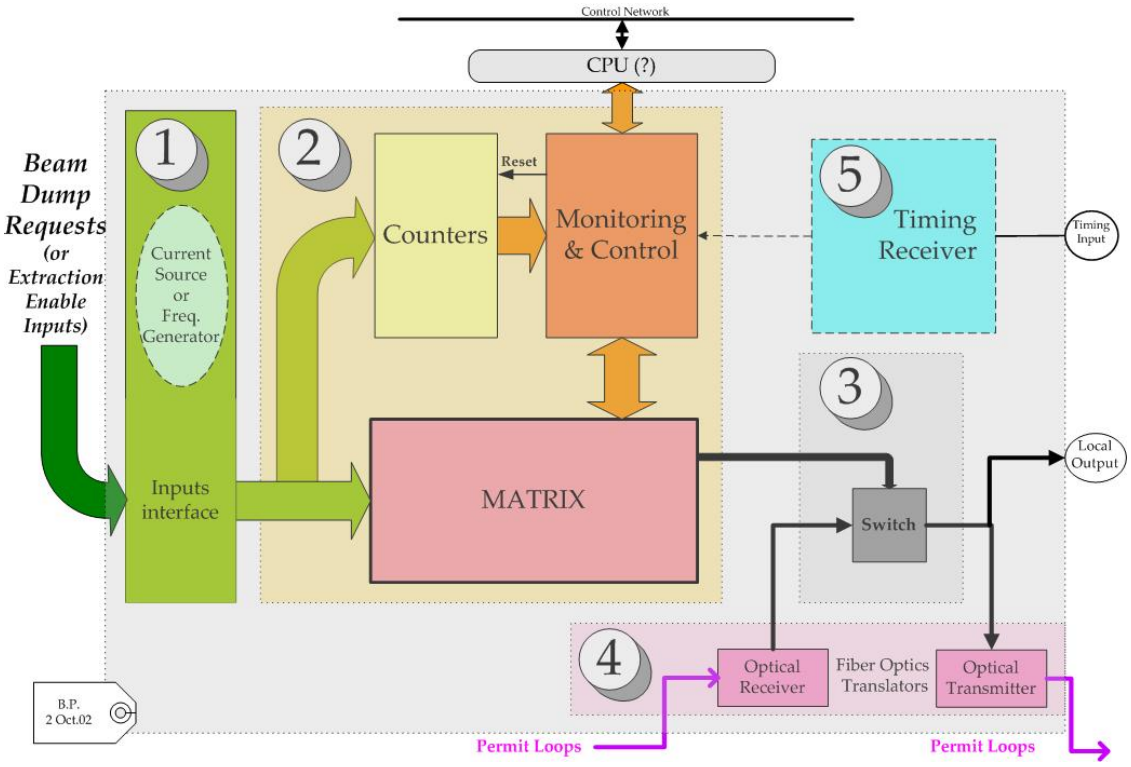

Figure 5 : Block diagram of an interlock module.

4.3 The SPS Local Interlock Controller

The first component of the interlock system consists of a module with a fixed logic matrix. This module will be referred to as the SPS Local Interlock Controller (SLIC). Each SLIC module concentrates interlock signal from clients associated to a given machine or transfer line sector that can be grouped together without requiring the

use of machine timing for the interlock logic. The SLIC interlock matrix can be considered to be static because it is essentially loaded "once and for all" (i.e. very rarely).

The input interface should accept between 12 and 16 input channels.

The SLIC must provide at least 2 identical output signals reflecting the state of the input signals using a standard interface.

The SLIC must be able to interrupt an interlock loop, an approach that is well suited for the beam interlock system with distributed clients.

All state transitions of the input and output signals must be time-stamped and stored in an internal buffer of sufficient depth. The monitoring part of the module is not safety-critical, its role is to provide adequate diagnostics and post-mortem information for the interlock system. The General Machine Timing may be used to store and time-stamp the state of inputs and outputs at certain critical time (extraction) using selected timing events.

4.4 The SPS Central Interlock Controller

The second component of the interlock system consists of an interlock unit that has the same basic functionality than the SLIC. The only difference with the SLIC stems from the fact that this second component must be able to (de-)activate selected input signals according to the SPS cycle and beam type. Its logical matrix is therefore depending on the SPS cycle. This module will be referred to as the SPS Central Interlock Controller (SCIC). The SCIC must be connected to the General Machine Timing to obtain information on beam type and extraction conditions. Fail-safe handling and distribution of the timing information is required.

The requirements for input and output signals and for monitoring are identical to the SLIC.

For the SLIC unit, the timing input is only used for diagnostics while for the SCIC it is used actively to (de-)activate input channels. Since this is the main difference between the 2 modules, the final modules may actually be identical, except that for the SLIC some functionality related to cycle dependence is not activated. In that case this leaves open to 'upgrade' the SLIC to SCIC in case more flexibility is required in the future.

4.5 Architecture of the SPS Beam Interlock System

For the SPS beam interlock system, the present concept used by the Emergency Interlock System where all timing depended effects are handled inside the equipment systems can be maintained in the future.

The proposed beam interlock system architecture is shown in Figure 6. It is conceptually identical to the LHC architecture, with SLIC modules distributed over all SPS access buildings and linked together by a ***BEAM PERMIT LOOP***. Whenever a client interlock signal is set, the BEAM PERMIT LOOP is interrupted by the corresponding SLIC. One of the SLIC modules in BA1 must be connected to the SPS beam dump and injection kicker systems and request a beam dump whenever the loop is interrupted. Alternatively, the dump and injection kicker systems could be connected directly to the beam interlock loop. A connection to the PS machine could be provided to inhibit extraction of the beam from the PS whenever the dump interlock loop is broken.

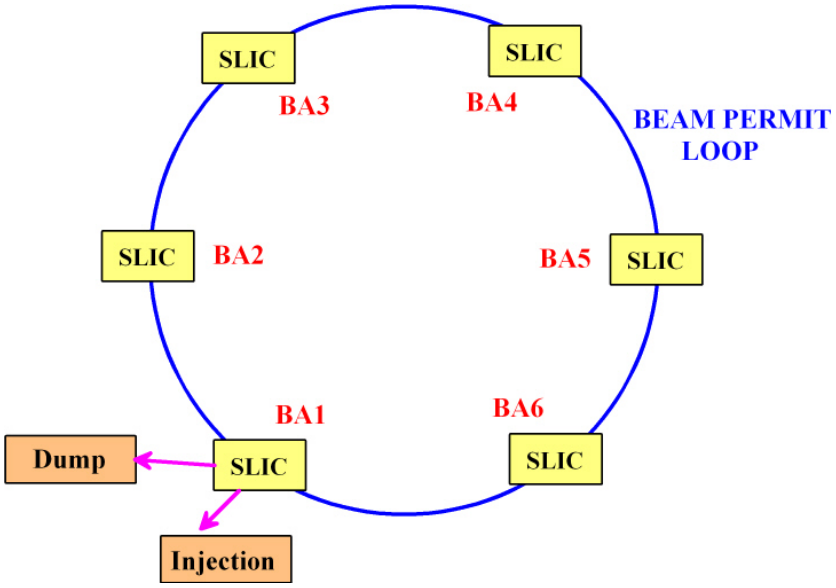

Figure 6 : Architecture of the SPS beam interlock system. One SLIC module must be installed in each SPS access point. All SLIC modules are connected to the BEAM PERMIT LOOP. The state of the BEAM PERMIT LOOP is forwarded to the SPS beam dump and injection kickers.

Interlocks should remain latched until they are reset, either by the operator or by an automatic procedure. To avoid useless downtime due to erratic (beam related) interlocks, an automatic reset procedure must be foreseen. The automatic reset must be fast enough to re-enable the BEAM PERMIT in time for the following beam cycle. The number of automatic resets must be limited to a given maximum. When the number of resets exceeds this limit for a given input channel, the interlock must remain latched until it is reset by the operator. This interlock latching procedure may also be implemented by the new software interlock system which can request a beam stop for a given beam type when the number of interlock resets exceeds the limit. Furthermore the software interlock system can easily be made flexible enough to separate interlocks arising from the different beam types.

A limitation for multi-cycling arises from this architecture of the beam interlock system. Being entirely composed of SLIC modules, the system cannot mask input channels according to beams or cycles. Masking of input channels can only be done 'manually' by the operator, and the mask will be effective for all beams and cycles. This limitation can be removed by replacing the SLIC modules with SCIC modules at a later stage.

4.6 Architecture of the Extraction Interlock System

The extraction interlock systems require a more complex architecture involving both SLIC and SCIC modules. The client interlock signals are grouped together logically by function (extraction) or by transfer line, each group being associated with a SLIC module. The output signals of the SLIC units are forwarded to a single SCIC unit. The SCIC module produces the ***EXTRACTION PERMIT*** signal for the extraction kicker

system. The EXTRACTION PERMIT enables the extraction following an interlock logic where selected inputs can be masked according to the beam or cycle type. The SCIC module must be connected to the BEAM PERMIT LOOP either directly or through one of the beam interlock system SLIC modules. Figure 7 illustrates a possible layout for the extraction to CNGS and LHC ring 2 in LSS4. The layout of the entire SPS interlock system is shown in Figure 9.

More details on the input signals for the different extraction interlock systems are given in the Appendix, section 12.

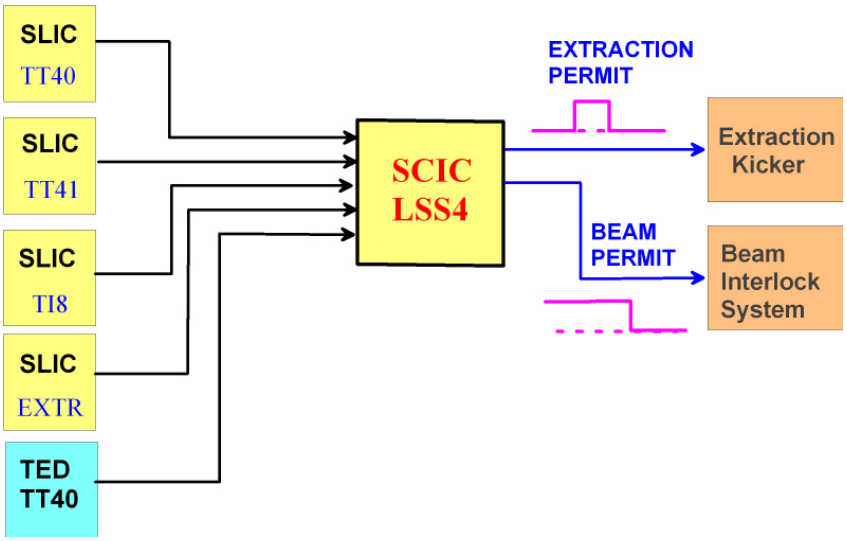

Figure 7 : Architecture of the extraction interlock system for LSS4. Here four SLIC modules gather the interlock signals from the clients which are grouped together logically (TT40, TT41 and TI8 lines, extraction elements). The SCIC module inputs correspond to the output signals of SLIC modules. The TED dump status in the TT40 line is an independent input (see section 7.7) that is required to mask the TT41 and TI8 interlocks when the TED dump is IN beam. Depending on the type of beam, the SCIC module masks some of its inputs.

The following requirements, illustrated in Figure 8, must be fulfilled by the extraction interlock system:

- The EXTRACTION PERMIT must be provided to the extraction kicker using the standard client interface. The EXTRACTION PERMIT must be given ~ 50 ms before extraction and maintained a short time (~few ms) beyond the moment of extraction.
- A beam dump request (BEAM PERMIT OFF) must ALWAYS be generated when the EXTRACTION PERMIT is given to the kicker, but then reset before the time of extraction. The two main reasons for this requirement:
    - The prevention of erratic triggers from the extraction kickers when the energy may already be transferred to the pulse forming networks.
    - A fast beam dump in case the interlock is due to an erratic firing of one of the kicker modules.

- When the EXTRACTION PERMIT is not given during a cycle, there are 2 options :
    - The beam can be dumped using the standard end of cycle dump.
    - A beam dump may be requested by the interlock system a few ms after the normal moment of extraction.

The beam dump request (BEAM PERMIT OFF) must be reset before the start of the following cycle. Latching of beam dump requests issued by the extraction interlock system should be performed by the beam interlock system.

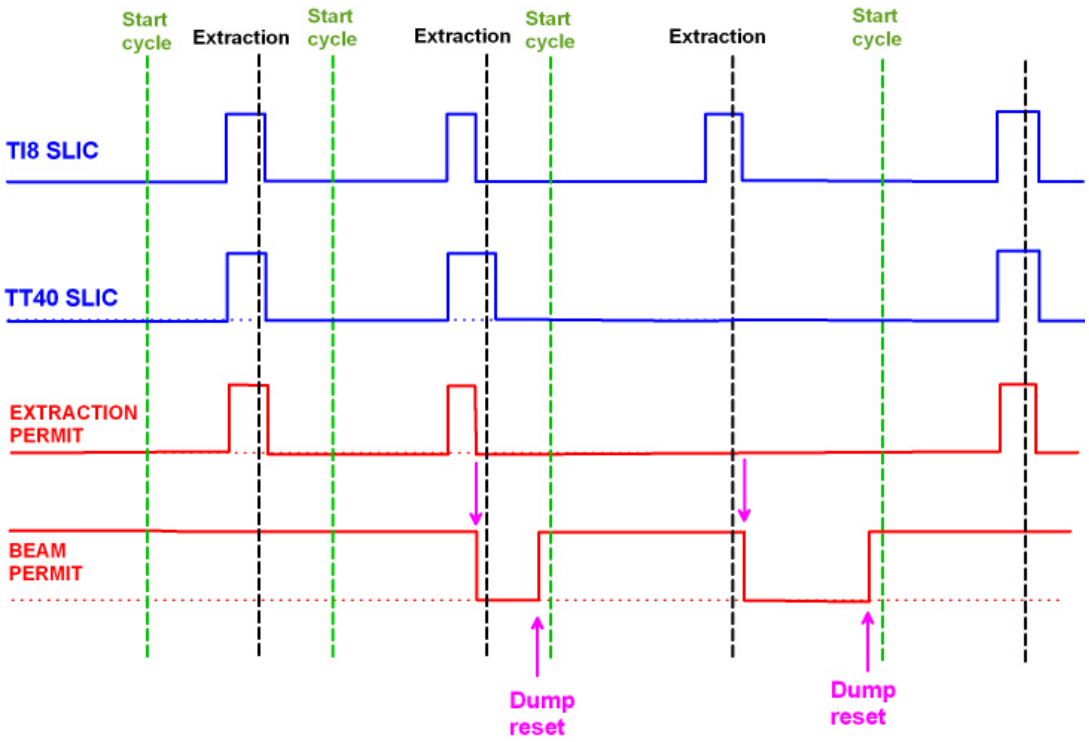

Figure 8 : Example of SCIC signals including two SLIC inputs, the EXTRACTION PERMIT and the BEAM PERMIT for one extraction interlock system. On the first cycle (left), no interlock is set at extraction time and the EXTRACTION PERMIT is given to the kicker. On the second cycle, the TI8 SLIC interlock is set just before extraction, after the EXTRACTION PERMIT was given to the kicker: the EXTRACTION PERMIT is cleared and the BEAM PERMIT is removed to request an immediate beam dump. In the third cycle, EXTRACTION PERMIT is never enabled and the BEAM PERMIT is removed just after the nominal moment of extraction to dump the beam. Finally, in the last cycle (left), all signals are again in the correct state to allow beam extraction.

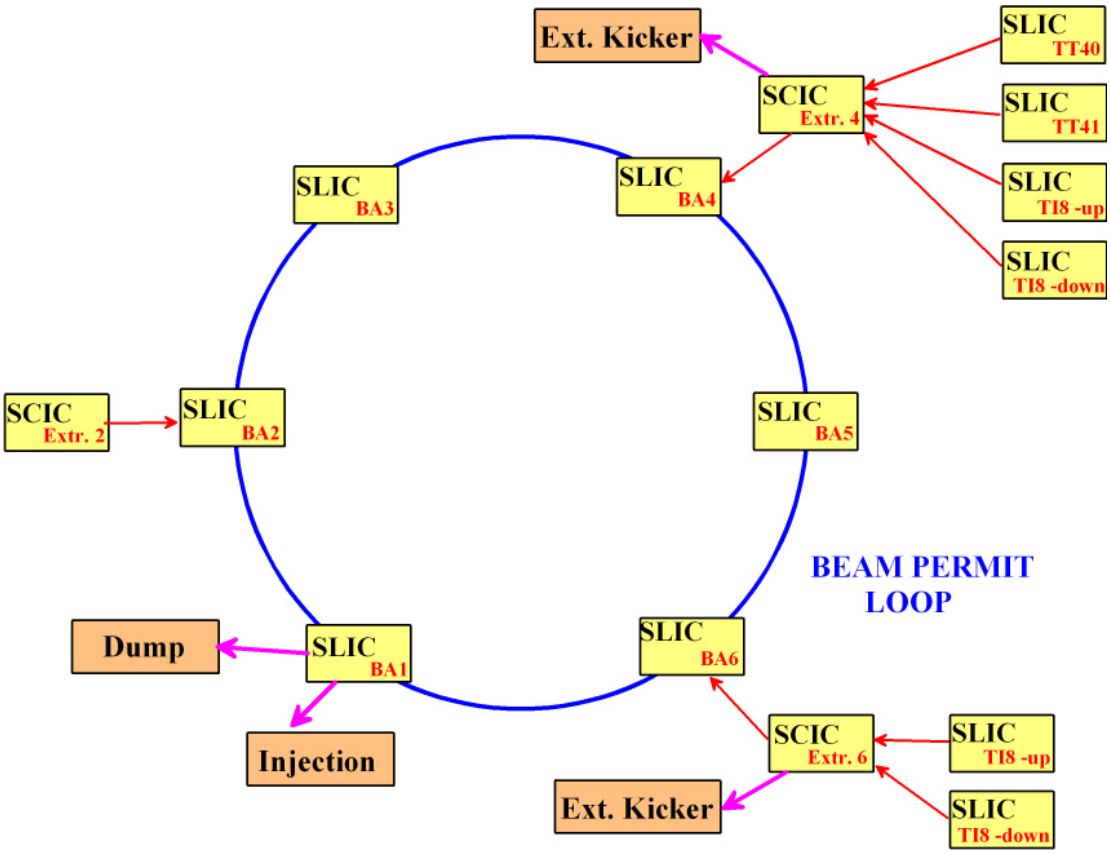

Figure 9 : Architecture of the SPS hardware interlock system, including the beam and extraction interlock systems.

4.7 Interface to Interlock Clients

The interface to the interlock system clients must be:

- Simple.
- Reliable.
- Unique for all clients.
- Fast (transition time ~ 1 µs).

The interface to the clients and to the interlock loop is not necessarily identical. Possible solutions are current loops or frequency signals.

4.7.1 Output Signals

The interlock system must provide at least three output signals using this standard interface. The output channels are used to:

- interconnect interlock modules.
- provide the EXTRACTION PERMIT signal of the SCIC.
- provide the BEAM PERMIT signal of the SCIC.

4.7.2 Interlock Signal Logic

There are two basic choices for the client signal logic:

1. The signals are always in state OK when the interlock client system is running and has no interlock signal in VETO. The signal state changes to VETO when an interlock is detected. It is extremely important to ensure that the state is VETO whenever the equipment system is not operational, in a process of rebooting…
2. By default the signal state is VETO. The signal state is OK only within the short time interval following and during a successful test or measurement.

Strategy No. 1 must be followed for the beam interlock loop (with permanent surveillance) during the entire cycle. The beam interlock modules should not interrupt the beam interlock loop during the beam-out segment where the magnets are prepared for the next cycle (and where there is no beam present). Strategy No. 1 is obviously also adapted for equipment that has no dynamic behaviour during a cycle, for example the vacuum system.

Strategy No. 2 must be adopted for the fast beam extractions where the surveillance tasks of certain systems are only required and meaningful around the moment of extraction, for example for the power converter currents. This strategy also presents a higher level of safety if it is applied correctly. In particular, the interlock system has the possibility to verify that the OK is removed between cycles, therefore providing additional protection against some failures.

4.8 Interlock latching and reset

The policy for latching and resetting interlocks is likely to evolve with time, in particular when more experience is gained with the fast extractions for CNGS and LHC. Here we give some general guidelines using the experience from the present SPS interlock system.

4.8.1 Beam interlock system

Beam interlocks should be latched by default, and an automatic reset procedure must be foreseen for certain interlock categories, in particular all interlocks that can be due to transients occurring randomly in a certain fraction of the cycles (for example beam losses). Whenever the number of successive automatic resets exceeds a given threshold, the interlock should remain latched. A manual reset by the operator is then required the re-enable the beam.

The software interlock system will, among many other things, survey the beam and extraction interlock systems: it may therefore be used to perform the interlock latching by requesting a beam stop whenever the number of resets exceeds the limit. The software system could easily associate the interlocks with the corresponding beam and cycle. More complex cycle dependent correlations should be performed by the software interlock system and not by the beam interlock system.

4.8.2 Extraction interlock system

No interlock must a priori be latched by the extraction system, but such a facility should nevertheless be foreseen for the SCIC modules. Latching of extraction interlocks should be performed by the beam interlock system. The extraction interlock system must

reset its own beam dump requests before the start of the next cycle (and before the beam interlock systems resets its BEAM PERMIT).

4.9 Interlock activation and deactivation

Cycle dependent interlock activation or deactivation (masking) must be provided for the SCIC module. It must be possible to store at least 20 configurations (for 20 different cycles) at any time in the SCIC.

The operator must have the possibility to 'manually' deactivate selected input channels to the interlock systems. Such an action must be protected by adequate software and every change of configuration must be logged. An alarm and a software interlock must be set whenever the interlock conditions differ from the nominal configuration, as is the case for the present interlock system. Before beam can be injected with a masked interlock channel, the operator must also mask this software interlock. Such a second software interlock level provides protection against accidental changes of the interlock matrix.

With low intensity beams (below damage threshold), it must be possible to relax interlock tolerances or to disable input channels to perform tests or understand problems. There are two basic philosophies to perform such an action:

- The interlock system and its clients handle the interlock relaxing/masking 'automatically', in which case they must be provided with appropriate information (over the timing system) on the beam intensity and on which channels to mask under such conditions. Beam quality interlocks (see section 7.3.5) on the beam intensity must be used to ensure that the intensity remains below a pre-defined threshold. Beams above the requested intensity limit should be dumped as soon as they arrive in the machine.
- The operator takes the responsibility to disable the interlocks manually and must make sure that the intensity does not exceed a certain threshold. In that case the operator can either rely on the beam intensity interlock (as for the previous case) or he must ensure by other means that the intensity is within an acceptable range.

The interlock system must be able to cope with both strategies. Operational experience will eventually determine which scenario is preferred in practice.

4.10 Monitoring and post-mortem

All state transitions of input and output signals must be monitored with a precise timestamp (~ μsec) and stored in an internal buffer. This timestamp should be given in UTC or equivalent time as well as in SPS cycle number and time inside the cycle. The start and end of cycle must also be recorded in the buffer. All state transitions must be saved for at least 5 to 10 subsequent SPS super-cycles, to be read out at any time by a surveillance program.

The monitoring of input signals that are known to be in the form of a PERMIT given during a short window (see section 4.7.1) can be used to detect abnormal behavior when the PERMIT is not reset in every cycle. In that case, an interlock should be set by the internal monitoring system of the interlock module.

5 Requirements for the General Machine Timing System

To ensure a correct handling of machine timing and to enable all systems to be fully multi-cycling, by the interlock systems and its clients, additional information must be provided by the timing system on a cycle by cycle basis. The following information must be provided:

- A unique MTG cycle number.
- A unique beam cycle identifier (to identify a given ensemble of settings).
- The beam type: FT, LHC, CNGS…
- The particle type: proton, ion species.
- The LHC ring # for LHC beam cycles.
- The # of SPS batches that are requested by the LHC.

A special timing event is required to signal the moment of extraction to the interlock system. This event is used to fire the beam dump whenever the extraction request disappears before reception of this event. Extraction warning events are required to trigger appropriate actions by the various interlock clients. The number of timing signals should however be kept to the minimum to avoid errors during cycle generation.

6 SPS Beam Modes

For operation of the LHC and CNGS (or any other future beam) new dedicated beam modes must be defined for the SPS to trigger appropriate actions of the software interlock system. For example the beam modes for LHC could be:

- *BEAM_TO_TI2_TED* : LHC beam requested to the downstream TED dump in TI2. A similar mode must exist for TI8.
- *BEAM_TO_TT40_TED* : LHC or CNGS beam requested to the upstream TED dump in TT40. A similar mode must be defined for TT60.
- *BEAM_TO_LHC* : LHC beam requested to be injected into LHC.
- *BEAM_TO_CNGS_TARGET* : CNGS beam requested to be sent to the neutrino target.

Further specialized modes may be required.

7 Interlock Signals from SPS Equipment

7.1 Power Converter Interlock Signals

7.1.1 Main SPS Ring Power Converters

For surveillance of the SPS ring main power converters (dipoles, quadrupoles and sextupoles) the existing interlock signals will be re-used for the new beam interlock system. Two interlock signals are presently provided:

- A slow state signal from the power converters. This signal goes to fault when the main power converters are not ON.
- A fast signal derived from a detection of transients on the 18 kV network in order to dump the beam before the field changes significantly in the main magnets. The total delay of this system is of the order of 1-2 50 Hz periods (50 ms).

The signals that are provided must remain enabled unless a fault is detected.

7.1.2 Transfer Line and Extraction Element Converters

The surveillance of the current in the power converters is of prime importance for protection of the transfer line and extraction elements: the settings must be correct before the beam can be send through the line. The settings of the extraction bumpers in the SPS ring, which bring the beam close to the septum magnet, must also be checked prior to extraction.

The following requirements apply to the surveillance:

- The output signal from the power converter surveillance must consist of a short ENABLE signal. By default this signal must be in the FAULT state.
- The power converters need not be surveyed during the entire cycle, but only during a short time interval before and during the extraction. The integration time for the current measurement should be the shortest possible compatible with the accuracy requirements. Typical accuracies are indicated in Table 2.
- The surveillance interval limits must be derived from the timing events used to drive the power converters. The interval limits depend on the SPS cycle. In the absence of timing events, no ENABLE must be given.
- At the beginning of every cycle, the ENABLE signal must be cleared and restore to the FAULT state.
- The current measured over the surveillance window must be compared against a reference value I_{nom} and a tolerance ΔI_{tol}. Both reference and tolerance depend on the cycle. The values must be loaded and stored independently of the normal functions that are used to drive the power converter to provide protection against out of tolerance settings of the power converters (power converter function load error, DB errors, bad trims…). The values must be stored in non-volatile memory to protect against errors after system resets. A protected procedure must be available to update and load the reference settings.
- When the power converter is in fault state, the state of the signal must always be FAULT.
- A cycle dependent mask must be provided to select the power converters that have to be surveyed in each cycle.

Figure 10 below indicates schematically the principle of the surveillance.

PC surveillance is most important for the magnetic septa as well as for the main elements of the lines (dipoles and quadrupoles). For orbit correctors a relatively large window around the nominal setting must be provided for steering (for TI2/TI8 the orbit correctors provide deflections of up to 80 μrad). Experience with operation of the lines will help define acceptable window sizes to guarantee safe operation while leaving sufficient margin for operation.

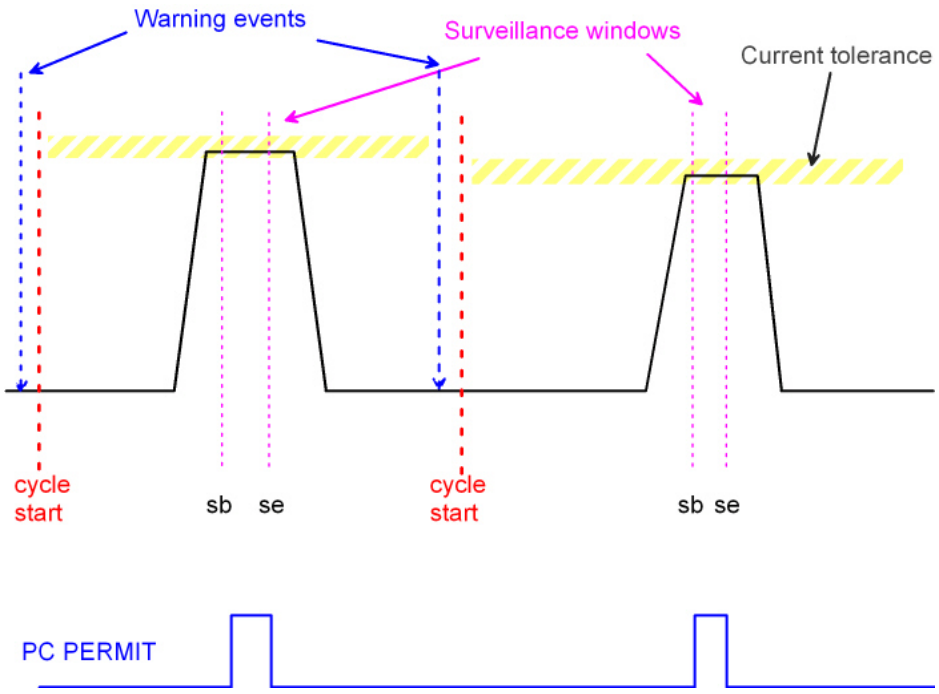

Figure 10 : Power converter surveillance windows and PERMIT signal. sb and se refer to the limits of the surveillance window.

Table 2 : Interlock levels on different power converter/magnet types. The accuracy of the current surveillance should be a factor 3 to 4 better than the interlock tolerance indicated in this table.

Zone	Magnet type	Tolerance (%)
SPS ring	Orbit bumper	1
LHC Transfer Lines	Main dipoles	0.1
LHC Transfer Lines	Other dipoles	0.1 to 0.5
LHC Transfer Lines	Main quadrupoles	0.1
LHC Transfer Lines	Other quadrupoles	0.1 to 0.5

In the context of the ROCS system, an internal surveillance has already been tested [10]. The surveillance task is being improved to implement the requirements presented herein.

7.1.3 LSS4 extraction interlock signals

Interlock signals from the power converters for the extraction in LSS4 to the TT40, TT41 and TI8 lines must be properly segmented to avoid crossed interlocks between the lines that would stop both beams in case the interlock affects only TT41 or TI8. To ease the diagnostics and provide sufficient flexibility, ***distinct*** interlock signals should be provided for:

- The extraction bumper power converters.
- The TT40 power converters (including the magnetic septa).
- The MBSG410 dipole string (switch TT41-TI8) power converter.

- The MBI816 (TI8) / MBG417 (TT41) main dipole strings connected to the same power converter equipped with a mechanic/electronic switch to select the line to be powered.
- The TT41 power converters (excluding MBSG410/MBG417).
- The TI8 power converters (excluding MBSG410/MBI816).

For TT41 and TI8, a further highly desirable refinement consists in splitting the interlocks into two distinct channels, one for quadrupoles and dipoles and one for orbit correctors. Such a segmentation would simplify the steering of the lines, since it is then sufficient to de-activate the interlock signal associated to the orbit correctors and ensure sufficiently low intensity if large corrections need to be applied. Without dedicated signal for the orbit correctors, it is necessary to modify the tolerances on the corrector currents to provide sufficient room for steering.

As an alternative the current surveillance for the MBSG410 dipole string and for the MBI816 (TI8) / MBG417 (TT41) main dipole strings may be included directly in the surveillance of TT41 and TI8.

The main dipoles string requires further attention due to the presence of the switch inside the power converter.

7.2 Kicker System Interlocks

7.2.1 Extraction Kickers

The extraction kickers in LSS4 and LSS6 must be surveyed for correct synchronization and energy tracking. One signal indicating the state of the kickers will be provided.

In LSS4 the kickers are equipped with clipper switches that allow a fast discharge of the energy stored in the Pulse Forming Networks (PFNs). The clipper switches can be used to abort the kicker pulse whenever one of the kicker modules misfires. In such an event, an interlock signal will be sent by the kickers to the extraction interlock system to request an immediate beam dump.

Whenever the PFNs of the extraction kickers are charged but no trigger signal is received (extraction not enabled, no pre-trigger…), the PFNs will be discharged by triggering the main switch (i.e. through the magnets). This operation can only be done when the beam is safely dumped and must be performed during the ‘beam-out’ segment of the cycle, when the magnets ramp down to injection setting. No beam is present during that period of the cycle: if the beam was not dumped, it will have been lost during the magnet ramp down.

A dedicated signal indicating the LOCAL/REMOTE control mode of the kickers must be provided to the beam interlock system. Whenever the kicker is operated in LOCAL mode, the magnet can be pulsed asynchronously with the SPS machine and an interlock must be set to inhibit all beams in the SPS.

7.2.2 Dump Kickers

The internal surveillance signals of the beam dump should be maintained for the new interlock system. The signals to be provided are:

- Energy tracking faults.
- Absence of trigger faults.

- Internal dump faults (vacuum, temperature, LOCAL mode…).
- Synchronization faults.
- Timing event distribution errors.
- Beam tracking.

In the future the triggering of the SPS beam dump system should be modified to provide synchronized beam dumps in all cases, including emergency dumps.

7.3 Interlocks on Beam Measurements

7.3.1 SPS Ring and Transfer Line Beam Loss Monitoring

The present SPS beam loss system is connected to the SPS emergency dump. The system provides the following signals to the emergency beam dump system:

- Fast beam losses LSS1 [injection]
- Fast beam losses LSS2 (now also TT20) [extractions]
- Fast beam losses LSS6 (now also TT60) [extractions]
- Beam losses BLRING [distributed losses]

Interlocks generated by the fast BL system (LSS1, LSS2, LSS6) are handled by hardware and the detection delay is ~ 1 μs, not including the delay to the dump kicker. The SPS ring system (BLRING) has a response time of ~ 20 ms and it is distributed in all BAs where each crate is connected to a cable circling the SPS ring. The interlocks are handled by software with some user settable parameters (like the # of channels required to trigger the dump…). The BLRING system shares the interlock cable to the dump with the Beam Current Interlock. The Beam Current Interlock sets a reference intensity after transition crossing and then monitors the intensity over the ramp at intervals of 5 ms. If it detects a beam loss above a certain threshold, a beam dump is requested. The beam current interlock is active for intensities above 10^{13} protons.

The present beam loss system can handle up to 10 different elementary cycles. A warning, a start and a stop event are required for each of them. The warning event (~ 150 ms before injection) is used to set cycle dependant configuration parameters. A limitation arises presently from the timing system: the event code contains only the particle type (proton/ions = 01, e^+ = 03, e^- = 04) and the cycle number inside the super-cycle (01,02,03,…). Such a scheme does not allow a proper identification of the beam type (i.e. FT, LHC, CNGS…). In the future more information must be transmitted over the timing system in order to properly identify all different beam types. The reception of the timing events is checked by internally the BLM system. If no event is received over an interval of ~40 seconds, the emergency beam dump is triggered. This delay implies that for certain cycles, the system is blind for about one cycle if the correct timing events are not received. In the future the length of the SPS cycle must be transmitted by the General Machine Timing System to improve this situation, as indicated in Chapter 5.

The system as it exists today almost meets the requirements for the future interlock system. New requirements are:

- Independent signals for TT40, TT41, TI2 and TI8. For losses in LSS4, the exiting BLRING system may be sufficient to protect against problems with the orbit bumpers, but additional fast BLMs may be an asset for fast failures. For the CNGS beam in TT41 with 2 fast extractions separated by 50 msec, beam loss interlocks

must be sufficiently fast to prevent the second extraction in case of abnormal losses. For the LHC beam the duration of a complete cycle is available, such an interlock should be implemented as part of the software interlock system.

- Failsafe handling of timing events, which requires a parallel change of the machine timing system to include more information.

7.3.2 SPS Ring Beam Position Interlocks

The beam position in the SPS is presently interlocked to prevent fast growing beam excursions in the horizontal plane. It is based on an analogue system connected to monitors BPH.120 and BPH.122. The output signal is directly connected to the SPS emergency beam. A beam dump is triggered when the oscillation amplitude exceeds 30 mm for intensities above ~10^{13} protons. The response time is ~ 2 turns.

A new digital system is foreseen for both planes based on a coupler in cell 323. This interlock will also be connected to the beam interlock system in 2003.

7.3.3 Extraction Bump Beam Position Interlocks

Special large aperture BPMs (BPCEs) will be installed in LSS4 and LSS6 to measure the position of the bumped beam prior to extraction. A new fast interlock signal must be provided to inhibit the extraction when the beam position is outside a given window. Since the bumped beam position is different for LHC and CNGS beams, the system must be aware of the cycle (beam type) that is being played. The tolerance on the beam position is ±0.6 mm for bump amplitudes of 30 to 40 mm.

7.3.4 Transfer Line Beam Position Interlocks

The beam position measured in the LHC and CNGS transfer lines must be used to prevent further extractions if the position offsets exceed a given threshold. This interlock could be implemented either through a hardware channel or through a software interlock.

7.3.5 Beam Quality Interlocks

Beam quality interlocks concern mainly the LHC beam where such interlocks should ensure that the parameters of the beam sent to the LHC remains within given bounds. But the concept of beam quality is also useful for the other SPS beams.

Beam quality interlocks may be sub-divided into 3 categories:

- Level 1 interlocks that protect the LHC components against damage.
- Level 2 interlocks that protect the LHC against possible quenches or against injection failures that require an abort of the filling sequence, a beam dump in the LHC and a restart of the whole injection from scratch.
- Level 3 interlocks that are only used to maximize the LHC performance.

While level 1 interlocks are mandatory, level 2 and 3 interlocks may not be required immediately for the LHC start-up. A quench at injection, although a nuisance for operation, does not present a risk for the LHC. Level 3 interlocks may possibly be implemented over software rather than hardware interlock channels.

The main quality attributes that have to be interlocked are, in rough order of importance:

- Total beam intensity - Level 1

- Number of batches - Level 2
- Bunch pattern (number of bunches, distance between bunches) - Level 2
- Bunch intensity spread - Level 3
- Presence of ghost bunches (at the level of 1%) - Level 2 / 3.
- Emittance and tails (longitudinal and transverse) - Level 2 / 3.
- Momentum - Level 2 / 3.

The first three beam quality interlocks related to intensity and structure of the LHC beam are likely to become a very important interlocks for an efficient operation of the LHC. Since the instruments used to determine the beam quality are distributed over the SPS ring, the quality interlocks should be connected to the beam (and not the extraction) interlock system to avoid long cable between clients and interlock system. The responsibility for the beam quality interlocks will most likely be distributed between the instrumentation and RF groups.

A reliable interlock based on the SPS BCTs must ensure that the intensity range is always as requested by the LHC or by the SPS operator. This level 1 interlock is crucial to ensure that the beam sent to the LHC never exceeds the intensity range requested by the LHC.

Due to their limited time resolution, the fast BCTs in the SPS cannot resolve ghost bunches. Interlocks on ghost bunches must be provided by the SPS RF system.

The transmission of the beam parameters and their ranges must be addressed in the context of the LHC/SPS/PS signal exchange. The information must be sent in a reliable way to all systems involved in the interlock handling. Part of this information (for example the number of LHC batches) changes from one cycle to the next and must be transmitted over the Machine Timing System, see Chapter 5. More ‘static’ information like the bunch structure, the number of bunches… could be transferred by other means.

Beam quality measurements must be performed at the latest possible moment in the cycle, i.e. ~ 100-200 ms before the extraction time.

7.4 RF System Interlocks

The SPS RF system must provide interlocks on timing and synchronization between SPS and LHC. In the event of a synchronization problem, the extraction pre-pulse signal should not be provided to the extraction kickers, thereby preventing the extraction of the beam to the LHC.

7.5 Vacuum System Interlocks

Presently the vacuum system of the whole SPS complex connected to a single interlock channel. As a consequence valves closed in transfer lines prevent injection of any beam in the SPS. In the future more than one signal must be provided to segment the machine logically into different areas such that local vacuum problems do not affect the whole SPS complex.

The proposed vacuum sectors are TT10+SPS ring, TT20, TT40, TT41, TI8, TT60 and TI2.

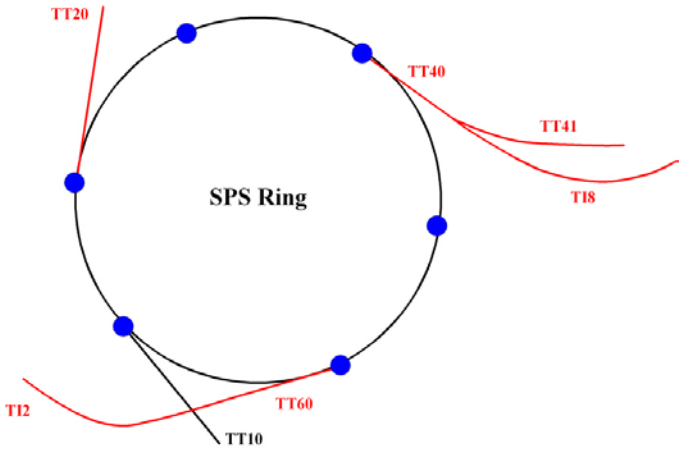

Figure 11 : The proposed interlock sectors for the vacuum system.

7.6 LHC Interlocks

Injection into one of the LHC rings is only possible if :

- The BEAM PERMIT signal is given by the LHC beam interlock loop. This condition ensures that all safety elements of the LHC are ready for beam and that no critical powering faults have been detected [3].
- The settings of all LHC elements are at their injection settings.
- For injection of beam intensities above a given threshold, a low intensity beam must already circulate inside the corresponding LHC ring [11].

Presently only the LHC beam interlock loop signal is clearly defined. An input signal derived from this interlock loop must be provided to the 2 SPS extraction interlock systems in IR2 and IR8.

The settings check of the LHC elements can potentially be surveyed by a software interlock system that has to communicate with the SPS software interlock system to prevent extraction. If the propagation delay between software interlock systems is not sufficient, a direct input of the LHC software interlock system into the SPS extraction interlock system may have to be provided.

To enforce the condition that high intensity beam can only be extracted when beam is circulating in the LHC, interlock signals must provided by the LHC and SPS BCTs to the two SPS extraction systems to prevent the extraction of beam from the SPS whenever no beam is circulating in the LHC while at the same time the requested beam intensity lies above the threshold where a circulating beam is required. This solution requires cables from the BCTs to BA4 and BA6.

7.6.1 LHC Injection Elements

Although the monitoring of state and setting of the LHC injection elements (kicker and septum) must be part of the LHC settings surveillance, it might be desirable to include the state of LHC injection kicker and septa into the SPS extraction interlock system. The magnetic septum provides a horizontal deflection while the kickers deflect the beam vertically, as shown in Figure 12. Failures of the magnetic septum provoke

important damage to the septum itself or to machine components downstream. If the septum is switched off the beam hits the septum itself. For intermediate current errors, the beam may hit the machine elements before it reaches the collimators where it will be stopped and where it can potentially damage the jaws. In the event of a failure of one or more of the kickers, the beam will hit the TDI absorber block.

Since the decision on how to incorporate all LHC interlocks is not finalized, the SPS extraction interlock system should reserve input channels for the LHC injection elements, for the state of the LHC Beam Permit Loop and some spare channels.

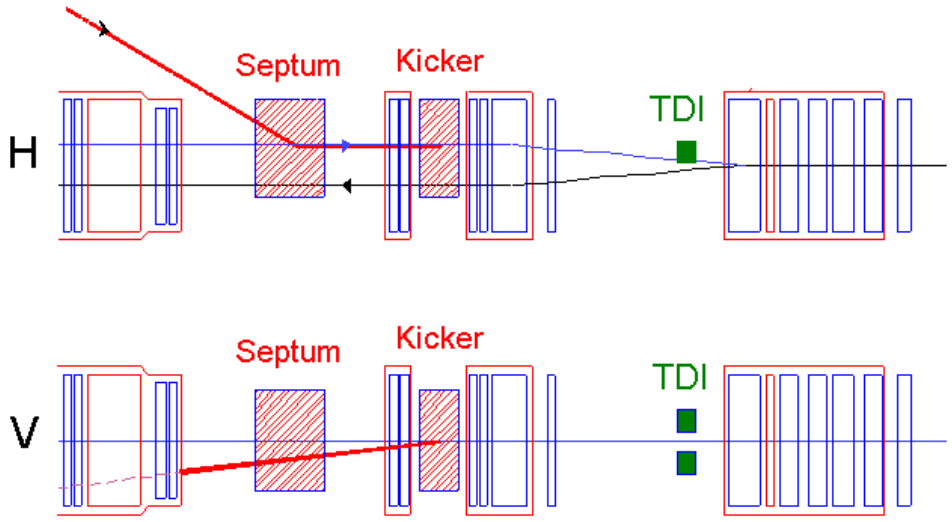

Figure 12 : Layout of the LHC injection area. The septum magnet deflects the beam horizontally while the kicker provides a vertical kick. If one or more kicker modules misfire, the beam hits the TDI absorber block.

7.6.2 LHC Energy Interlock

As soon as the LHC ramp has been triggered, a hardware interlock signal should be sent to the SPS extraction interlock systems to prevent any further extraction.

7.7 TED Dumps

To test the LHC transfer lines when the LHC is not ready for beam, interlocks from the LHC must be masked provided the TED dumps are in place to intercept the beams in the lines. Presently all interlocks related to TED dumps in the SPS are handled by the SSIS system. A software interlock is generated whenever the dump block position does not match the required beam state of the SPS.

Although the present software interlock scheme should be maintained in the future, this scheme alone will not allow an efficient testing of the transfer lines. Since the LHC will provide hardware interlock signals to the SPS extraction interlock system, test of the transfer lines are only possible when the LHC does not set any interlock or when such an interlock is masked. Without a facility to mask the hardware interlocks from the

LHC depending on the position of the dumps, setting up and testing of the lines may systematically require a manual masking of the LHC interlocks.

Consequently the status (IN/OUT/MOVING) of the TED dumps should be provided as input to the extraction interlock system. The signal must be in FAULT state and an interlock set whenever the dumps are out or are moving. The signal must be in state OK when the dumps are in beam, and the interlock must be combined with the LHC requests or interlocks using an OR logic.

The LHC interlocks that must be masked (ignored) are:

- ***Downstream TED TI8 in position IN***: all LHC ring 2 hardware interlocks.
- ***TED TT40 in position IN***: all hardware interlocks related to CNGS, LHC ring 2, the TT41 and TI8 lines.
- ***Downstream TED TI2 in position IN***: all LHC ring 1 hardware interlocks.
- ***TED TT60 in position IN***: all hardware interlocks related to LHC ring 1 and TI2.

Furthermore, the Software Interlock system must inhibit the beam according to TED position and the requested mode of the SPS, see section 6. When the SPS mode is '*BEAM_TO_LHC*', an alarm and interlock should be set whenever the TED dump is IN beam (which does not match the request for beam to the LHC). Beam must be allowed in the SPS with the TED inserted IN beam when the SPS mode is '*BEAM_TO_TI2(8)_TED*'. Such a software interlock will prevent sending the beam to the TEDs by mistake and avoid useless activation of the TED.

If NO hardware signal is provided by the TED dumps, masking the LHC interlocks requires:

- Either a manual intervention by the operator while the software interlock system ensures that SPS mode and position of the TEDs are consistent.
- Or a more complex logic within the interlock controls that must set automatic masks derived from the SPS mode, thus adding more problems of software and secure information exchange with the interlock system.

7.8 CNGS Target Interlocks

Interlocks on the CNGS T40 target will include the target position and the status of the cooling stations. A large number of input channels will be provided to the software interlock systems, since those alarms are not time critical.

7.9 Software Interlock System

A software interlock system, either in its present form or with a new design compatible with multi-cycling, must complement the hardware interlock system.

The software interlock system must provide additional surveillance and information of all critical machine components.

The software interlock system has the possibility to request a beam stop independently of the hardware interlocks. A dedicated input channel is reserved for this system in the beam interlock system.

The software interlock system should be used in the future to latch interlocks that occur repeatedly for a given beam type or cycle. When the number of successive interlocked cycles exceeds a given threshold, the software interlock systems should request a beam stop for the corresponding beam.

8 Planning and Milestones

8.1 SPS machine planning

The first extraction tests in LSS4 are foreseen for September 2003, where low intensity beams below any damage threshold (maximum intensity of ~ 2 10^{11} protons/extraction) will be extracted and send to the TED dump at the end of the TT40 line.

In 2004 the TI8 line will be commissioned to the downstream TED dump. First beam tests are foreseen in May 2004.

In 2006 beams will be send towards the CNGS target and towards the LHC ring 2 through TI8. The CNGS beams will have intensities of few 10^{13} protons/pulse. This intensity is largely above the damage threshold for machine components. An extraction interlock system and the associated client signals must be available in 2006.

8.2 SPS interlock system planning

The following milestones are proposed for the SPS interlock system:

- A proto-type SLIC module should be prepared for the 2003 extraction test, or at the latest for the 2004 extraction tests. During the 2004 run, the SLIC modules must be tested under realistic conditions. No SCIC module is a priori required for 2003 and 2004 since only LHC beams will be extracted during dedicated machine experiments.
- The new SPS beam interlock system, including the BEAM PERMIT LOOP should be installed in 2005 to profit from the one-year shutdown of the SPS. At the same time the extraction interlock systems must be installed in LSS2, LSS4 and LSS6.
- The full system must be tested in 2006.

9 Conclusions

A conceptual design for the new SPS hardware interlock system was presented in this report. The system that is proposed has several properties :

- It is compatible with a multi-cycling SPS machine.
- The use of timing is minimized within the interlock system itself, although its use can be extended when sufficient experience is gained or when new requirements arise.
- The system flexibility can be enhanced further by a more systematic use of timing signals in the system.
- The components of this interlock system are compatible with the LHC system. Interfaces to clients will be identical for the SPS and the LHC.

10 References

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11 Glossary

System or signal name	Description
SPS EMERGENCY INTERLOCK SYSTEM	Present interface between the SPS beam dump system and its clients.
SPS SOFWARE INTERLOCK SYSTEM (SSIS)	The present software surveillance system.
BEAM INTERLOCK SYSTEM	The system, including electronics and links to enable the BEAM PERMIT and issue BEAM DUMP REQUESTS
EXTRACTION INTERLOCK SYSTEM	The system, including electronics and links to enable the EXTRACTION PERMIT.
BEAM PERMIT LOOP	Optical fiber link between the BEAM INTERLOCK SYSTEM modules that transmits the BEAM PERMIT signal.
BEAM PERMIT	The signal that enables beam: ***YES*** : beam can be injected / circulated. ***NO*** : no beam can be injected / circulated. A transition from YES to NO generates a BEAM DUMP REQUEST.
EXTRACTION PERMIT	The signal that is send to the extraction kicker and that enables an extraction: ***YES*** : the beam can be extracted. ***NO*** : the beam cannot be extracted. A transition from YES to NO before the moment of extraction generates a BEAM DUMP REQUEST.
BEAM INTERLOCK CONTROLLER (BIC)	Electronic module designed for the LHC that handles interlock signals related to the LHC beam. The 16 BIC modules in the LHC are distributed over the 8 access points and are linked together by the LHC BEAM PERMIT LOOP.

12 Appendix A

Table 3 : Interlock modules and expected input signals for the LSS4 extraction. 4 SLIC modules (SLIC.LSS4.1/2/3/4) and one SCIC are foreseen. All SLIC/SCIC modules are installed in BA4, with the exception of SLIC.LSS4.4 installed in SR8.

Interlock Module	Interlock signals			
	Location	No.	Name	Comments
SLIC.LSS4.1	BA4	101	TT40 PCs & magnets	
SLIC.LSS4.1	BA4	102	TT40 vacuum valves	
SLIC.LSS4.1	BA4	103	TT40 Beam losses	
SLIC.LSS4.1	BA4	104	Bumped beam position at BP.418	
SLIC.LSS4.1	BA4	105	MSE septum current	
SLIC.LSS4.1	ECA4	106	MKE kicker	
SLIC.LSS4.1	BA4	107	Orbit bumper magnets	
SLIC.LSS4.2	BA4	201	TT41/TI8 main dipole PC	MBG410 - identical to No. 301
SLIC.LSS4.2	BB4	202	TT41/TI8 switch PC	MBSG410 - identical to No. 302
SLIC.LSS4.2	BB4	203	TT41 PCs & magnets	Quadrupoles
SLIC.LSS4.2	BB4	204	TT41 PCs & magnets	Orbit correctors
SLIC.LSS4.2	BA4	205	TT41 vacuum valves	
SLIC.LSS4.2	BA4	206	TT41 beam losses	
SLIC.LSS4.2	BA4	207	TT41 trajectory	Optional : possibly SW Intlk
SLIC.LSS4.2	TSG4[1]	208	ν Target T40	
SLIC.LSS4.3	BA4	301	TT41/TI8 main dipole PC	MBI 816 - identical to No. 201
SLIC.LSS4.3	BB4	302	TT41/TI8 switch	MBSG410 - identical to No. 202
SLIC.LSS4.3	BA4	303	TI8 PCs & magnets	Quadrupoles
SLIC.LSS4.3	BA4	304	TI8 PCs & magnets	Orbit correctors
SLIC.LSS4.3	BA4	305	TI8 vacuum valves	
SLIC.LSS4.3	BA4	306	TI8 beam losses	Optional : possibly SW Intlk
SLIC.LSS4.3	BA4	307	TI8 trajectory	Optional : possibly SW Intlk
SLIC.LSS4.4	SR8	401	TI8 PCs & magnets	Downstream quadrupoles
SLIC.LSS4.4	SR8	402	TI8 PCs & magnets	Downstream orbit correctors
SLIC.LSS4.4	SR8	403	TI8 downstream TED	
SLIC.LSS4.4	SR8	404	LHC request ring 2	
SLIC.LSS4.4	SR8	405	LHC spare ring 2	
SCIC.LSS4	BA4	1	SLIC.LSS4.1 OUT signal	SLIC output signal
SCIC.LSS4	BA4	2	SLIC.LSS4.2 OUT signal	SLIC output signal
SCIC.LSS4	BA4	3	SLIC.LSS4.3 OUT signal	SLIC output signal
SCIC.LSS4	SR8	4	SLIC.LSS4.4 OUT signal	SLIC output signal
SCIC.LSS4	ECA4	5	TT40 TED	

For Table 3, it has been assumed that the interlock signals for the main dipoles strings (No. 201/301) and for the switch dipoles (No. 202/302) are split into two identical signals that are used in the SLICs responsible for the TT41 and TI8 line. Alternatively it can be envisaged to use only a single signal from each of those PCs, but as direct inputs to the SCIC module that has in that case 2 additional inputs (directly from the clients and

[1] CNGS service gallery

not through a SLIC). At least 2 spare channels must be available for each interlock module.

The TED in TT40 must be connected directly to the SCIC module since its state determines whether the TI8 and TT41 interlocks can be ignored or not.

Table 4 : Interlock modules and expected input signals for the LSS6 extraction. 3 SLIC modules (SLIC.LSS4.1/2/3/4) and one SCIC are foreseen. All SLIC/SCIC modules are installed in BA6, with the exception of SLIC.LSS4.4 installed in SR2. One should note that the upstream PCs for TI2 are installed in BA7 and not in BA6.

Interlock Module	**Interlock signals**			
	Location	**No.**	**Name**	**Comments**
SLIC.LSS6.1	BA6	101	TT60 PCs & magnets	
SLIC.LSS6.1	BA6	102	TT60 vacuum valves	
SLIC.LSS6.1	BA6	103	TT60 beam losses	
SLIC.LSS6.1	BA6	104	Bumped beam position at BP.618	
SLIC.LSS6.1	BA6	105	MSE septum current	
SLIC.LSS6.1	BA6	106	MKE kicker	
SLIC.LSS6.1	BA6	107	Orbit bumper magnets	
SLIC.LSS6.2	BA7	201	TI2 PCs & magnets	Upstream quadrupoles
SLIC.LSS6.2	BA7	202	TI2 PCs & magnets	Upstream orbit correctors
SLIC.LSS6.2	BA6	203	TI2 vacuum valves	
SLIC.LSS6.2	BA6	204	TI2 beam losses	Optional : possibly SW Intlk
SLIC.LSS6.2	BA6	205	TI2 trajectory	Optional : possibly SW Intlk
SLIC.LSS6.3	SR2	301	TI2 PCs & magnets	Downstream quadrupoles, main dipoles.
SLIC.LSS6.3	SR2	302	TI2 PCs & magnets	Downstream orbit correctors
SLIC.LSS6.3	SR2	303	TI2 downstream TED	
SLIC.LSS6.3	SR2	304	LHC beam interlock loop ring 1	
SLIC.LSS6.3	SR2	305	LHC spare ring 1	
SCIC.LSS6	BA6	1	SLIC.LSS6.1 OUT signal	SLIC output signal
SCIC.LSS6	BA6	2	SLIC.LSS6.2 OUT signal	SLIC output signal
SCIC.LSS6	SR2	3	SLIC.LSS6.3 OUT signal	SLIC output signal
SCIC.LSS6	BA6/BA7	4	TT60 TED	

It can be envisaged to merge the TI2 signals originating from BA6 (203 to 205) with the SLIC.LSS6.1 module, at the price of a modest reduction in flexibility (no beam allowed in TT60 when TI8 is in 'fault', even with the TT60 TED in beam). In such a case SLIC module SLIC.LSS6.2 could be moved to BA7 (location of the upstream TI2 power converters) or be completed suppressed. At least 2 spare channels must be available for each interlock module.

Table 5 : Interlock modules and expected input signals for the LSS2 extraction. A single SCIC module is sufficient.

Interlock Module	Interlock signals			
	Location	**No.**	**Name**	**Comments**
SCIC.LSS2	BA2	1	ZS electrostatic septum	
SCIC.LSS2	BA2	2	MSE/MST magnetic septa	
SCIC.LSS2	BA2	3	TT20 TED	

Table 6 : List of the expected input signals to the SPS beam interlock system.

Site building	Interlock signal	Comment
BA1	BL Ring Sextant 1	
BA1	BLD LSS1 + TT10	Fast beam losses LSS1 / injection
BA1	Ring Vacuum	
BA1	Main Power Supplies (MPS)	
BA1	MPS Fast Chain	Fast transients on 18 kV
BA1	TT10 PC surveillance	Possible future PC surveillance for TT10
BA1	Beam Dump Internal Fault	
BA1	Beam Dump Energy Tracking	
BA1	Beam Dump no trigger	
BA1	Beam Dump beam tracking	
BA1	Software interlock system	Input signal from software interlock system
BA1	Beam Position > 30 mm	Existing beam position interlock
BA2	BL Ring Sextant 2	
BA2	BLD LSS2 + TT20	Fast beam losses LSS2 / extraction
BA2	Extraction Interlock System LSS2	SCIC beam dump request
BA3	BL Ring Sextant 3	
BA3	RF	
BA3	Software interlock system	Input signal from software interlock system
BA3	BCT (ramp losses)	
BA3	BCT (beam structure)	Quality interlock from FBCT
BA3	Beam Position	New beam position interlock
BA4	BL Ring Sextant 4	
BA4	BLD LSS4 + TT40	Fast beam losses LSS4 / extraction
BA4	Extraction Interlock System LSS4	SCIC beam dump request
BA4	Extraction kicker mode	Interlock set when the kicker is in LOCAL mode.
BA5	BL Ring Sextant 5	
BA6	BL Ring Sextant 6	
BA6	BLD LSS6 + TT60	Fast beam losses LSS6 / extraction
BA6	Extraction Interlock System LSS6	SCIC beam dump request
BA6	Extraction kicker mode	Interlock set when the kicker is in LOCAL mode.

As an alternative to the proposed scheme, it can be envisaged to connect the extraction interlock systems for LSS2, LLS4 and LSS6 directly to the BEAM PERMIT LOOP. At least 2 spare channels must be available for each interlock module.

12.1 Preliminary inventory of the SPS Interlock System

The estimated inventory of interlock modules for the SPS ring and transfer lines is:

- 6 interlock modules and an interlock loop for the SPS beam interlock system.
- 1 SCIC module for the LSS2 extraction interlock system (slow extracted beam).
- 4 SLIC and 1 SCIC module for the LSS4 extraction interlock system (CNGS and LHC ring 2).
- 3 SLIC and 1 SCIC module for the LSS6 extraction interlock system (LHC ring 1).

The entire system requires 13 SLIC and 3 SCIC modules.

13 Appendix B : Layouts

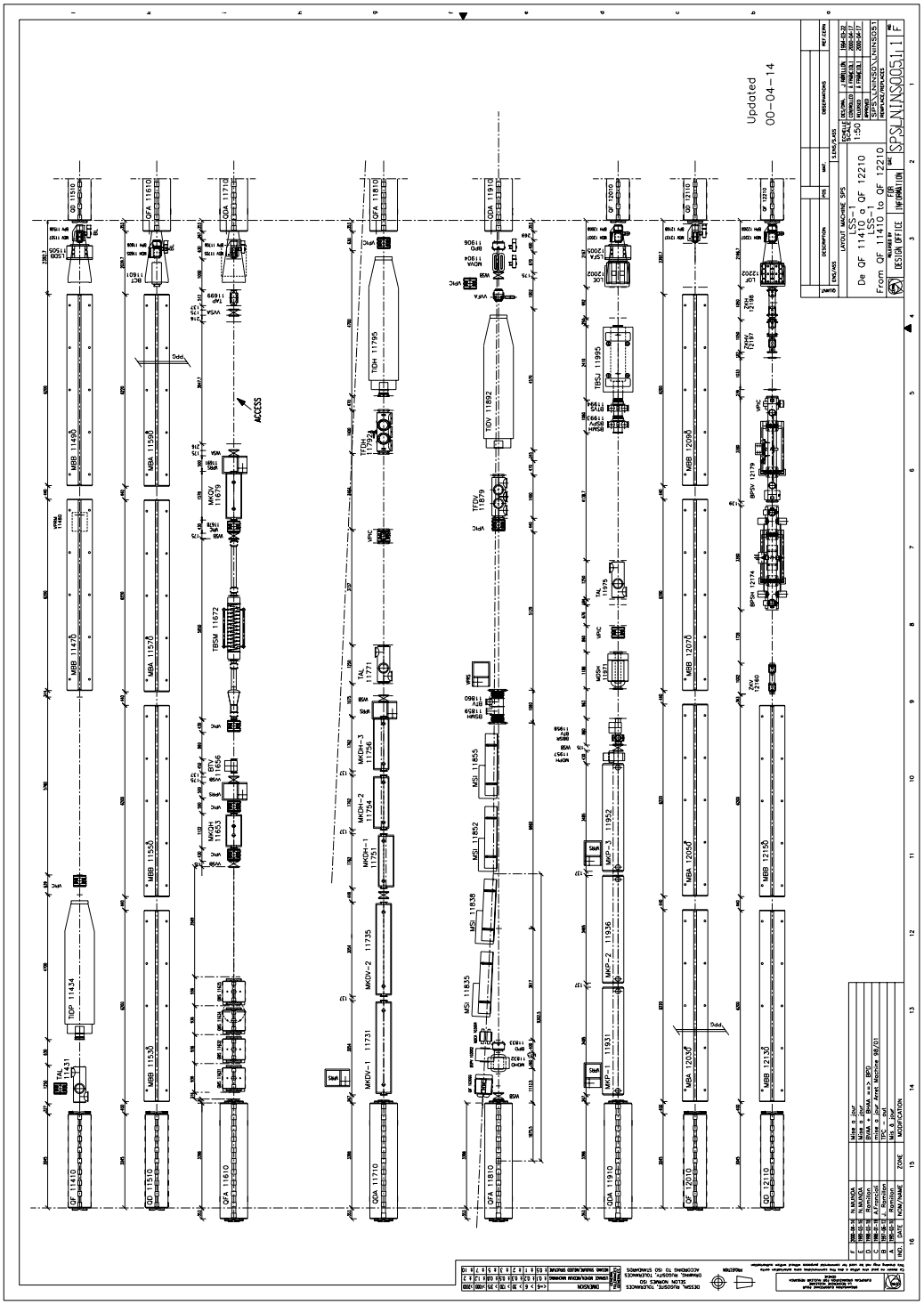

Figure 13 : Layout of the SPS injection and beam dump area in LSS1.