Design and Test of a Power Board for an intelligent PMT for the JUNO-Detector

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Abstract

JUNO is a reactor anti-neutrino experiment currently under construction in Jiangmen, China. The aim of this experiment is the determination of the neutrino mass hierarchy. The JUNO detector is located at a distance of $53\,\mathrm{km}$ from two nuclear power plants. The instrumented volume has a mass of $20\,\mathrm{kt}$ liquid scintillator, which is monitored by 18000 20" and 25000 3" photomultiplier tubes (PMT). With an optical coverage of $78\,\%$, an energy resolution of $3\,\%$ at $1\,\mathrm{MeV}$ can be achieved. This resolution is needed to distinguish the inverted and the normal mass hierarchy. The data taking is planed to start in 2021.
In order to read out the large photomultiplier tubes, a novel readout concept is developed, where the analog signals are digitized directly at the sensor. This so-called intelligent PMT (iPMT) transmits the digitized data to back-end cards outside the central detector. The readout electronics mounted at the PMT consists of a base, a high voltage unit, a control unit including the analog-to-digital converter and the Power Board.
The Power Board, which is presented in this thesis, supplies all different systems of the iPMT. In addition, the data driver and receiver are placed on the board. Strict requirements on the performance concerning data transmission and the output voltage ripple have to be fulfilled.
The power lines of the analog and the digital part are strictly separated and the direct-current/direct-current converters are designed advisedly to achieve a low ripple. Despite the focus on low voltage noise a total efficiency of $88\,\%$ is achieved. The data transfer to the back-end system is done with a synchronous link for trigger and clock information and an Ethernet link for read-out data.
The non-accessibility of the electronics requires a high reliability and stability of the boards. Based on the reliability data of selected manufacturers, a failure rate for the Power Board is estimated. The predicted rate is 40.4 failures per $10^9\,\mathrm{h}$ with a confidence level of $60\,\%$. The stability of the output of the DC/DC converters is measured with various methods and conservative stability criteria are fulfilled.
In preparation of the mass production of 18000 Power Boards, test methods are developed to quickly determine all critical characteristics. The setup is successfully tested with 96 Power Boards.

Kurzfassung

JUNO ist ein Reaktor-Neutrino-Experiment mit dem Ziel die Neutrino-Massenhierarchie zu bestimmen. Der JUNO-Detektor wird aktuell in Jiangmen, China, in einem Abstand von $53\,\mathrm{km}$ zu zwei Atomkraftwerken gebaut. Der zentrale Detektor besteht aus $20\,\mathrm{kt}$ flüssigem Szintillator, in welchem Neutrinos wechselwirken und Energie deponieren. Das erzeugte Licht wird von 18000 20" und 25000 3" Photomultipliern (PMT) detektiert. Damit erreicht der Detektor eine Energieauslösung von $3\,\%$ bei einer Energie von $1\,\mathrm{MeV}$, welche nötig ist um die normale und die invertierte Massenhierarchie zu unterscheiden. Die Datennahme des JUNO Experiments wird voraussichtlich 2021 starten.

Für die Auslese der großen Photomultiplier wurde ein neuartiges Konzept entwickelt. Dabei wird die Ausleseelektronik direkt an den PMTs angebracht. In diesem intelligenten PMT (iPMT) Konzept werden die analogen Signale am PMT digitalisiert und an die verarbeitende Elektronik außerhalb des zentralen Detektors gesendet. Die Ausleseelelektronik am PMT besteht aus einem Spannungsteiler, einer FPGA-Platine, die auch den Analog-Digital-Umsetzer beherbergt, und einer Spannungswandler- und Verteilungsplatine (eng. Power Board, Abk. PB).

Das PB, welches in dieser Arbeit beschrieben wird, versorgt alle Systeme des iPMTs. Zusätzlich sind die Sender und Empfänger für die Kommunikation auf der Platine untergebracht. Es müssen hohe Anforderungen an die Spannungs-Restwelligkeit und die maximal übertragbaren Datenraten erfüllt werden.

Die Spannungsversorgung für die analogen und digitalen Systeme sind strikt getrennt um eine möglichst geringes elektronisches Rauschen zu erreichen. Obwohl die Spannungswandler auf eine geringe Restwelligkeit optimiert sind, wird eine Effizienz von insgesamt $88\,\%$ erreicht. Die ausgelesenen Daten werden über eine Ethernet Verbindung übertragen, während Trigger- und Taktsignale über synchrone Verbindungen gesendet werden.

Da die Elektronik im Detektor nicht austauschbar ist, wird eine hohe Ausfallsicherheit und Stabilität verlangt. Die Ausfallrate wird mit Hilfe von Herstellerangaben abgeschätzt, wobei die Hersteller strenge Qualitätsanforderungen erfüllen müssen. Die berechnete Ausfallrate sind 40.4 Ausfälle in $10^9\,\mathrm{h}$. Die Stabilität der Spannungswandler wird bestimmt und konservative Kriterien werden erfüllt.

Um die Massenproduktion der Platinen vorzubereiten, werden Tests für eine schnelle Überprüfung vorbereitet. Die Methoden des Schnelltests konnten erfolgreich mit 96 Platinen getestet werden.

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Chapter 1

Introduction

The neutrino was postulated by Wolfgang Pauli in 1930 to conserve the energy and the momentum in the beta decay. More than 25 years later, the neutrino was detected directly in a reactor experiment using liquid scintillator as a target material [1]. With the detection of the neutrino the investigation of the neutrino properties began and continues to this day. In 1968, the Homestake experiment showed a significant discrepancy between the expectation and the actual solar neutrino flux [2]. Further experiments confirmed this deficit in the following decades using different detector principles.
The so-called solar neutrino problem was not solved until 1998, when the Super-Kamiokande experiment showed first direct evidence for neutrino oscillation. The results showed that muon neutrinos from cosmic air showers change their flavour depending on the energy and the travelled distance [3]. Furthermore, in 2002 the Sudbury Neutrino Observatory (SNO) was able to demonstrate that the solar neutrino flux is consistent with solar models when all neutrino flavours are included [4].
Since the detection of neutrino oscillations several experiments have been carried out to gain a better understanding of the mechanism. Reactor neutrino experiments like Double Chooz [5], Daya Bay [6] and Reno [7] were built to determine the smallest mixing angle $\sin\theta_{13}$ using liquid scintillator as a target material.
Based on the experience from these experiments the concept for the Jiangmen Underground Neutrino Observatory (JUNO) was developed. The main goal of JUNO is to determine the neutrino mass hierarchy using reactor neutrinos. However, the target volume of the detector is increased significantly compared to previous generations[1] to compensate for the reactor-detector distance of $53\,\mathrm{km}$.
The larger detector requires a new readout concept to match the increased size and number of channels. In order to tackle these challenges the intelligent photomultiplier concept (iPMT) is developed. The readout electronics are mounted to the photomultiplier tube (PMT) increasing the performance and simplifying the scalability. The core of the electronics is a novel ADC, developed at the FZ Jülich, in combination with an FPGA.

[1] Double Chooz: $8\,\mathrm{t}$, Daya Bay: $20\,\mathrm{t}$, Reno: $16\,\mathrm{t}$, JUNO: $20000\,\mathrm{t}$

The FPGA can perform a first analysis of the data and can for example generate trigger signals or compress the data. A long-term objective is to reduce the data stream to single photons with timing information.
This thesis describes the design and test of the Power Board (PB) which is part of the electronic system mounted to the PMT providing the power and handling of the data streams. The boards fulfils high voltage ripple requirements by strictly separating the power supplies for digital and analog systems. The low voltage ripple should ensure an optimal performance of the system. The data connection to the back-end cards is done with an Ethernet connection and synchronous links. In preparation for the mass production quick test methods are designed and demonstrated using 96 Power Boards.
The JUNO physics goals require a long operation and stable operation. Therefore, only $1\,\%$ of all channels should fail during the first 6 years. In the new concept the readout electronics is not interchangeable in case of a failure. In order to reach this requirement an extensive reliability investigation is done and the results are used to calculate an upper limit on the Power Board failure rate.

Chapter 2

Theory of Neutrino Oscillation

It is a well-established fact that three neutrino flavours couple through neutral and charged current interactions to standard model particles. Additionally, it was shown that the probability to measure a certain neutrino flavour changes periodically depending on the neutrino energy and travel distance. The oscillations imply that the lepton number is not conserved. In the model of quantum mechanics the oscillations can be explained by the difference between the flavour and the mass eigenstates of the neutrinos [8][9]. The flavour eigenstates $(\nu_e, \nu_\mu, \nu_\tau)$ can be written as a linear combination of the mass eigenstates (ν_1, ν_2, ν_3):

$$|\nu_l\rangle = \sum_j U_{lj}\nu_j \tag{2.1}$$

In this notation l denotes the flavour, j the mass eigenstate and the U_{lj} the neutrino mixing matrix. This so-called Pontecorvo-Maki-Nakagawa-Sakata (PMNS) matrix is a unitary matrix and usually divided into three rotations:

$$\begin{aligned} U_{\text{PMNS}} &= \begin{pmatrix} 1 & & \\ & c_{23} & s_{23} \\ & -s_{23} & c_{23} \end{pmatrix} \begin{pmatrix} c_{13} & & s_{13}e^{i\delta} \\ & 1 & \\ -s_{13}e^{-i\delta} & & c_{13} \end{pmatrix} \begin{pmatrix} c_{12} & s_{12} & \\ -s_{12} & c_{12} & \\ & & 1 \end{pmatrix} \\ &\quad \times \text{diag}(1, e^{ia_{21}/2}, e^{ia_{31}/2}) \\ &= \begin{pmatrix} c_{12}c_{13} & s_{12}c_{13} & s_{13}e^{-i\delta} \\ -s_{12}c_{23} - c_{12}s_{23}s_{13}e^{i\delta} & c_{12}c_{23} - s_{12}s_{23}s_{13}e^{i\delta} & s_{23}c_{13} \\ s_{12}s_{23} - c_{12}c_{23}s_{13}e^{i\delta} & -c_{12}s_{23} - s_{12}c_{23}s_{13}e^{i\delta} & c_{23}c_{13} \end{pmatrix} \\ &\quad \times \text{diag}(1, e^{i\alpha_{21}/2}, e^{i\alpha_{31}/2}) \end{aligned} \tag{2.2}$$

Where, $c_{ij} = \cos(\theta_{ij})$, $s_{ij} = \sin(\theta_{ij})$ and δ is the Dirac CP-violating phase. The additional diagonal matrix includes the two Majorana CP-violating phases α_{21} and α_{31}, which can be absorbed if neutrinos are Dirac particles. In case of Majorana particles, the anti-particle is identical with the particle $\nu_j = \bar{\nu}_j$ [8]. Lepton number violating processes are investigated to solve this question, e.g. the search for the neutrino less double beta decay [10].

Table 2.1: Best-fit values for the 3-flavour neutrino oscillation model and the 3σ allowed ranges. For the Dirac phase δ, the 2σ range is given, as 3σ include all physical values. The values correspond to the normal hierarchy ($m_1 < m_2 < m_3$), while the values in brackets correspond to the inverted hierarchy ($m_3 < m_1 < m_2$). The definition of Δm^2 is: $\Delta m = m_3^2 - (m_2^2 + m_1^2)/2$ [8].

Parameter	Best-Fit	3σ
Δm^2_{21} $[10^{-5}\,\mathrm{eV}^2]$	7.37	$6.93 - 7.97$
$\lvert\Delta m^2\rvert$ $[10^{-3}\,\mathrm{eV}^2]$	2.50 (2.46)	$2.37 - 2.63$ $(2.33 - 2.60)$
$sin^2\theta_{12}$	0.297	$0.250 - 0.354$
$sin^2\theta_{23}$	0.437 (0.569)	$0.379 - 0.616$ $(0.383 - 0.637)$
$sin^2\theta_{13}$	0.0214 (0.0218)	$0.0185 - 0.0246$ $(0.0186 - 0.0248)$
δ/π	1.35 (1.32)	$0.92 - 1.99$ $(0.83 - 1.99)$

The current best-fit neutrino oscillation parameters can be found in table 2.1. Although the massive neutrinos add 7 (9 for Majorana particles) parameters to the minimal standard model, the oscillation can be described by 6 (or often less) parameters for current experiments. The absolute neutrino mass does not affect the neutrino oscillation for relativistic neutrinos and the Dirac phase can only be limited by few experiments [8].
The sign of the larger mass square difference is one of the last unknown parameters. Equations 2.3 and 2 show that the sign of Δm_{31} (and Δm_{32}) depends on the mass hierarchy.

$$\Delta m^2_{31} = m_3^2 - m_1^2 \tag{2.3}$$

$$m_1 < m_2 < m_3, \text{ Normal Hierarchy}$$
$$m_3 < m_1 < m_2, \text{ Inverted Hierarchy}$$

While the sign of Δm_{31} remains unknown the sign of the smaller mass square difference is chosen to be positive. The two independent absolute mass square differences can be interpreted as the oscillation frequencies, which differ by a factor of

$$|\Delta m^2_{31}|/\Delta m^2_{21} \approx |\Delta m^2_{32}|/\Delta m^2_{21} \approx 30.$$

The mass square difference $\Delta m_{31} (\approx \Delta m_{32})$ is also called $\Delta m_{\text{atmosphere}}$ and Δm_{21} is noted as Δm_{solar} as they can be measured in according experiments. The composition and ordering of the mass eigenstates for normal hierarchy (NH) and inverted hierarchy (IH) can be seen in figure 2.1.
The oscillation probability of a neutrino is defined as the probability that a neutrino produced as flavour α is detected as flavour β in a detector. Using the PMNS-matrix, the

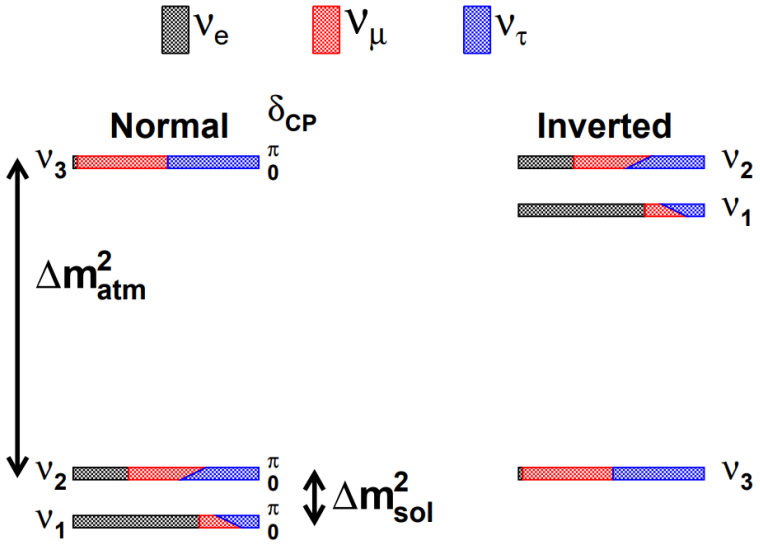


Figure 2.1: Ordering and composition of the neutrino mass eigenstates in the normal and the inverted case. The changing flavour composition as a function of δ_{CP} is indicated [11].

time evolution of the flavour eigenstates can be calculated assuming highly relativistic particles, which is fulfilled for all current and planned experiments. Equation 2.4 shows the probability of oscillation in vacuum assuming that the PMNS matrix is unitary, which is consistent with current measurements [8][12].

$$P_{\alpha\to\beta} = \left| \sum_j U^*_{\alpha j} U_{\beta j} e^{-\frac{m_i^2 L}{2E}} \right|^2 \tag{2.4}$$

For reactor neutrino experiments – like JUNO – the survival probability of electron anti-neutrinos can be calculated using equation 2.4 and the PMNS-matrix 2.2:

$$\begin{aligned} P_{\bar{\nu}_e\to\bar{\nu}_e} = 1 &- \sin^2 2\theta_{12} \cos^4\theta_{13} \sin^2\Delta_{21} \\ &- \sin^2 2\theta_{13} \cos^2\theta_{12} \sin^2\Delta_{31} \\ &- \sin^2 2\theta_{13} \sin^2\theta_{12} \sin^2\Delta_{32} \end{aligned} \tag{2.5}$$

Here Δ_{ij} includes the travelled distance L, the neutrino energy E and the mass square difference Δm_{ij}:

$$\Delta_{ij} = \frac{\Delta m^2_{ij} L}{4E} \tag{2.6}$$

The probability equation in 2.5 can be rewritten using the effective mass-squared differences e.g.:

$$\Delta m^2_{ee} = cos^2\theta_{12}\Delta m^2_{31} + sin^2\theta_{12}\Delta m^2_{32} \tag{2.7}$$

Here higher orders are neglected [13]. The effective mass-squared differences are sensitive to the MH and are therefore used to display the JUNO sensitivity.
The vacuum oscillation probability is sufficient for the JUNO reactor measurement, as matter effects are negligible for reactor experiments [12].

Chapter 3

The JUNO Experiment

The Jiangmen Underground Neutrino Observatory (JUNO) is a $20\,\mathrm{kt}$ multi-purpose liquid scintillator detector currently under construction in Jiangmen, China. In August, 2014 the JUNO collaboration was founded with the main objective to determine the neutrino mass hierarchy using a reactor neutrino experiment. The experimental site is located $53\,\mathrm{km}$ from two power plants with a maximal thermal power of $\approx 2 \times 18\,\mathrm{GW}$ (see figure 3.1).

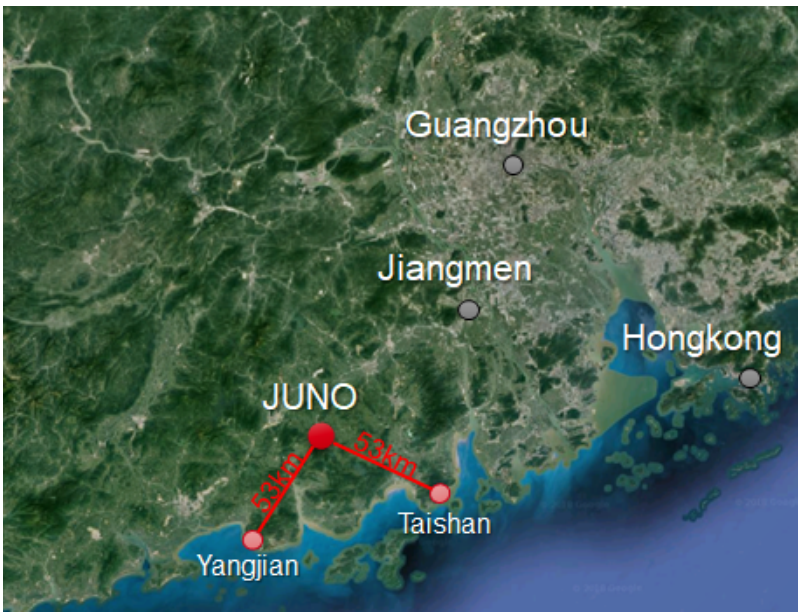


Figure 3.1: Location of the JUNO detector in southern China.

3.1 Physics with JUNO

The main goal of the JUNO experiment is the determination of the neutrino mass hierarchy. Furthermore, the large fiducial mass and good energy resolution of the detector offer a perfect environment for an extended physics program.

3.1.1 Neutrino Mass Hierarchy

The expected reactor neutrino spectrum for normal and inverted hierarchy as a function of the travel distance and energy can be seen in figure 3.2. The large reduction compared to the non oscillation is dominated by the slow oscillating $\sin^2 2\theta_{12}$-term which is approximately 10 times larger in amplitude than the $\sin^2 2\theta_{13}$-terms (see equation 2.5). The small variations are a result of the interference of the terms including the mass square differences Δm^2_{31} and Δm^2_{32}.
In order to separate the hierarchies, the energy resolution of JUNO has to be better than $3\,\%$ at $1\,\mathrm{MeV}$ with an energy scale linearity of $< 1\,\%$, which were two of the main requirements during the design phase. To maintain the resolution during most of the lifetime, less than $1\,\%$ of the channels should fail during the first 6 years [12].

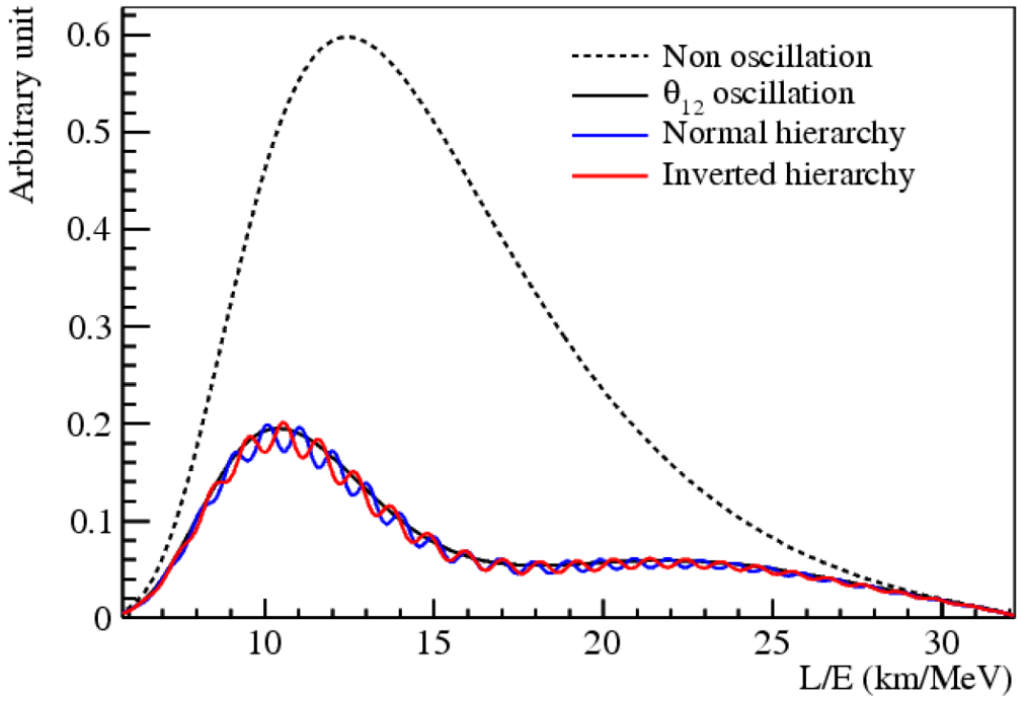
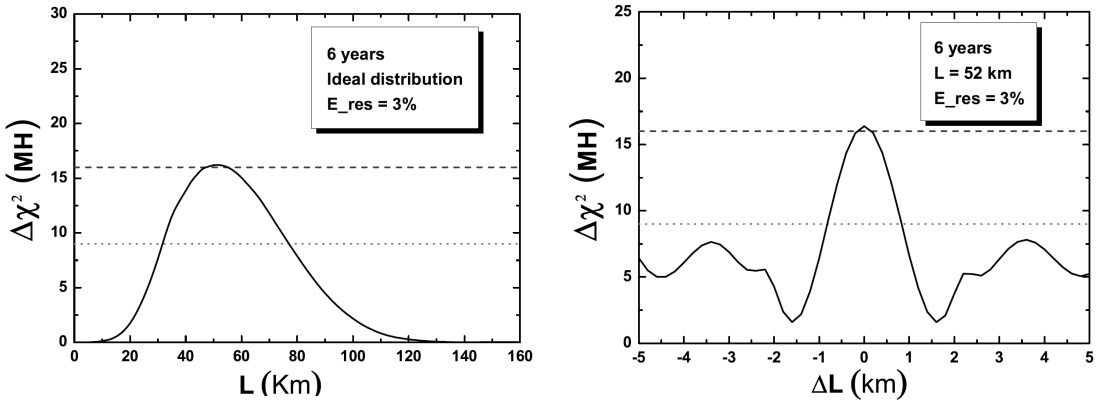


Figure 3.2: Shape difference between normal and inverted hierarchy of the reactor electron anti-neutrino spectrum for JUNO [12].

The sensitivity of JUNO strongly depends on the distance to the reactors (see figure 3.3(a)) and the baseline differences between the different reactor cores (see figure 3.3(b)). Other nuclear reactors close to JUNO, namely Daya Bay[1] and Huizhou[2] nuclear power plants, will smear out the neutrino spectrum. Figure 3.4(a) shows the sensitivities for the ideal and the real case, including the baseline differences and the other NPPs. All 10 reactor cores will be within a range of $\approx 700\,\mathrm{m}$ leading to a sensitivity reduction of $\Delta\chi^2 = 3$. However, the sensitivity of JUNO can be increased significantly by measuring the effective mass-squared difference $\Delta m_{\mu\mu}$ to the $1\,\%$ level (see figure 3.4(b)), which could be done by a long baseline muon-neutrino disappearance experiment. All in all, a sensitivity of $3 - 4\sigma$ will be achieved by the JUNO experiment after 6 years of measurement(see figure 3.4(b))[12].



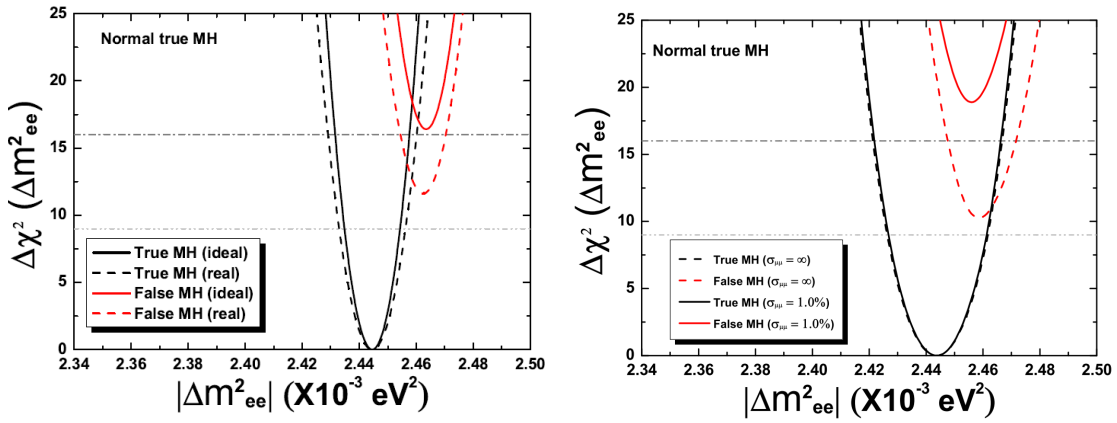
(a) (b)

Figure 3.3: Discrimination ability of the JUNO experiment in dependence on the distance for a single reactor (a). Figure (b) shows the sensitivity as a function of the baseline difference of two detectors [12].

3.1.2 Extended Physics Program

Since JUNO is doing an exact measurement of the reactor neutrino spectrum, several neutrino oscillation parameters, namely $\sin^2\theta_{12}$, Δm^2_{21} and $|\Delta m_{31}|$, can be determined with a precision of better than $1\,\%$. In combination with other future and current experiments this will allow to test the unitarity of the PMNS matrix to the $1\,\%$ level.
In case of a galactic core-collapse supernova at a distance of $10\,\mathrm{kpc}$, JUNO will measure ≈ 5000 neutrino events from the inverse beta decay and ≈ 2000 events from elastic scattering, thus being able to measure a supernova neutrino spectrum. In combination with

[1]Distance: $215\,\mathrm{km}$
[2]Distance: $265\,\mathrm{km}$



(a) (b)

Figure 3.4: (a) Sensitivity of JUNO in an ideal and real setup and (b) with and without an accurate measurement of $\Delta m_{\mu\mu}$. [12].

other detectors, like gravitational waves and optical measurements, a detailed picture and thus a great understanding of a supernova explosion will be developed. In addition, JUNO might be able to detect the diffuse supernova neutrino background produced by continuous supernovae explosion throughout the universe.
If the radio-purity of JUNO is excellent (e.g. ^{238}U : $10^{-16}\,{}^{\mathrm{g}}/_{\mathrm{g}}$) the instrument will be able to measure solar neutrinos. Unlike reactor-neutrinos, these events have no distinct signature and are indistinguishable from radioactive events. The high energy resolution and low energy threshold of JUNO could improve current solar neutrino measurements greatly.
Another important part of the JUNO physics program are geoneutrinos, which are produced by radioactive materials, mainly Uranium and Thorium, in the earth crust. Around 400 geoneutrinos will be detected in JUNO per year enabling high statistic measurements with geoneutrinos. Within the first 6 month JUNO will double the world-wide geoneutrino data [14, 12].

3.2 Detector Design

The detector design of JUNO is motivated by the requirements from the physics program:

- $3\,\%$ energy resolution at $1\,\mathrm{MeV}$
- energy scale linearity of $1\,\%$
- radio-purity
- large target mass

These requirements are on the same or higher level of current liquid-scintillator neutrino detectors, while a much larger target volume is necessary.

3.2.1 Experimental Site

The experimental site is located close to two nuclear power plants near Jiangmen, China. The detector is placed below a small hill within a deep underground cavern, which will add up to a total overburden of $\approx 700\,\mathrm{m}$ granite. The shielding corresponds to $2000\,\mathrm{m}$ water equivalent reducing the atmospheric muon rate to about $3\,\mathrm{Hz}$. The cavern will be accessible through two independent shafts, one vertical and one inclined with a slope of $42\,\%$. On the surface – close to the exit of the sloped tunnel – will be storage facilities, accommodation and parts of the liquid scintillator purification and storage system [12].
The ground breaking was in 2015 and the civil construction will be finished in 2020.

3.2.2 Central Detector

The heart of the JUNO detector is a liquid scintillator target enclosed by an acrylic sphere with a diameter of $35.4\,\mathrm{m}$, that is supported by a steel truss (see figure 3.5). Energy deposited within the liquid scintillator, for example by charged particles, leads to light emission. Thereby, the emitted light is proportional to the deposited energy, hence liquid scintillator can be used for calorimetric detectors. Liquid scintillator is the only material that combines large target volumes (like water), great energy resolution and a low energy threshold. Additionally, the fast scintillation component of the liquid scintillator is around $\approx 3\,\mathrm{ns}$ enabling a good vertex reconstruction [15].
The detection of the emitted photons is done with photomultiplier tubes (PMTs), which is currently the best possibility for large area single photon detection. A coverage of $78\,\%$ of the inner volume is achieved by using approximately 18000 large PMTs (20") and 25000 small PMTs (3").
The small PMTs are mounted between the large PMTs and are not considered to increase the optical coverage, but should improve the linearity at high energies and enhance the time resolution of the central detector. The improved timing resolution might improve the position reconstruction. All PMTs are mounted on the steel truss submerged into a water

buffer.
The water buffer surrounding the central detector acts as shielding and is additionally monitored by PMTs acting as a veto system. The veto PMTs are mounted on the steel truss facing outward and on the bottom of the cavern. Moreover, on the top of the water pool, a muon tracker will be installed to measure the muons entering the main tank. The tracker modules are plastic scintillator modules from the decommissioned OPERA experiment [16]. In order to maximise the efficiency a 3-layer layout is considered, leading to a coverage of $25\,\%$ of the water buffer. Centrally in the main detector, a chimney connects the central detector to the outside for filling and calibration.

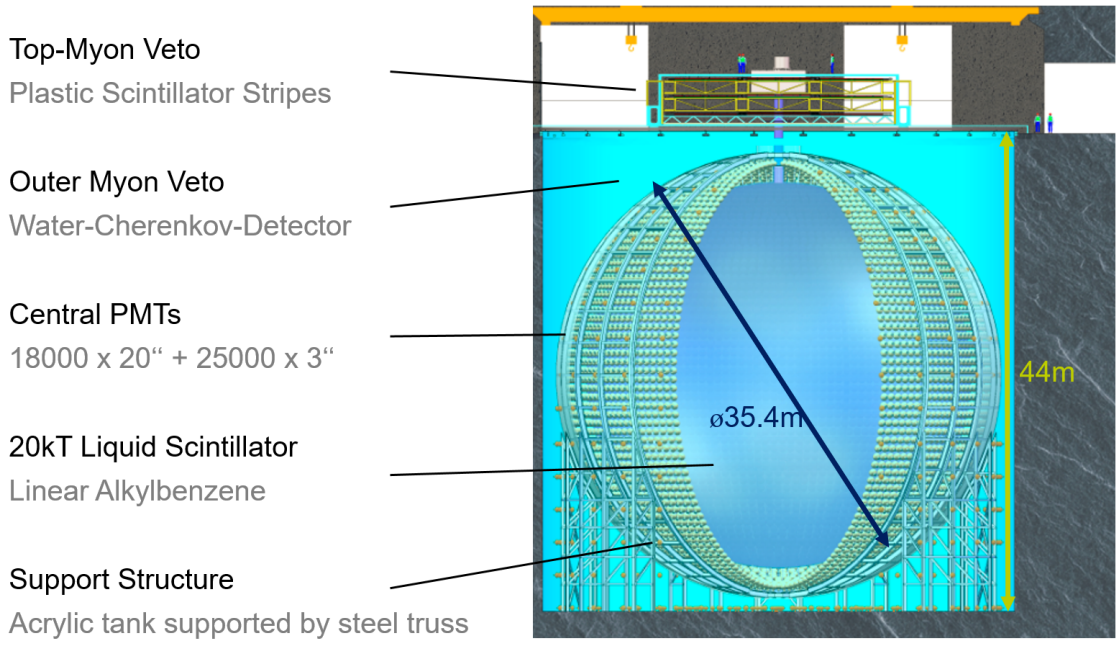


Figure 3.5: Schematic view of the central detector of the JUNO experiment.

3.2.3 Detection Channel

The main detection channel for reactor neutrinos is the inverse beta decay (IBD), where an anti-electron neutrino $\bar{\nu}_e$ interacts with a proton and reacts into a positron and a neutron (see figure 3.6). The positron loses energy and annihilates with an electron, leading to a prompt signal, while the neutron scatters in the detector until it is thermalized. A proton captures the thermalized neutron after $\approx 220\,\mu\mathrm{s}$ and emits a $2.2\,\mathrm{MeV}$ photon. The combination of a prompt and a delay signal leads to a good separation from radioactive events. The threshold for the interaction is approximately

$$E_{\text{threshold}} = m_e + m_N - m_P \approx 1.8\,\mathrm{MeV}. \tag{3.1}$$

The neutrino energy can be reconstructed from the positron energy, as it carries most of the kinetic energy, since $m_e \ll m_n$[17]. When the full thermal power of the reactors of $36\,\mathrm{GW}$ is achieved a rate of 83 IBD events per day is expected [12].

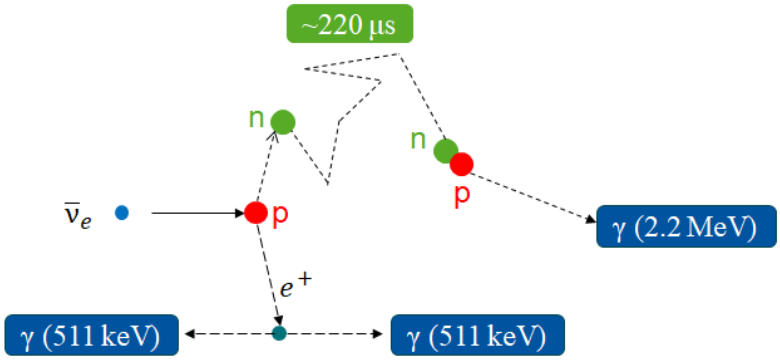


Figure 3.6: Schematic representation of the inverse beta decay.

3.2.4 Liquid Scintillator

The liquid scintillator (LS) used is a linear alkylbenzene (LAB), which is an organic compound, and is similar to the one used in Daya Bay. LAB has a great transparency, a good light yield, a high flash point and a low chemical reactivity, fulfilling all physics and safety requirements. Added into the LAB are 2,5-diphenyloxazole (PPO) as a flour and p-bis-o-methylstyryl-benzene (bis-MSB). The energy deposited in the LAB leads to an emission of $290\,\mathrm{nm}$ photons, which are shifted by PPO - the primary wavelength shifter - and the secondary wavelength shifter Bis-MSB into the blue range of the visible spectrum ($430\,\mathrm{nm}$) to be detected by the PMTs. Currently, the concentration of the shifter is optimzied with $3\,\mathrm{g/l}$ PPO and $15\,\mathrm{g/l}$ bis-MSB as a baseline from Daya Bay[12].
In order to reach the desired resolution of $3\,\%$ at $1\,\mathrm{MeV}$, 1200 photoelectrons (p.e.) have to be detected at $1\,\mathrm{MeV}$. Around 10000 photons per MeV are emitted by the liquid scintillator [18]. Therefore, an attenuation length of approximately $20\,\mathrm{m}$ has to be reached, considering primarily absorption processes. Scattered photons can still contribute to the energy resolution, since only the directional information is lost. For purified samples, attenuation length of $20\,\mathrm{m}$ have been found, with the scattering length and absorption length of $40\,\mathrm{m}$ each [19].
The purification of the LS will be done on the detector site.

3.2.5 Photomultiplier Tubes

The second key element – apart from the liquid scintillator – are the photomultiplier tubes. Figure 3.7 shows a brief explanation of the dynode PMT principle. A PMT is a vacuum tube with an opening window, a photo cathode and amplifier electronics [20]. Photons enter through the window into the tube, where it excites an electron of the photo cathode. The electron moves through an electric field to the amplifier electronics and gets multiplied with a typical gain of 10^7. Finally, the current signal is collected, lead to the outside and measured by external electronics.

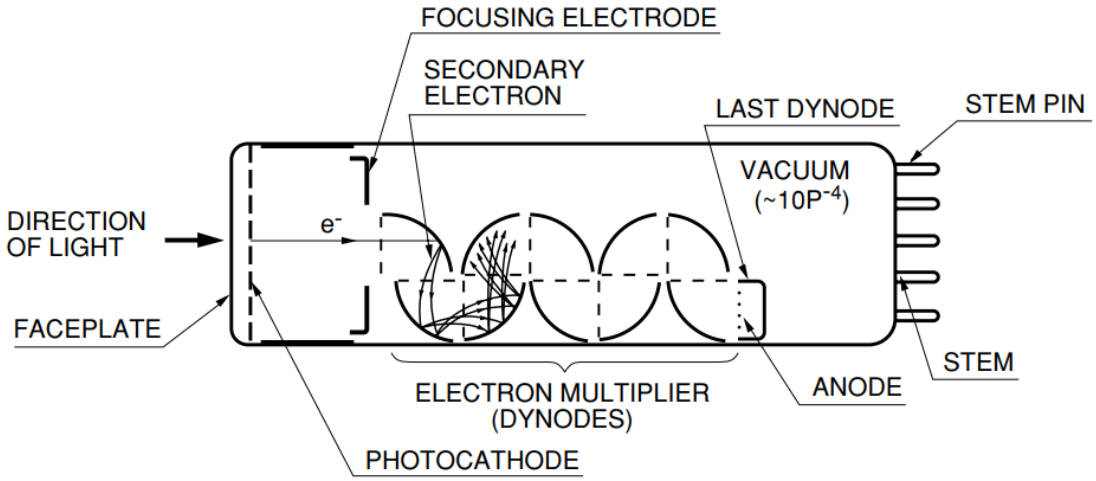
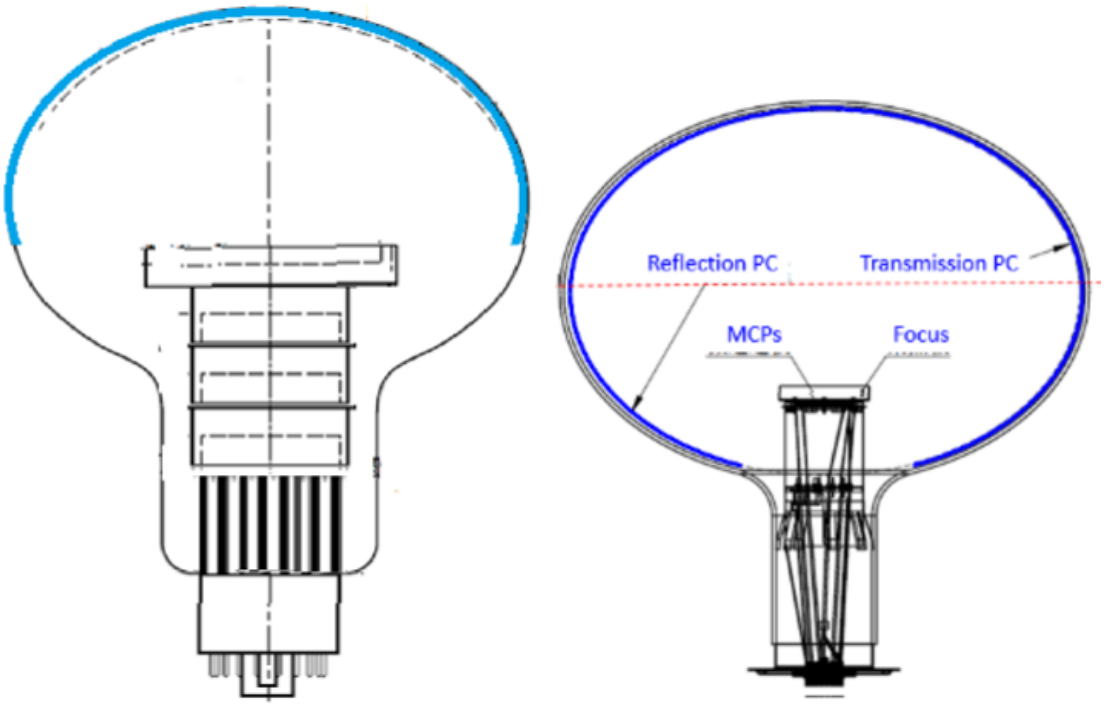


Figure 3.7: Schematic of the principle of a Dynode PMT [20].

Two different amplification methods can be used. Firstly the well-established dynode structure, where the electrons are accelerated towards the dynodes by an applied high voltage and multiplied through secondary electron emission (see figure 3.7). The second method is the so-called multichannel plate (MCP) amplification, that is also used for night vision devices. Thereby, the electrons get accelerated through microscopic channels and multiply by interactions with the channel walls. Typically, MCP based PMTs have a better time resolution due to the more compact amplification setup. However, for the JUNO MCP-PMTs the transient time spread of the photo-electrons is high, due to the additional reflective photo cathode.
For the central detector of JUNO two different kind of 20" PMTs are used. 5000 PMTs are dynode PMTs provided by Hamamatsu (R12860) and 15000 MCP-PMTs produced by NNVT (see figure 3.8). All large PMTs should have a quantum efficiency of at least 26 % and a dark rate below 20 kHz (50 kHz for MCP) [21, 22].
The 25000 small 3-inch PMTs are supplied by HZC and have a slightly lower quantum efficiency of 24 %. Due to the small photo cathode, the dark rate is $\approx$ 1 kHz. Groups of

128 PMTs are connected to an underwater box and read out by a multichannel front-end readout board. This system is completely independent of the large PMT system and will provide an independent second energy calibration using photon counting technology [23]. The large PMTs are currently tested using a container testing system for standard properties, like efficiency, and a scanning station for enhanced measurements [24].



(a) (b)

Figure 3.8: Schematic view of the dynode PMT (a) and the MCP-PMT (b). Apart from the difference in the amplification, the PMTs also differ in the size of the photo cathode. To increase the quantum efficiency the MCP-PMT has an additional cathode at the backside of the PMT [22].

Chapter 4

JUNO Readout Concept

The size of neutrino detectors increases with each generation. In order to read out these detectors, new readout concepts are being investigated. During the process, various critical points are considered:

1. Signal quality and linearity
   - Good signal-to-noise ratio
   - Timing resolution $1\,\mathrm{ns}$
   - Resolution $0.1 - 1000\,\mathrm{p.e.}$
2. Power consumption
3. Trigger
4. Reliability

The first three points are driven by the size of the JUNO detector, while the last element is a general problem for particle physics experiments with life times of several years or decades. The signal quality is determined by two major factors, firstly the transfer from the sensor to the digitizer and secondly the analog-to-digital converter itself. Typically, the transfer of the signal is done passively for photomultiplier tubes, as the internal amplification is sufficient. As a result of the size of JUNO the cables from the PMTs to the outside of the central detector have a length of up to $100\,\mathrm{m}$, which decreases the signal-to-noise ratio (SNR). The low SNR leads to a decreased timing resolution and a lower quantum efficiency due to the higher threshold necessary, which decreases the overall JUNO performance.
The power consumption is limited by the cooling in the cavern and the connection to the electric grid. The great number of channels limits the power to $\approx 15\,\mathrm{W}$ per channel for the readout electronics.
In small detectors like Double Chooz the readout and trigger system has front-end electronics to split the analog signal and transfer it to a trigger and a digitizer module separately. The number of channels in JUNO makes this approach impractical. Therefore, the

trigger generation is included into the digitizer board, a concept also proposed for the new HyperK detector [25].
The reliability of the channels is critical for the main goal of JUNO. In order to reach the desired sensitivity, no more than $1\,\%$ of the channels must fail in the first 6 years of operation. In consequence, all non-exchangeable components, like cables and inaccessible electronics, are optimized.
From these criteria emerged the intelligent PMT (iPMT) concept. The idea is to digitize the signal as close as possible to the base to get the best performance. Thus, the readout electronic is connected directly to the PMT base. As a result of this concept, no cable is needed between base and the analog-to-digital converter, improving the performance further. The matching of the PMT to a $50\,\Omega$ cable is usually done with resistors, which leads to reflections and hence a smaller signal.
The concept is scalable because the PMTs operate – aside from possible external triggers – independent of each other. All in all the iPMT should be a good solution for large and also small experiments using PMTs as a readout system.

4.1 Design

The readout electronics mounted to the PMT are divided into four major parts designed by different working groups, namely the High Voltage Unit (HVU), the Power Board (PB), the General Control Unit (GCU) and the base. The schematic buildup can be seen in figure 4.1.

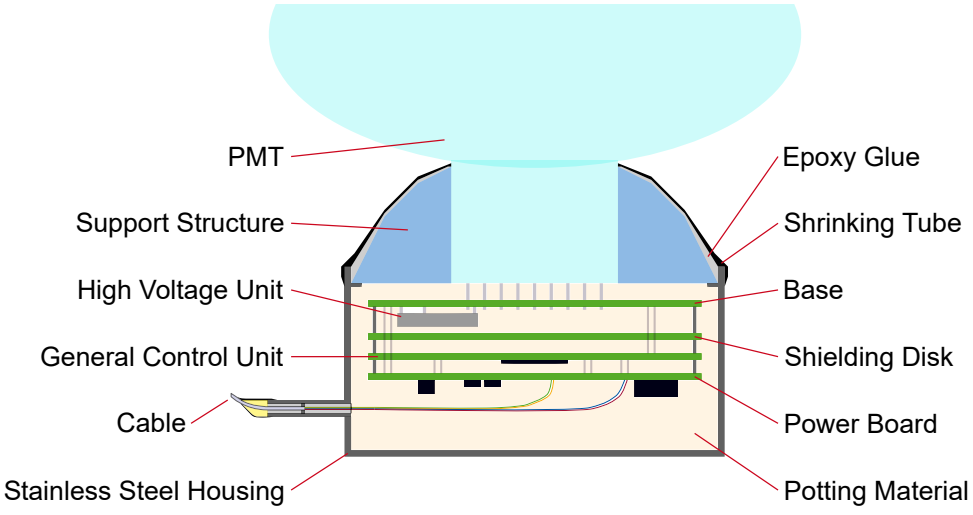


Figure 4.1: Schematic setup of the intelligent PMT including the current potting approach.

The first of the three boards is the base, which is soldered directly to the PMT and includes the HVU. The next layer contains the GCU, including the ADC and some computing power for the intelligent PMT. The final board is the Power Board which generates and distributes all required voltages and in addition receives and transmits all communication. The electronics will be potted in a non-conductive material, like mineral oil or silica gel, inside a stainless steel housing. The housing is glued to the glass of the PMT using two-component epoxy glue. In between the GCU and the base is a copper disk foreseen to shield the PMT from the electromagnetic interference (EMI) of the coils placed on the PB and GCU. The cable to the outside is connected to the PB.
The connection to the back-end electronics is done with a standard Ethernet cable with 4 differential pairs with $100\,\Omega$ impedance.

4.2 Base

The base is designed by a group from the Institute for High Energy Physics (IHEP) in Beijing. It distributes the different voltages to the different amplifier stages of the PMT. This module is the only one which is different for MCP and dynode PMTs. One prototype version of the final board, which was designed in Aachen for testing purposes, can be seen in figure 4.2, including the HV module.

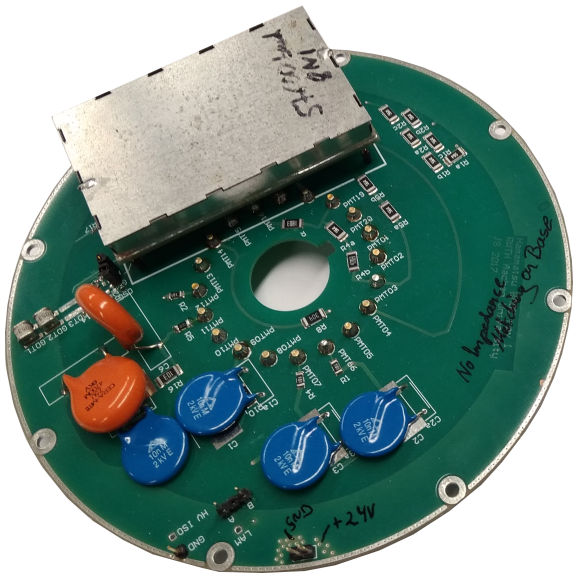


Figure 4.2: Picture of the prototype base for a Hamamatsu PMT designed by Jochen Steinmann.

4.3 GCU

The general control unit is the central part of the intelligent PMT with the VULCAN ADC as the crucial component. In figure 4.3 a simplified version of the GCU structure, which is developed by a working group in Padova, Italy, is shown.
The connection to the outside is based on two independent systems, firstly an Ethernet connection for read-out data and programming the FPGA and secondly a synchronous link for the clock and trigger information. The programming of the main FPGA is done using a second FPGA, so that problems in the programming can never lead to unresolvable problems. The analog signal is digitized by VULCAN and transmitted to the FPGA via 20 LVDS lines running at 500 MHz. During times of high event rates, like supernovae, raw data can be written to DDR3 memory to prevent data loss.
The high voltage unit is controlled via an RS485 connection and is monitored and regulated to stabilise the gain of the PMT over time. In addition, several slow monitoring parameters like input currents, voltages and the temperature are measured and analyzed.

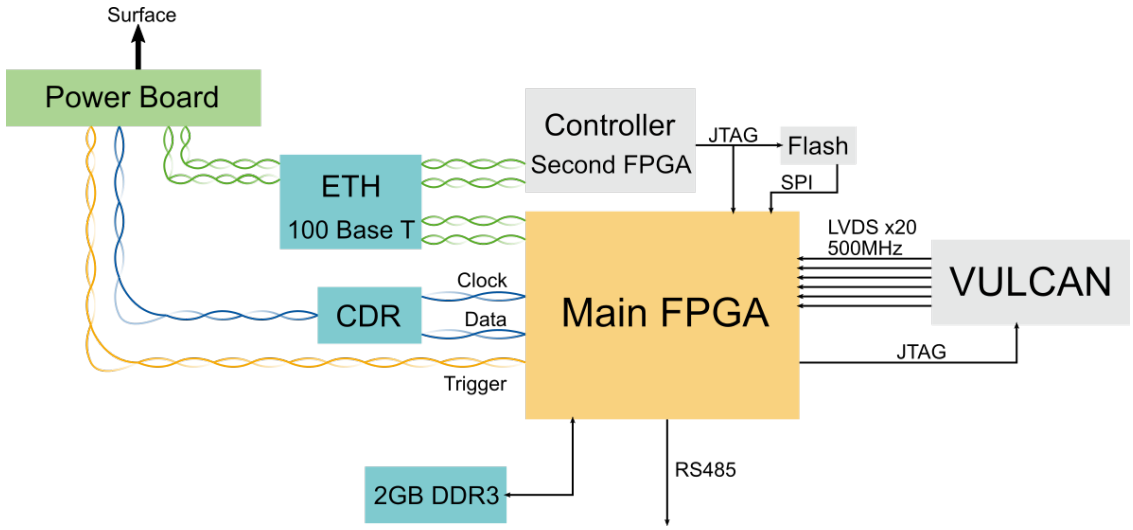


Figure 4.3: Simplified schematic of the GCU structure developed in Padova, Italy.

4.3.1 VULCAN Receiver Chip

The VULCAN chip is a novel readout chip designed by the ZEA-2 in the FZ Jülich. VULCAN is a highly-integrated receiver chip, which includes the analog front-end electronics and the analog-to-digital converter. The chip is equipped with 3 ADCs with programmable input impedance to increase the linearity, while keeping a high resolution at low voltages, as can be seen in figure 4.4.

Additonal important features are the active overshoot compensation and the baseline regulation. The overshoot compensation is preventing deadtime after high pulses by counteracting the overshoot, while the baseline regulation precludes baseline variations. The data output is actively reduced in case of noise [26].
A prototype of the VULCAN receiver have been produced and first tests are successful.

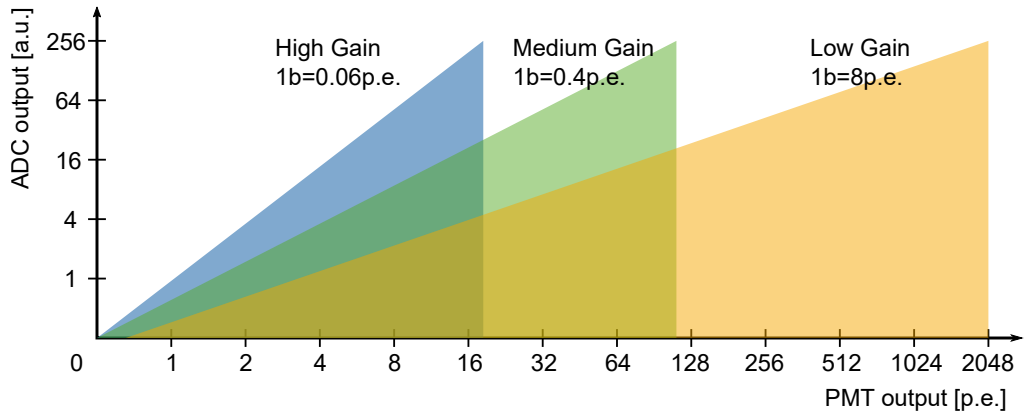


Figure 4.4: Possible configuration of the Vulcan front-end for the 3 ADCs. In this case, the resolution is below 0.1 p.e. for low photo-electron counts, while the total range of the receiver chip goes up to 2000 p.e.

4.4 High Voltage Unit

The high voltage unit (HVU) provides the voltage for the PMT and is controlled by the GCU. It is designed by a working group from Dubna, Russia, which has already designed HV-modules for other physics experiments.
The output voltage range is from 1500 V to 3000 V, with a maximum output current of 300 µA. A first prototype used in several tests can be seen in figure 4.5. In the current design the HVU is placed on the base. The HVU can be operated via an RS485 connection allowing constant adjustments, while the PMT gain is monitored.

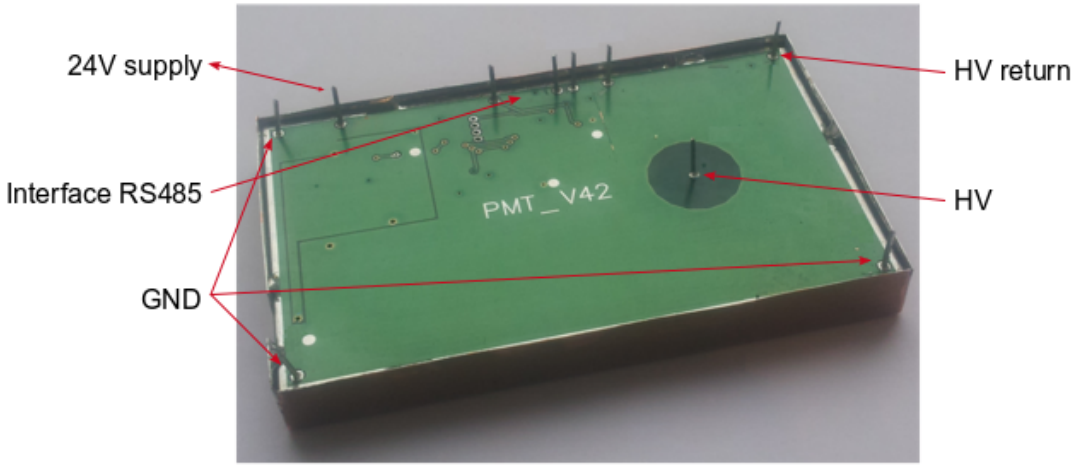


Figure 4.5: Picture of a prototype of the HVU from Dubna [27].

4.5 Power Board

The Power Board (PB) provides all voltages required by the different modules and also carries the Ethernet transformer and LVDS driver and receiver. This module is designed in the 3. Physikalisches Institut B at the RWTH Aachen and topic of this thesis. The PB is explained in detail in chapter 5.

4.6 Back-End Card

The back-end card (BEC) is the counterpart to the Power Board on the outside of the central detector and is designed at the Université Libre de Bruxelles. Figure 4.6 shows a simplified concept of the BEC for a single channel.
The main function is the injection of the power and data streams on the Ethernet cable connected to the Power Board. Important to notice is that the two injected voltages should have different ground levels, since the ground is connected on the GCU. The different voltage drops over the cable for the independent power lines have to be accounted by leaving one ground level floating.

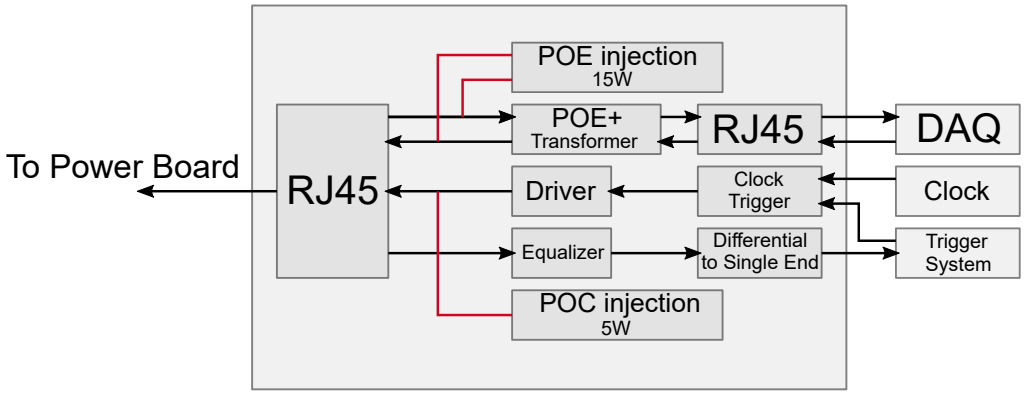


Figure 4.6: Simplified concept for one channel of the BEC by Yifan Yang.

Chapter 5

Power Board

In this chapter a detailed overview over the Power Board is given. The requirements for the Power Board arise from the overall concept and the requirements of the different modules.

5.1 Requirements

5.1.1 Connection to Back-End Card

The under water electronics is connected to the outside of the detector using a $100\,\mathrm{m}$ Cat5e Ethernet cable. An overview over the different assignments of the four cable pairs can be found in table 5.1. Two pairs are dedicated to a $100\,$Mbit/s Ethernet connection including Power-over-Ethernet (PoE). Through one remaining pair the clock and a superimposed trigger signal is sent, while the last pair is the live-uplink sending trigger signals. The data on the clock and trigger lines is Manchester encoded, so a transmission of $250\,$Mbit/s leads to an effective data rate of $125\,$Mbit/s (see figure 5.1). The advantage of this encoding is that it enables the recovery of a clock signal [28].

Table 5.1: Cable partitioning for the JUNO iPMT concept.

	Data	Power	Cable Usage
BEC $\rightarrow$ GCU	$250\,$Mbit/s Clock Trigger Accept	$24\,\mathrm{V}$	1 pair
GCU $\rightarrow$ BEC	$250\,$Mbit/s Trigger	-	1 pair
Data link/Ethernet	$100\,$Mbit/s Data Slow Control	$48\,\mathrm{V}$	2 pairs

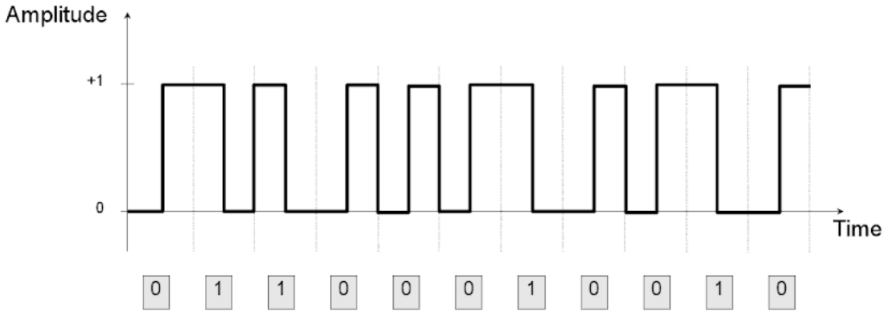


Figure 5.1: Example of Manchester encoding. The information is optained from the rising and falling edge of the signal [28].

5.1.2 Power Distribution

The PB has to supply three different modules, the General Control Unit, the High Voltage Unit and the VULCAN chip. The VULCAN chip is located on the GCU, but to minimize the voltage ripple a separate voltage supply on the PB is foreseen.
The GCU is provided with a voltage of $12\,\mathrm{V}$ at a maximal load of $15\,\mathrm{W}$, using the Power-over-Ethernet rail. All additional voltages needed, to operate the FPGA, are generated on the GCU-board.
VULCAN requires two voltages with tight voltage-ripple constraints. Therefore, a clean voltage is generated from the Power over Clock (PoC) supply. The ripple constrains of both voltages are $10\,\mathrm{mV}$ without bandwidth limitation. An alternative ADC is designed by the Tsinghua University, the Tsinghua ADC. It requires a supply voltage of $6\,\mathrm{V}$ with a maximal current of $1\,\mathrm{A}$ and a ripple requirement of $10\,\mathrm{mV}$. The HVU needs a supply voltage of $24\,\mathrm{V}$ with a maximal current of $100\,\mathrm{mA}$ and a maximal voltage ripple of $20\,\mathrm{mV}$. The POC input voltage of $24\,\mathrm{V}$ is filtered and send to the HVU.
All supply requirements are summarized in table 5.2.

Table 5.2: Voltage requirements for the Power Boards and expected supply currents.

Module	Voltage [V]	Current [mA]	Ripple [mV]
GCU	12.0	800	20
HVU	24.0	100	20
VULCAN	3.3	200	10
VULCAN	1.8	180	10
Tsinghua	6	1000	10

5.1.3 Data Transmission

Driver and receiver of the the clock and trigger signals are placed on the PB and are transmitted to the GCU, where the clock-data recovery and the trigger generation is done. After the power is removed from the Ethernet link using magnetics the data is fed through to the GCU.
In addition the slow control of the PB is connected to the GCU-board via an I^2C interface[1].

5.2 Implementation

The implementations are done on a round board with a diameter of $14\,\mathrm{cm}$. The size origins from the metal disk at the bottom of the MCP-PMTs.
Figure 5.2 gives an overview of the different areas on the PB. Thick red lines indicate ground separation, which is only crossed by some silicon chips, common-mode-chokes (CMC) and the Ethernet transformer. Two cable pairs end on the analog part (bottom left area) and two pairs are connected to the digital area (right). Four holes in the middle of the PCB are foreseen to mount the cable using cable ties.

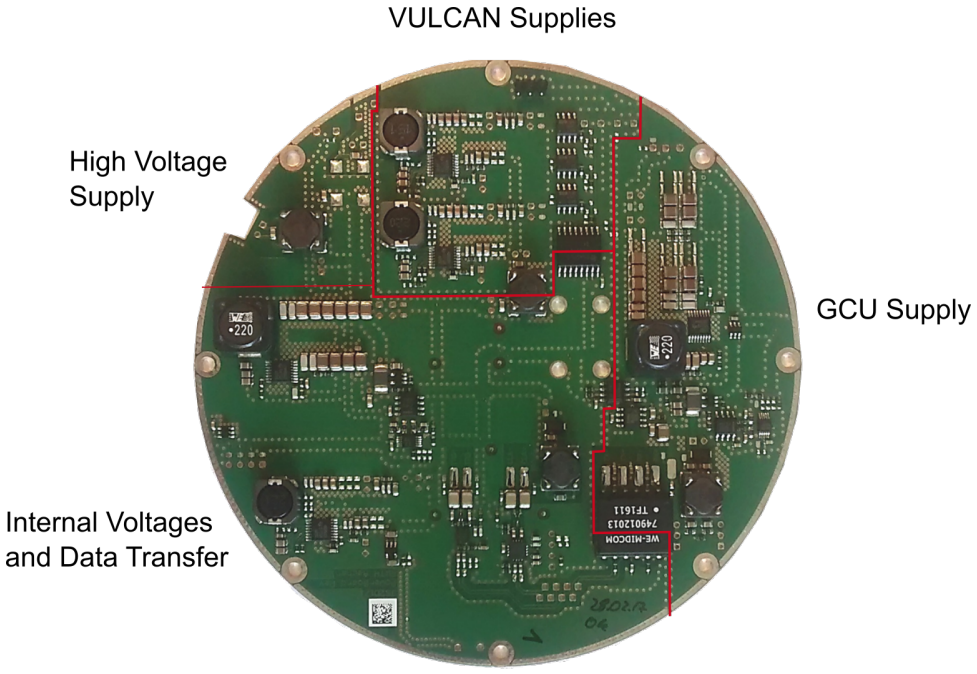


Figure 5.2: Overview over the Power Board. The HV supply is has not a different ground level, but a CMC suppresses the voltage ripple.

[1] Inter integrated Circuit, Standard for inter-chip connections

5.2.1 LVDS

The low voltage differential signals (LVDS) are received and send from the Power Board. To achieve a stable link between the iPMT and the surface, the chips DS15EA101 (receiver) and DS15BA101 (driver) were chosen. These are designed for driving and receiving constant data streams and are specified for $0.5\,\mathrm{Gbps}$ over $100\,\mathrm{m}$ CAT5e cable [29], which is sufficient for our trigger and clock signals ($250\,\mathrm{MHz}$).
The implementation was done in close contact with Yifan Yang from Brussels, who is the designer of the back-end card.

5.2.2 Power over Clock

As the analog and the digital part should have completely independent power supplies, the clock data link is used for power transmission (PoC - power over clock). The implementation is done using two coils to decouple the signal (see figure 5.3). The additional components needed to add and receive the power increase the impedance of the system, but the goal of $250\,\mathrm{MHz}$ can still be achieved.

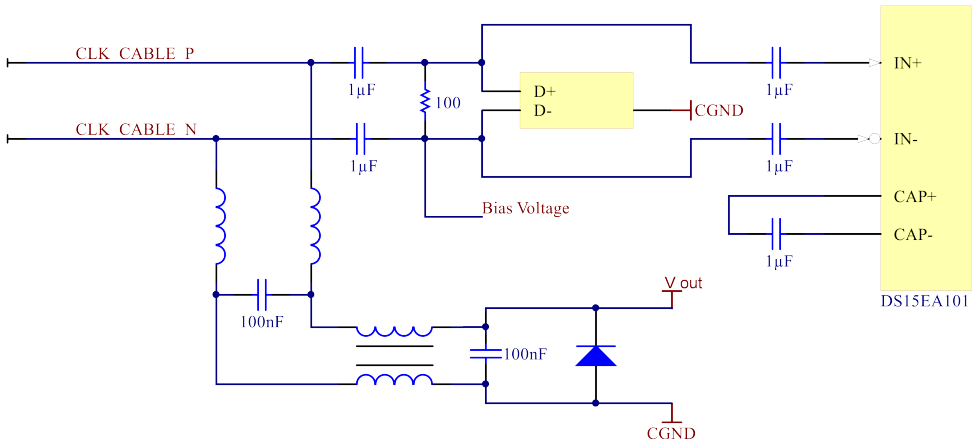


Figure 5.3: Simplified implementation of the receiver DS15EA101. The power is stripped using coils and and is cleaned with a common mode choke. The diode provides protection against inverted voltage input.

5.2.3 Ethernet and Power-over-Ethernet

The Ethernet data link has the requirement to transfer $100\,\mathrm{Mbit/s}$ of data in addition to the power over $100\,\mathrm{m}$ CAT5e cable. This is within the specification of the Ethernet standard. To improve the reliability and simplify the circuit the standard PoE handshake is not

implemented, which saves some components. A standard PoE connection starts with a detection and classification of the consumer, which is not needed for the iPMT.

5.2.4 Output Voltages

The output voltages are divided into two independent parts with different ground levels. Firstly, the digital power part is supplied through the PoE and secondly the analog part is supplied using the PoC. In figure 5.4 a schematic overview of the power setup can be seen.

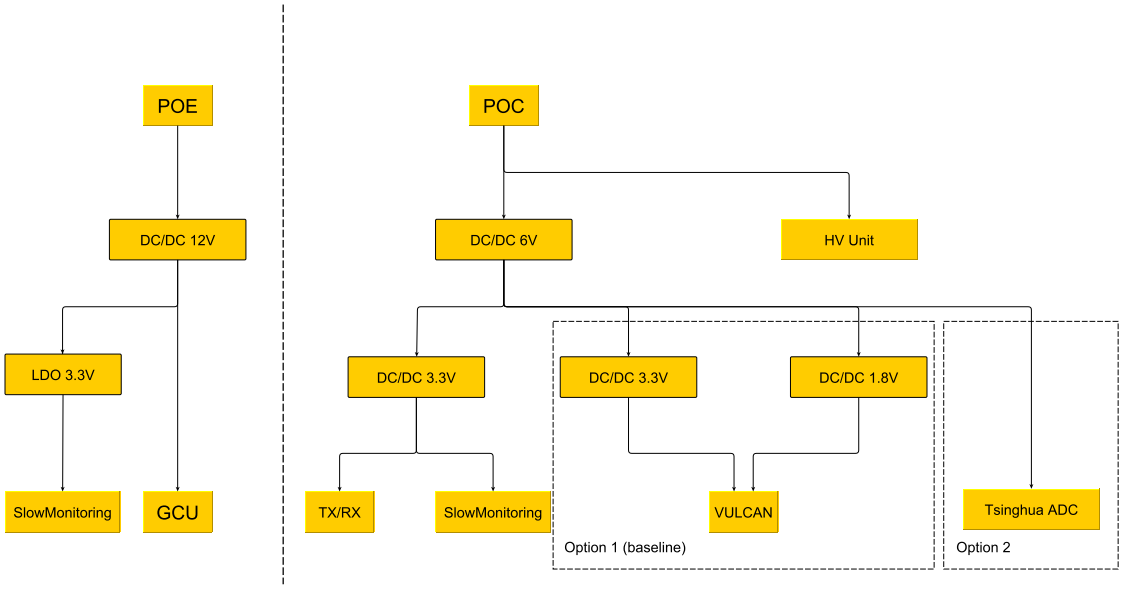


Figure 5.4: Schematic overview of the power generation and distribution on the Power Board.

The output voltage of $12\,\mathrm{V}$ for the GCU is generated by using an LM46002 with a maximum output current of $2\,\mathrm{A}$. In order to supply the slow monitoring chips a low-dropout regulator providing $3.3\,\mathrm{V}$ is used.
In the analog part an internal voltage is created from which the output voltages for the VULCAN chip and the cable driver and receiver are generated. This design improves the output ripple and the reliability, because less input capacitors are connected to the high input voltage. In the first step an internal voltage of $6\,\mathrm{V}$ is generated also using an LM46002. The voltage is chosen as the VULCAN backup solution from China needs a voltage of $6\,\mathrm{V}$.
From the internal voltage the two voltages for the VULCAN chip – $3.3\,\mathrm{V}$ and $1.8\,\mathrm{V}$ – are produced and $3.3\,\mathrm{V}$ for the driver, receiver and the slow control are generated. Two

separate $3.3\,\mathrm{V}$ rails are used to decouple the VULCAN supply from the cable drivers. The low voltages are all generated using a LM46000. In the output of the converter a Π-filter is placed to further suppress output noise.
All DC/DC converters are operated with a different switching frequency to prevent the synchronisation of the converters, which would increase the EMI-emissions and the output ripple.

Table 5.3: Voltages produced by the PB and switching frequencies of the DC/DC converters.

Usage	Voltage [V]	Max. Current [mA]	Frequency [kHz]
GCU Supply	12.0	2000	500
Internal	6.0	2000	560
Internal	3.3	500	650
VULCAN Supply	3.3	500	590
VULCAN Supply	1.8	500	960

5.2.5 Slow Monitoring

In order to monitor the status of the Power Board and the complete iPMT, slow monitoring is implemented. All input voltages and currents are measured, because long or short term changes might indicate problems. In addition the temperature is monitored at up to four different positions on the board. For the prototypes only the two temperature on the top side of the PCB are mounted to simplify the automatic assembly. All devices are read out using the I^2C standard. Figure 5.5 shows the position of the different monitoring chips on the Power Board prototype.
The PB prototype holds an additional I^2C device to control the voltages for the VULCAN chip, as the first VULCAN prototype needs a special start-up sequence. The sequence consists of three steps:

1. $3.3\,\mathrm{V}$ supplying the LVDS
2. $3.3\,\mathrm{V}$ for the ADU
3. $1.8\,\mathrm{V}$

The temperature sensors have a range from $-55\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$ with a resolution of $12\,\mathrm{bit}$ [30]. One temperature sensor measures the ambient temperature, as no strong heat sources are close, while the second sensor measures the temperature close to the GCU-supply, which is the largest power consumer on the PB. On the bottom side one sensor is opposite the GCU supply inductor and the other sensor is in the very center, were the FPGA is

placed on the GCU.
On the analog side (PoC) the input voltage, the input current and the internal voltage are monitored. On the GCU supply side the input and output voltage and the input current are monitored. The PoE input voltage was increased from $24\,\mathrm{V}$ to $48\,\mathrm{V}$, which decreases the power loss on the cable. The range and expected values of the monitoring can be seen in tabular 5.4.
The ground levels of the PoC and the PoE part are not connected on the PB, so an I^2C isolator is used to connect all I^2C components.

Table 5.4: Voltages and currents monitored by the slow monitoring using the ADC input range of $\pm 2\,\mathrm{V}$.

	Current [A]			Voltage[V]		
	Expected	Min.	Max.	Expected	Min.	Max.
PoC input	0.1	0.0	1.0	24.0	0.0	37.0
Internal	-	-	-	6	0	6.5
PoE input	0.3	0.0	0.6	48.0	0.0	50.0
GCU supply	-	-	-	12.0	0.0	13.5

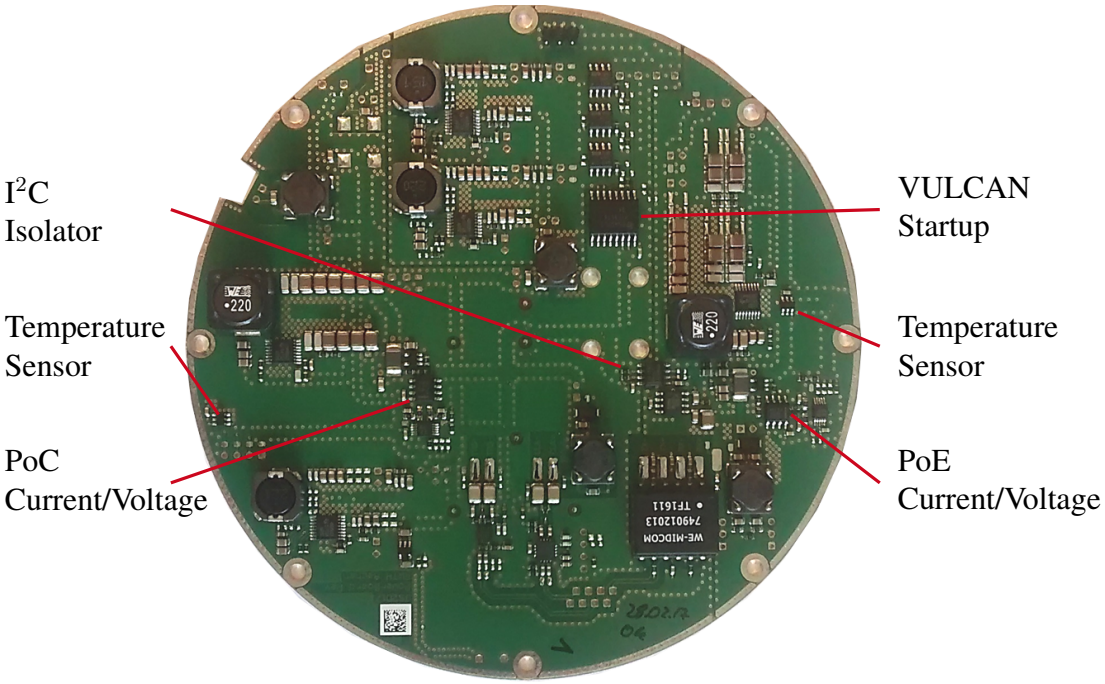


Figure 5.5: Overview of the slow monitoring of the Power Board.

Chapter 6

Reliability

The reliability of the electronics mounted to the PMT is critical, as it can not be accessed after the filling of the detector. From the physics originates the requirement that less than $1\,\%$ of all PMT channels fail during the first 6 years of operation. This failure rate is distributed equally between the submerged electronics and the PMT including the base, so only $0.5\,\%$ of the readout electronics should fail.
After a introduction to reliability of electronic components the used minimisation approach will be presented.

6.1 Reliability of Electronic Components

The failure rate over time for electronic components consists of three major parts which can be illustrated using the bathtub curve (see figure 6.1).
In the beginning of the operation, the failure rate is dominated by infant mortality. During this phase, devices or components with small defects, like bad solder joints, fail. For high reliability electronics infant mortality can be faced with early failure tests (see section 6.3.4).
Throughout the useful lifetime of a device random failures are dominant, leading to a constant failure rate. This time is usually declared as useful lifetime. All discussions and definitions in the following sections describe the random dominated lifetime. Assuming a constant failure rate the failure probability can be calculated using an exponential function:

$$P(\text{fail}) = 1 - e^{-\lambda \cdot t} \tag{6.1}$$

The failure rate λ is usually normalised to $10^9\,\mathrm{h}$, which shifts typical electronics to FIT-values of $\mathcal{O}(1)$. For consumer electronics the failure rate is usually expressed in mean time to failure (MTTF). Examples of failures rates for electronic components can be found in table 6.1.

At the end of the lifespan of electronic components the hazard increases due to ageing effects like decreasing chemical stability [31].
In table 6.2 the relevant acronyms used in reliability engineering are specified. The essential value is the failure rate λ, expressed in failures in time (FIT). $0.5\,\%$ fails in 6 years correspond to a failure rate of $95\,\text{FIT}$.

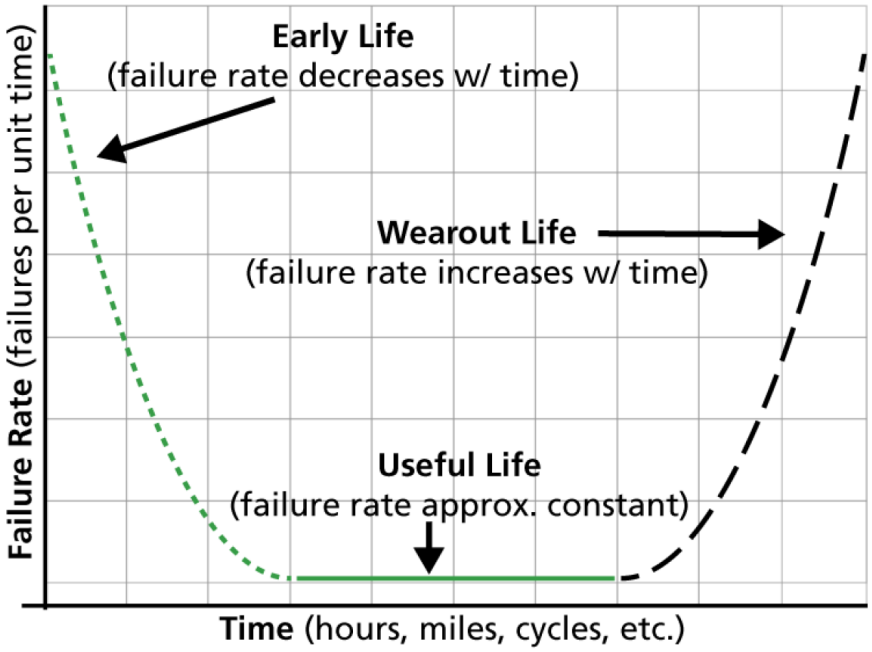


Figure 6.1: Failure rate of an electronic component throughout the lifetime [31].

Table 6.1: Example FIT values for electronic components with a confidence level of $60\,\%$ from the companies Würth Electronics (WE), Texas Instruments (TI) and Vishay.

Component	Manufacturer	Type	Environment	FIT [$1/10^9\,\text{h}$]
Capacitor	WE	WCAP-CSSA	$30\,\%$ stress, $40\,°\text{C}$	0.1
Inductor	WE	WE-PoE+	$40\,°\text{C}$	11.5
Resistor	Vishay	CRCW	$-55\,°\text{C}$ to $155\,°\text{C}$	0.1
Silicon chip	TI	LM46000	$55\,°\text{C}$	0.2

Table 6.2: Definition of acronyms used in reliability engineering [31].

Terms	Definition
Failure Rate λ	The failure rate describes number of failures per time for one component, assuming a constant failure rate. It is given in units of FIT.
Failure In Time (FIT)	Measure of the number of fails per device hours, e.g. $\lambda = 100\ FIT = 100$ failures in 10^9 h.
Mean Time To Failure (MTTF)	The Mean Time To Failure is the mean lifetime under operation before a defect occurs and is consequently the inverse of the failure rate $\lambda = \frac{1}{\text{MTTF}}$. Mean Time between Failures (MTBF) is a synonym if the device is repairable.

6.2 Calculating the Reliability

It is assumed a device's failure rate can be described as the sum of the reliability of all included components. For the calculation of the failure rate of single elements, different empirical models are used which were mainly developed for military usage. In order to have a baseline, the military handbook MIL-HDBK-217F Notice 2 and the FIDES[1] guide are investigated.
In addition, the Siemens Norm SN29500 is used to compare the results. The SN29500 is used for reliability predictions and is based on application experience within the Siemens company. The reference conditions and conversion models for stress conditions are based on the IEC 61709[2][32].

6.2.1 Military Handbook

The military handbook is a well established tool for estimating the reliability of a device. It is based on data obtained during operation and uses simple assumptions to create easily usable models. Unfortunately, the last update was done in 1995[3], so the data the methods are based on is at least 23 years old. Nevertheless, many important standard methods are introduced in the military handbook.
For the reliability calculation, two different methods are introduced for different stages of the project: the "part count" and the "part stress" method.

[1] Latin: trust
[2] Reliability - Reference conditions for failure rates and stress models for conversion
[3] MIL-HDBK-217F, Notice 2

Part Count Method

The part count method is a conservative approach that can be used in the early phase of a project to get first estimated reliability predictions. To make an educated guess on the failure rate, the generic part types, the quantities, the quality level and the environment have to be specified. With this limited information an early estimate of the failure rate can be done:

$$\lambda_{\text{EQUIP}} = \sum_{i=1}^{n} N_i(\lambda_g \cdot \pi_Q)_i \tag{6.2}$$

Where,

- λ_{EQUIP} denotes the total equipment failure rate
- λ_g is the generic failure rate for the i^{th} generic part
- π_Q is the quality factor of the i^{th} component
- N_i is the number of parts of the item i
- n is the number of different generic parts.

Part Stress Method

In contrast to the part count method, the part stress method is designed for a later state of the development, as all part parameters, e.g. voltage stress and temperature, must be known. The calculation of the reliability per part λ_p is done by multiplying a base failure rate λ_b with acceleration factors π_i:

$$\lambda_p = \lambda_b \prod_i \pi_i \tag{6.3}$$

Thereby, the different acceleration factors also describe the quality of the component, the environment and the application (e.g. applied voltage for capacitors, forward current for laser diodes). The total failure rate is obtained by adding all components:

$$\lambda_{\text{EQUIP}} = \sum_{i=1}^{n} \lambda_{p,i} \tag{6.4}$$

Overall, the military handbook provides a detailed calculation method for the reliability of single components and assemblies. The results are conservative but reasonable, for devices and components that have not changed in the last 20 years [33]. However, for components with great improvements in processing in the last years, like CMOS-microcircuits, the reliability results calculated with the military handbook are too high. Additionally, SMD components are not described, which have crucial part in nowadays electronics design.

6.2.2 FIDES Guide

The FIDES guide was developed by the FIDES group, which is a consortium of companies from aerospace and military[4], and is intended to be a sucessor of the Military Handbook 217 [34].
In the FIDES approach the failure rate λ for a single component depends on two parts, an additive and a multiplicative term (see equation 6.5). The additive term describes physical and technological contributions to the failure rate, while the multiplicative term represents the impact of development, production and processes on the reliability. In practice, the formula can be simplified to equation 6.6.

$$\lambda_{\text{item}} = \left(\sum \text{Physical Contributions} \right) \cdot \left(\prod \text{Process Contribution} \right) \tag{6.5}$$

$$\lambda_{\text{item}} = \lambda_{\text{Physical}} \cdot \Pi_{\text{PM}} \cdot \Pi_{\text{Process}} \tag{6.6}$$

$\lambda_{\text{Physical}}$ describes the failure rate of a component based only on the physical characteristics, such as temperature and humidity. The factors Π_{PM} and Π_{Process} grade the quality of the part manufacturing (PM) and the quality of the process (assembly).

Physical Contribution

The physical part depends strongly on the life profile of the component, e.g. the annual time the device is switched off, in standby, in operation, et cetera (see equation 6.7). Every phase has a corresponding weight $\Pi_{\text{acceleration-i}}$ and induced factor (see equation 6.8). A brief introduction for the basic physical acceleration factors is given in table 6.3. λ_0 denotes the failure rate of the device in optimal conditions.

$$\lambda_{\text{Physical}} = \sum_i \frac{\text{Annual time}_{\text{phase-i}}}{365 \cdot 24\,\text{h}} \cdot \lambda_{\text{phase-i}} \tag{6.7}$$

$$\lambda_{\text{phase-i}} = \sum_{\text{Physical Contributions}} (\lambda_0 \cdot \Pi_{\text{acceleration-i}}) \cdot \Pi_{\text{induced-i}} \tag{6.8}$$

Furthermore, the stress induced by changing the phase is included in the calculation of the failure rate $\lambda_{\text{phase-i}}$, since phase changes can increase the failure probability significantly. Therefore, it is not always reasonable to increase the number of cycles to reduce the annual time in a specific phase. At some point the acceleration factor Π_{TCy} will be dominant (see equation 6.9).

$$\Pi_{\text{TCy}} \propto N_{\text{annual-cy}} \tag{6.9}$$

[4] AIRBUS France, Eurocopter, Nexter Electronics, MBDA France, Thales Systèmes Aéroportés SA, Thales Avionics, Thales Corporate Services SAS and Thales Underwater Systems

Table 6.3: Basic physical acceleration factors as used in the FIDES guide [34].

Factor	Definition
Π_{Thermal}	The failure rate typically increases with higher temperature, as the activation energy of the failure mechanisms is temperature dependent
$\Pi_{\text{Electrical}}$	The electrical stress describes the electrical conditions. A component used close to the maximum ratings is more likely to fail.
Π_{TCy}	Temperature cycles decrease the lifetime of components, e.g. by mechanical stress.
$\Pi_{\text{Mechanical}}$	Mechanical stress on the component, e.g. vibrations in a running car.
Π_{RH}	High humidity decreases the lifetime of some components drastically, especially in combination with temperature cycles.
Π_{Chemical}	The chemical acceleration includes the product protection (hermetic sealing) and the pollution of the application and environment.

Through the induced factor, also called overstress factor, the handling and usage of the device is included:

$$\Pi_{\text{induced-i}} = (\Pi_{\text{placement-i}} + \Pi_{\text{application-i}} + \Pi_{\text{ruggedising}})^{0.511 \cdot \ln(C_{\text{sensitivity}})} \tag{6.10}$$

To evaluate this equation all different parameters have to be investigated using the FIDES guide. A short explanation can be found in table 6.4.

Table 6.4: Induced factors as used in the FIDES guide [34].

Factor	Definition
$\Pi_{\text{placement}}$	Describes the function of the component, e.g. power interface, digital interface, analog low level for resistors.
$\Pi_{\text{application}}$	This factor includes the product operation, e.g. exposed to human activity, system mobility or possible drops/shocks.
$\Pi_{\text{ruggedising}}$	Ruggedising describes the effort to design a device that can withstand rough usage.
$C_{\text{sensivity}}$	Sensitivity of the used technology to the different external influences.

Process and Quality Management

After the determination of the physical contributions, the quality of the part manufacturing and the overall process needs to be investigated. The component manufacturing factor is based on the experience with the company, quality assurance level (e.g. level of ISO certification) of the manufacturer and the component quality relative to the state of the art.
The process quality is focused on audits in all critical phases of the design, production and integration. The FIDES guide distinguishes seven different phases:

1. Specification (8 %)
2. Design (16 %)
3. Manufacturing of the board or sub-assembly (20 %)
4. Integration into equipment (10 %)
5. Integration into the system (10 %)
6. Operation and maintenance (18 %)
7. Support Activities (18 %)

The audits get marked and weighted for each phase, default weights can be seen next to the phases. Nevertheless, the weights should be adjusted for every project to include the specific requirements.
The reviews held regularly within the JUNO collaboration are similar to the suggested audits, but are not marked as required by the FIDES guide. Thus it was decided to use the default value recommended of $\Pi_{\text{process}} = 4$ for the process quality. Figure 6.2 shows the process grading compared to the process quality. The standard process quality is on the level of an ISO 9001 certified manufacturer, which seems reasonable for the review system of the JUNO collaboration.
In summary, the FIDES guide is an extensive manual to calculate and monitor the reliability of electronic devices. Comparisons to SN29500 showed usually agreement within one order of magnitude. However, it is designed for projects with more manpower and dedicated reliability managers, so for JUNO some default assumption have to be made. Nevertheless, the FIDES calculation used for some components and ideas are incorporated into the reliability calculations of the JUNO electronics.

6.2.3 Calculation of the PCB Reliability

The reliability of the printed circuit board (PCB) of the Power Board is calculated using the FIDES guide, because the military handbook does not provide this data. The failure rate depends mainly on the used technology, the number of solder joints, the environment

Level	Process	Π_{Process}	Process grade
Very high reliability	Process almost with no weakness	<1.7	> 75%
High reliability	Controlled process, reliability engineering	1.7 to 2.8	50% to 75%
Standard	Usual ISO 9001 version 2000 type quality procedures	2.8 to 4.8	25% to 50%
Unreliable	Reliability problems not taken into account	>4.8	<25%

Figure 6.2: Reliability levels in depnedence on the grading from audits [34].

of the final assembly and the manufacturer.
The base failure rate of the PCB can be estimated in the following way:

$$\lambda_{b,\text{PCB}} = 5 \cdot 10^{-4} \cdot (N_{\text{layers}})^{\frac{1}{2}} \cdot \frac{N_{\text{connection}}}{2} \cdot \Pi_{\text{class}} \cdot \Pi_{\text{Techno-PCB}} \tag{6.11}$$

where

- N_{layers} denotes the number of layers of the PCB
- $N_{\text{connection}}$ is the number of connection points (surface mounted and through hole)
- Π_{class} rates the difficulty of the PCB production based on the minimal conductor width ($500\,\mu\text{m}$ for the Power Board)
- $\Pi_{\text{Techno-PCB}}$ describes what kind of via technology is used (through holes for the Power Board)

The values for the estimation of Π_{class} and $\Pi_{\text{Techno-PCB}}$ can be found in tables 6.5 and 6.6. As introduced in the previous section the base failure rate $\lambda_{b,PCB}$ of the PCB needs to be multiplied with the physical and process factors. All used weights for JUNO can be obtained from the parameters listed in tables 9.1 and 9.2 in the appendix.

Table 6.5: Printed circuit technology identification according to FIDES [34].

Technology	Value of $\Pi_{\text{Techno-PCB}}$
Trough holes	0.25
Blind holes	0.5
Micro-via technology	1
Pad on via technology	2.5

Table 6.6: Class identification depending on the minimum conductor width and minimum spacing between conductors or pads according to FIDES [34].

Minimum conductor width(μm)/ Minimum spacing between conductors (μm)	Value of Π_{class}
$800/800$	1
$500/500$	1
$310/310$	2
$200/200$	3
$150/150$	4
$125/125$	5
$100/100$	7

6.2.4 Creating a Mission Profile

An important step to calculate the reliability of a device is to create a mission profile. This stage is described in the military standard MIL-STD-756B and has the objective to depict the "intended utilization of the elements of the item to achieve mission success" [35]. In short, it describes how different modules interact and encourages to mark the importance of every part. In this section, only the particularly important topic for systems with partial redundancy is covered, to motivate that no redundancy is used on the PB.
The schematic in figure 6.3 shows an active redundant system, where both devices A and B run in parallel, but only on device is required for operation. The reliability can be calculated using simple probability theory:

$$\begin{aligned} P_{\text{success}} &= P_{\text{A,working}} + P_{\text{B,working}} \cdot P_{\text{A,failing}} \\ &= P_{\text{A,working}} + P_{\text{B,working}} - P_{\text{B,working}} \cdot P_{\text{A,working}} \end{aligned} \tag{6.12}$$

In an active system the adding of a parallel system will always increase the success probability if second order effects are neglected.
One example for an second order effect is that some failure modes of A make B inoperable, e.g. a shortened input. Consequently, to protect the independent systems against each

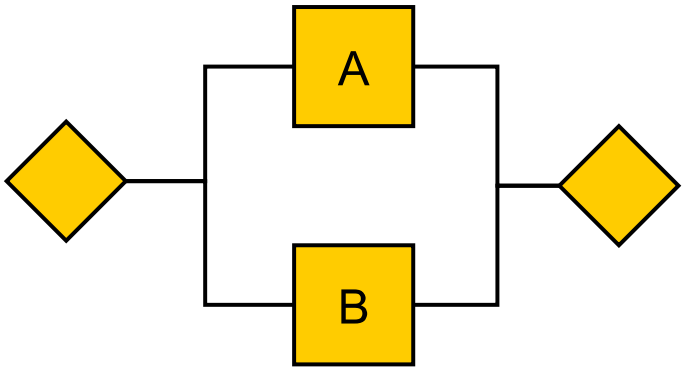


Figure 6.3: Schematic view of two active parallel systems, one operative system (A or B) is sufficient for mission success.

other a switch circuit, which can be active or passive, should be introduced (see figure 6.4).
The failure rate with a passive switch is just the standard failure rate for active parallel systems multiplied with the switch failure rate:

$$P_{\text{success}} = P_{\text{S,working}} \cdot (P_{\text{A,working}} + P_{\text{B,working}} - P_{\text{B,working}} \cdot P_{\text{A,working}}) \tag{6.13}$$

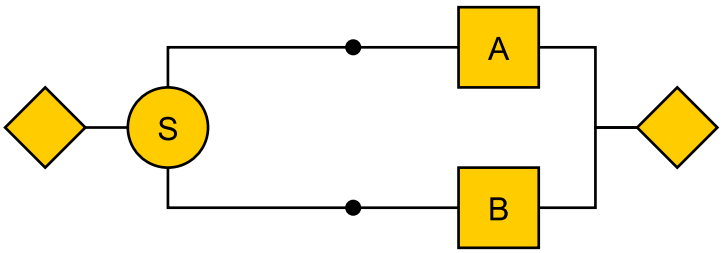
This description of two active devices shows that an active redundant system only improves the reliability if the failure probability of the switch is lower than the failure probability of the redundant devices.
An active switch has the main advantage that the disabled part is not running and thus is ageing slower (see figure 6.4(b)) [35]. In this case, the failure probability can be calculated using the following equation:

$$\begin{aligned} P_{\text{success}} &= P_2 \cdot P_{\text{A,working}} + (1 - P_2) \cdot P_{\text{B,working}} \cdot P_{\text{A,working}} \\ &\quad + P_1 \cdot P_{\text{B,working}} \cdot P_{\text{A,failing}} \\ &= P_2 \cdot P_{\text{A,working}} + P_1 \cdot P_{\text{B,working}} \\ &\quad + (1 - P_1 - P_2) \cdot P_{\text{B,working}} \cdot P_{\text{A,working}} \end{aligned} \tag{6.14}$$

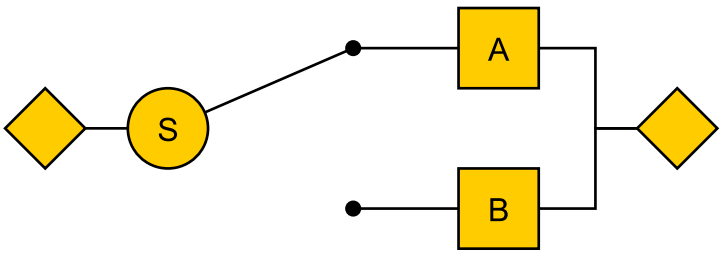
Where:

- P_1 is the probability of no failure to switch when required
- P_2 is the probability of no premature switching

Overall, these simple examples show that redundant systems might not always be an improvement to the reliability, especially if the failure probability of the switches is of the same magnitude as the failure probability of the redundant element.
In addition, failures of one device A might cause failures in connected systems (e.g. voltage spikes), which could not be resolved by changing to device B.



(a) Active parallel system with a passive switch (e.g. security circuit).



(b) Standby parallel system with an active switch.

Figure 6.4: Schematic view of two parallel systems controlled by a switch, one operative system (A or B) is sufficient for mission success. In (a) both systems are active, while in (b) the switch is an active component, thus B is in passive standby [35].

6.3 Measuring the Reliability of Electronic Components

When building highly reliable devices the first idea is to test the final devices for failures. With this approach, the problem arises that a component failing usually leads to a cascade of failing components and the origin of the failure might not be identified.

Alternatively, testing all components by themselves is a valid way to figure out the overall failure rate of the device. As the failure rate of standard components is very low, many components and a long testing time are needed. The failure rate can be increased by changing the environmental conditions and reckoned back to the used conditions.

6.3.1 Acceleration Factor

A very common way to increase the stress on a component is to increase the temperature and calculate the acceleration of chemical processes leading to failures. This is done by modifying the Arrhenius equation, which describes the temperature dependence of the rate of a chemical reaction:

$$k = A \cdot e^{\frac{E_\mathrm{a}}{R \cdot T}} \tag{6.15}$$

Where,

- k denotes the rate of a chemical reaction
- A is a constant factor depending on the chemical reaction
- E_a is the activation energy for the reaction
- R is the universal gas constant
- T is the absolute temperature.

The activation energy is in units of energy per mole. In physics and electronics it is more common to use the particle energy, thus the equations is modified to

$$k = A \cdot e^{\frac{E_\mathrm{a}}{k_\mathrm{B} T}} \tag{6.16}$$

where k_B denotes the Boltzmann constant. Based on this equation an acceleration factor (AF) can be calculated:

$$\mathrm{AF} = exp\left(\frac{E_\mathrm{a}}{k_\mathrm{B}}\left(\frac{1}{T_\mathrm{use}} - \frac{1}{T_\mathrm{stress}}\right)\right) \tag{6.17}$$

Hereby, the stress temperature denotes the test temperature and the use temperature is the device operation temperature in the used setting. As the components should be operated during the test the junction temperature should be used to calculate the acceleration factor. This temperature can be obtained by calculating the self-heating of the device using the package properties and the power consumption. One component has usually several failing mechanisms with different activation energies E_a.
Other possibilities to increase the ageing of components like increasing humidity where not considered. For JUNO the final electronics will be in a stable environment without additional stress conditions.

6.3.2 Measuring the Failure Rate

The simplest way to calculate the propability of a device to fail can be discribed by an exponential function, but some assumptions have to be made in this model. The failure rate of the device has to be constant, which is valid for components after infant mortality and before wear out. Thus, the component has to be in a chemical and mechanical stable environment. In order to minimize the infant mortality in the test sample the first $1000 - 3000$ test hours should be ignored [36].
The failure rate of a component fulfilling the criteria stated above can be calculated using:

$$\lambda = \frac{\chi^2(2 \cdot (f+1), \mathrm{CL}) \cdot 10^9\,\mathrm{h}}{2 \cdot t \cdot d \cdot \mathrm{AF}} \tag{6.18}$$

Where,

- λ is the failure rate
- f is the number of failed devices
- χ^2 is the χ^2 factor for $(2 \cdot (f+1))$ degrees of freedom
- CL is the confidence level
- t is tested hours per device
- d is the number of tested devices
- AF is the acceleration factor.

For a lot of statistics with a high number of failures the χ^2-function[5] can be replaced by the number of failures, but usually the number of failures is very small. Typically, a confidence level of $60\,\%$ is used for electronics components. The factor of $10^9\,\mathrm{h}$ normalises the result.
In equation 6.18, it is assumed that a single failure mechanism is causing component failure. This assumption can be made in two cases:

1. One failure mechanism is dominant for a component.
2. The failure mechanism with the lowest acceleration factor is used as a basis for the calculation.

Also combination of those can be done, where the lowest dominant mechanism is chosen, e.g. for silicon chips usually an activation energy of $0.7\,\mathrm{eV}$ is used [37].
The failure of a device can be due to different failure mechanisms, for example oxide defects, silicon defects or electro-migration for silicon chips. Therefore, for a complete

[5] The divider of 2 normalises the χ^2 and must also be removed.

description of the failure rate, each failure needs to be matched to a failure mechanism. The equation can be written as:

$$\lambda = \sum_{i=0}^{N} \frac{\chi^2(2 \cdot (f_i + 1), CL) \cdot 10^9 \,\mathrm{h}}{2 \cdot t \cdot d \cdot AF_i} \tag{6.19}$$

Here, N denotes the number of different known failure mechanism.

Non-Constant Failure Rate

The assumptions mentioned before are valid for most electronic components. However, for components such as electrolyte capacitors, which degrade over time, the failure rate is not constant and also the wear out time might be within the lifetime of a project. In this case, the Weibull probability density function is a better description than a simple exponential function [31]:

$$f(t) = \frac{\beta}{\eta} \left(\frac{t - \gamma}{\eta} \right)^{\beta - 1} e^{-\left(\frac{t-\gamma}{\eta}\right)^{\beta}} \tag{6.20}$$

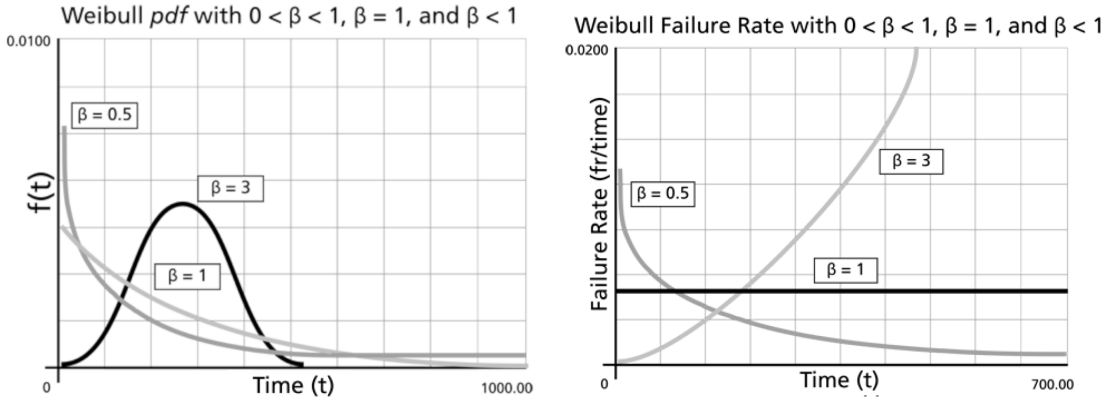
Where,

- β is the shape parameter
- η is the slope parameter
- γ is the location parameter.

The failure rate can be calculated using:

$$P(\text{fail}) = 1 - \int f(t)dt = 1 - e^{-\left(\frac{t-\gamma}{\eta}\right)^{\beta}} \tag{6.21}$$

In figure 6.5 the PDF and failure rate of the Weibull function for different values of the shape parameter are shown. The slope parameter η is comparable to λ in the basic exponential approach, while the location parameter can be used to shift the time, e.g. to include early failures in the description of the failure rate [31].
The only big drawback of the Weibull function compared to the exponential approach is the increased number of parameters. Therefore, for the determination of the failure rate over time, several measurements with different acceleration factors have to be performed. For all components used in JUNO the exponential approach is reasonable. On the one side the infant mortality should be negligible after early failure scans (see section 6.3.4) and through the careful choice of components the wear-out time should be after the end of the JUNO lifetime.



(a) PDF (b) Failure rate

Figure 6.5: Probability density function (PDF) and failure rate for the Weibull distribution for different shape parameters. For $\beta = 1$ it corresponds to an exponential function. Lower values for β lead to a decreasing failure rate, e.g. for infant mortality. The failure rate rises for shape parameters bigger than 1. This usually discribes wear out over time [31].

6.3.3 Measuring the Failures in Time with unknown Activation Energy

The FIT value for a component can be estimated without knowing the failure mechanisms. A failure rate measurement at different temperatures has to be done, because the activation energy E_a is temperature dependent. The effective activation energy can be estimated, if a failure rate could be measured at two different temperatures [38]:

$$E_a = k \cdot \frac{ln(R_{\text{f1}}) - ln(R_{\text{f2}})}{(\frac{1}{T_1} - \frac{1}{T_2})} \tag{6.22}$$

Assuming that different activation energies dominate the failure rate at different temperatures this estimation is only correct close to the test temperatures. Figure 6.6 shows an illustration of the problem with test measurements at $105\,^{\circ}\text{C}$ and $140\,^{\circ}\text{C}$. The red curve shows the estimated failures per time. For a typical use temperature of $40\,^{\circ}\text{C}$ the FIT value is wrong by one order of magnitude.
Thus, this approach can only be used if at least some information about the failure mechanisms is available.

6.3.4 Early Failure Scanning

The early failures of electronic components observed in the beginning of an operation results from the defects that occur in production and assembly. Several techniques can be

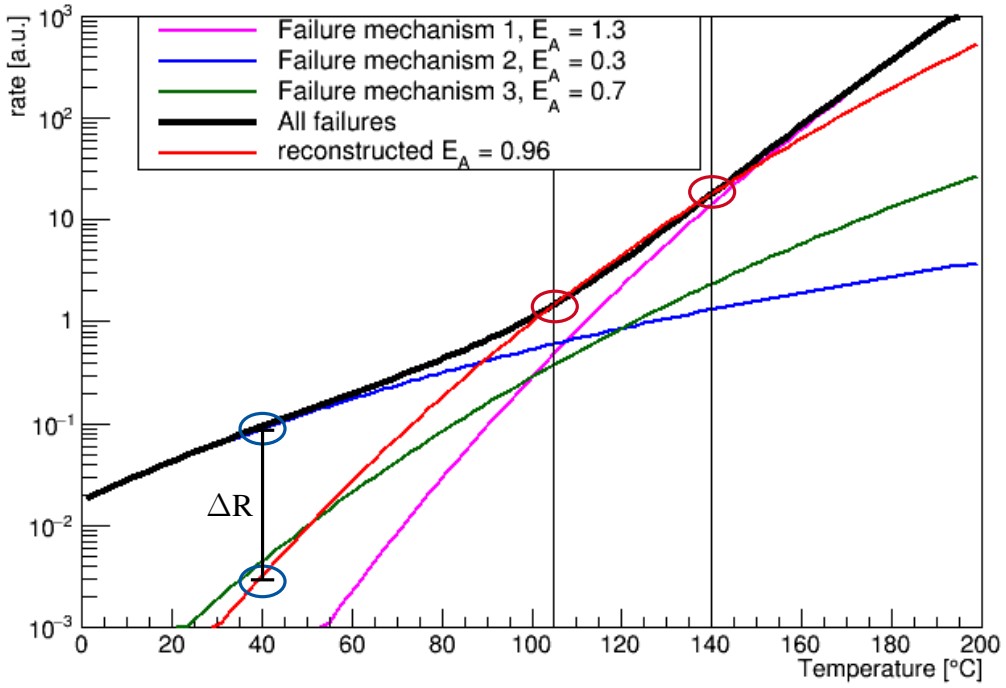


Figure 6.6: Example for the calculation of the activation energy for an electronic component. At two temperatures failures were observed (red circle) which leads to an effective activation energy of $0.96\,\mathrm{eV}$. The propagation to the use-temperature leads to a wrong estimated failure rate R.

used to reduce the number of defects, including process control, inspections and testing. Some typical defects are [39]:

- Oxide fault (silicon chip)
- Lifted/broken wire bonds (silicon chip)
- Bad solder connection
- Residual process or human derived chemicals
- Lifted component
- Mechanical defects in base material

For the JUNO electronics an early failure screening is foreseen to suppress the infant mortality as much as possible. Different screening methods are capable of detecting different defects, thus the screening method has to be adapted to the project. The most common methods are [39]:

- Thermal cycling
- Random vibration
- Voltage variation

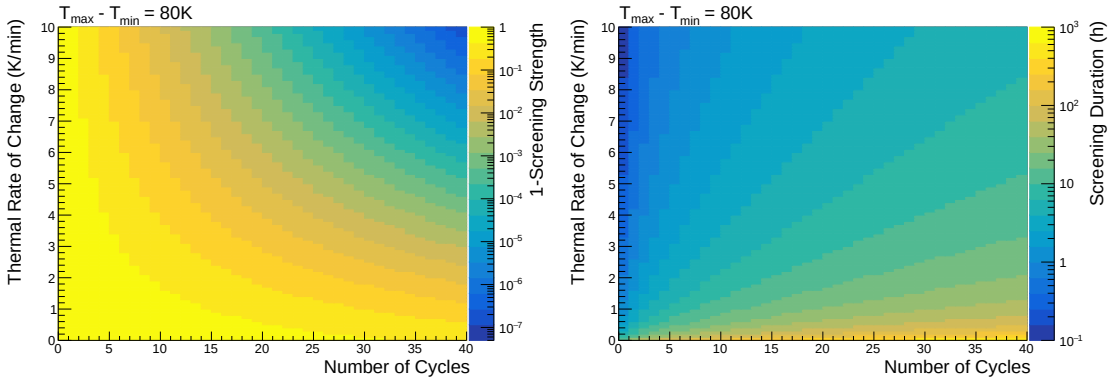
Certainly, these methods can also be combined or extended. The method of increasing the voltage while also increasing the temperature is often used as a burn-in for systems on chip (SoC) or systems in package (SiP), like RAM modules [40]. Vibration tests are used for components that will also experience vibrations in the final use-case, like in cars [41]. For the JUNO underwater electronics the thermal cycling screening is the method of choice. This stress consists of cycling the temperature of the test device at a high rate, thus the temperature range, the temperature change rate and the number of cycles are the defining parameters. The tests results in stress on solder joints, microcracks and impurities through the thermal expansion and contraction of the different materials [39].
During the stress tests the electronics should be running, as performance variations can indicate problems. The screening strength describes the efficiency of the stress test, an efficiency of $100\ \%$ would indicate that all defects were found. For thermal cycling the screening strength (SS) can be calculated using equation 6.23.

$$\text{SS} = 1 - \exp[\ \text{-}0.0017 \cdot (R + 0.6)^{0.6} \cdot (\ln(e + \Delta T))^3 \cdot N_{\text{cy}}] \tag{6.23}$$

In this equation R denotes the temperature range, ΔT is the thermal rate of change (in $^\circ\mathrm{C}/\mathrm{min}$) and N_{cy} stands for the number of cycles. Figure 6.7(a) shows the screening strength as a function of the number of cycles and the thermal rate of change for a temperature difference $T_{\text{max}} - T_{\text{min}} = 80\,\mathrm{K}$, while figure 6.7(b) shows the corresponding screening duration. The temperature range of $80\,\mathrm{K}$ is within the specification for industrial standard components without having negative temperatures to prevent condensation.
The screening strength needed for the underwater electronics depends mainly on two parameters. Firstly on how many early failures can be tolerated to still achieve the physics goals and secondly on the number of defects to detect. A short example will motivate these points. If 5 early failures can be tolerated out of 20.000 boards, the screening efficiency needed depends on the average number of defects per board. Assuming $10\,\%$ of the boards have a defect a screening strength of $SS = 99.75\,\%$ is needed.

$$\begin{aligned} \text{SS}_{\text{required}} &= 1 - \frac{\text{Early failures allowed}}{\text{Expected number of boards with failures}} \\ &= 1 - \frac{5}{20000 \cdot 10\,\%} = 99.75\,\% \end{aligned} \tag{6.24}$$

For the JUNO underwater electronics, the number of possible early defects has not yet been estimated, as it depends on the assembler, the temperature and vibrations during transportation and also the mounting to the PMT. Preferably, the first electronics sets should be used to approximate the average number of defects, using a high screening strength.



(a) (b)

Figure 6.7: Figure (a) shows $1-$ the screening strength as a function of the change of the temperature per minute and the number of cycles. Figure (b) displays the corresponding screening duration.

6.4 Reliability of the Power Board

In the design of the Power Board the goal was to minimize the FIT value without compromising functionality and performance while using commercially available components. The target FIT value for the underwater electronics is 95 FIT for the High Voltage Unit, the General Control Unit including the VULCAN chip and the Power Board.

6.4.1 Approach of Minimization

As described previously, the measurement of failure rates of single components is not easy, so it was decided to only use components which are tested by the manufacturer. This step reduces the number of admissible manufactures and also increases the cost of the boards significantly[6], but also reduces the number of working hours, money and time that have to be spent for a test setup. In addition, the manufacturer have to be at least EN ISO 9001:2015[7] qualified to decrease the chance of inconsistency in the production.
The reliability of the Power Board is calculated with a conservative approach. All components are classified as critical for the operation of the board, assuming the failure of a temperature sensor has the same impact as the failure of the Ethernet transformer. This decision is done because the failure modes of the components are not known. Non-vital parts might fail and disable the board because it shortens the supply voltage to ground.

[6]Capacitor: $10\,\mu$F, $U_{max} = 10\,$V, X7R, 2,000 wheel, Würth Electronics: 0.339€, Standard: 0.03€
[7]Quality Management System

6.4.2 Software to Calculate the Reliability

The software *ReliabilityCalc*[8], which is used to calculate the reliability, is developed and maintained in the JUNO-hardware group in Aachen. The program calculates the reliability using the manufacturer's data or the military handbook, including temperature dependencies and stress levels.
Most data of the manufacturers Texas Instruments (TI) and Würth Electronics (WE) is currently accessed automatically, via internet for TI and with a self-build database for WE. The manufacturers Maxim Integrated, Vishay and WIMA are partly included. In addition, the adding of default components just using the FIT value is possible.
Furthermore, the PCB calculation from the FIDES guide is added, but although the FIDES guide gives good estimations, no other components were added due to the complexity.

6.4.3 Result of Reliability Estimation

The estimated failure rate of the Power Board is calculated adding the FIT-value of all 266 components, leading to a value of

$$\lambda = 40.6\,\text{FIT}$$

assuming a temperature of $40\,^{\circ}\text{C}$ for every component. This worst case scenario for the temperature is obtained using dummy electronics that was potted in oil (see section 7.5).
The contribution of the different parts of the Power Board can be seen in figure 6.8. The failure rate is dominated by one passive component: the Power-over-Ethernet coil from Würth Electronics. Unfortunately, no alternative with a better failure rate could be found. The second largest contribution is the slow monitoring of the board, which could in principle be left out.
Since the first calculation using the full component list at the end of 2016, some manufacturers have updated there data, therefore a second calculation with data from summer 2018 is performed:

$$\lambda = 40.4\,\text{FIT}$$

The small improvement results from the continuous testing of Texas Instruments. The second manufacturer with a significant number of parts on the Power Board, Würth Electronics, uses a combination of measurements and calculations based on the telcordia prediction method [42], therefore the values do not change with time.
Figure 6.10(a) shows the failures in time in dependence on the temperature. The exponential rise is dominated by silicon chips, due to their high activation energy.
The Power-over-Ethernet input voltage is critical, since the high reliability capacitor series that is used has a maximum voltage rating of $50\,\text{V}$. Accordingly, the input capacitors of the DC/DC converter are connected in series and parallel to allow a maximum voltage

[8] https://github.com/JochiSt/ReliabilityCalc, DOI 10.5281/zenodo.1134161

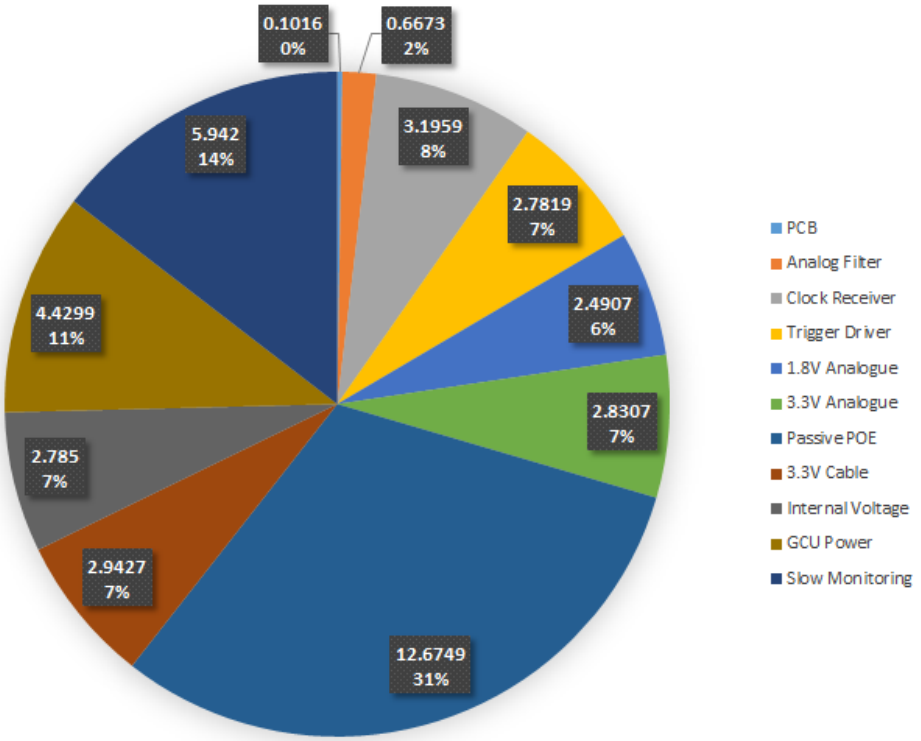


Figure 6.8: Contribution of different parts to the total reliability of the Power Board.

of $100\,\mathrm{V}$ while having the same input capacity. The schematic in figure 6.9 has a FIT value of 1, compare to a FIT of 1.6 for two capacitors with a stress level[9] of nearly $100\,\%$, but the costs are quadrupled.

In figure 6.10(b) the reliability can be seen as a function of the PoE input voltage. The steps arise from the structure of the WE reliability data (see appendix) which provides reliability data depending on stress levels of $30\,\%$, $50\,\%$, $70\,\%$ and $100\,\%$. Since the calculation is based on a worst case scenario, for a stress level of $31\,\%$ the $50\,\%$ stress data is used.

Up to now, all estimations are very conservative, also because the failure modes of the components are not known. In order to show the improvement this knowledge would provide, the failure modes of resistors and capacitors were investigated (see table 6.7). The underlying idea is that the failure of some components might only lead to a tolerable performance drop, instead of a complete breakdown. To give an example, the failure of one input capacitor will only lead to a malfunctioning device if it breaks down into a short

[9] Stress for capacitors $= \frac{\text{Applied Voltage}}{\text{Rated Voltage}}$

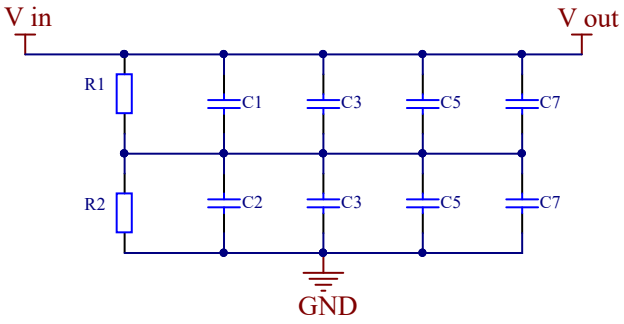


Figure 6.9: The schematic shows the PoE input voltage filter used on the Power Board. The resistors define the voltage between the capacitors to $\frac{V_{\text{in}}}{2}$. All capacitors have the same capacity C_0 leading to a total capacity of $2C_0$.

cut.
Accordingly, the inclusion of the failure modes of selected capacitors and resistors leads to a FIT value of

$$\lambda_{\text{PB}} = 35.8\,\text{FIT}$$

which is an improvement of $13\,\%$. A simulation of the average detected failure rate in 6 years of runtime is shown in figure 6.11.

Table 6.7: Resistor and capacitor failure modes from "Failure Mode/Mechanism Distributions", published 1991 [43].

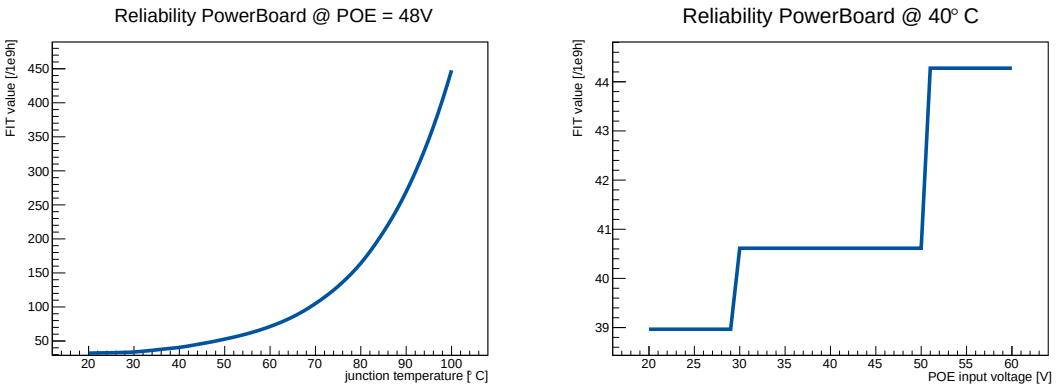
Resistor

Failure Mode	Probability
Short	0.05
Open	0.59
Value Change	0.36

Capacitor

Failure Mode	Probability
Short	0.49
Open	0.22
Value Change	0.29

The achieved estimated failure rate consumes $\approx 40\,\%$ of the failure rate budget allowed for the complete under water electronics. Considering the PB holds most of the power electronics this is acceptable. However this estimate is only an upper limit ($60\,\%$ CL), so the real value might be lower. A final conclusion can only be drawn, if the final design of the high voltage and general control unit is done.
Not included in the calculation are the solder joints to the cable and the different boards and possible protection against exceptional events, like power cuts and lightning strikes. Currently, it is not known whether the Power Board has to include protection against these events or if the protection on the back-end card is sufficient.



(a) (b)

Figure 6.10: The figures (a) and (b) show the failures in time as a function of the temperature and the PoE input voltage.

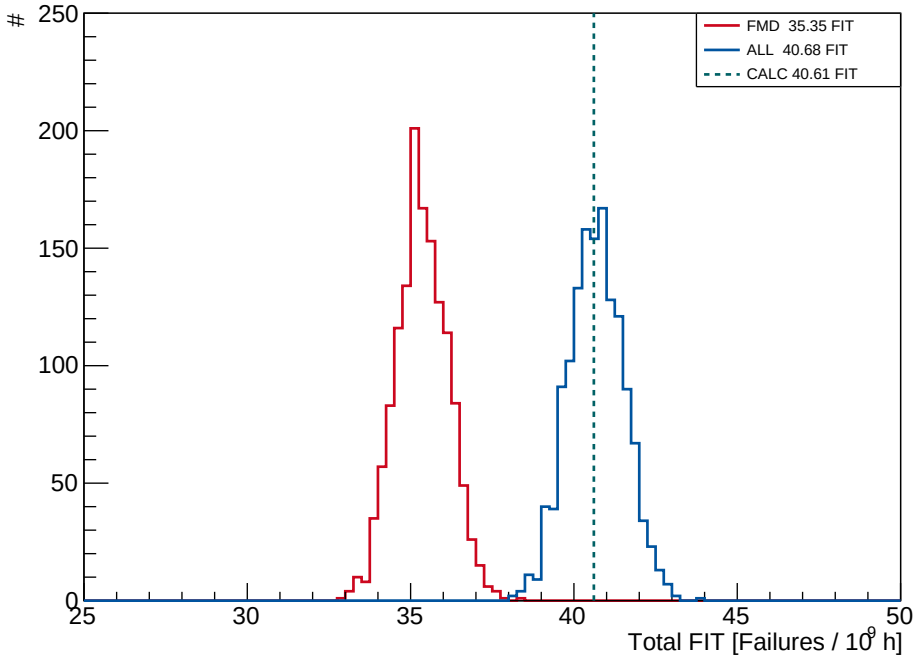


Figure 6.11: Simulation of the failure rate observed in the first 6 years for the PB with and without failure mode distributions.

Chapter 7

Measurements

All measurements shown in this chapter are done with the second prototype version of the Power Board. In the beginning of 2017, 120 of these boards were produced, however most of the measurements are done with single boards. Some parameters like efficiency and ripple of the DC/DC converters is varying within the component specification, but the overall performance is similar.
It should also be mentioned that all measurements are done in air, while the final electronics needs to be potted in a fluid or solid material to improve the thermal transfer to the potting shell. The performance of the Power Board may be potting-material dependent, as the inductors have air gaps. If these gaps are filled with a potting material the conductivity changes. Further test in this regard will be done with the final electronics.

7.1 DC/DC Converter

7.1.1 DC/DC Converter - a Short Introduction

On the Power Board only DC/DC buck converter are used, which convert higher to lower voltages.
The generation of lower voltage is done by producing a pulse-width-modulated (PWM) signal and smoothing it using inductors and capacitors (see figure 7.1). Simplified, the output voltage is given by the duty cycle and the input voltage[1]:

$$V_{\text{out}} = \frac{T_{\text{on}}}{T_{\text{on}} + T_{\text{off}}} \cdot V_0 \tag{7.1}$$

In figure 7.2 a simplified implementation of a DC/DC converter is shown. The current flow during operation is sketched. If the switch is closed the external voltage V_{in} is connected to the inductor and the current increases, due to the voltage difference of input

[1] Neglecting the efficiency.

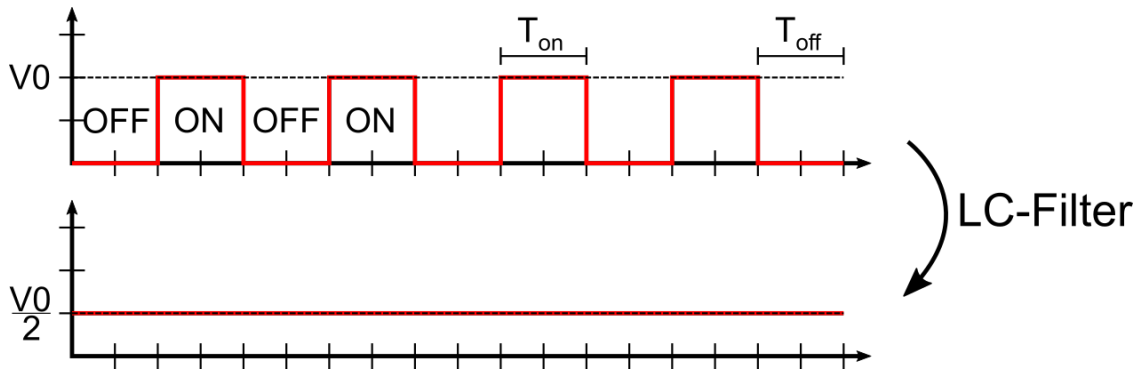


Figure 7.1: Example for a PWM signal with a duty cycle of $50\,\%$, leading to an output voltage of $V_0/2$.

and output. However, the impedance of the inductor prevents fast current changes, so the output voltage change is small. The capacitor is loaded during this phase of operation. When the switch is off the input voltage is no longer connected and the current decreases. Again, the inductor will adjust to hold the current relatively constant, the current loop is now closed by a diode or a second switch. During the off time the capacitor is discharged stabilising the output voltage. The efficiency of the converter is given by the switching speed of the switches. The inductor current through the phases can be seen in figure 7.3.

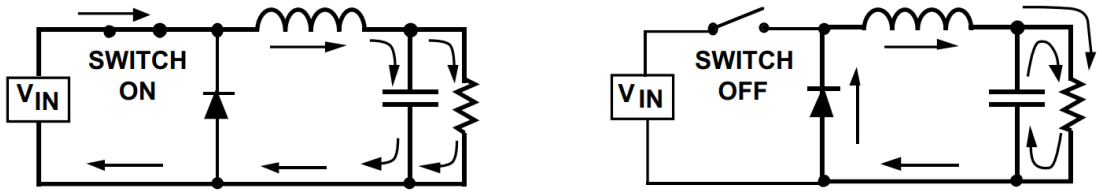


Figure 7.2: Schematic explanation of a buck converter, the arrows indicate currents [44].

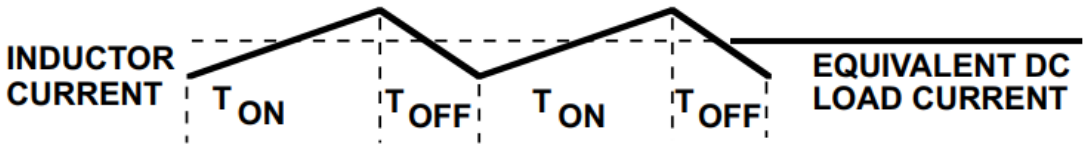


Figure 7.3: Inductor current during the on and off phases [44].

The switch, which is typically a field-effect transistor, is usually included into a chip, that additionally contains a diode/second switch and a feedback system. Through the feedback system the output voltage is controlled, adjusting the duty cycle to load and input voltages changes. A simplified schematic of a converter from the LM46000 series, which is used on the PB can be seen in figure 7.4. In order to minimize the output ripple two

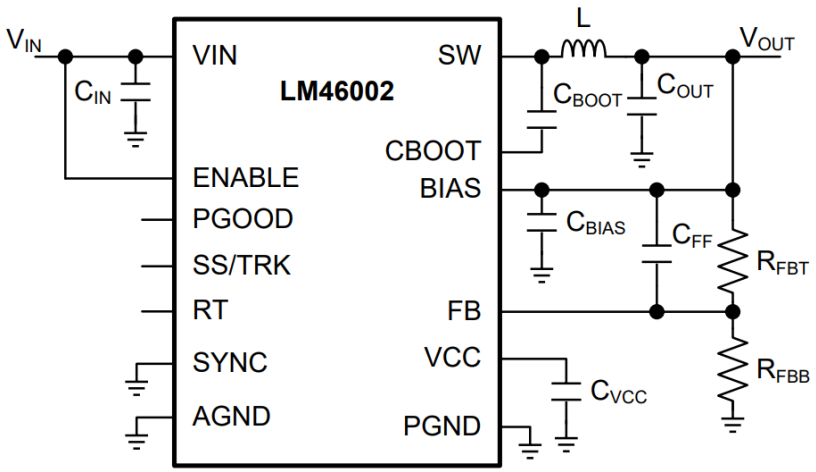


Figure 7.4: Simplified schematic of the LM46002 DC/DC converter [45].

main variables have to be adjusted, the inductance and the output capacity. Increasing both parameters will decreases the output voltage ripple, but too high values might affect the stability and efficiency of the converter.
First problems might occur during the start-up, as the capacitors need to be charged completely, which might exceed the maximum output current of the DC/DC converter, leading to a shut down. Choosing a longer start-up time can reduce this problem significantly [46].
High values for the inductor can harm the feedback stability. Thereby the feedback system might get self-energising for some frequencies leading to a resonance in the output, possibly destroying the DC/DC converter or supplied devices. Considering these problems a trade-off between low ripple and stability has to be made.
Up to now only output ripple has been discussed, but a second ripple is superimposed - the transient switching ripple, that is generated by the switching of the modes (see figure 7.5). This ripple can be reduced by lowering the switching speed, between ON and OFF modes. A negative side-effect of this change is a lower efficiency of the DC/DC converter.

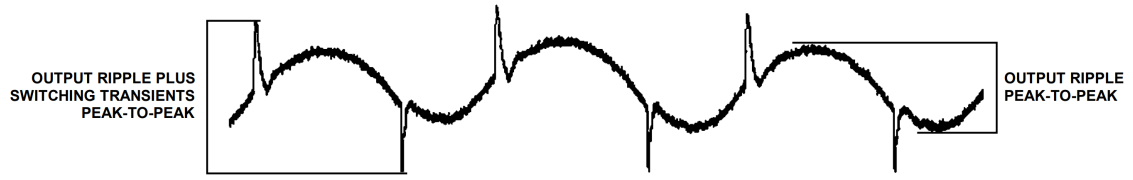


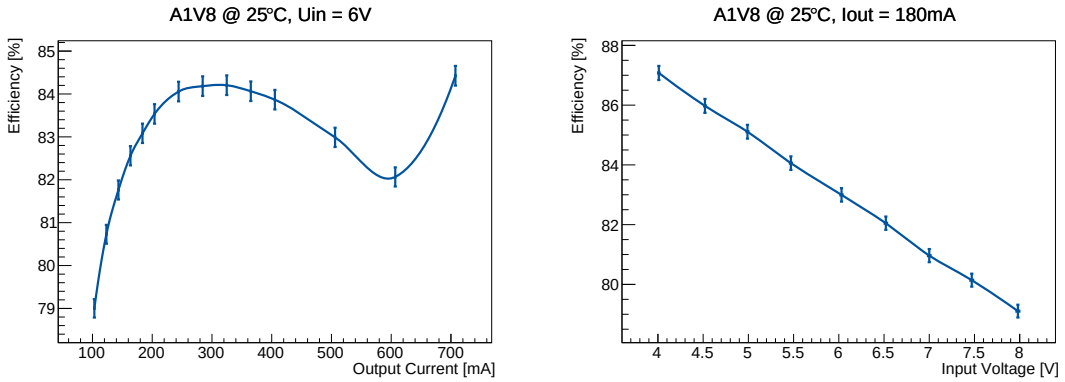
Figure 7.5: The plot shows the different between output ripple and switching transient noise [47]. In the following ripple is always output ripple plus switching transient noise.

7.1.2 Efficiency

The manufacturer give examples of efficiencies to expect from the chip based on standard designs. However, in the effort to minimize the output voltage ripple the selected inductors have a high inductance, which might affect the efficiency negatively. The uncertainty on the efficiency arises from the different measuring instruments and is around $0.27\,\%$. The input voltage uncertainty is around $0.2\,\%$.

VULCAN Supply 1V8

The $1.8\,\mathrm{V}$ supply voltage for the VULCAN chip has an efficiency of about $80\,\%$ at the expected output current of $180\,\mathrm{mA}$ (see figure 7.6(a)). In figure 7.6(b) the dependence of the efficiency on the internal voltage is shown.
The official maximum output current of the converter is $0.5\,\mathrm{A}$, efficiency values above might vary strongly between different chips and furthermore should also never be reached during operation.

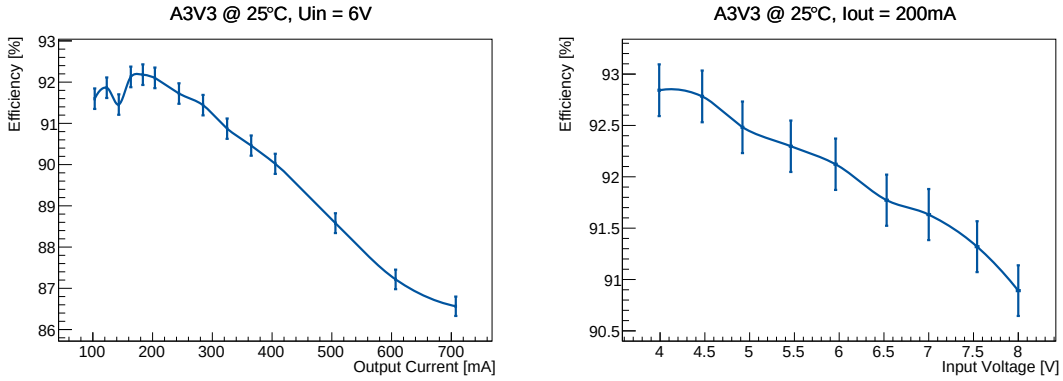


(a) (b)

Figure 7.6: Efficiency of the 1.8V DC/DC converter.

VULCAN Supply 3V3

In figures 7.7(a) and 7.7(b) the efficiency of the second supply voltage for the VULCAN chip can be seen as a function of the output current and input voltage. Again the official maximum output current of the DC/DC converter is $500\,\mathrm{mA}$. The efficiency of $> 90\,\%$ for the predetermined output current of $200\,\mathrm{mA}$ is perfectly acceptable.



(a) (b)

Figure 7.7: Efficiency of the A3.3V DC/DC converter.

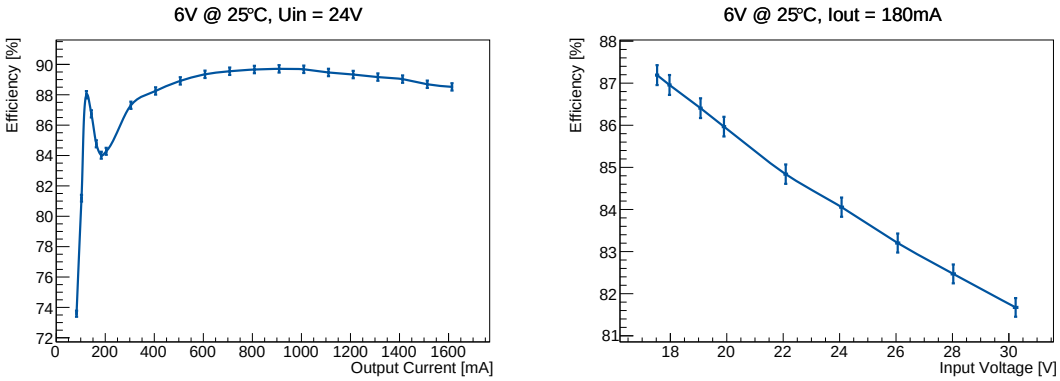
Internal Voltage 6V0

The internal voltage needs to supply the VULCAN chip, the LVDS receiver/driver and the slow monitoring, leading to a output power of maximal $2.5\,\mathrm{W}$ including the efficiency of later stages. The DC/DC converter must also be able to supply the Tsinghua ADC, the alternative to the VULCAN chip, which needs $6\,\mathrm{W}$.
Figure 7.8(a) shows the efficiency as a function of the load. The kink between $100\,\mathrm{mA}$ and $200\,\mathrm{mA}$ is a documented behaviour of the DC/DC converter [45]. Due to the relatively high input voltage, see figure 7.8(b), the efficiency is between $83\,\%$ and $89\,\%$ for voltages between $18\,\mathrm{V}$ and $30\,\mathrm{V}$.

GCU Supply 12V0

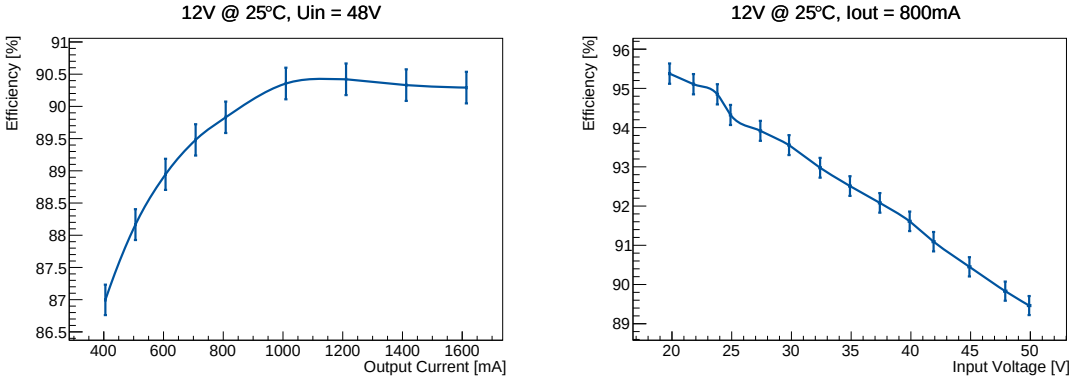
The main power consumer is the GCU, with an estimated power consumption of up to $12\,\mathrm{W}$[2], mainly driven by the FPGA. At this power the efficiency of the DC/DC converter is around $89.5\,\%$, to minimize the losses the input voltage would have to be lower (see figure 7.9). The final input voltage of $48\,\mathrm{V}$ is the standard for Power over Ethernet.

[2]Peak power might be higher.



(a) (b)

Figure 7.8: Efficiency of the $6.0\,\mathrm{V}$ DC/DC converter.

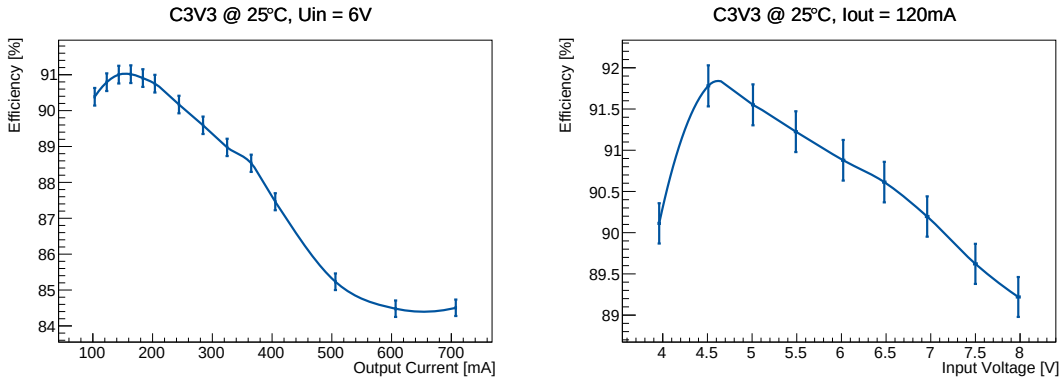


(a) (b)

Figure 7.9: Efficiency of the $12.0\,\mathrm{V}$ DC/DC converter.

C3V3

The supply for the slow monitoring and the LVDS receiving and driving units has a load between $100\,\mathrm{mA}$ and $200\,\mathrm{mA}$. Figures 7.10(a) and 7.10(b) show that the expected efficiency is around $88.5\,\%$.



(a) (b)

Figure 7.10: Efficiency of the C3V3 DC/DC converter.

Total Efficiency

The efficiency of the DC/DC converter is not optimized, as the focus of the prototype V2 is to achieve the ripple and reliability goals. Nevertheless, assuming the predicted load values, a total efficiency of $88\,\%$ is reached, as can be seen in table 7.1. Clearly the GCU supply dominates the efficiency, while the internal voltage has also some impact. The poor efficiency of the internal DC/DC converter origins from the design goal, to be compatible with VULCAN and the Tsinghua ADC. If the current assumptions are correct the total power consumption of one iPMT are around $15\,\mathrm{W}$.
Until now only the losses on the PB have been discussed, but additional losses occur in the cable. The current cable has a resistance of $9\,\Omega$ per $100\,\mathrm{m}$, which is less than specified in the Ethernet standard. The PoE line uses two cable pairs leading to a resistance of $4.5\,\Omega$. Combining this information with the converter efficiency leads to a voltage dependent total loss, which can be seen figure 7.11. At the final input voltage of $48\,\mathrm{V}$ the total loss of the GCU side is $\approx 1.3\,\mathrm{W}$. The PoC line with a power of $\approx 2.2\,\mathrm{W}$ has a loss of $80\,\mathrm{mW}$ on the single $9\,\Omega$ cable.
All in all, considering that the efficiency was not the main objective, the efficiency is satisfying and sufficient. Further improvements can be done, as soon as the electronics is finalized.

Table 7.1: Efficiency of the Power Board assuming the default power consumption. The VULCAN supplys, the LVDS and Slow Monitoring are supplied by the internal voltage.

Consumer	Voltage [V]	Current [mA]	Output Power [mW]	Efficiency [%]	Loss [mW]
VULCAN	3.3	200	660	92	57
VULCAN	1.8	180	320	82	71
LVDS & Slow Monitoring	3.3	200	660	91	65
Internal	6.0	310	1860	86	299
GCU	12.0	800	9600	89	1186
Total			13000	88	1678

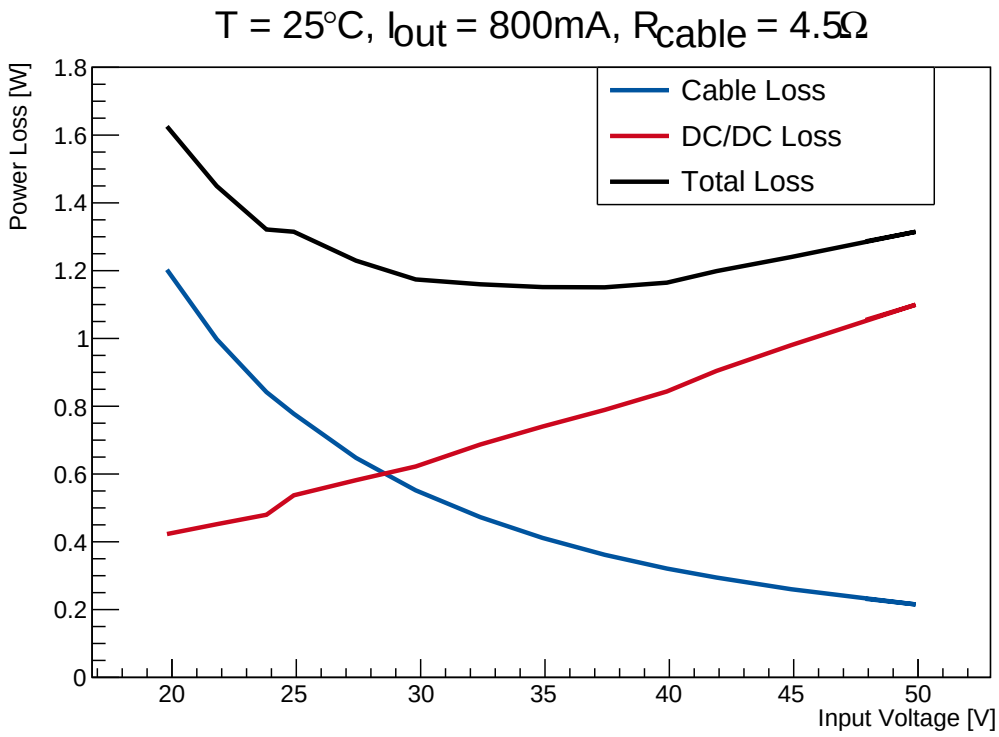


Figure 7.11: Power loss as a function of the input voltage. The DC/DC converter loss increases with higher input voltages as the voltage drop gets higher, whereas the cable losses decrease with higher voltages as the current gets smaller.

7.1.3 Ripple

The voltage ripple minimization is one of the main foci in the design of the PB. The goals are a peak-to-peak ripple of $10\,\mathrm{mV}$ for both VULCAN supplies and the internal voltage, as it might be used for the Tsinghua ADC, and $20\,\mathrm{mV}$ for the GCU supply.

Setup

The definition of the output ripple is non standard, as usually the DC/DC converter ripple is measured up to a bandwidth $20\,\mathrm{MHz}$. However, in this noise sensitive application it is decided to use a full bandwidth measurement ($1\,\mathrm{GHz}$) [48]. The difference between the different limits can be seen in figures 7.13 (a) to (c). Especially the switching spikes of the converter get suppressed by the bandwidth limitations. In the following, switching transient noise and output ripple will be not distinguished, so output ripple describes always whichever is higher.
In [47] is stressed that the measuring results improve greatly, if a $50\,\Omega$ transmission environment is used. Therefore a coaxial cable with a $50\,\Omega$ resistor as a termination is used, while the connected oscilloscope[3] has an input impedance of $1\,\mathrm{M}\Omega$ (see figure 7.12).

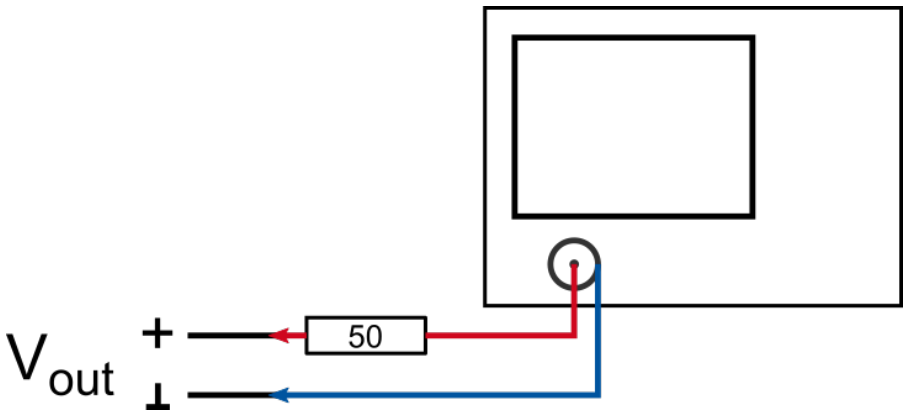
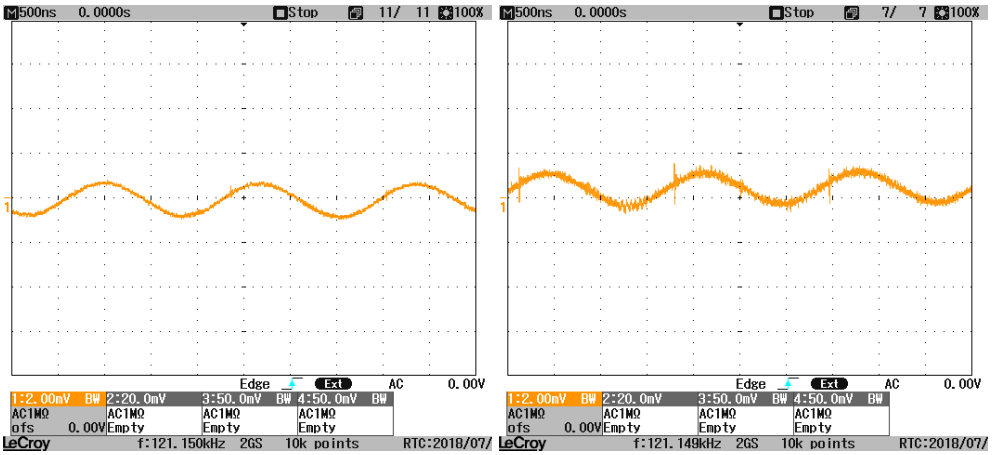
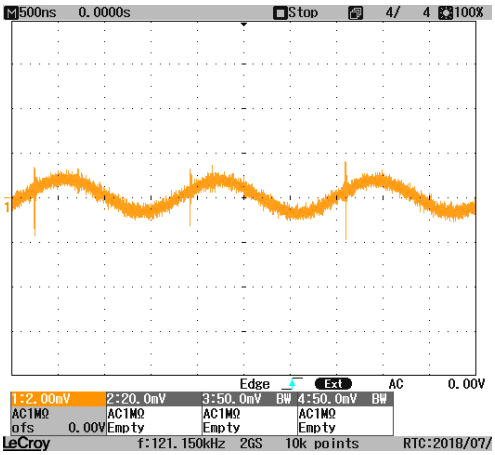


Figure 7.12: Setup used for the measurement of the output ripple.

[3] LeCroy WaveJet 354A



(a) 20 MHz (b) 100 MHz



(c) 1 GHz

Figure 7.13: Ripple of a DC/DC converter with different bandwidth limitations.

Results

The result of the optimization can be seen in figure 7.14. All goals were reached clearly within there margin of error. The ripple of the internal voltage (in case the Tsinghua ADC is used) is achieved with all connected DC/DC converters deactivated, that is necessary to reach the ripple limits. In case of the Tsinghua configuration the digital supply voltage should be generated from 24 V directly.
In addition to the oscilloscope measurement the frequency distribution is analyzed using a spectrum analyzer. All spectra show the corresponding multiple of the switching frequencies. Figures 7.15(a) to 7.15(c) show the result for the VULCAN supply voltages and the internal voltage. All spectra are dominated by the corresponding switching fre-

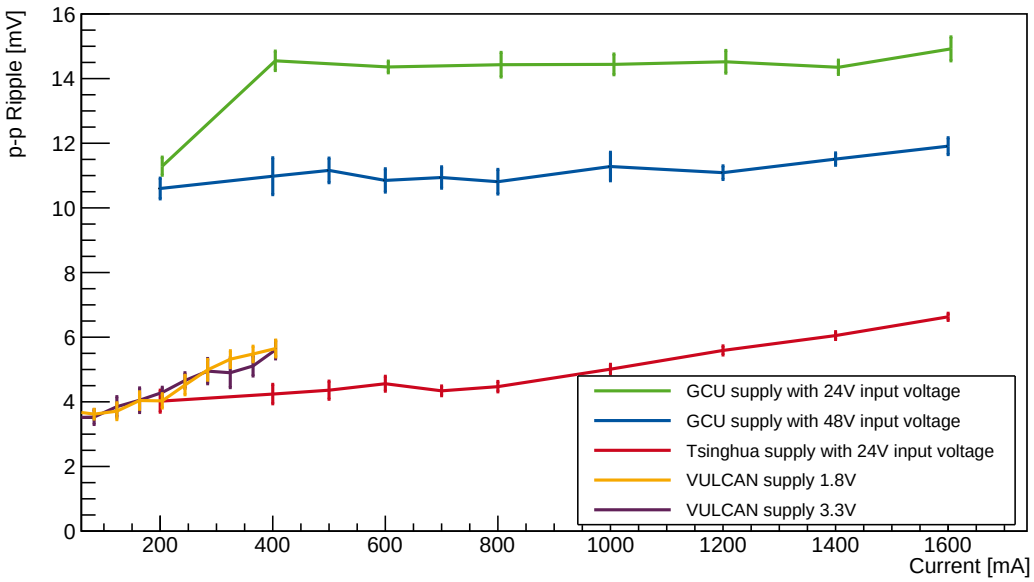
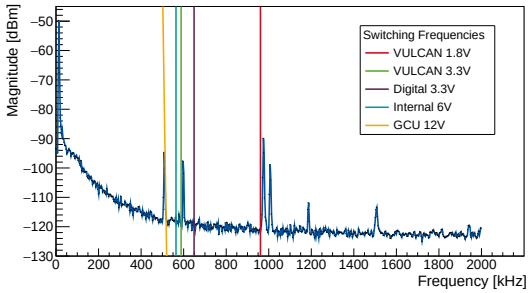
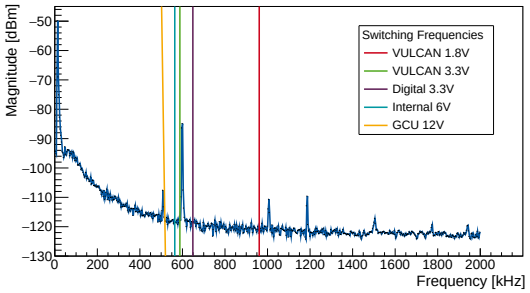


Figure 7.14: The output voltage ripple of the different DC/DC converters as a function of the output current.

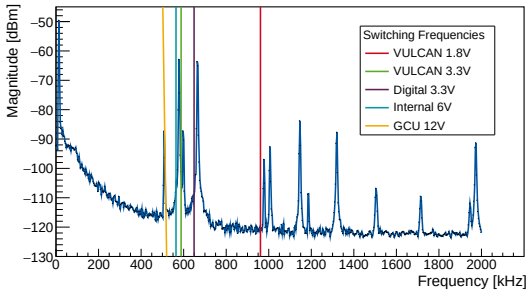
quency, but especially the internal voltage has strong contributions from the other converters connected. In contrast, in the internal voltage spectrum without the attached DC/DC converters only the GCU DC/DC and the internal DC/DC show contributions (see figure 7.15(d)). The spectrum of the 12 V GCU supply shows only contributions from the own switching frequency (see figure 7.15(e)).
All in all the ripple is well understood and all requirements were fulfilled. These measurements were done with the unmodified second prototype of the Power Board, which was adapted to improve the DC/DC converter stability. As a result of the changes the peak-to-peak ripple of some DC/DC converters has changed slightly. Primarily, the sinusoidal part of the ripple increased due to the reducing of the inductivity, but the peak-to-peak ripple measurements are dominated by transient noise. Since the changes are small and to keep the consistency with the mass-test the original configuration for the Power Board is used for these measurements.



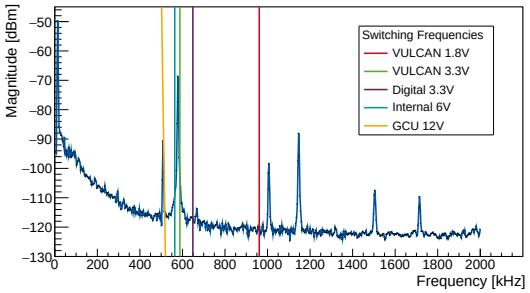
(a) 1.8 V VULCAN supply voltage.



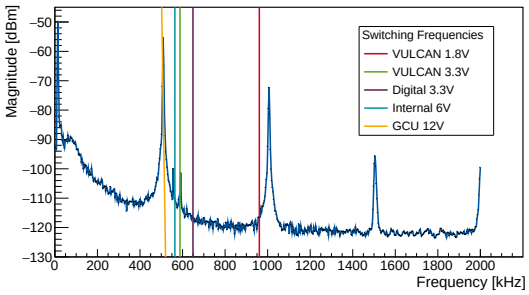
(b) 3.3 V VULCAN supply voltage.



(c) Internal voltage in VULCAN configuration.



(d) Internal voltage in Tsinghua configuration.



(e) 12 V GCU supply voltage.

Figure 7.15: Ripple of the different DC/DC converters measured with a spectrum analyzer.

7.1.4 Stability

The stability of DC/DC converters is critical, as variations in the output voltage might also damage the supplied components. The most common instability is the oscillation of the output produced by clocked loads, which is amplified by the feedback loop. Two opposing effects have to be considered in the frequency dependent feedback of the loop. On the one hand, noise or fast load changes can lead to instability, if fast changes in the feedback loop are not suppressed. On the other hand, fast changes in load should not lead to large output voltage changes.
In the following the stability will be tested with two methods, firstly a systematic scan of the feedback loop by injecting a sinusoidal signal and secondly fast load changes.

Gain/Phase Margin measurement for Feedback Loop Oscillation

In the first method a signal is injected into the feedback loop and the phase and gain difference is measured in the output. In figure 7.16 the injection and the measurements points are shown [49].

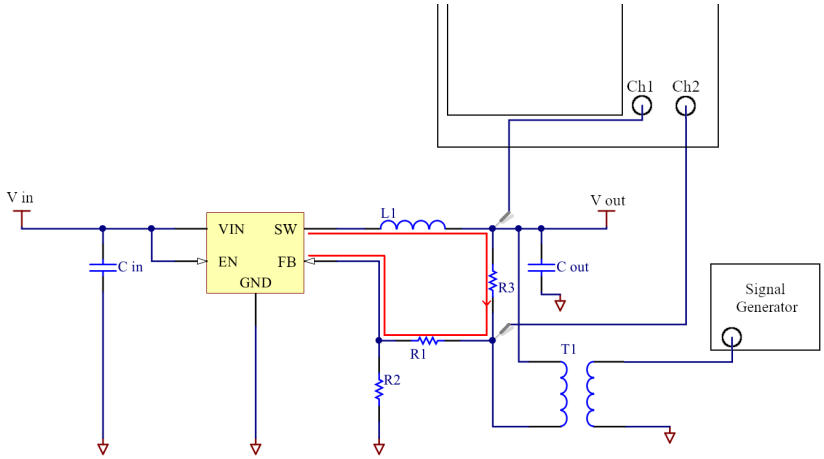


Figure 7.16: The figure shows a schematic view of the feedback loop oscillation stability test. Into the feedback loop (red) a small resistor R3 (in this case $10\,\Omega$) is added. The resistor needs to be small compared to R1 and R2, so the output voltage is not effected. At the choosen injection point the impedance of the DC/DC output is also much lower ($\mathcal{O}(\mathrm{m}\Omega)$) than the feedback loop, hence the measured loop gain is close to the real loop gain [50].

The stability criteria for a converter are, that as long as the feedback gain is one or higher the phase shift should be lower than $360°$ (higher $0°$) and if the phase shift is $360°$ ($0°$)

the gain has to be smaller one. However, to make the converters stable at all conditions a safety margin has to be maintained, which is $-15\,\mathrm{dB}$ for the gain and $45°$ for the phase. In addition, the gain slope should be $-20\,\mathrm{dB}/\mathrm{decade}$ close to the crossover. These criteria are suggested for the stability of DC/DC converters in satellites [51]. In figure 7.17 this principle is explained, using the induced and the output voltage.

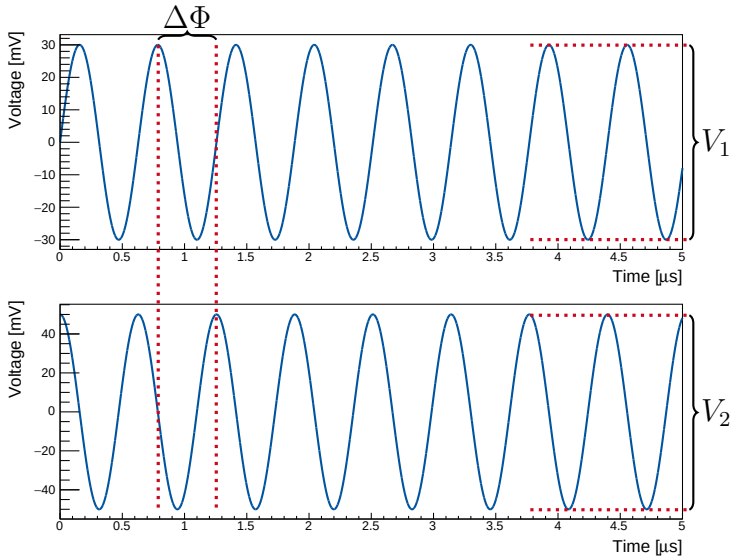
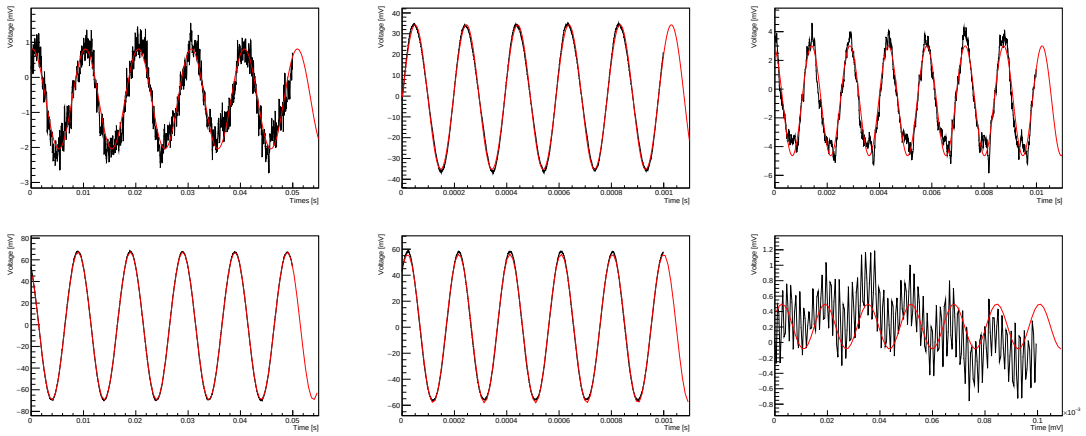


Figure 7.17: The measured variables are the phase difference $\Delta\Phi$ and the gain $G = V_2/V_1$. In this figure the injected signal can be seen at the top and the output at the bottom. The gain is expressed in dB, $G = 20 \cdot \log(\frac{V_2}{V_1})$.

It is important to mention, that the stability of a DC/DC converter is load depended, and particularly at low loads instabilities might occur [51]. Therefore, these test should be redone, if the power requirements change.
Using a signal generator and a transformer sinusoidal waveforms between $100\,\mathrm{Hz}$ and $150\,\mathrm{kHz}$ are induced into the feedback loop. The amplitude of the induced signal is regulated that input and output are always below $100\,\mathrm{mV}$. Higher voltages are unrealistic and might introduce unwanted effects. Therefore for very low and high frequencies one of the two signals is always very low and close to the oscilloscope resolution[4]. At high frequencies occurs the additional problem, that the transformer suppresses the signal, for examples of both problems see figure 7.18. Unfortunately, this leads to failing measurements in these regions, thus all scans are repeated several times to compensate for the problems.

[4]LeCroy WaveJet 354A



(a) 100 Hz (b) 5109 Hz (c) 65897 Hz

Figure 7.18: The different figures show the measurents of the injected signal (bottom) and the feedback of the DC/DC converter (top). In red the fit to the data can be seen. At low frequencies low induced voltages lead to a high response of the converter, while at medium frequencies the injected and feedback amplitude are similar, leading to the best scan results.

Load Step Measurement

An additional standard test is the so-called load step. Hereby, the output load of the DC/DC converters is changed rapidly, and the output voltage is monitored. An example for a measurement can be seen in figure 7.19. The most important characteristic parameter is the output voltage drop, that should be small enough to be still within the specification of the supplied components. The equivalent series resistor (ESR) and equivalent series inductance (ESL) of the output capacitors are causing a small step (ESR) and a spike (ESL), when the capacitors start discharging.
The measurements give similar stability information to the scan described before. In figure 7.20 the shape of the overshoot can be seen in dependence of the phase margin, that is investigated using the stability scan. All DC/DC converter should have a phase margin of at least $45°$, so the pulse shape is known, but the actual amplitude of the peak has to be investigated. These peaks are especially interesting for the high current DC/DC converter, so the internal supply and the GCU voltage.
Typically these load tests have a rising edge for the current of the order of $20\,\mu s$. In a second setup load changes with a rising edge of $< \mu s$ are tested with the GCU DC/DC converter. The fast changes are achieved using a field-effect transistor controlled by an Arduino Nano. A resistor of $110\,\Omega$ provides a constant load and a $10\,\Omega$ resistor can be switched on and off. Without the constant load the DC/DC converter is in light-load operation, which is unrealistic for our use-case [45].

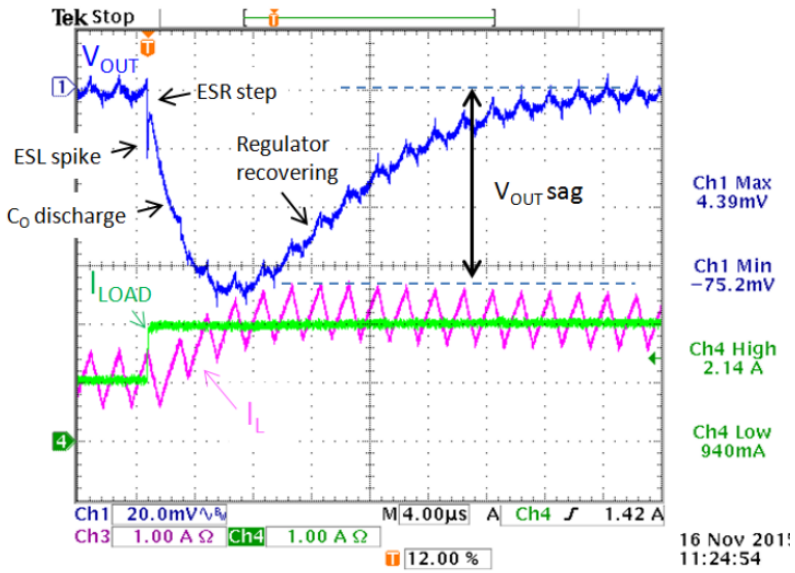


Figure 7.19: In this example with a $3.3\,\mathrm{V}$ converter a load step of $1\,\mathrm{A}$ leads to a voltage drop of $\approx 75\,\mathrm{mV}$ [52].

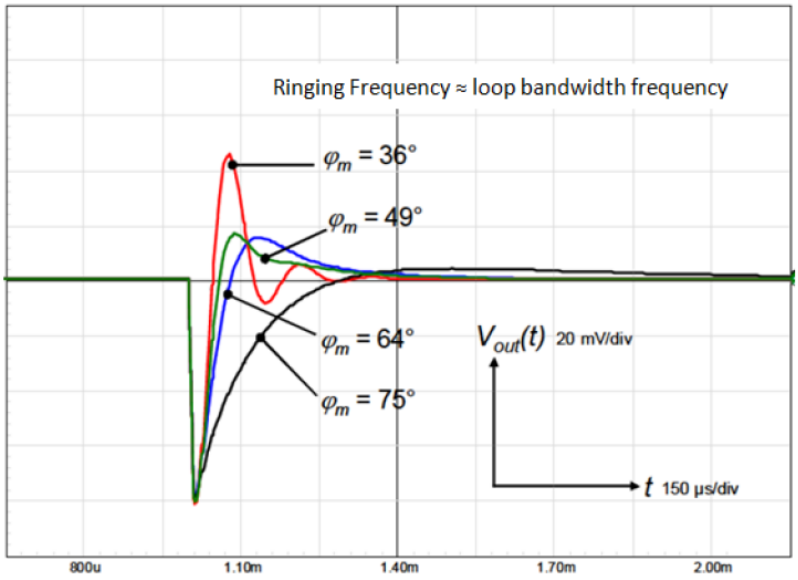


Figure 7.20: Overshoot of the DC/DC converter for different phase margins at a gain of $0\,\mathrm{dB}$ [52].

GCU Supply 12V

The result of the GCU supply stability measurement can be seen in figure 7.21. Both stability criteria are fulfilled clearly with a phase margin of $\approx 90°$ and a gain margin of $\approx 20\,\mathrm{dB}$. For high frequencies the amplitude curve flattens, which is an effect of the setup. Up to $30\,\mathrm{kHz}$ the gain slope is constant confirming the stability.

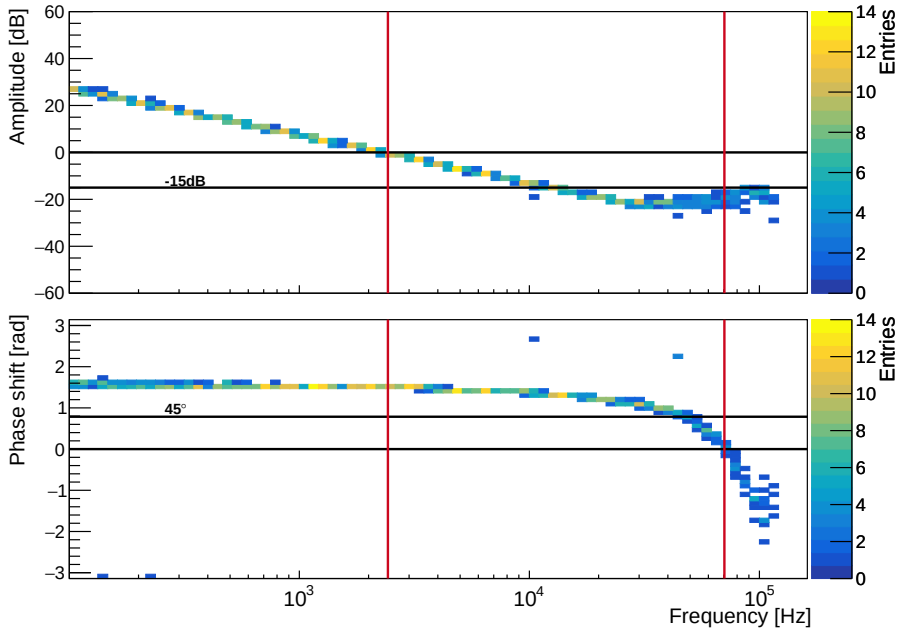


Figure 7.21: Gain/Phase measurement for the GCU DC/DC converter for a load current of $1200\,\mathrm{mA}$.

The load step amplitude measurement shows a maximal voltage change of $2.5\,\%$ of the output voltage, which is sufficient for the GCU input stage. Furthermore, these amplitude is only observed for the most extreme cases and for more realistic changes, e.g. $400\,\mathrm{mA}$ to $1400\,\mathrm{mA}$, the voltage drop is only $1.7\,\%$. Furthermore, even at faster load changes, see figure 7.23, the maximal amplitude are not higher. The zoom into the falling edge reveals a ESR/ESL spike, caused by the limited response speed of the capacitor, but the small forming confirms the low-ESR/ESL rating of the chosen components.

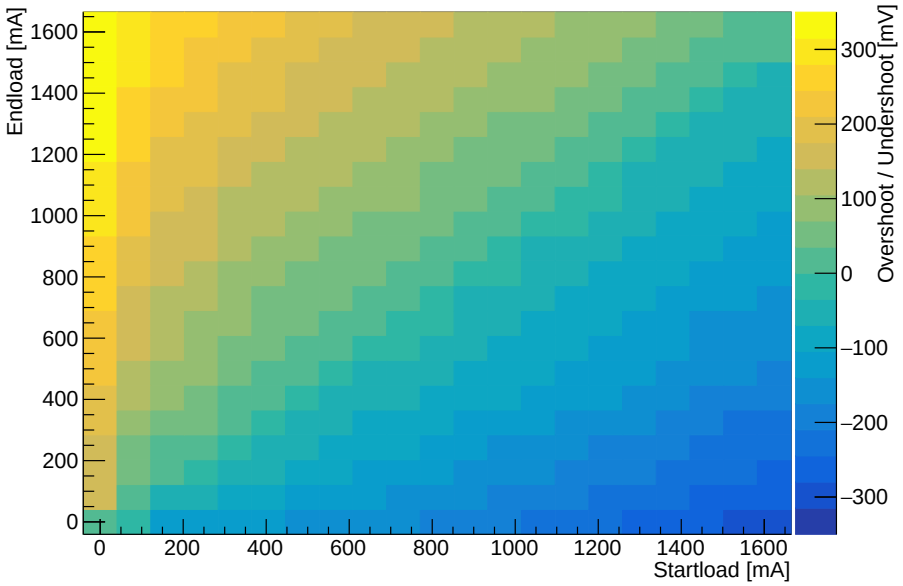
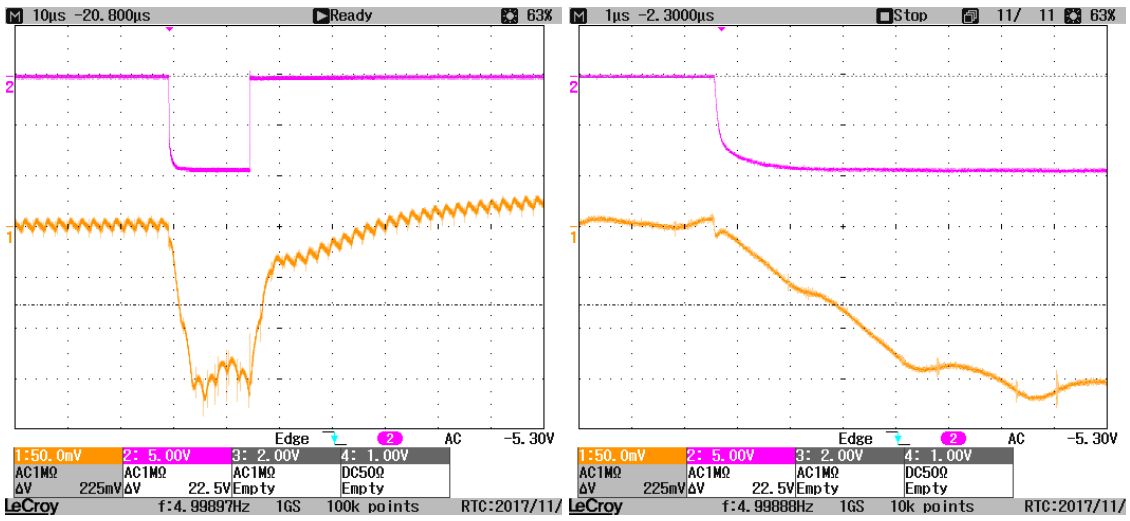


Figure 7.22: Amplitude of the over- and undershoots for load steps using the GCU supply.



(a) (b)

Figure 7.23: Loadstep measurement with the GCU supply. In both figures channel 1 denotes the output voltage of the converter and channel 2 is proportional to the output current. The current change is from 0.11 A to 1.2 A in 1 µs.

Internal 6V

The stability test of the internal voltage shows a phase margin of $90°$ and a amplitude margin of $30\,\mathrm{dB}$, fulfilling the stability criteria. The corresponding measurement can be found in the appendix 9.2. The fast load amplitude changes are similar to the GCU supply with up to $3.3\,\%$ of the output voltage. Comparing these output variations to the input range of the subsequent DC/DC converters confirms that these deviations will not disturb the supplies (see appendix 9.3).

Analog 1V8

The $1.8\,\mathrm{V}$ VULCAN supply voltage is also stable, but with a lower phase margin of $\approx 60°$ and a gain margin of $\approx 20\,\mathrm{dB}$ (see appendix 9.4). However, these values are still within the already conservative margins of $45°$ and $15\,\mathrm{dB}$, therefore the stability should be certain. Nevertheless, the margins could be improved by increasing the feedback capacity in parallel to the feedback resistor.

Analog 3V3

Figure 7.25 shows that the DC/DC converter is not stable. The phase margin is below $45°$ at a gain of one and at the phase shift of $0°$ the gain is higher than $-15\,\mathrm{dB}$.
The stability of the feedback loop is determined by three components: the output inductance, the output capacity and the feedback capacity (see figure 7.24). Reducing the output capacity is not investigated to keep the output ripple low.

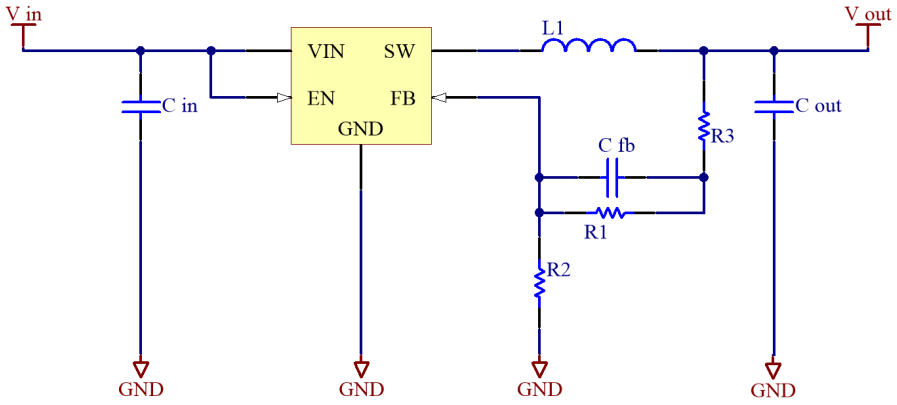


Figure 7.24: Schematic of a simple DC/DC converter including the feedback capacity. The feedback capacity is used for adjusting the feedback behauviour, especially the phase margin [45].

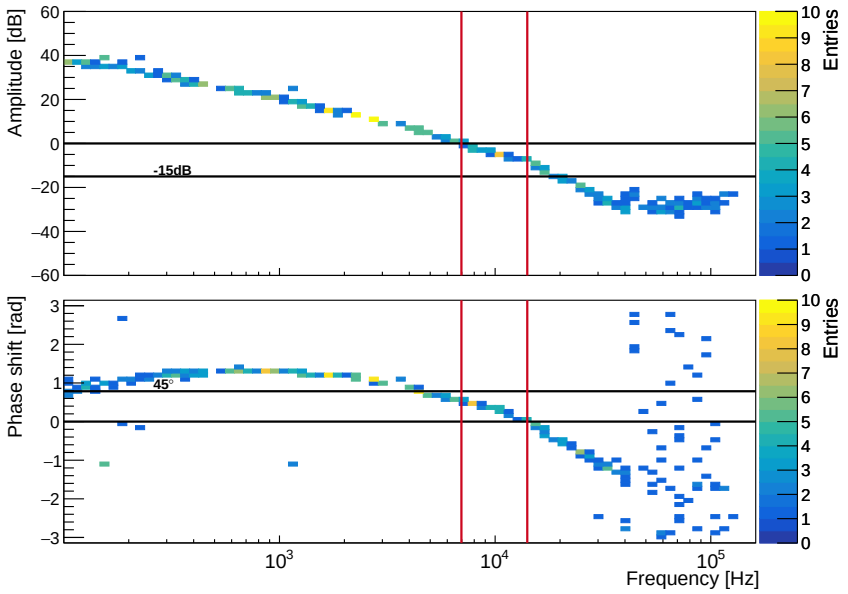


Figure 7.25: Gain/Phase measurements for the $3.3\,\mathrm{V}$ DC/DC converter for a load current of $330\,\mathrm{mA}$ before any changes.

The reason for the instability is the large inductor of $150\,\mu\mathrm{H}$. To minimize the voltage ripple the inductance is chosen higher than suggested by the manufacturer of the DC/DC converter. While higher inductivity decreases the output ripple, the efficiency and the stability can suffer. Therefore the $150\,\mu\mathrm{H}$ inductor is replaced with a $47\,\mu\mathrm{H}$ and a $22\,\mu\mathrm{H}$ inductor, respectively. The measurement can be found in the appendix 9.5. The corresponding margins can be seen in the first part of table 7.2. Compared to the original measurement the phase shift measurement changes, while the gain measurement is similar. Due to these changes the stability criteria are fulfilled, however at the low frequencies the phase margin is small.
In the next step the influence of the feedback capacity is investigated. The higher feedback capacity might help with stability, as the output capacitors have a low equivalent series resistance (ESR) [45]. The resulting margins can be seen in the second part of table 7.2. The results lead to the conclusion that a higher feedback capacity greatly improves the phase margin (see appendix 9.6). The gain crossing shifts to lower frequencies, while the zero phase crossing stays at the same frequency. Around the $-15\,\mathrm{dB}$ threshold the gain curve flattens for too high feedback capacities.
Based on these results the feedback capacitor should be changed to $27\,\mathrm{pF}$ (before $15\,\mathrm{pF}$) and the inductor to $22\,\mu\mathrm{H}$ (before $150\,\mu\mathrm{H}$). The resulting stability scan shows that all stability criteria are fulfilled (see table 7.2, see figure 7.26).

Table 7.2: Phase and gain margin in dependence of the feedback capacity and inductance.

Feedback Capacity [pF]	Inductance [µH]	Phase Margin [°]	Gain Margin [dB]
15	150	35	8.5
15	47	45	15
15	22	51	22
27	150	57	10
47	150	80	12
100	150	87	15
27	22	66	22

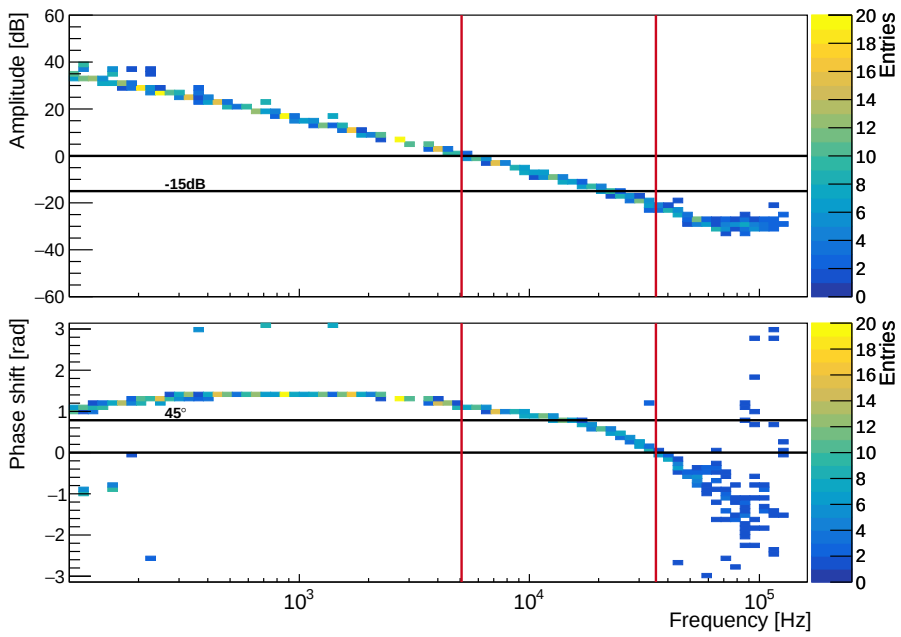


Figure 7.26: Gain/Phase measurements for the 3.3 V DC/DC converter for a load current of 330 mA. The inductor is changed from 150 µH to 22 µH and feedback capacity from 15 pF to 27 pF.

Cable 3V3

Based on the experience from the analog $3.3\,\mathrm{V}$ converter the inductor and the feedback capacity were adjusted to the same values as the A3V3 converter. The gain and phase margin of $20\,\mathrm{dB}$ and $\approx 65°$ are well within the limits. All stability scans with the cable converter can be found in the appendix (see figures 9.7 and 9.8).

7.2 Slow Monitoring

The slow monitoring is tested using an Arduino Nano to request and receive data. The final implementation has to be done on the FPGA on the GCU.
All devices can be accessed without problems using the corresponding I^2C addresses and respond with correct data. The precalibrated temperature and voltage sensors worked flawless. For the current measurement a slight adjustment has to be done. A simplified schematic of the current measurements can be seen in figure 7.27. In order to perform a stable measurement the shunt resistor was increased to enlarge the voltage drop, while reducing the gain of the amplifier itself to ensure a matching output range. The results can be seen in figures 7.28.

Table 7.3: Configuration for the current measurement.

	R_{shunt} [Ω]	R_{gain} [kΩ]
PoE input	0.5	10
PoC input	0.5	18

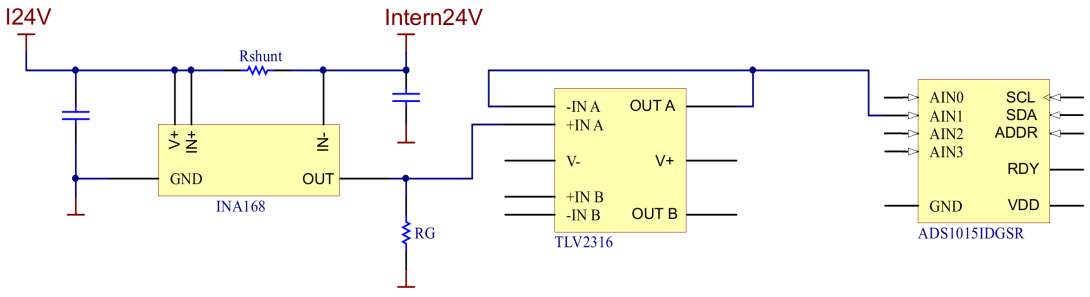
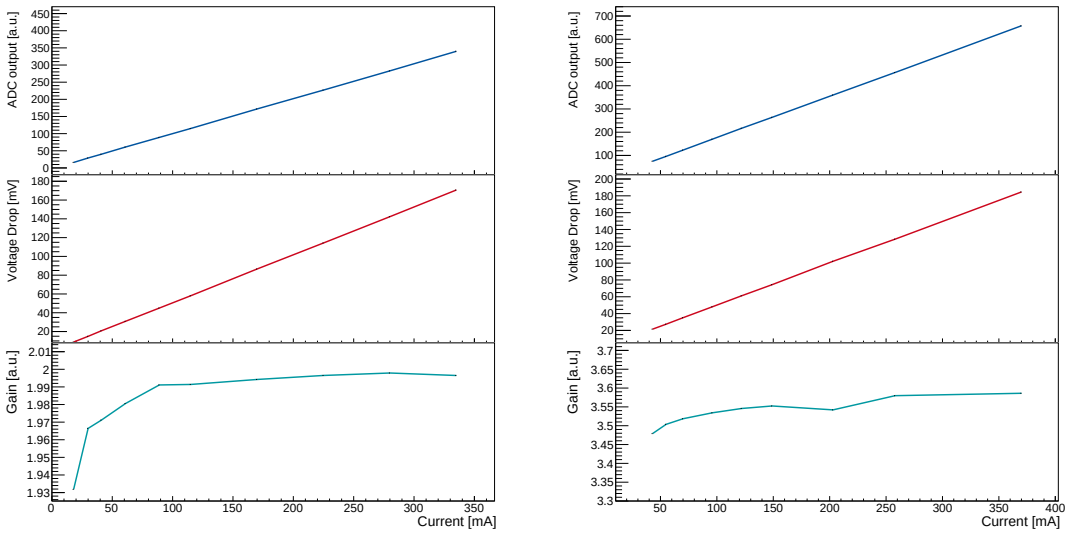


Figure 7.27: Simplified schematic of the current measurement as implemented on the PB.



(a) (b)

Figure 7.28: Voltage drop over the shunt resistor, gain of the INA168 and ADC output as a function of the input current for PoE (a) and PoC (b).

7.3 Ethernet

The Ethernet was tested using one Power Board on each end of the $100\,\mathrm{m}$ CAT5e cable (see figure 7.29). During the test $\approx 15\,\mathrm{W}$ are transferred using the same cable pairs. The modified board is connected to a router, while the test board is connected to a PC and a simple speed test is run (see figure 7.30). The Ethernet connection was stable at all tested circumstances, including LVDS signals on the additional pairs of the same cable.
In a final testing setup this speed test should be done using an FPGA.

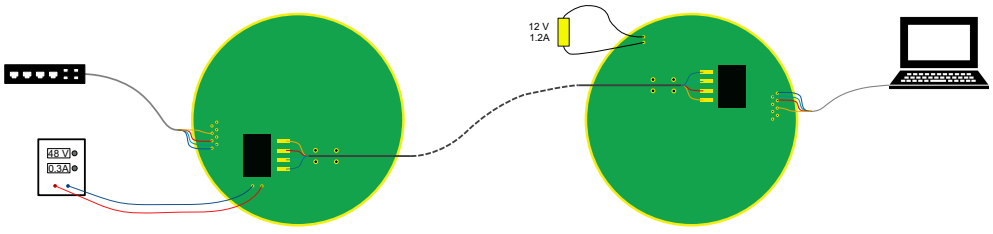


Figure 7.29: Schematic setup of the Ethernet test.

Figure 7.30: Simple Ethernet speed test with an internet connection.

7.4 LVDS Link

The LVDS link was tested using two Power Boards connected via the 100 m CAT5e cable. Unfortunately, the equipment for a pseudo-random-bit stream is not available so a simpler setup with two signal generators is used (see figure 7.31). Testing with a generator, a frequency of 125 MHz corresponds to the required data rate of 125 Mbit/s. Frequencies up to 200 MHz are tested to ensure a stable operation.
A complete LVDS test using one Power Board and one back-end card was done in Brussels by Yifan Yang, which showed that the used RX and TX chip can fulfil the JUNO requirement. A slight modifications compared to our implementations is needed to suppress high frequency crosstalk (see figure 7.32).
A test result can be seen in figure 7.33 and shows that the transmission is working using two different frequencies. Tests in parallel to Ethernet transmissions showed no reduced stability.

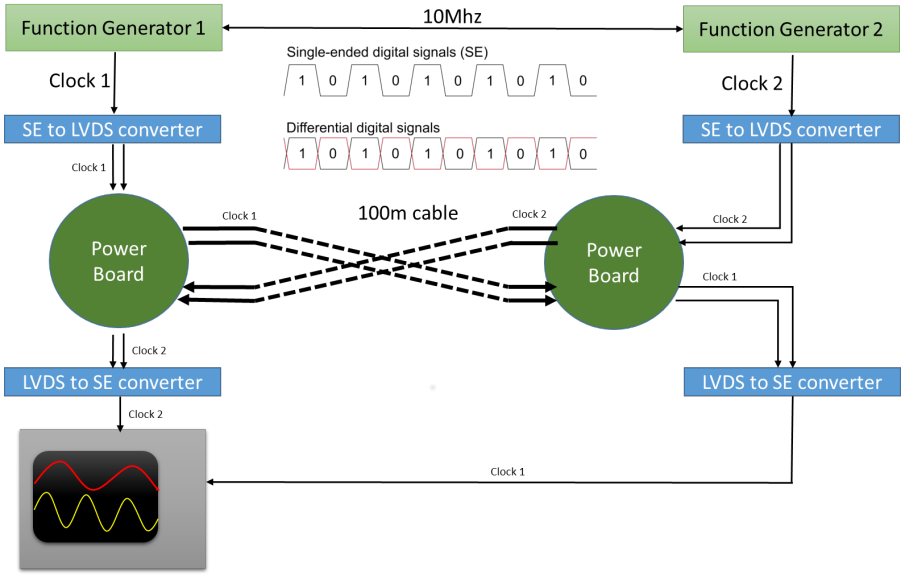


Figure 7.31: Schematic setup for the measurement of the LVDS connection. The generator signals are converted to differential signals, which are transferred through the 100 m cable.

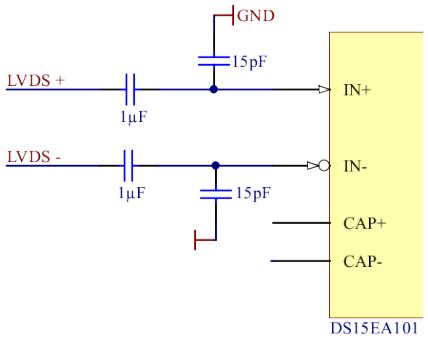


Figure 7.32: The small 15 pF capacitors suppress high frequency crosstalk.

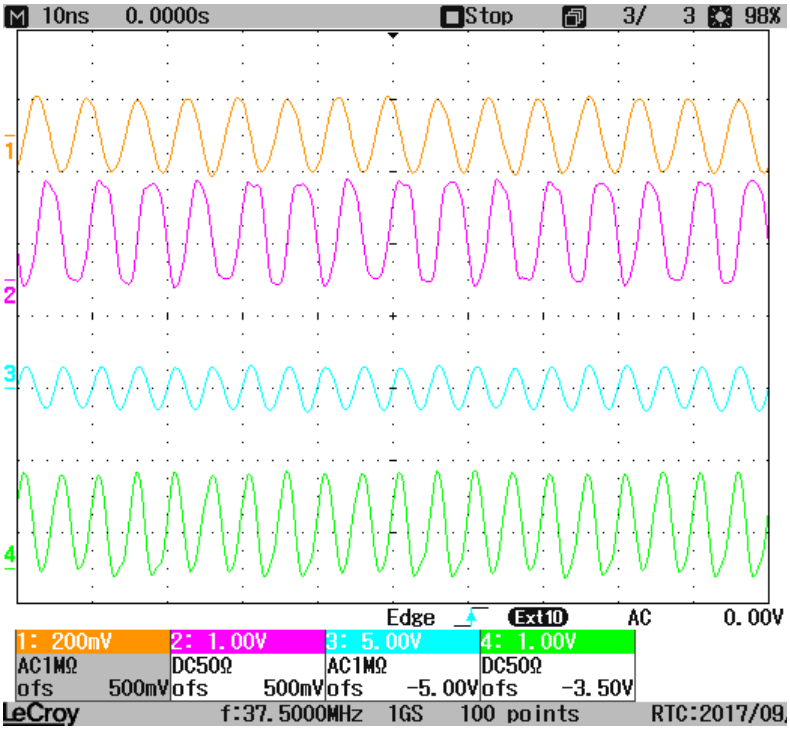


Figure 7.33: Result of an LVDS test of board 162. Function generator 1 produces a 150 MHz signal (channel 1), which is transferred through 100 m cable. After conversion to a single-ended signal it can be measured in channel 2. Simultaneously is the second signal generated (200 MHz, channel 3) and send through the same cable in the opposite direction resulting in the second output (channel 4).

7.5 Board Temperature after Potting

In the final iPMT setup the electronics are potted into a closed housing, therefore some temperature tests using dummy electronics are done. The goal of this measurement is to determine the board temperatures to make sure all components are within their specification. The dummy electronics mimics the power usage and distribution of the final electronics. In the tables 7.4 and 7.5 the used load resistors and the resulting power consumption for the Power Board and the General Control Unit can be seen.

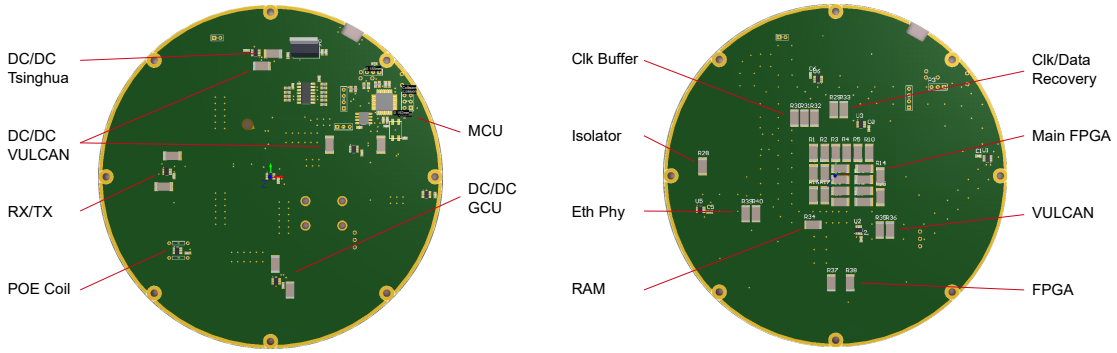
Table 7.4: Dummy Power Board configuration assuming $24\,\mathrm{V}$ supply for the board. All power usage estimations are conservativ.

Component	Power[W]	Resistor[Ω]	Power Dummy[W]	Rel.[%]
TX	0.15	3900	0.15	98.5
RX	0.21	2700	0.21	101.6
PoE Coil	0.3	1820	0.32	105.5
DC/DC GCU	1.3	440	1.31	100.7
DC/DC VULCAN	0.31	1800	0.32	103.2
DC/DC Tsinghua	0.8	730	0.79	98.6
Total	3.07		3.10	100.8

Table 7.5: Dummy GCU Board configuration assuming $24\,\mathrm{V}$ supply for the board. All power usage estimations are conservativ.

Component	Power[W]	Resistor[Ω]	Power Dummy[W]	Rel.[%]
FPGA	8.8	65.75	8.76	99.6
FPGA 2	1.15	540	1.07	92.8
RAM	0.4	150	0.38	96.0
VULCAN	1.1	540	1.07	97.0
ETH PHY	0.25	2400	0.24	96.0
DC/DC	3.3	171	3.37	102.1
CLK-Buffer	0.9	660	0.87	97.0
Isolator	0.2	2700	0.21	106.7
Clock Recovery	0.8	750	0.77	96.0
Total	16.9		16.74	99.1

The ground connection (heat transfer connection) of the different components was imitated by using surface mount or wired resistors and the position is matched the original positions (see figure 7.34, see appendix 9.10 for bottom side). The power usage of the high voltage unit mounted to the base is neglected in the dummy setup.



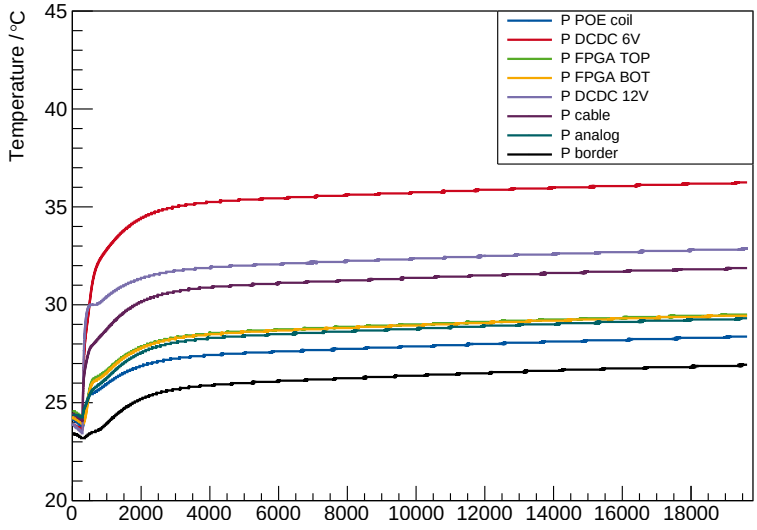
(a) Power Board (b) General Control Unit

Figure 7.34: Dummy board load distributions.

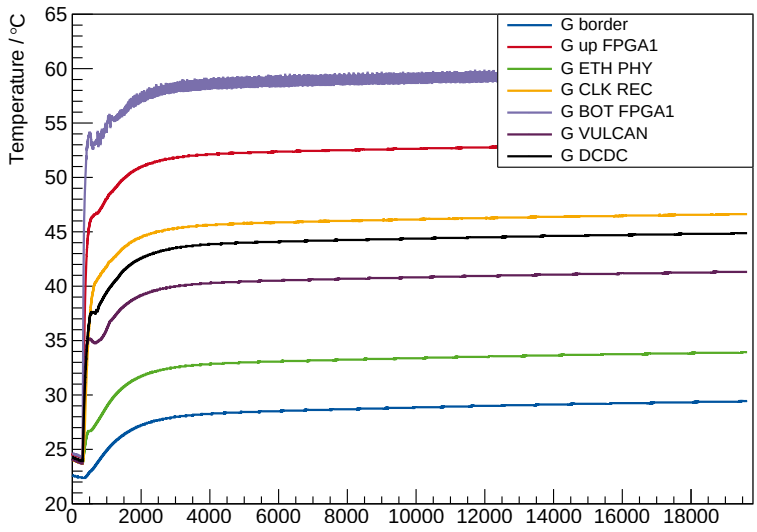
To monitor the temperature, eight temperature sensors and a micro controller unit are mounted on the dummy PB. Additionally seven temperature sensors are mounted on the dummy GCU connected using a I^2C multiplexer. The temperature data is send out using RS485.
The dummy electronics was potted into a prototype housing for the iPMTs using mineral oil as filling material. The potting is done similar to the final assembly steps. Firstly, a prototype base gets soldered to a (defect) MCP-PMT. In the next step a stack of a shielding disk, a GCU dummy board and a PB dummy board is connected to the base. Finally, an Ethernet cable is soldered to the Power Board to supply the dummies and receive the temperature data. This stack with PMT is glued to the oil-filled housing (see figure 7.35). The temperature measurements are done, while the housing is submerged into water with a temperature of $19\,^{\circ}\mathrm{C}$. The water heats by $\approx 0.5\,^{\circ}\mathrm{C}$ during the measurement. During the measurements the PMT is always at the top and the housing at the bottom.
Figure 7.36 shows the result of the measurement. The maximal temperature is measured on the GCU board on the bottom, opposite of the main FPGA. The main FPGA could be $10\,^{\circ}\mathrm{C}$ to $15\,^{\circ}\mathrm{C}$ warmer. A simple head spreader may be used to reduce the temperature. This test should be redone with a final GCU board, as this two layer board shows different heat conductivity than the original 16 layer board. The fluctuations observed for some temperatures seems to be an effect of the oil, as measurements in air show no similar effect.
The temperatures on the Power Board reveal that the maximal temperature is observed close to the internal DC/DC converter. Surprisingly, the center of the PB, directly over

Figure 7.35: Picture of potted Dummy Electronics.

the FPGA, does not rise above $28\,^{\circ}\mathrm{C}$.
For the reliability calculation of the PB a temperature of $40\,^{\circ}\mathrm{C}$ for all components is assumed, which no PB-component in this test exceeded. The maximal temperature of $35\,^{\circ}\mathrm{C}$ is a good safety margin as the water buffer temperature is not fixed.
All in all the temperature test is encouraging, that the final electronics will have no heating problems. Additional tests with the final electronics and also different tilts of the housing should be done.



(a)



(b)

Figure 7.36: Temperature of different components of the Power Board (a) and GCU (b) using dummy electronics. The start temperature of $25\,^{\circ}\mathrm{C}$ is the result of a test measurement earlier in the day.

Chapter 8

Mass-Testing

In the beginning of 2017, 20 prototypes of the iPMT electronics were supposed to be assembled and tested. In order to simultaneously test the production and reliability 116 boards were ordered from two different assembly companies. Twenty boards were tested immediately and send to China for assembly.
The remaining boards were used for further testing and the development of a first board-test setup. In the large scale production every board has to be tested in less than $1\,\mathrm{min}$. The tested specifications are:

- Slow Control
- Voltages
- Voltage Ripple
- Trigger sending/Clock receiving
- Power over Ethernet
- Power over Clock

The methods for all tests have been developed and were tested in a prototype setup automatically.

8.1 Setup

The setup for the Power Board tests can be seen in figure 8.1. The grey $100\,\mathrm{m}$ Ethernet cable is connected to a modified second PB, where power is induced on the clock line and the Ethernet line. In order to tests the boards without GCU boards simple, but appropriate, tests were developed.
The connections to the tested board were done with solder joints, board-to-board connectors and PCB spring probes. Although , the results of the tests are good, for a faster test

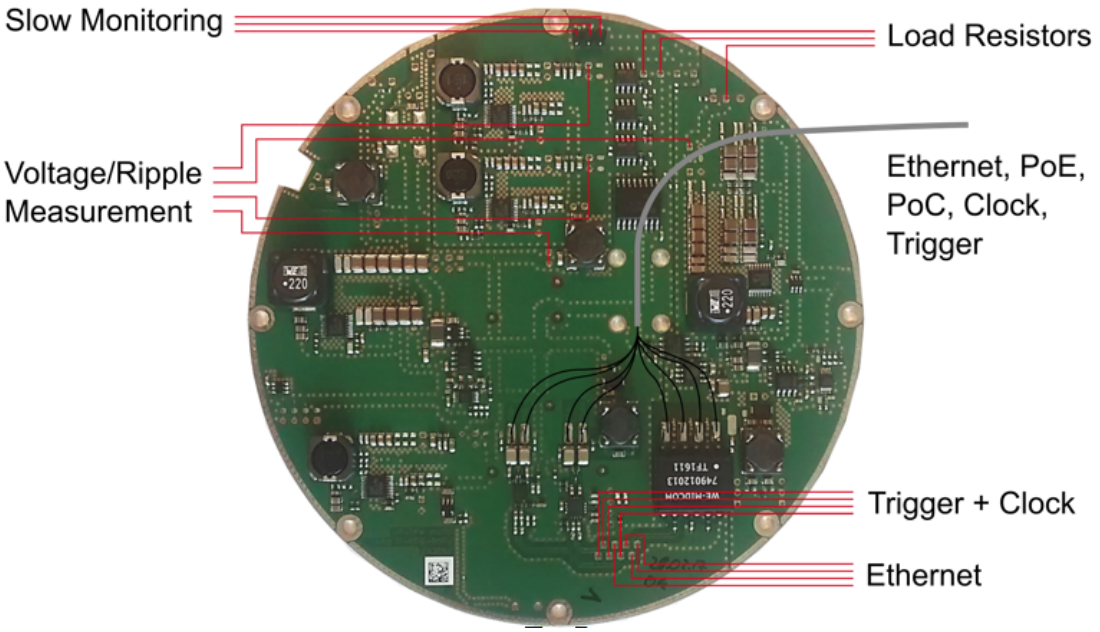


Figure 8.1: Schematic of the Power Board test setup. Note the maximal voltages of $-2\,\mathrm{V}$ and $1\,\mathrm{V}$.

only spring probes should be used, which are soldered to a specially designed adapter-PCB. Whether parts of the test-equipment should be placed on the adapter board (e.g. ADCs) depends on the desired tests. Moreover, the standard spring probes have strong bandwidth limitations, which might make the current LVDS/Ethernet and voltage ripple tests impossible. This problem can be solved in two ways: Firstly high bandwidth spring probes are available, but often require expensive mating connectors on the tested board. The second option is to just measure at lower bandwidth and extrapolate the results based on experience, e.g. if the trigger sending unit works at low data rates, it should work at high data rates.
The modified Power Board had some reliability problems, that can be traced back to the PoC. The LVDS sending unit (DS15BA101) has a limited ESD protection in the output, which leads to chip failures in combinations with fast on and off switching of the power. The voltage drop at the input of the chip can be seen in figure 8.2. Introducing a voltage ramp ($20\,\mathrm{V/s}$) eliminates this problem. Nevertheless, it is important to remember the chips vulnerability to fast voltage changes.

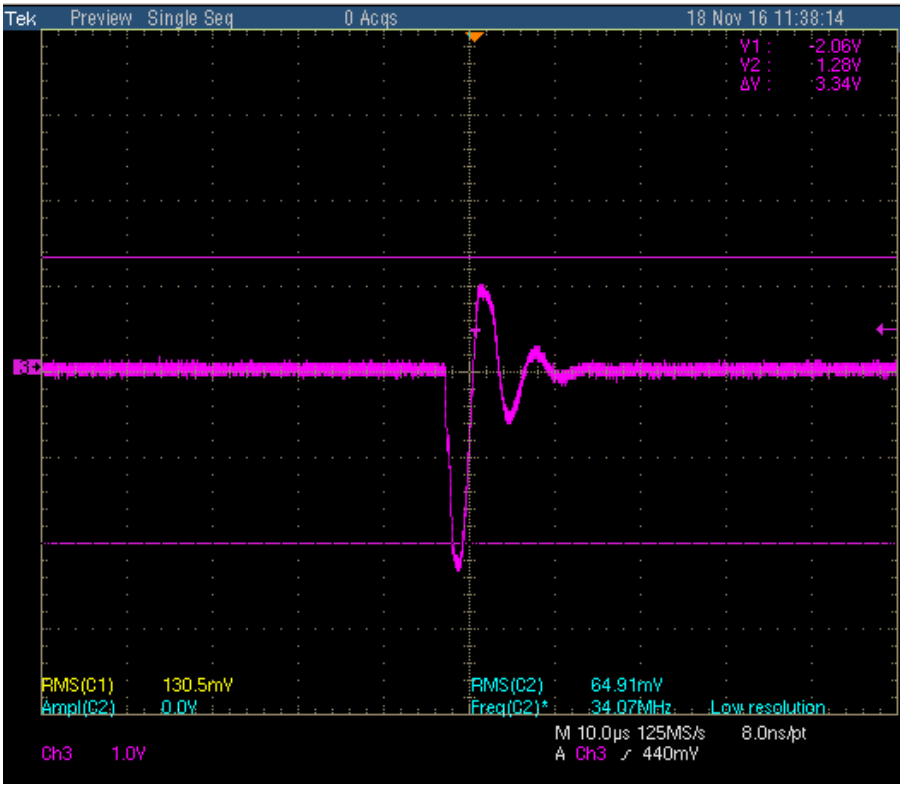


Figure 8.2: Voltage signal at the input of the DS15BA101 when switching the voltage.

8.2 Ethernet

The Ethernet was not tested for each board, since it is a completely passive system and and it was anticipated that problems with the Ethernet transformer would also present as problems with the Power over Ethernet. For some boards the connection was tested soldering short Ethernet cables to the modified Power Board and the tested Power Board. In a final full mass test the Ethernet should also be checked using the FPGA. However, the compatibility with spring probes has to be ensured.

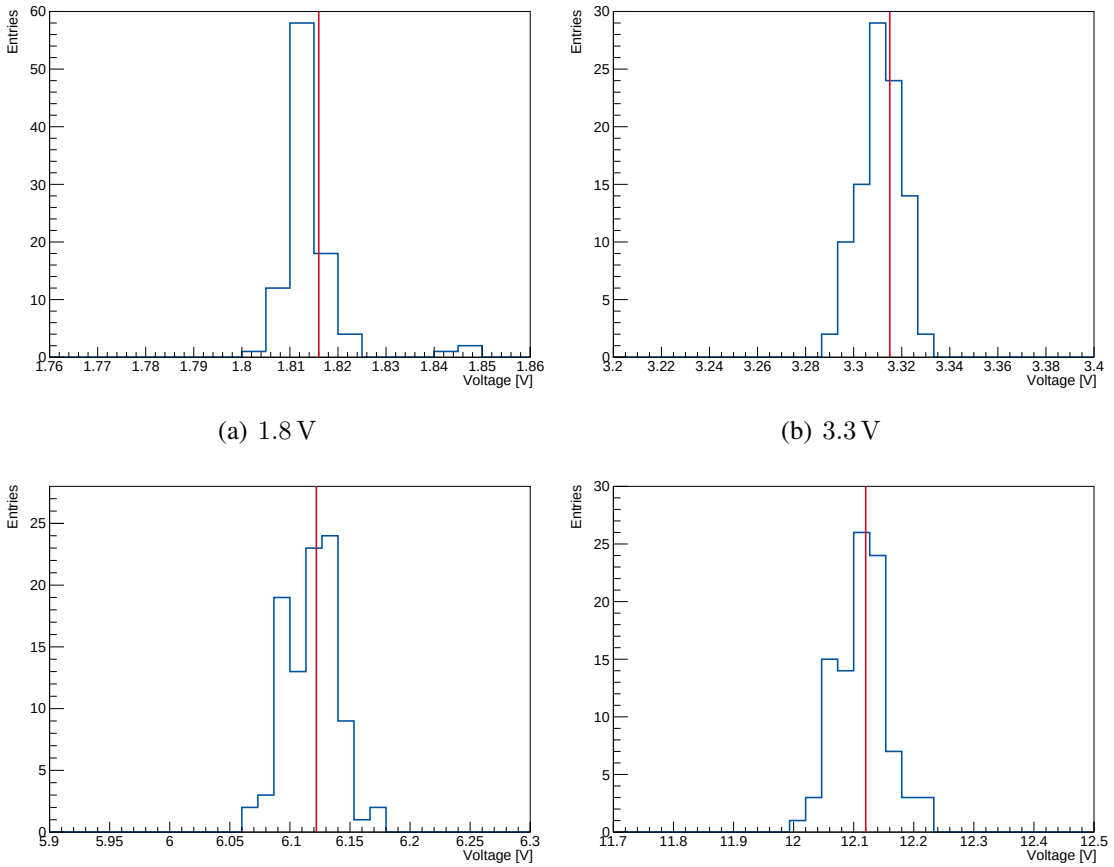
8.3 Output Voltage

The output voltage was measured using a simple hand-held multimeter[1], with an accuracy of $\pm 0.8\,\% \pm 2\mathrm{dgt}$[2][53]. For a larger test sample this should be done with a multimeter connected to the computer or a simple micro controller unit (MCU). Even small MCUs

[1] Voltcraft M-3890DT

[2] dgt: digits, $4\,\mathrm{V}$ range: $1\,\mathrm{mV}$ resolution, $40\,\mathrm{V}$ range: $10\,\mathrm{mV}$ resolution

offer ADCs with a resolution of $8 - 10$ bit, which is sufficient to determine the output voltages.
The output voltage is determined while a load resistor of $10\,\Omega$ is connected. In light load mode the DC/DC converters change the switching frequency to increase the efficiency (see figure 9.9(a)), leading to a voltage shift. Around $100\,\mathrm{mA}$ load has to applied to reach the desired voltage (see appendix 9.9(b)).
The output voltages of all measured boards can be seen in figure 8.3. Variations within $1\,\%$ are expected, as the resistors and the reference voltage to set the voltage and also the multimeter to measure the voltage has an accuracy of $\approx 1\,\%$. The outliers for the $1.8\,\mathrm{V}$ output voltage were investigated and could not be repeated, which leads to the conclusion, that the load resistor was not properly connected during the measurement.



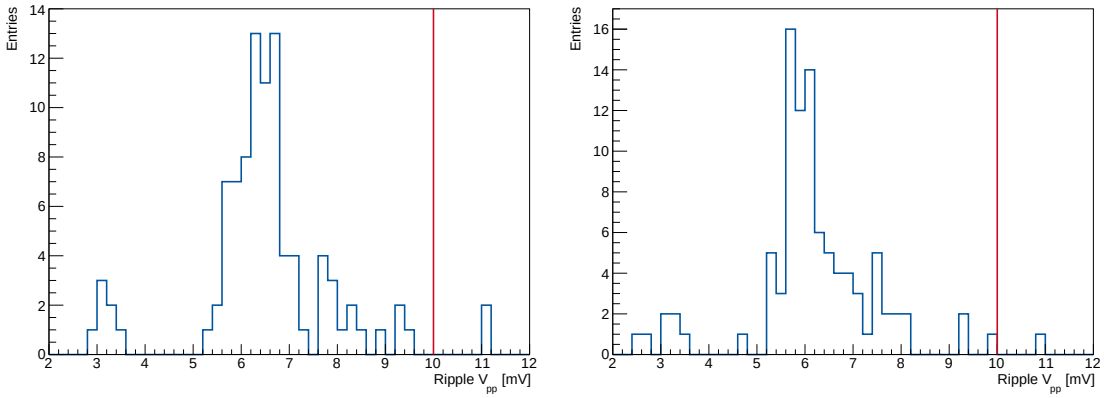
(a) $1.8\,\mathrm{V}$ (b) $3.3\,\mathrm{V}$

(c) $6.0\,\mathrm{V}$ (d) $12.0\,\mathrm{V}$

Figure 8.3: Output voltages measured for 96 power boards, the red lines indicate the set voltage. Since only common resistor values are used the voltages are not exactly matched.

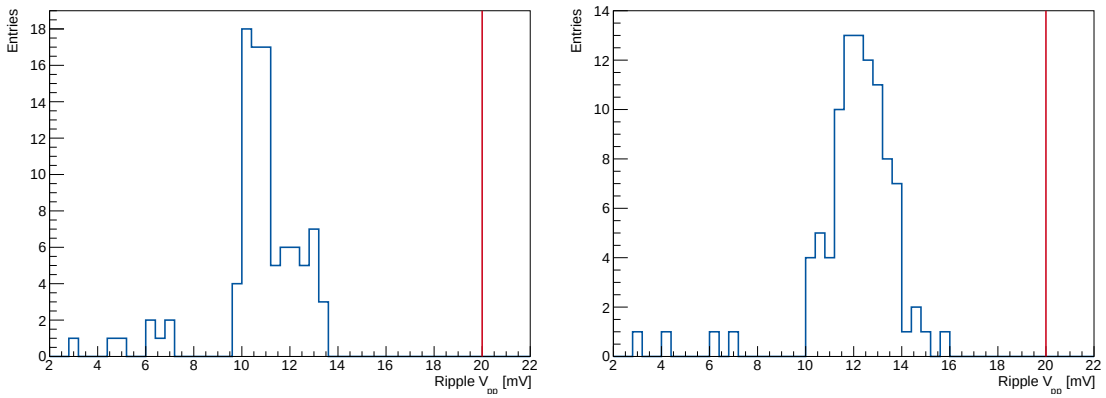
8.4 Output Ripple

The output voltage ripple is measured with a similar setup as the output voltage using an oscilloscope with $1\,\mathrm{GHz}$ bandwidth. Per voltage ten measurements are done with 500000 points each taken over a time of $1\,\mu\mathrm{s}$. Thereby not only typical DC/DC converter noise, whose changes are on the time scale of the switching frequency, but also low frequency noise is recorded. The ten measurements are averaged, to eliminate the impact of outliers, which might be caused by environmental noise.
The results in figures 8.4 and 8.5 are mostly within the requirements of the Power Board. The outliers of the $1.8\,\mathrm{V}$ and $3.3\,\mathrm{V}$ converters were investigated and could not be repeated, fulfilling the requirements in the second measurement. Therefore, a simple retesting of the boards could eliminate this problem. In a fixed setup with an adapter-PCB the measurement would be more stable, as even small imprecision change the outcome, e.g. angle of the probe to the board. The very low ripple values can be traced back to a bad connection to the board.
From the measurements at a bandwidth limit of $20\,\mathrm{MHz}$ the DC/DC converter dominated by switching transient noise ($1.8\,\mathrm{V}$, $3.3\,\mathrm{V}$, $6\,\mathrm{V}$) can be separated from the converter dominated by voltage ripple ($12\,\mathrm{V}$), as the bandwidth limitation mainly suppresses transient noise (see figure 8.6).
An alternative to using a oscilloscope for the final testing is not realistic considering the bandwidth limitations.



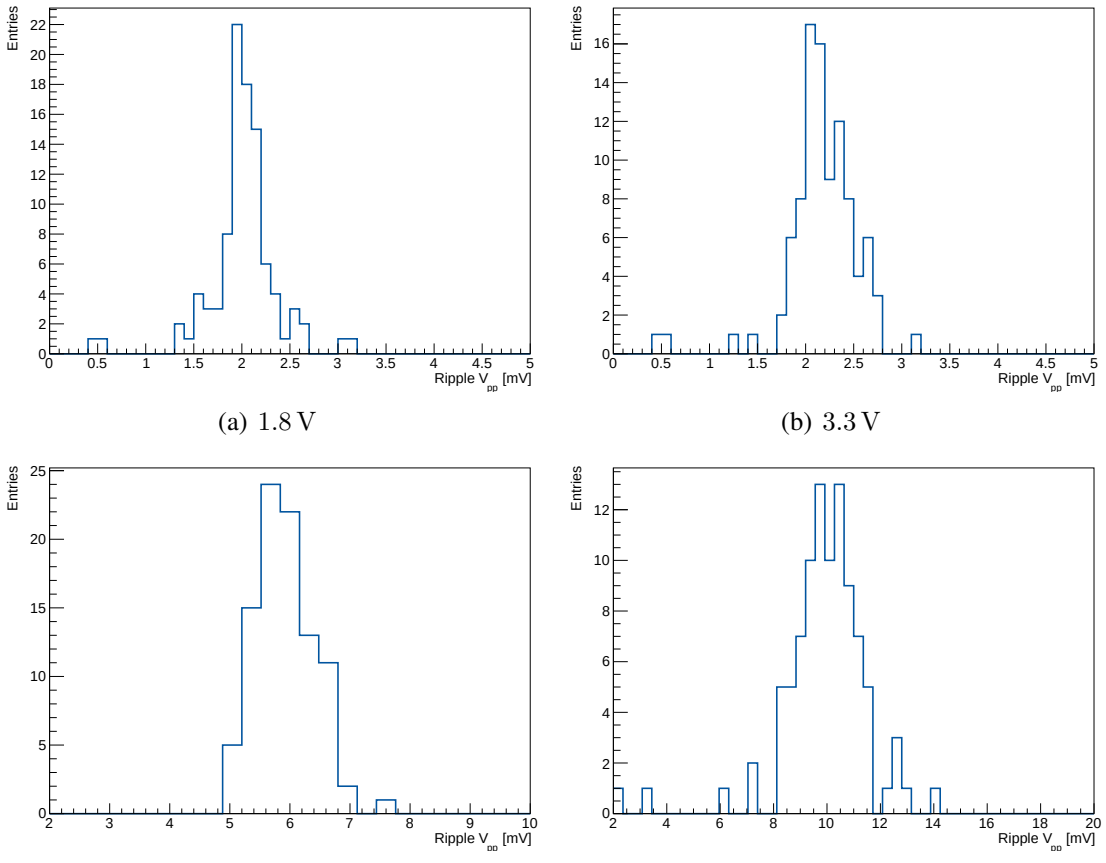
(a) $1.8\,\mathrm{V}$ (b) $3.3\,\mathrm{V}$

Figure 8.4: Voltage output ripple of 1V8 and 3V3 measured with full bandwidth.



(a) 6.0 V (b) 12.0 V

Figure 8.5: Voltage output ripple of 6V0 and 12V0 measured with full bandwidth.



(a) 1.8 V (b) 3.3 V

(c) 6.0 V (d) 12.0 V

Figure 8.6: Ripple measured with 20 MHz bandwidth.

8.5 Slow Monitoring

The slow monitoring is tested using a Arduino with an I^2C implementation connected to the PB. In order to verify everything is working the monitoring output is checked by the tester for reasonable results and the VULCAN starting sequence is tested using LEDs in parallel to the load resistors. Finally, the tester confirms the temperature and voltage readings.
All in all, the monitoring works good for all board, but sevens boards had problems with the VULCAN starting sequence. The $1.8\,\mathrm{V}$ could only be switched while the $3.3\,\mathrm{V}$ is active. The problem is not further investigated since the starting sequence is only needed for the first VULCAN prototype.
This work flow would be automatised in the mass testing, but for the current setup it is good to check these manually to make sure everything is connected properly.

8.6 LVDS

The LVDS transmission is tested in the same way as described in the previous chapter using two signal generators and an oscilloscope. Three different combinations of clock transfers are tested, while avoiding that up- and downlink have the same frequency ($100\,\mathrm{MHz}$ and $75\,\mathrm{MHz}$, $125\,\mathrm{MHz}$ and $150\,\mathrm{MHz}$, $200\,\mathrm{MHz}$ and $150\,\mathrm{MHz}$). Possible crosstalk in the cable and the setup prevents running at the same frequency, as crosstalk cannot be distinguished. The results of the measurements are saved on the PC and reviewed by the tester.
Despite some skipped bits at $200\,\mathrm{MHz}$ due to the experimental setup all boards were able to deliver the required speeds. In a final test real data should be send, using a back-end card and an FPGA instead of a PB with signal generators as the counterpart. An example measurement can be seen in the previous chapter (see figure 7.33).

Chapter 9

Conclusion and Outlook

This thesis discusses the design and test of a high reliability power distribution board for a novel readout concept for the JUNO detector. In the intelligent photomultiplier concept the readout electronics are mounted to the PMT. The electronics consist of a base with a high voltage module, a control unit including the ADC and the Power Board.
The connection to the outside is done using a standard Ethernet cable. Two cable pairs are used for the data connection using Ethernet and two pairs are used for synchronous connections transferring clock and trigger signals. The Ethernet and the clock line are additionally used to power the electronics, the clock line powers the low noise analog part and the Ethernet supplies the digital part.
The Power Board has to meet a number of challenging requirements concerning performance and reliability. In order to achieve the optimal readout performance, the output voltage ripple of the ADC supply should be below $10\,\mathrm{mV}$ peak to peak and all other supply voltages below $20\,\mathrm{mV}$. The prototype boards meet the requirements while also featuring a high overall efficiency of $88\,\%$.
The reliability limit originates from the JUNO goal to determine the mass hierarchy within the first 6 years. During this time only $0.5\,\%$ of the readout electronics should fail, which corresponds to 95 failures in $10^9\,\mathrm{h}$. Using selected manufacturers and high quality components, an upper limit on the failure rate of 40.4 failures in $10^9\,\mathrm{h}$ with a confidence level of $60\,\%$ is estimated for the Power Board. An additional step is taken to ensure a reliable operation by meeting high stability criteria for the DC/DC converters.
The temperature of the iPMT electronics is tested using dummy boards, which mimic the power consumption and distribution of the original electronics. The dummies are mounted to a PMT and potted in oil with a steel housing. Maximal temperatures of $\approx 35\,^\circ\mathrm{C}$ for the Power Board and $\approx 60\,^\circ\mathrm{C}$ for the control unit are reached.
In preparation of a mass production of the Power Board a fast test is developed. The goal is to determine if all important characteristics of the board are within the limits. 96 boards are tested with the test setup and after retesting some boards all passed. Since the iPMT concept was rejected by the JUNO collaboration, the final preparations to ensure a stable

and fast operation of the test setup have not been completed.
All in all, it can be shown that a power distribution board fulfilling high reliability requirements can be built and a fast mass production test is possible. The reliability estimation of the new JUNO readout concept will be done with the developed methods.
The intelligent PMT concept will be used to read out the OSIRIS detector, which is part of the JUNO liquid scintillator monitoring, but a redesign of the iPMT electronics is required.

Appendix

A. Reliability Estimation

Table 9.1: Information needed to calculate the PCB reliability according to Fides.

Factor	Value	Definition
$\Pi_{\text{placement}}$	1	The placement factor is 1 for printed circuit boards.
$C_{\text{sensitivity}}$	6.5	The sensitivity factor describes the sensitivity to overstress inherent to the item technology.
$\text{QA}_{\text{manufacturer}}$	1	The quality assurance level of the tested manufacturer is level 1 (ISO 9000 version 2000 certified).
$\text{QA}_{\text{component}}$	2	Component quality assurance level relative to the state of the art, Higher $= 3$, Equivalent $= 2$, Lower $= 1$, Very much lower $= 0$.
E_{risk}	3	Risk related to this manufacturer, recognised manufacturer: Mature process for the item considered = 4, recognised manufacturer: Process not analyzed or not mature for the item considered = 3, manufacturer not recognised (for example never audited) or small series production = 2, Previous disqualification or problem with feedback from operations = 1.

Table 9.2: Fides for JUNO.

Factor	Value	Definition
n_{annual}	2	Number of annual shutdowns of the JUNO detector.
t_{annual}	10 h	Total duration of the shutdowns per year.
Δt	20 °C	Temperature difference of electronics between on and off-state. First tests of potted dummy electronics showed differences of around 20 °C.
π_{sal}	1	Saline pollution level, Low = 1, High = 2.
π_{prod}	1	Protection level during production, hermetic = 0, non hermetic = 1
π_{zone}	1	Application pollution level, Low = 1, Moderate = 2, high = 4.
π_{envir}	1	Environmental pollution level, Low = 1, Moderate = 1.5, high = 2.
G_{RMS}	0	Stress associated with each random vibration phase.
RH	10 %	Humidity during operation. After potting the electronics in oil the humidity should be 10 % at most.
Π_{process}	4	Process factor for the JUNO experiment.
$\Pi_{\text{application}}$	1.8	The calculation of the application factor for the Power Board can be found in the appendix.
$\Pi_{\text{ruggedising}}$	1.7	The ruggedising factor describes the effort to make a device sturdy. For the Power Board the default value is used.
$QA_{\text{manufacturer}}$	1	The quality assurance level of the tested manufacturer (Electronics Service Willms) is level 1 (ISO 9000 version 2000 certified).
$QA_{\text{component}}$	2	Component quality assurance level relative to the state of the art, Higher = 9, Equivalent = 2, Lower = 1, Very much lower = 0.
E_{risk}	3	Risk related to this manufacturer, recognised manufacturer: Mature process for the item considered = 4, recognised manufacturer: Process not analyzed or not mature for the item considered = 3, manufacturer not recognised (for example never audited) or small series production = 2, Previous disqualification or problem with feedback from operations = 1.

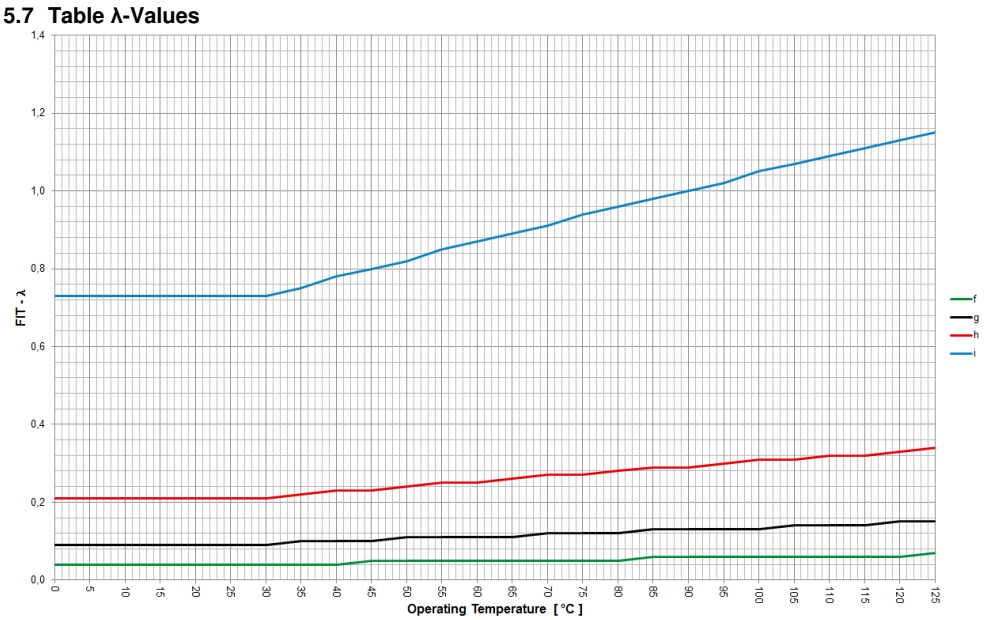


Figure 9.1: The line graphs show the temperature dependence of the FIT value of WE ceramic capacitors. The color indicates the applied voltage relative to the absolute voltage, where f $= 30\,\%$, g $= 50\,\%$, h $= 70\,\%$ and i $= 100\,\%$ [42].

B. DC/DC Converter Stability

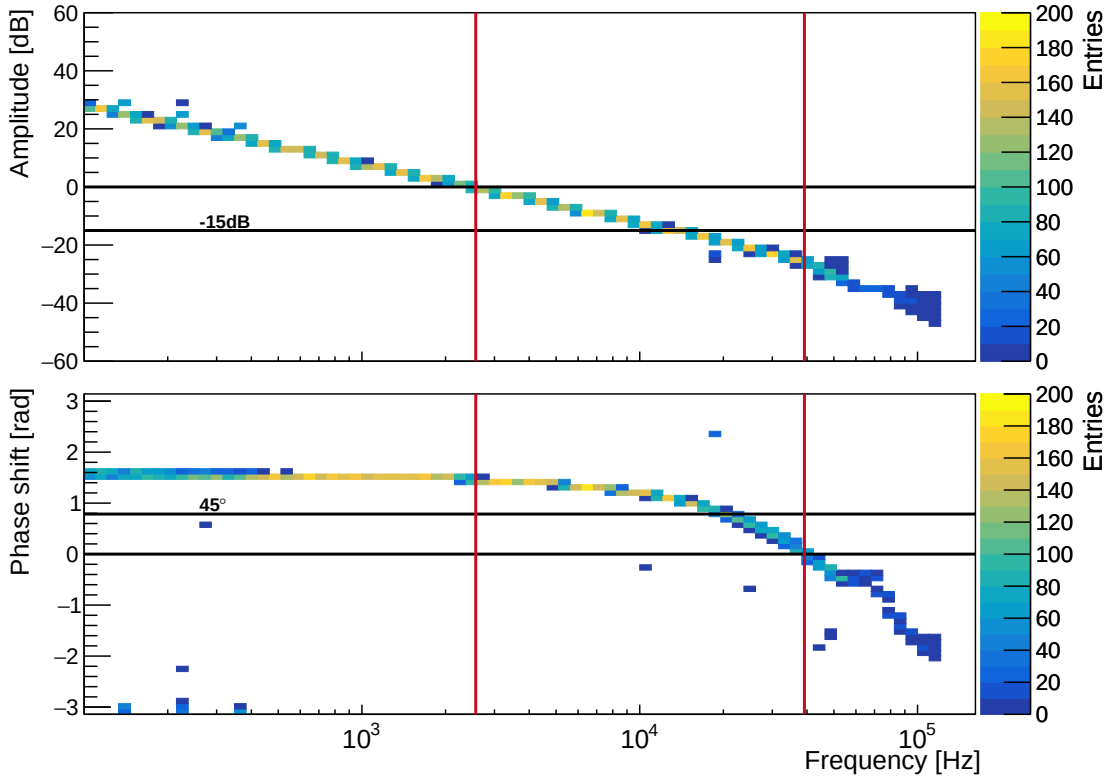


Figure 9.2: Gain/Phase measurement for the internal DC/DC converter for a load current of 600 mA.

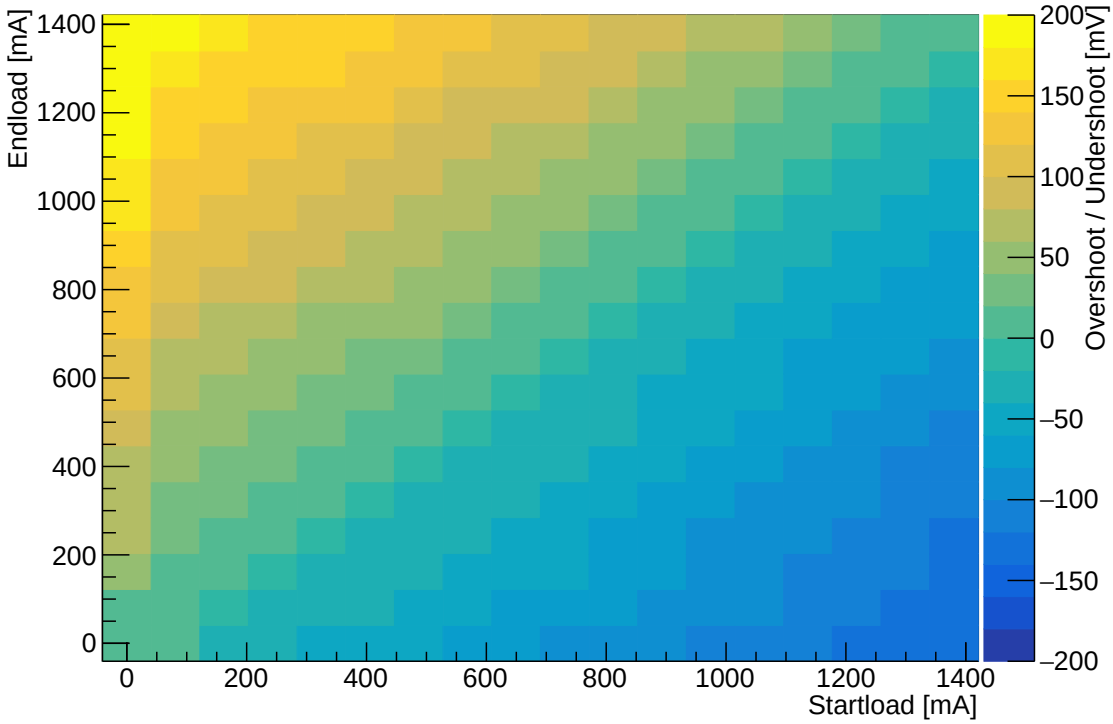


Figure 9.3: Amplitude of the over- and undershoots for load steps using the internal voltage supply.

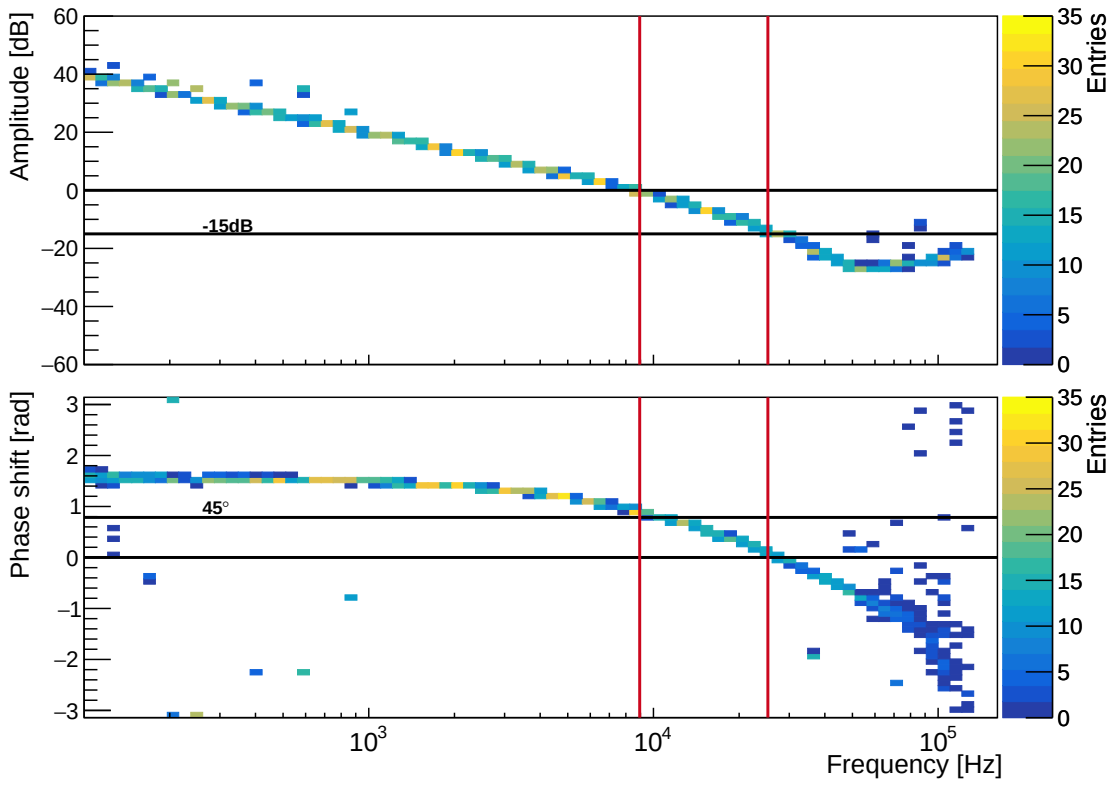
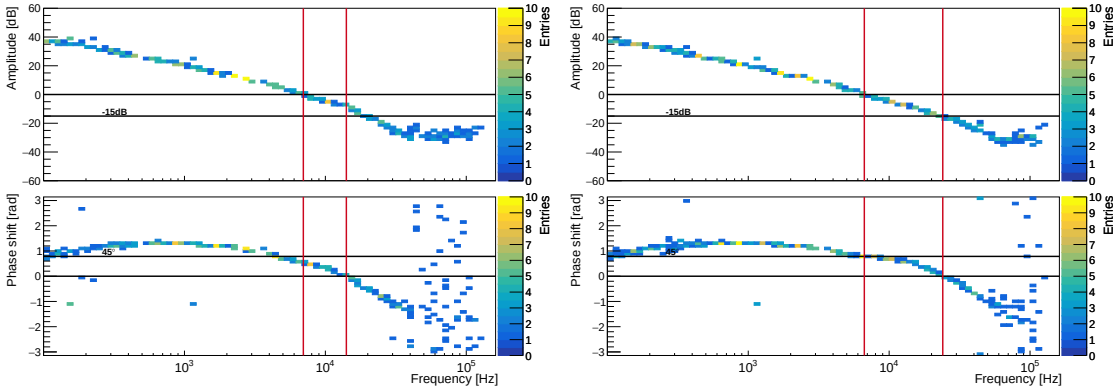
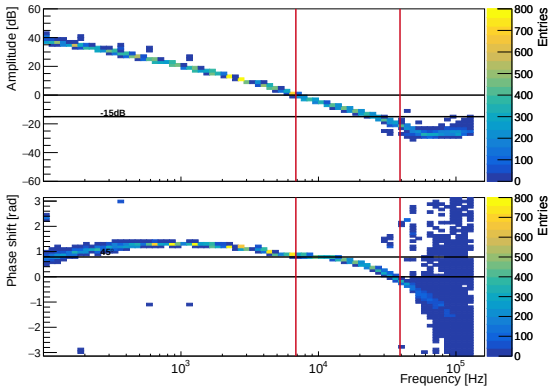


Figure 9.4: Gain/Phase measurement for the 1.8 V DC/DC converter for a load current of 180 mA.

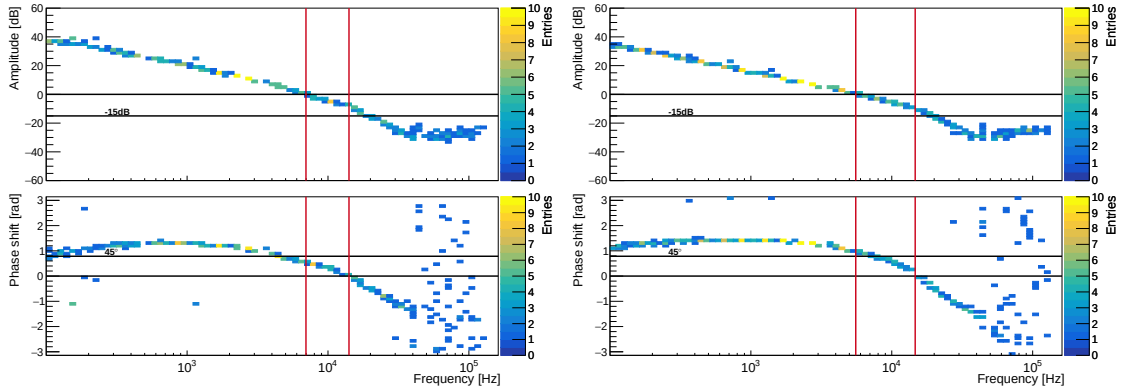


(a) $L = 150\,\mu\mathrm{H}$ (b) $L = 47\,\mu\mathrm{H}$

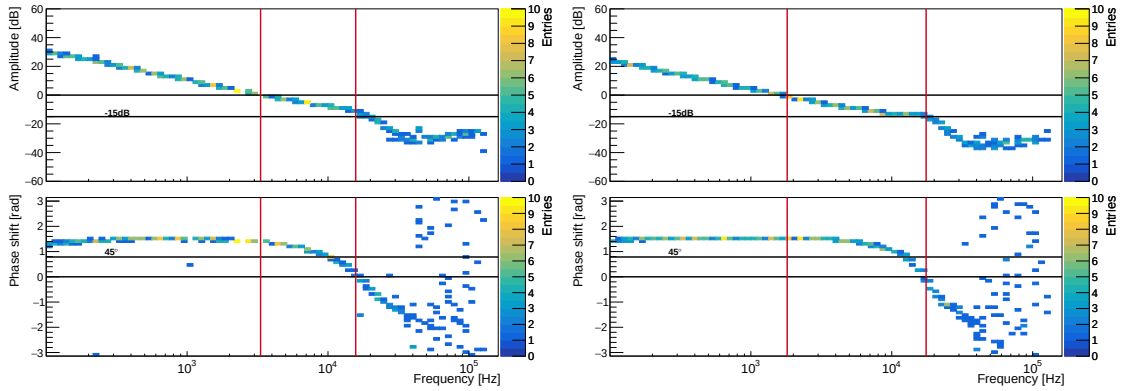


(c) $L = 22\,\mu\mathrm{H}$

Figure 9.5: Gain/Phase measurement of the A3V3 converter with different inductivities and a feedback capacity of $15\,\mathrm{pF}$. The output current is $330\,\mathrm{mA}$ for all measurements.



(a) $C_{\mathrm{FB}} = 15\,\mathrm{pF}$ (b) $C_{\mathrm{FB}} = 27\,\mathrm{pF}$



(c) $C_{\mathrm{FB}} = 47\,\mathrm{pF}$ (d) $C_{\mathrm{FB}} = 100\,\mathrm{pF}$

Figure 9.6: Gain/Phase measurement of the A3V3 converter with different feedback capcities and an inductor of $150\,\mu\mathrm{H}$. The output current is $330\,\mathrm{mA}$ for all measurements.

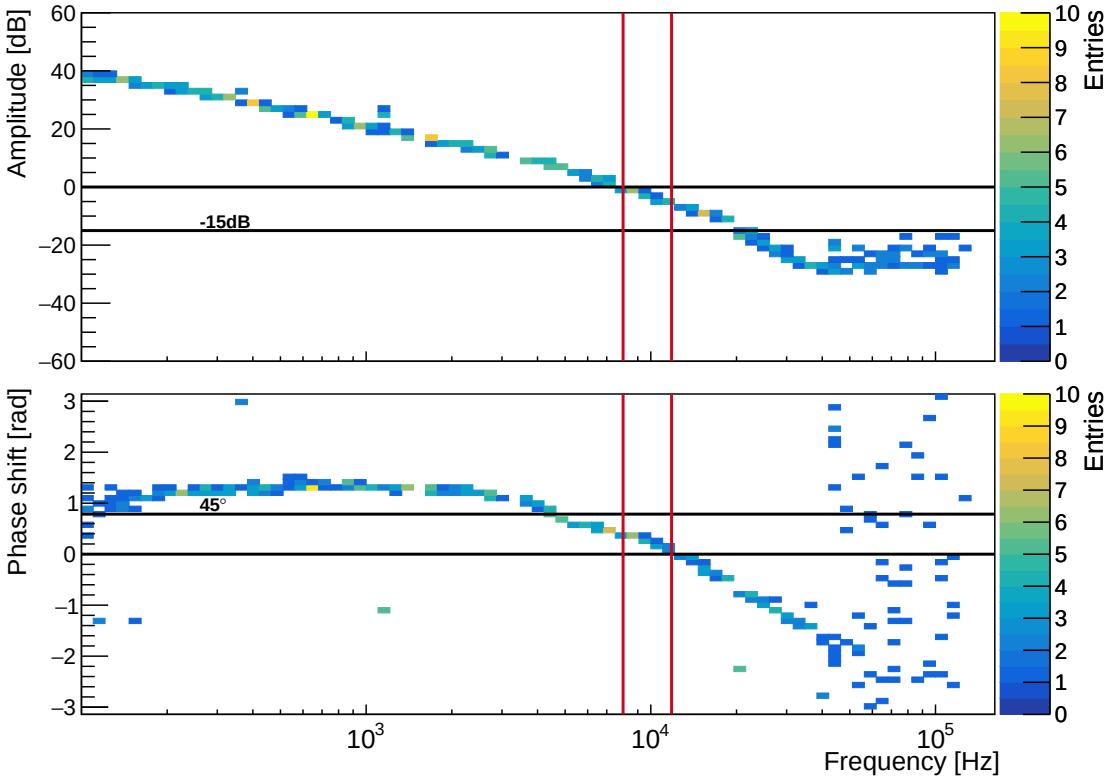


Figure 9.7: Gain/Phase measurement for the C3V3 converter for a load current of $330\,\mathrm{mA}$ before adjustment.

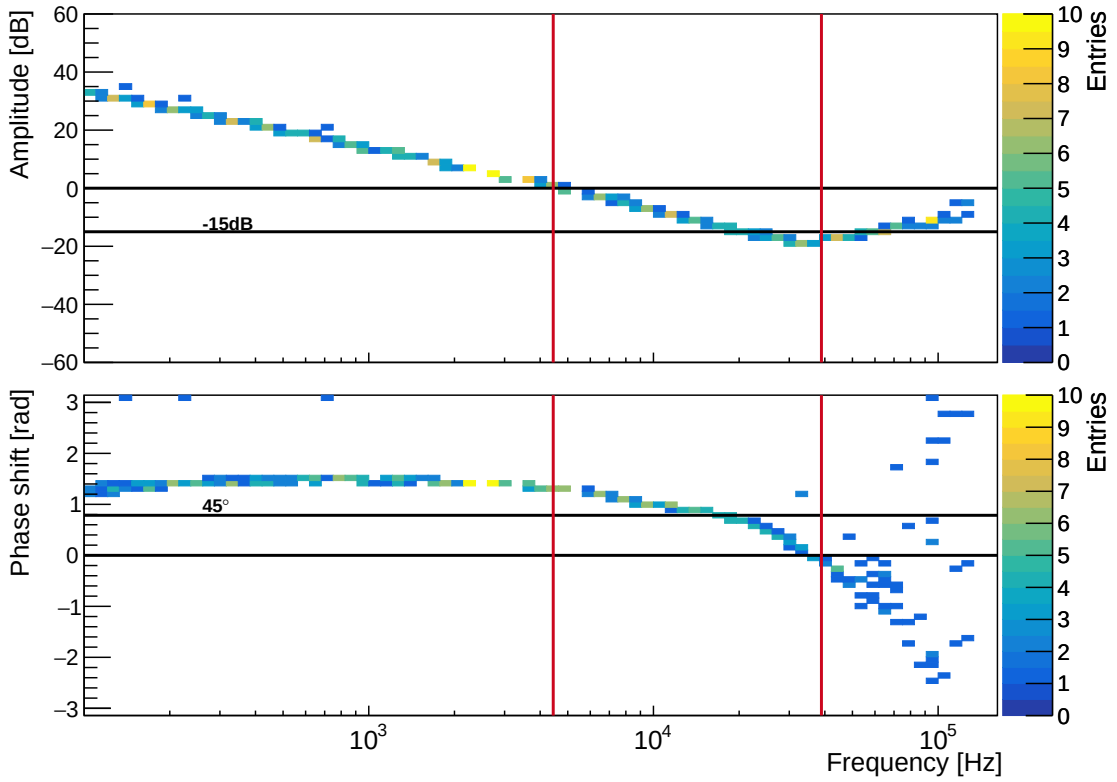
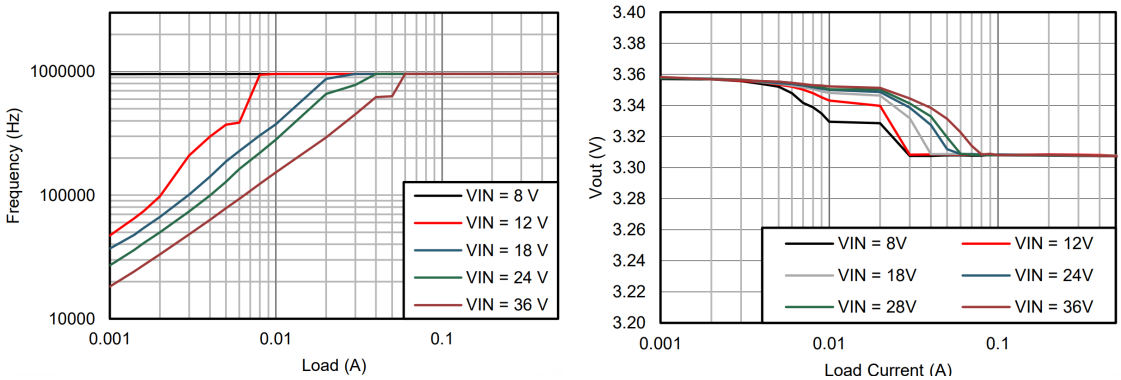


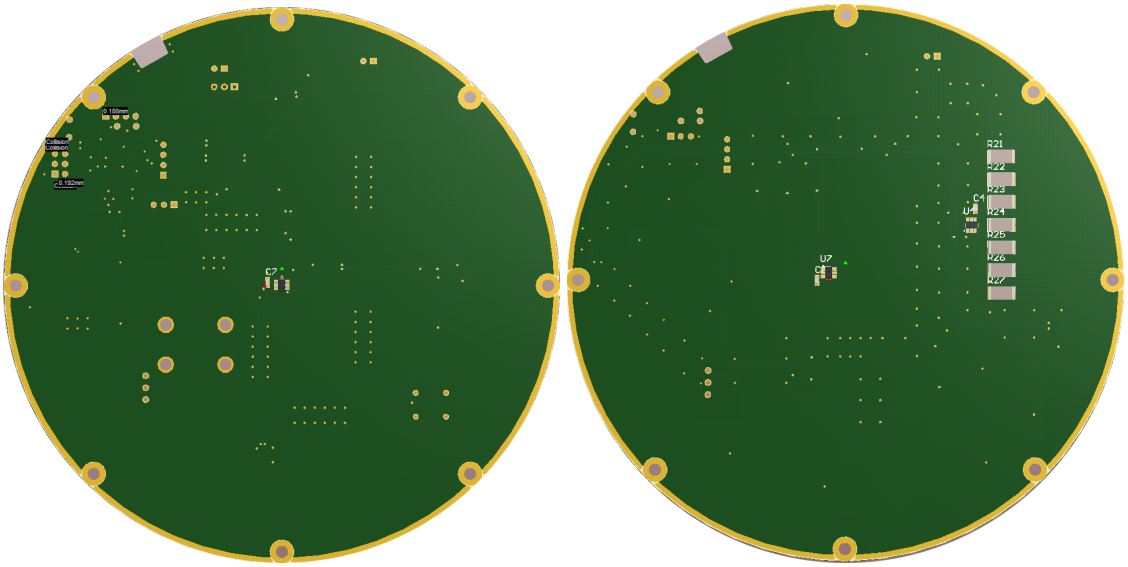
Figure 9.8: Gain/Phase measurement for the C3V3 converter for a load current of $330\,\mathrm{mA}$ after changing the inductor from $220\,\mu\mathrm{H}$ to $22\,\mu\mathrm{H}$ and the feedback capacitor from $15\,\mu\mathrm{F}$ to $27\,\mu\mathrm{F}$.



(a) $V_{\text{out}} = 5\,\text{V}, F_{\text{S}} = 1\,\text{MHz}$ (b) $V_{\text{out}} = 3.3\,\text{V}, F_{\text{S}} = 500\,\text{kHz}$

Figure 9.9: The plots show the frequency (a) and output voltage (b) at low output currents for the DC/DC converter LM46000 [54].

B. Dummy Electronics



(a) Power Board (b) General Control Unit

Figure 9.10: Bottom side of the dummy boards. The DC/DC converter on the GCU are placed on the bottom.

Bibliography

[1] COWAN, C. L. et al.: *Detection of the Free Neutrino: a Confirmation*. Science, 124(3212):103–104, 1956.

[2] DAVIS, RAYMOND et al.: *Search for Neutrinos from the Sun*. Phys. Rev. Lett., 20:1205–1209, May 1968.

[3] FUKUDA, Y. et al.: *Evidence for Oscillation of Atmospheric Neutrinos*. Phys. Rev. Lett., 81:1562–1567, Aug 1998.

[4] AHMAD, Q. et al.: *Direct Evidence for Neutrino Flavor Transformation from Neutral-Current Interactions in the Sudbury Neutrino Observatory*. Phys. Rev. Lett., 89:011301, Jun 2002.

[5] CRESPO-ANADÓN, J. I. et al.: *Double Chooz: Latest results*. Nucl. Part. Phys. Proc., 265-266:99–104, 2015.

[6] AN, FENG PENG et al.: *Measurement of electron antineutrino oscillation based on 1230 days of operation of the Daya Bay experiment*. Phys. Rev., D95(7):072006, 2017.

[7] AHN, J. K. et al.: *Observation of Reactor Electron Antineutrino Disappearance in the RENO Experiment*. Phys. Rev. Lett., 108:191802, 2012.

[8] BERINGER, J. et al.: *Review of Particle Physics*. Phys. Rev. D, 86:010001, 2012.

[9] SOIRON, MICHAEL: *The sensitivity of liquid scintillator detectors for the measurement of the neutrino mass hierarchy with atmospheric neutrinos*. PhD Thesis, RWTH Aachen University, 2017.

[10] XING, ZHI-ZHONG and YE-LING ZHOU: *Majorana CP-violating phases in neutrino-antineutrino oscillations and other lepton-number-violating processes*. Phys. Rev., D88:033002, 2013.

[11] QIAN, X. and P. VOGEL: *Neutrino Mass Hierarchy*. Prog. Part. Nucl. Phys., 83:1–30, 2015.

[12] AN, FENGPENG et al.: *Neutrino Physics with JUNO*. J. Phys., G43(3):030401, 2016.

[13] LI, YU-FENG et al.: *Unambiguous Determination of the Neutrino Mass Hierarchy Using Reactor Neutrinos*. Phys. Rev., D88:013008, 2013.

[14] GENSTER, CHRISTOPH: *Development and test of reconstruction methods for muon tracks in the JUNO liquid scintillator neutrino detector*. Master Thesis, RWTH Aachen University, 2015.

[15] SCHWARZ, MARIO et al.: *Measurements of the Lifetime of Orthopositronium in the LAB-Based Liquid Scintillator of JUNO*. 2018.

[16] AGAFONOVA, N. et al.: *Final Results of the OPERA Experiment on ν_τ Appearance in the CNGS Neutrino Beam*. Phys. Rev. Lett., 120(21):211801, 2018.

[17] QIAN, XIN and JEN-CHIEH PENG: *Physics with Reactor Neutrinos*. 2018.

[18] SÖRENSEN, ARND: *Temperature quenching in LAB based liquid scintillator and muon-induced backgrounds in the SNO+ experiment*. PhD Thesis, Technische Universität Dresden, 2016.

[19] ZHOU, XIANG et al.: *Rayleigh scattering of linear alkylbenzene in large liquid scintillator detectors*. Rev. Sci. Instrum., 86(7):073310, 2015.

[20] HAMAMATSU: *Photomultiplier Tubes - Basics and Applications*, 1 2007. THIRD EDITION.

[21] WANG, ZHIMIN and JUNO COLLABORATION: *JUNO PMT system and prototyping*. Journal of Physics: Conference Series, 888(1):012052, 2017.

[22] GAO, FENG et al.: *Status of the 20 inch MCP-PMT prototype development for JUNO experiment*. Journal of Physics: Conference Series, 888(1):012050, 2017.

[23] HE, MIAO: *Double Calorimetry System in JUNO*. In *International conference on Technology and Instrumentation in Particle Physics'17 (TIPP2017) Beijing, China, May 22-26, 2017*, 2017.

[24] ANFIMOV, N.: *Large photocathode 20-inch PMT testing methods for the JUNO experiment*. JINST, 12(06):C06017, 2017.

[25] ABE, K. et al.: *Hyper-Kamiokande Design Report*. 2018.

[26] MURALIDHARAN, P et al.: *An Automatic Baseline Regulation in a Highly Integrated Receiver Chip for JUNO*. J. Phys.: Conf. Ser. 888 012051, 888 012051, 2017.

[27] OLSHEVSKY, ALEXANDER. Private Communication, 2016.

[28] MEINEL, CHRISTOPH and HARALD SACK: *Internetworking: Technological Foundations and Applications*. Springer Science & Business Media, 2013.

[29] TEXAS INSTRUMENTS: *DS15EA101 0.15 to 1.5 Gbps Adaptive Cable Equalizer with LOS Detection*, 4 2013. Rev. 2.

[30] TEXAS INSTRUMENTS: *TMP10x Temperature Sensor With I2C and SMBus Interface with Alert Function in SOT-23 Package*, 9 2015.

[31] RELIASOFT CORPORATION: *Life Data Analysis Reference*, 5 2015.

[32] SIEMENS: *SN 29500*, 4 2015. Note 1.

[33] MARIN, J.J. and R.W. POLLARD: *Experience report on the FIDES reliability prediction method*. Reliability and Maintainability Symposium, 2005. Proceedings. Annual, 2005.

[34] FIDES GROUP: *Reliability Methodology for Electronic Systems*, 9 2009. Edition A.

[35] DEPARTMENT OF DEFENCE: *Military Handbook - Reliability Prediction of Electronic Equipment*, 12 1992. Notice 2.

[36] KECECIOGLU, DIMITRI B.: *Reliability Engineering Handbook*. DEStech Publications, 2002.

[37] TEXAS INSTRUMENTS: *Calculating FIT for a Mission Profile*, 3 2015. Rev. 1.

[38] INTERSIL: *Calculation of Semiconductor Failure Rates*, 2000. William J. Vigrass.

[39] UNITED STATES ARMY, DEVELOPMENT AND ENGINEERING CENTER: *Environmental Stress Screening Guide*, 1 1989. A206350.

[40] KINGSTON: *Kingston's Server Memory Dynamic Burn-In Testing: Setting a New Standard of Reliability*, 9 2004.

[41] WANG, LIANG et al.: *Random Vibration Testing Development for Engine Mounted Products Considering Customer Usage*. SAE International Journal of Materials and Manufacturing, 6:254–261, 04 2013.

[42] WÜRTH ELECTRONICS: *WE Standard: WES FIT - Reliability Data*, 9 2017.

[43] RELIABILTY ANALYSIS CENTER: *Failure Mode/Mechanism Distribution*, 9 1991.

[44] TEXAS INSTRUMENTS: *Switching Regulator Fundamentals*, 9 2016.

[45] TEXAS INSTRUMENTS: *LM46002 SIMPLE SWITCHER® 3.5 V to 60 V 2 A Synchronous Step-Down Voltage Converter*, 9 2014.

[46] AIMTEC: *Calculating Max Capacitive Load*, 7 2010. Rev. 0.

[47] ANALOG DEVICES: *Measuring Output Ripple and Switching Transients in Switching Regulators*, 1 2013. rev 0.

[48] RICHTEK: *Output Ripple Measurement Methods for DC-DC Converters*, 1 2016.

[49] OMICRON LAB: *DC/DC Converter Stability Measurement*, 1 2017.

[50] OMICRON LAB: *Loop Gain Measurement*, 1 2017.

[51] NASA STI: *DC/DC Converter Stability Testing Study*, 7 2008.

[52] RICHTEK: *DC/DC converter testing with Fast Load Transient*, 11 2015.

[53] VOLTCRAFT: *Digital-Multimeter M-3890DT*, 3 2005. Manual.

[54] TEXAS INSTRUMENTS: *LM46000 3.5-V to 60-V, 0.5-A Synchronous Step-Down Voltage Converter*, 3 2018.

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