SLAC-TN-68-14
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THE TWENTY-TWO AND A HALF DISPLAY CONSOLE

Introduction

Computer driven displays are found to be essential in the analysis of graphical data. At SLAC a great deal of use has been made of the IBM 2250 display, which forms part of the 360/75 configuration.

For example, the entire operation of all scanning devices* is remotely controlled from the console of the 2250. The setting of the scanning parameters, immediate display of the data taken off the film as well as the monitoring of the process in the various stages of analysis has proven invaluable in the engineering stages as well as for program development.

Unfortunately the use of the 2250 requires a great deal of interac tion with the operation of the large system. This is tenable if such interaction is sporadic and just for debugging purposes, but becomes objectionable if such system is used in a production mode of operation of the analysis system.

In any such system one has to contend with a small percentage of events which have not been acceptable to the computer programs for failure to meet certain predetermined criteria. A small percentage, however, may amount to large numbers and a practical way has to be found to handle those rejects.

It is the purpose of the described equipment to facilitate the reject handling and serve as a diagnostic tool for program development, with a minimum of interaction with the operation of the large system.

General Description

A twenty-one inch, rectangular cathode ray tube (CRT) has electromagnetic deflection and electrostatic beam focussing. A core storage, internal to the display, of 4096 words, 32 bits wide, refreshes the image on the face of the CRT. This memory is loaded and unloaded from the 360/75 when the display operator generates an attention interrupt.

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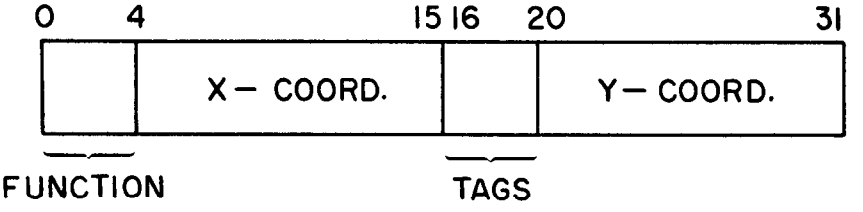
*SLAC-82.

The display is connected to the device selector, which in turn is connected to the IBM 2701 for the transfer of data from the 360/75. After the device has been selected with the very first word of a block of data, the integral display memory is loaded with data in sequential addresses, always starting at location zero. A transmission is terminated with the WC = 0 signal from the 2701 upon which an END OF RECORD is generated. Since loading and unloading of the memory always starts at location 0, this enables a partial update of the data starting with location 0.

Two modes of operation have been implemented at this time; point plotting and vector plotting. In the point plotting mode up to 4096 points may be randomly positioned on the face of the CRT.



The 32-bit word of internal storage is divided into a left and right half word for X- and Y-coordinates, respectively. The twelve rightmost bits of each half word are converted into analog voltages for deflection, and the four bits preceding these are used to indicate the mode of operation and for tagging purposes.

A one in position 0 prevents the data from being displayed. A one in position 16 means that that particular coordinate has been tagged by the lightpen and should be brightened.

A one in position 17 disables the lightpen for that word. If a one is present in position 18, it will cause the data that has been tagged by the program or the lightpen in position 16 to blink at a rate of three times per second to draw the attention of the operator.

A 0 in bits, 1, 2 and 3 indicates the point plotting mode of operation in this mode the 32-bit word, read out of the internal core, is strobed into register one (R1) and jam transferred into register two (R2). Two registers are used to generate some overlap in the time needed for memory read out and the time necessary to deflect the electron beam. The memory is read into R1 while the data is displayed from R2 as well as reloaded into the memory. Although the

time the amplifiers need for maximum deflection is 30 μsec, a scheme has been devised to shorten this time for coordinates that are closer together than the maximum distance. This has been made possible, because of the availability of the two registers mentioned above, since R1 at a specific point in time contains the "future" coordinates of the beam while R2 holds the present location of the spot. The time for deflection has been made almost linear with the distance travelled. By examining the two most significant bits of X and Y in both R1 and R2, the total CRT screen is divided into sixteen virtual rectangles. The time necessary to move the electron beam is derived from the data to be 8 μsec to move within one box, 16 μsecs to go to an adjacent box, 24 μsecs to jump one box and 32 μsecs to jump two. The net result of this "collate" system is that the average time per point displayed is significantly reduced.

The computer display program may, by arranging the data for a minimum number of border crossings, assist in this optimization process.

A 0 in bits 1 and 2, and a 1 in bit 3 indicates the vector mode of operation. The X- and Y-coordinates now indicate the starting and end point of a solid line drawn between those points. At all times are the absolute positions of the end points specified, thus avoiding the accumulation of positioning errors. For reasons of hardware simplicity the largest line drawn may cover 1/4 of the screen. Longer lengths are to be built up by chaining of short vectors. The drawing time per 1/4 screen, or smaller vector, is 10 μs. The same tagging scheme used in the point plotting mode also pertains to the vector drawing mode of operation. Two means of input have been provided.

The lightpen on this particular display has been designed to flag data, rather than to generate an interrupt upon detecting light on the CRT face. The data that is seen by the lightpen is immediately brightened, providing guidance to the operator. Conversely, data that has been marked may be erased to eliminate overshoots in the filtering process. The brush action of this lightpen is extremely valuable to facilitate the manual filtering process in which the tracks of interest are to be separated from crossing tracks or other data, interfering with the automatic filtering program.

Whereas the lightpen may interact with data that is being displayed, a trackball is used to insert data into the system. Two potentiometers are driven from a ball which in turn is moved in any direction by the display operator. The analog output voltage of these potentiometers is continually converted into digital coordinates and written in location 0 of the internal core storage. The location is

easily read by the program after the data has been unloaded. The trackball coordinates are displayed as a brightened, flickering point on the screen. Command 3 in bits 1, 2 and 3 of location 0 activates the trackball.

TECHNICAL DESCRIPTION OF THE 22 1/2 DISPLAY CONSOLE

The 22 1/2 Display Console is a point plotting device. It has an internal memory, a C.R.T. for a display screen, is on line to an IBM 360 computer through the Device Selector, and an IBM 2701 Parallel Data Adapter. The Device Selector is used to connect a maximum of seven devices to the IBM 2701 via one common interface.

The memory is a Ferroxcube FX-14 coincident-current ferrite core memory with a capacity of 4,096 words in a bit length of 32 bits per word. The minimum full cycle time (read/restore, clear/write) is 8 microseconds. Access time is 3 microseconds. There is a split/cycle mode in which a read cycle is followed by a write cycle, the data may be changed between the read and write cycles. The split/cycle also takes 8 microseconds.

The 22 1/2 is controlled by logic made from Digital Equipment Corporations's modules of the R, W, and A Series, also some special circuits.

Logic of the 22 1/2

The logic of the 22 1/2 consists of two 32 bit registers, Digital to Analog Converters for C.R.T. deflection, an address register, unblank circuits, light pen circuits, level converters, various control circuits, a test pattern generator, a vector generator, and a trackball.

Data Flow (See Figure 1)

The two 32 bit registers are labeled Register 1 and Register 2. Data from the memory are received by Register 1 and then jam transferred to Register 2. Digital to Analog Converters are connected to Bits 4-15 and 20-31 of Register 2. (See Figure 1). Data in Register 2 are sent back to the memory in the display cycle. Data are also sent to the memory from Register 2 on the load cycle. On the unload cycle data are sent to Register 1 from the memory then jam transferred to Register 2, and then to the Device Selector. Since the Device Selector only has 16 data lines, the data are sent on a left-right basis. The Device Selector also

sends data on 16 lines. Consequently, data are also received from the Device Selector on a left-right basis.

Bits 0-3 are control bits. Bit 0 is the plot bit, if set true the point is not plotted. Bits 1-3 are decoded into 8 codes. At this time, code 1 is the vector code, code 2 is the character code, code 3 is the trackball code, code 7 is the skip to 4095 code. Codes 0, 4, 5 and 6 are not used. Bits 16-19 are tag bits. Bit 17 is the disable light pen bit, when Bit 17 is set true Bit 16 cannot be controlled from the 22 1/2 Console. Bit 18 is the flashing bit, when set true any word hit by the light pen will flash.

Data Registers

The data registers are divided in half. The first 4 bits of the left half are used for control bits. The first 4 bits of the right half are tag bits. The last 12 bits of the left half contain the X coordinate. The last 12 bits of the right half contain the Y coordinate. Bits 1 to 3 are decoded by a Binary to Octal Decoder. The codes are used for various functions: code 1 is the vector code, code 2 is the character code, code 3 is the trackball enable code, code 7 is the skip code.

Load Cycle (See Figures 2 and 3)

Data are received from the Device Selector on a left-right basis by inverters (DEC-R107). Since Bits 16-19 must be written into the memory in the word following the one they are associated with, they are stored in flip flops for a delay of 1 write cycle.

The W.G. and the Select lines are received by a nand gate (DEC-R111). The first output of the gate is used to enable the Load flip flop (DEC-R202) to be set on the 4095 pulse. The 0 output of the Load flip flop is sent to a pulse amplifier (DEC-R602) to generate a Start Load pulse. The 1 output of the Load flip flop is used to enable the Write Advance Address, the D.D. pulse amplifier, the CLR-R2 pulse amplifier, the W.G. pulse amplifier, and to stop the internal clock. The pulse generated by the Start Load pulse amplifier is used to set the Load Left-Right flip flop (DEC-R202) to the left position, to initially clear R2 and generate the first W.G. pulse. The Load Left-Right flip flop is toggled by the W.G. Pulse, however, the start Load pulse overrides the first W.G. pulse forcing the Load Left-Right flip flop into the left position for the first W.G. pulse. Five-hundred nanoseconds after the first W.G. pulse the address register is advanced to address 0000. The Set R2 Left pulse strobes the data into the left-half of Register 2, and a D.D. is given. On the second W.G. pulse the Load

Left-Right flip flop is toggled to the right position. Five-hundred nanoseconds after the second W.G. pulse, the SET R2 Right pulse strobes the data into the right-half of Register 2. The Lock-Up is started by the SET R2 Right pulse, which prevents another W.G. from coming for 8 microseconds. The D.D. is given on the SET R2 Right pulse and the word is written into the memory on the Clear Write pulse. After the last word the load flip flop is reset by the Reset pulse which is generated by the WORD COUNT = ZERO gated with the Select line. The Reset pulse also generates the END OF RECORD pulse to the computer.

Unload Cycle (See Figure 4 and 5)

Data are sent to the Device Selector on a left-right basis. The data are divided into a left-half and a right-half by the Data Out bus (DEC-R123), the bus is enabled by an enable left or by an enable right. The outputs of the data bus are connected to line drivers (DEC-R650) which send the data to the Device Selector.

The R.G. and the Select lines are received by a nand gate (DEC-R111), the first output of the gate is used to enable the Unload flip flop (DEC-R202) to be set on the 4095 pulse. The 0 output of the Unload flip flop is used to generate a Start Unload pulse. The 1 output is used to enable the R.G. pulse amplifier, to advance the Address Register to Adress 0000, to set the Unload Left-Right flip flop to the left position, to start the first Read/Restore cycle, and to stop the internal clock. The left Data Out bus is enabled at this time. Register 1 is then cleared with a CLR R1 pulse. After 4 microseconds the data from the memory is strobed into Register 1 with the SET R1 pulse. Two microseconds after the SET R1 pulse, the data are jammed into Register 2 on the JAM R1 to R2 pulse. Seven microseconds after the Start Unload pulse a D.D. is given and the address is advanced. On the second R.G. from the Device Selector, a R.G. pulse is generated which toggles the Unload Left-Right flip flop to the right position and the right Data Out bus is enabled. Register 1 is then cleared and a Read/Restore cycle is started. After 4 microseconds the data are strobed into Register 1. Since the data to be sent at this time is the right-half, and Bits 16-19 are in the word following the one they are associated with, a D.D. is given 1 microsecond after the SET R1 pulse (Bits 16-19 go to the Data Out bus from Register 1). One microsecond after the D.D. the data are jammed into Register 2. On the third R.G. pulse the Unload Left-Right flip flop is toggled into the left position, the address is advanced, and after 500 nanoseconds a D.D. is given. The sequence

is the same for the fourth R.G. as for the second, the same for the fifth as for the third, etc. The unload flip flop is reset by the W.C. = 0 Reset Pulse.

Display Cycle (See Figures 6 and 7)

On the display cycle, data from the memory is received by level converters (DEC-W510) inverted (DEC-R107) and strobed into Register 1 (DEC-R205 and R203) with a SET R1 pulse. Register 1 must first be cleared with a CLR R1 pulse. The data then sits in Register 1 for a 2 microsecond period. During this time Register 1 and Register 2 are compared for collate. Also, at this time if the word in Register 2 is to be marked or unmarked by the light pen, Bit 16 in Register 1 is set or reset. Thus, the light pen writes into the word following the one it has hit. After the 2 microsecond period, the data in Register 1 are then jam transferred into Register 2 (DEC-R205) on the JAM R1 to R2 pulse. The output of Register 2 is sent to level converters (DEC-W601) which are connected to the data input lines of the memory. The output of Bits 4-15 of Register 2 also go to the Digital to Analog Converter (DEC-A601) used for X deflection. The output of Bits 20-31 of Register 2 go to the Digital to Analog Converter used for Y deflection.

The display cycle is controlled by an internal clock (DEC-R401) which generates 100 nanosecond pulses at a 1 microsecond interval. The output of the clock is sent to three flip flops (DEC-R202) which are connected as a counter; the output of the counter is connected to a binary to octal decoder (DEC-R151). The decoder has eight outputs labeled 0-7. Each output generates a 1 microsecond pulse at an 8 microsecond rate. The pulse from output 1 of the octal decoder follows the pulse from output 0, the pulse from output 2 follows pulse 1, etc. The timing pulses are only used during the display or test pattern generator cycles.

There are two unblank signals, the normal unblank and the marked unblank. The unblank circuits are enabled only during the display cycle. Pulse #4 is used to trigger a 400 nanosecond pulse amplifier (DEC-W640). The output is used to generate both the normal unblank and the marked unblank. If Bit 0 is set true it will disable both unblank circuits. Bit 16, which is set or reset by the light pen circuit, must be set true in the word in Register 1 for the word in Register 2 to receive a marked unblank signal. If Bit 18 in Register 1 is set true it will enable the flashing circuit, which will cause the marked unblank to

flash. The flashing circuit is started by the 4095 pulse which triggers a one shot (DEC-R302) which in turn triggers a second one shot. The first one shot cannot be triggered by the 4095 pulse unless both one shots are in their stable position. The output of the second one shot is gated with the trackball and sent to the marked unblank circuit. The output of the second one shot also toggles a flip flop which toggles a second flip flop. The output of the second flip flop is used for the normal flashing rate. It is gated with Bit 18. The result is that the trackball point flashes 4 times as fast as a normal point that has Bit 18 and Bit 16 set true.

Collate (See Figure 8)

Due to the fact that the deflection amplifiers take longer for full screen deflection than for smaller deflections, points that are closer together can be plotted faster than those that are farther apart. To do this, Bits 4 and 5 (the two most significant bits in the X) and Bits 20 and 21 (the two most significant bits in the Y) in Register 2 are compared with the same bits in Register 1 by an Exclusive Or circuit (DEC-R131). Since the memory cycle is 8 microseconds, there is no need to collate for a deflection smaller than a fourth screen deflection. For a deflection larger than a fourth screen but smaller than 1/2 the internal clock is stopped for 10 microseconds,for a larger than a half but smaller than a 3/4th deflection the clock is stopped for 20 microseconds, and for 30 microseconds for a larger than 3/4th screen deflection.

If the most significant bits of the X and the Y are the same in Register 1 as in Register 2 but the second most significant bits are not, the clock will be stopped for 10 microseconds. If the most significant bits in either the X or the Y are not the same but the second most significant bits are, then the clock is stopped for 20 microseconds. If both the most significant and the second most significant bits are not the same, the clock is stopped for 30 microseconds. To do this, the output of the Exclusive Or circuits are coded by nand gates (DEC-R111) and strobed into three flip flops (DEC-R203) with pulse #4. On pulse #7, the flop flop that is set, if any, will start 1 of 3 one shots (DEC-R302) for 10, 20, or 30 microseconds. The outputs of the one shots are ored together and used to stop the clock.

Light Pen

The light pen is connected to a photomultiplier by fiber-optics. The signal from the photomultiplier is then filtered and sent to a comparator (DEC-W520). The comparator is used to set a threshold and as a level converter for the photomultiplier signal. The output of the comparator is gated with pulses 3 and 4, Bit 17, and the Light Pen switch. This makes the Light Pen pulse. The Mark/Erase

switch toggles the Mark/Erase flip flop. The outputs of the Mark/Erase flip flop is used to enable the set or reset gates of the Register 1 Bit 16 flip flop, which are strobed with the Light Pen pulse. When the Mark/Erase flip flop is in the mark position and the Register 1-Bit 16 flip flop is strobed with the Light Pen pulse, the Register 1-Bit 16 flip flop will be set true. If the Mark/Erase flip flop is in the mark position and the Register 1-Bit 16 flip flop is strobed with the Light Pen pulse, the Register 1-Bit 16 flip flop will be set true. If the Mark/Erase flip flop is in the erase position, the Register 1-Bit 16 flip flop is set false. When the Erase-All switch is operated it will set the Mark/Erase flip flop to the erase position and strobe the Register 1-Bit 16 flip flop, if Bit 17 is not set true.

Sixty Cycle Sync

Due to 60 cycle distortion, the display cycle is in Sync with the 60 cycle line. This is done with a 6.3 V.A.C. filament transformer connected to a comparator (DEC-A502). The output of the comparator is sent to a pulse amplifier which resets the Sync flip flop. The Sync flip flop is set by the 4095 pulse. The output of the Sync flip flop is used to stop the clock.

Address Register

The Address Register is made from 12 flip flops (DEC-R205) connected as a counter, with provision to be cleared to address 0000 or set to address 4095. The outputs of the Address Register go to level converters and then to the address input of the memory. In order to know when the Address Register is in the last address (4095) the output of the flip flops are gated. The output of the 4095 gate is used to start the Load and Unload cycles, to stop the Test Pattern Generator cycle, to set the Sync flip flop, and to trigger the flashing bit one shot.

Test Pattern Generator

The Test Pattern Generator is used to internally load the memory with a test pattern of 4096 points in a 64 × 64 matrix. The Generator loads the output of the Address Register into the 6 most significant bits of the X and the 6 most significant bits of the Y. The Test Pattern Generator cycle is started by the Off Line Load Switch which clears the Test Pattern Generator flip flop. The Test Pattern Generator flip flop is used to stop the display cycle, to enable the Test Pattern Load Bus, and to enable R2 to be cleared and set. The Address Register is cleared on the first #7 pulse after the switch has been operated. Register 2 is cleared on pulse #7 and set on pulse #0. The input of the Test Pattern Load

Bus (DEC-R123) is connected to the output of the Address Register, the output of the Load Bus is connected to the data input lines of Register 2 Bits 4-9 and 20-25.

Trackball (See Figure 9)

The trackball is a 4 inch ball mounted on the display console table. The ball drives two potentiometers, one for Y and one for X. The ball can move in any direction. Depending on the direction the ball is moved, one potentiometer may move more or less than the other, making it possible to move at any angle.

The analog voltage from the potentiometer is converted to a digital number by means of a counter converter.

Two 9 bit counters (one for X and one for Y) are connected to two Digital to Analog Converters (DEC-A604 & A601), the output of the Digital to Analog Converters are compared with the Analog voltage of the potentiometer. When the Digital to Analog voltage of the counter is higher than the Analog voltage of the potentiometer the counter is stopped. Thus, the counter has the digital number for the potentiometers.

If there is a code 3 in location 0000 the trackball will be enabled and the digital number in the trackball counter will be set in core storage location 0000. To do this when Address 0000 comes in the display cycle and there is a code 3 in that location, Register 1 will be cleared and the data from the counter will be set into Register 1. After the data is set in Register 1 the counter is cleared and it starts counting again. Thus, on each cycle the trackball is up-dated.

Vector Generator (See Figure 10 & 11)

To draw a vector two word locations are needed. The first word has the X and Y starting point of the vector, the second word has the final point of the vector.

To enable the vector generator, a code 1 is used in the function bits of the first word. If a code 1 is in the second word also, the second word will be the X and Y starting point of the second vector and the third word will be the final point of the second vector. Thus, vectors may be chained.

The vector starts on pulse #4 of the internal clock, at this time the first word is in Register 2 and the second word is in Register 1. Two Digital to Analog Converters are connected to Register 1 to give the Analog voltage of the final point of the vector, the starting point is in the Digital to Analog Converter connected to Register 2, normally used for point plotting.

When a vector is to be drawn, a one shot is triggered for 10 microseconds. The output of the one shot is used to stop the internal clock, to disable the normal unblank, and enable the vector unblank.

The starting X and Y are inverted and sent to the vector generator card. The final X and Y are sent to the vector generator card in their normal state. The output of the 10 microsecond one shot is also sent to the vector generator card.

The main component of the vector generator card is a Philbrick solid state amplifier model PP45. The amplifier is connected as an integrator.

The two analog voltages (the inverted start and the normal final point of the vector) are differentially added. The differential voltage is then integrated by the PP45. The feedback capacitor is discharged by a field-effect transistor after the vector has been drawn. (See Figure 11.)

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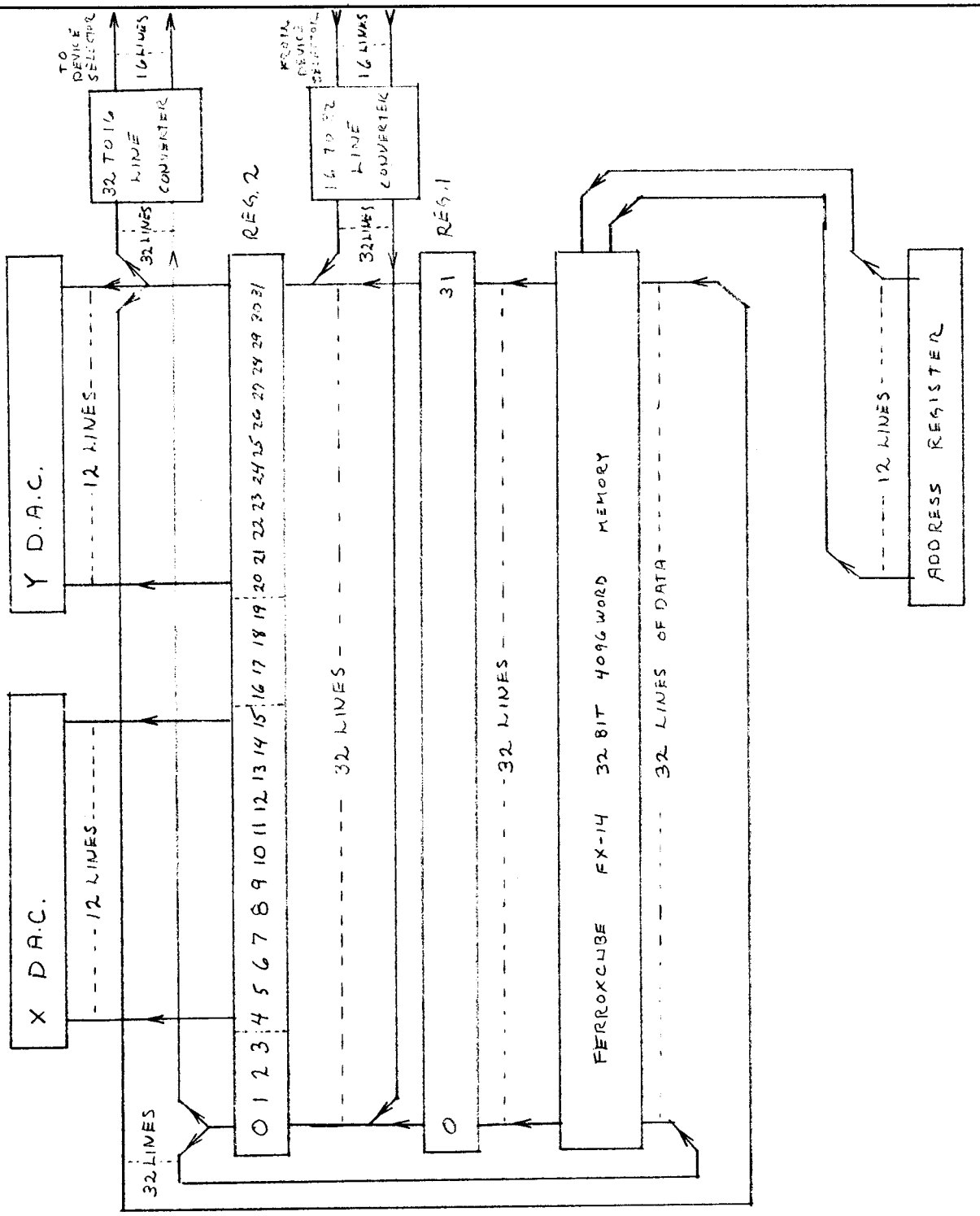
AUTHOR HAMILTON	DATE	PAGE OF	
PROJECT—JOB 22½ DISPLAY CONSOLE			
TITLE FIGURE 1--DATA FLOW			



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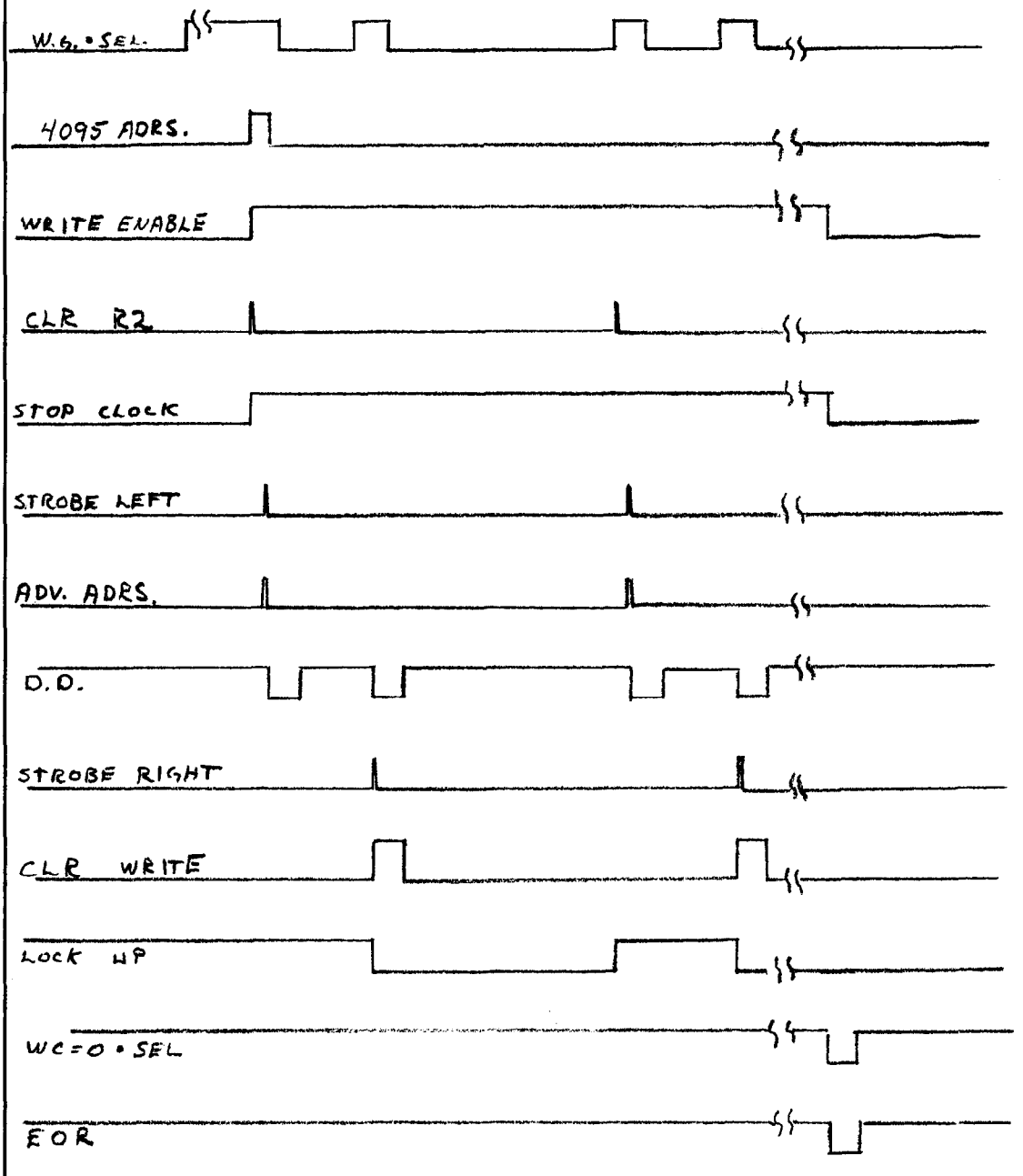
TITLE FIGURE 2 -- LOAD CYCLE



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TITLE FIGURE 3 -- LOAD CYCLE

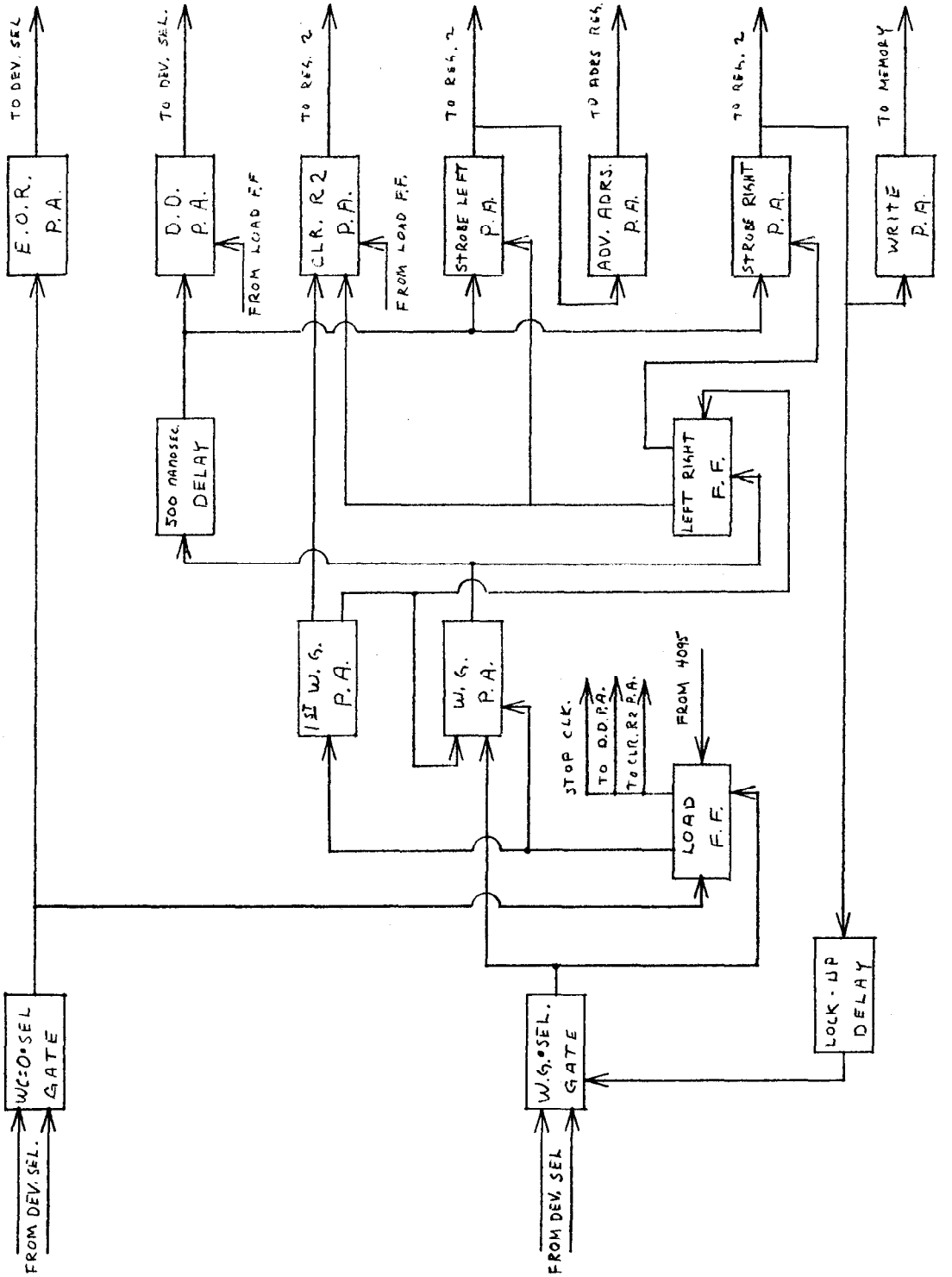

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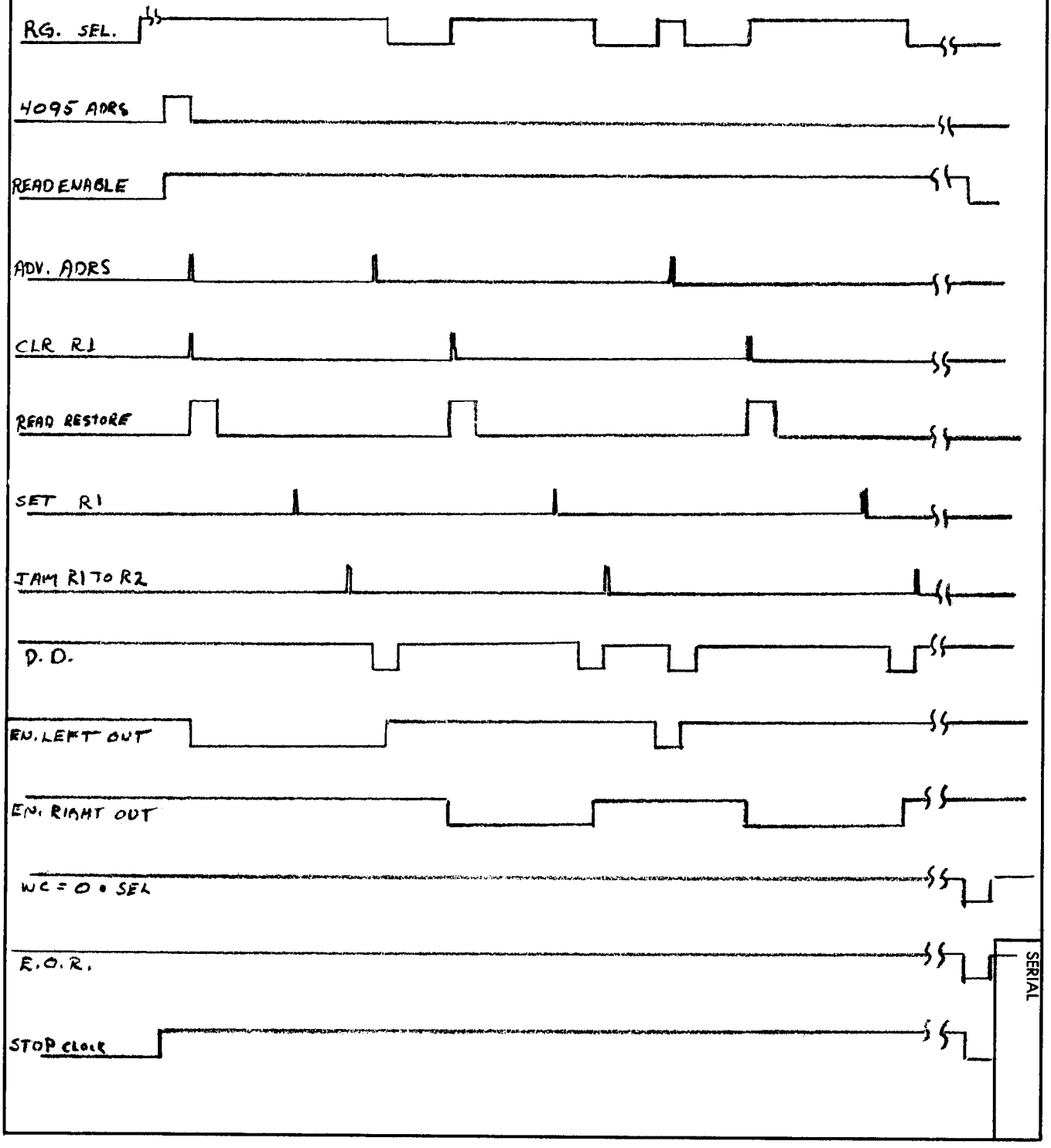
FIGURE 4 -- UNLOAD CYCLE



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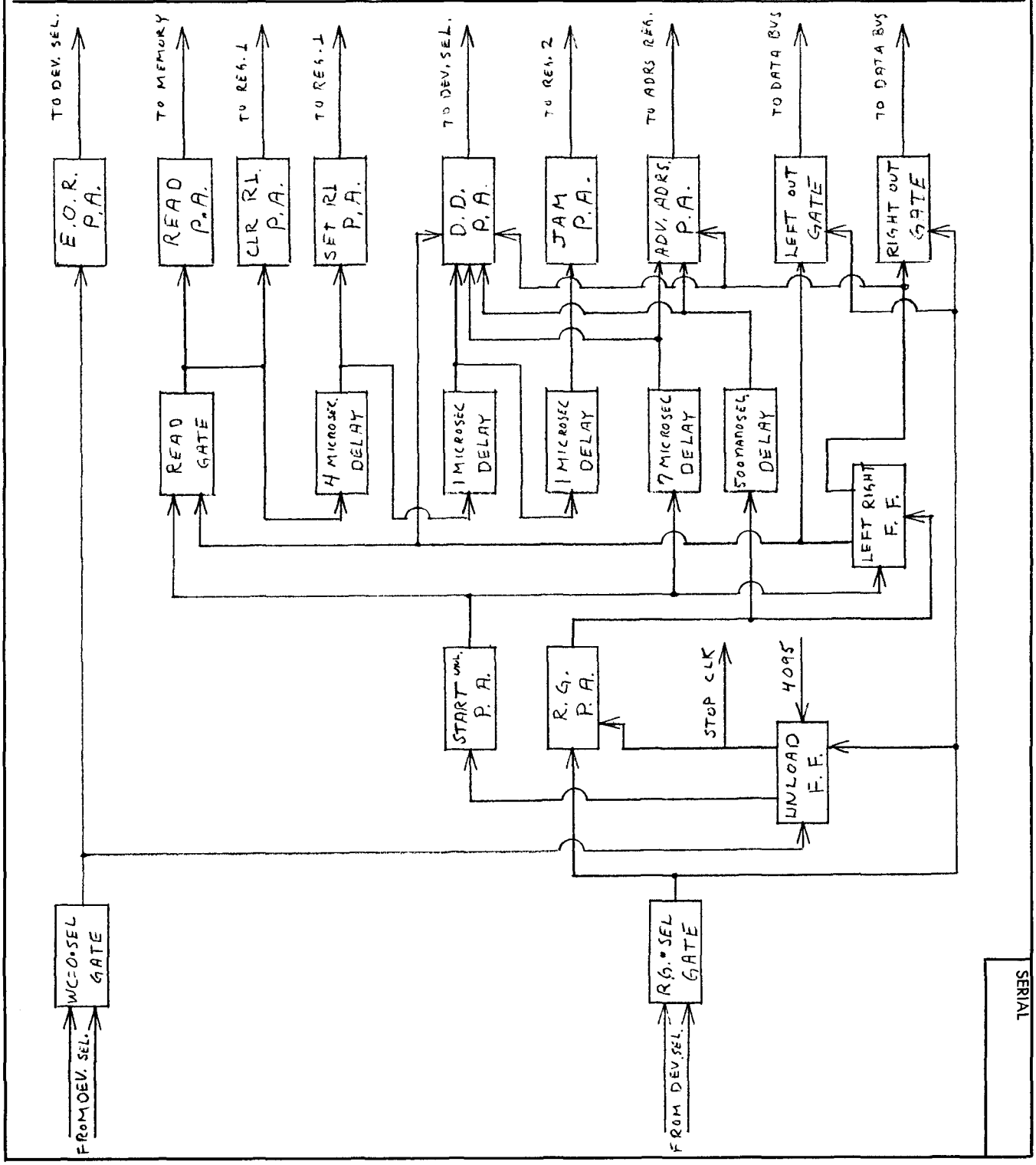
TITLE FIGURE 5 -- UNLOAD CYCLE			



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TITLE FIGURE 6 -- DISPLAY CYCLE			

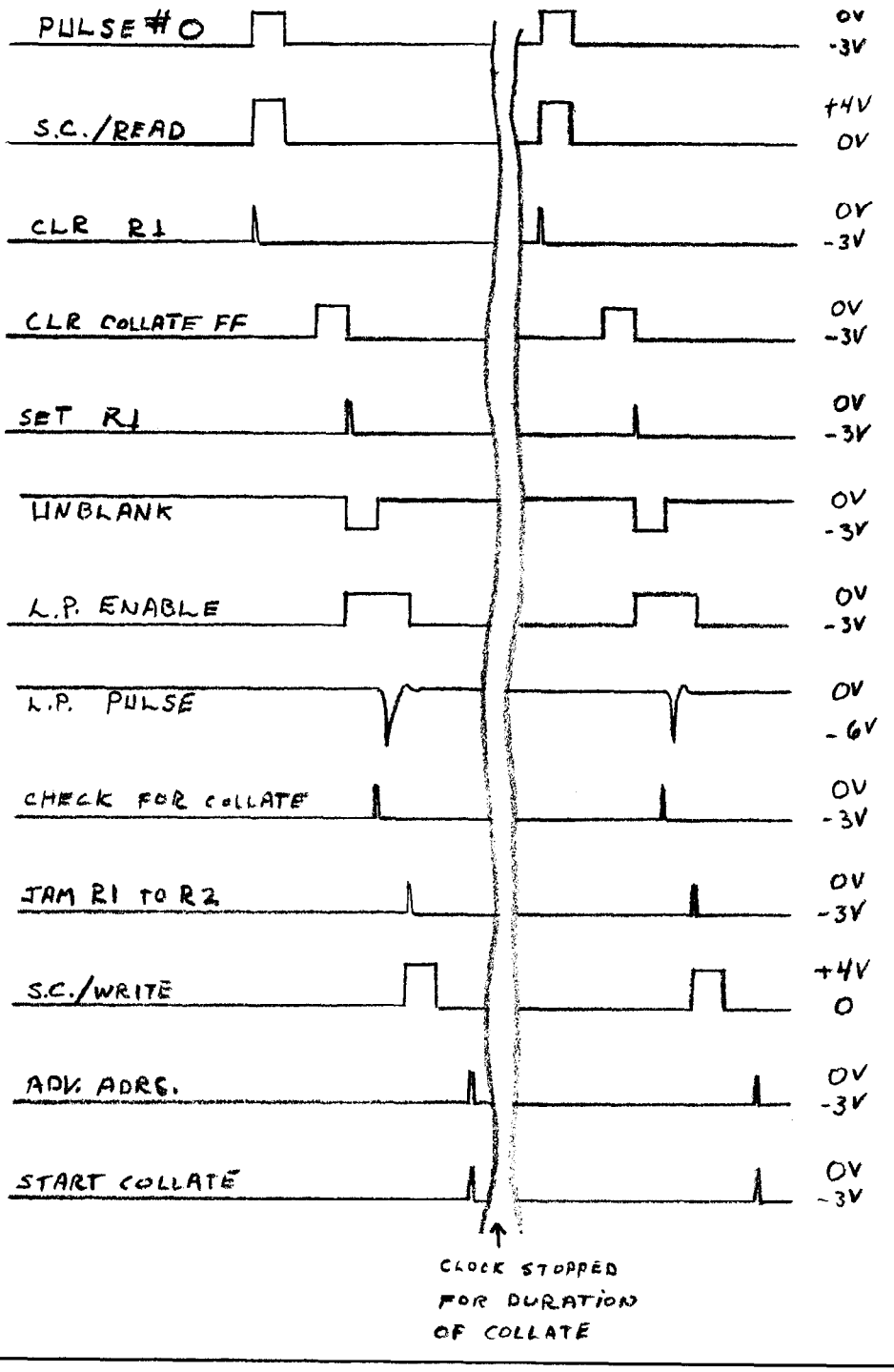

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FIGURE 7 -- DISPLAY CYCLE

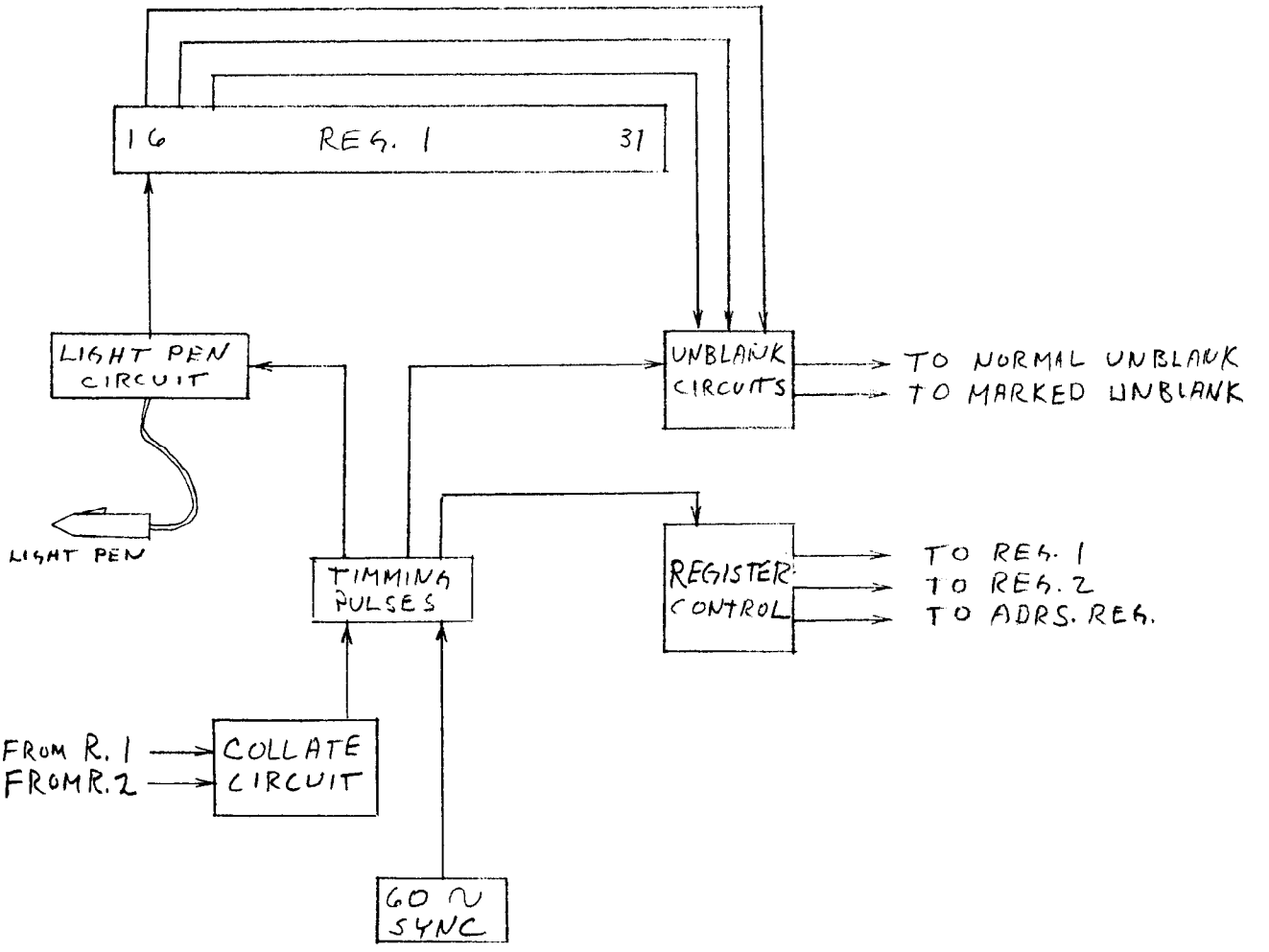

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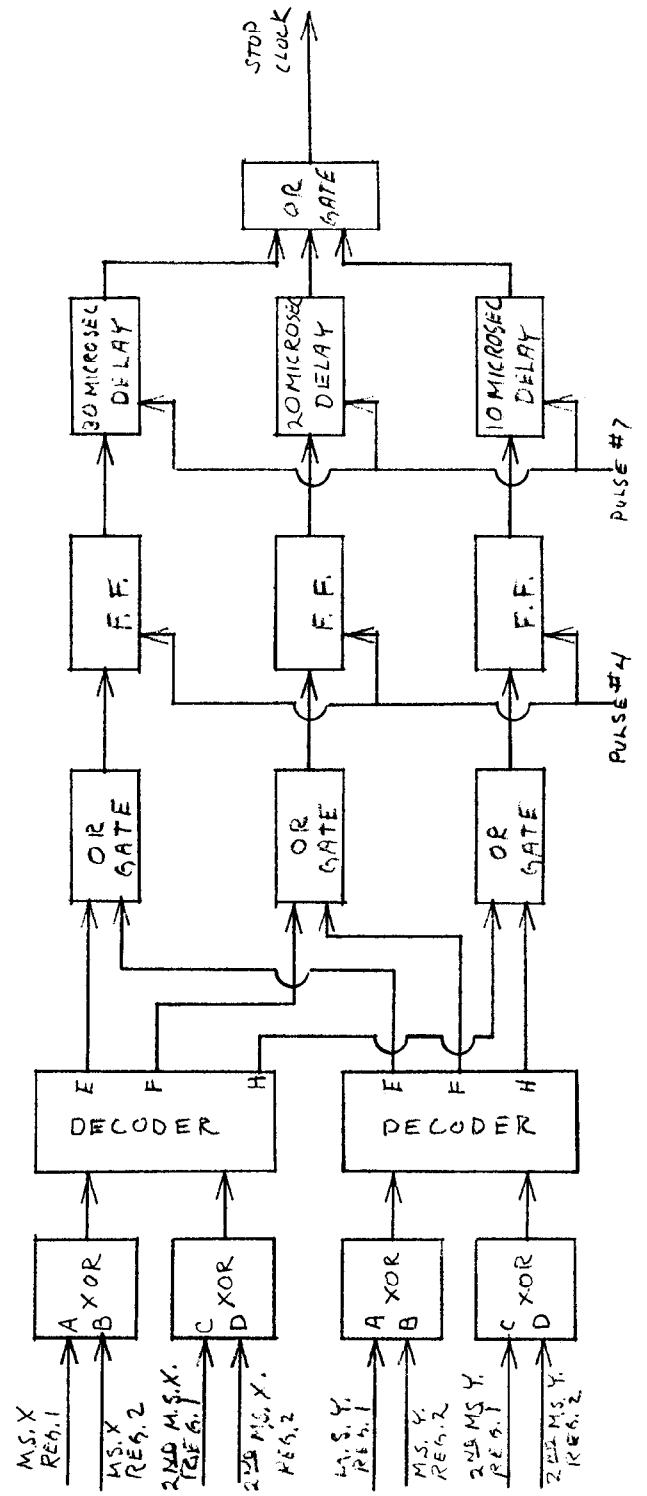
FIGURE 8 -- COLLATE



TRUTH TABLE

INPUTS				OUTPUTS		
A	B	C	D	E	F	H
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	0
0	1	0	0	0	1	0
0	1	0	1	1	0	0
0	1	1	0	1	0	0
0	1	1	1	0	1	0
1	0	0	0	0	1	0
1	0	0	1	1	0	0
1	0	1	0	1	0	0
1	0	1	1	0	1	0
1	1	0	0	0	0	0
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	0	0

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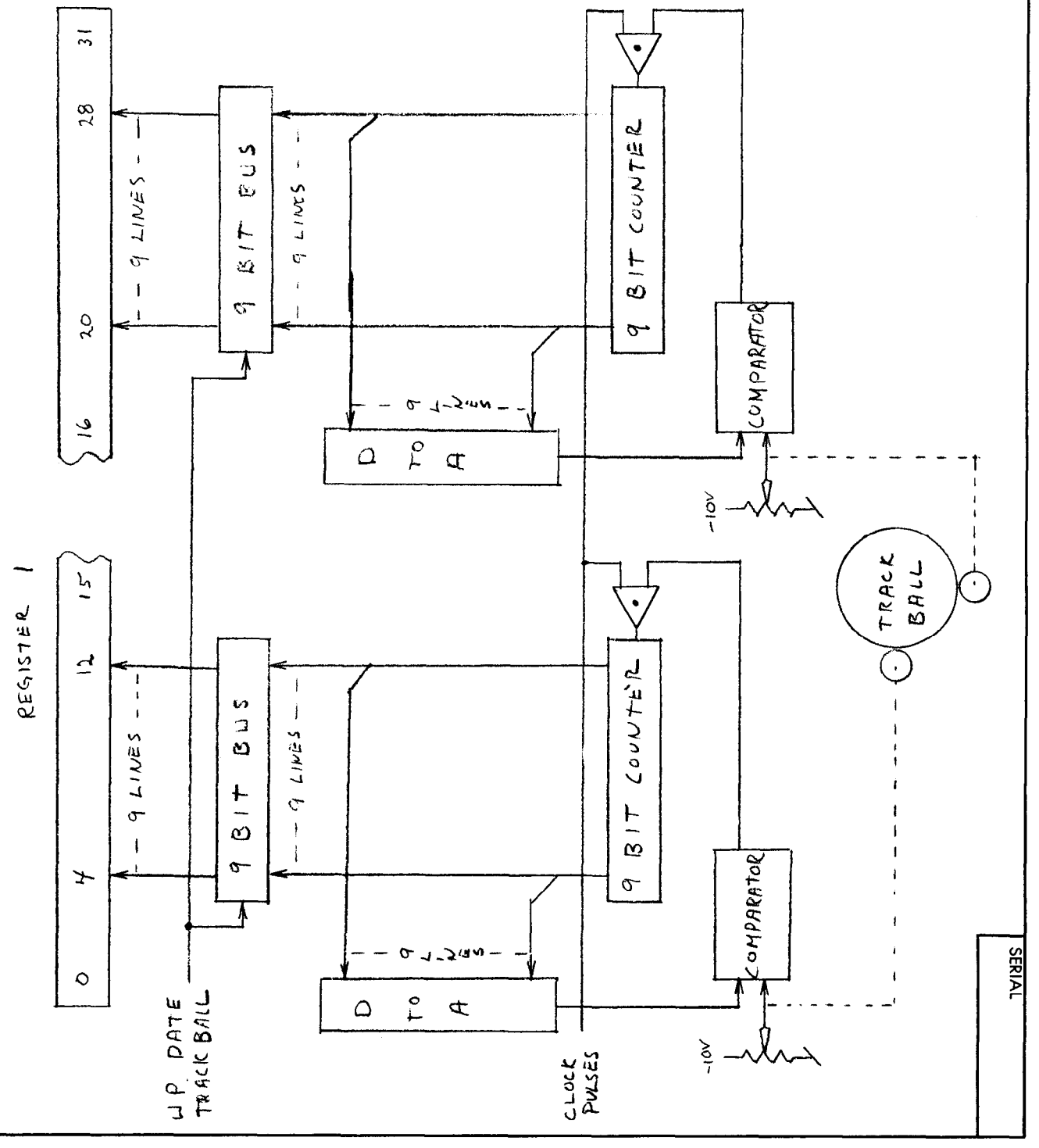
FIGURE 9 -- TRACK BALL



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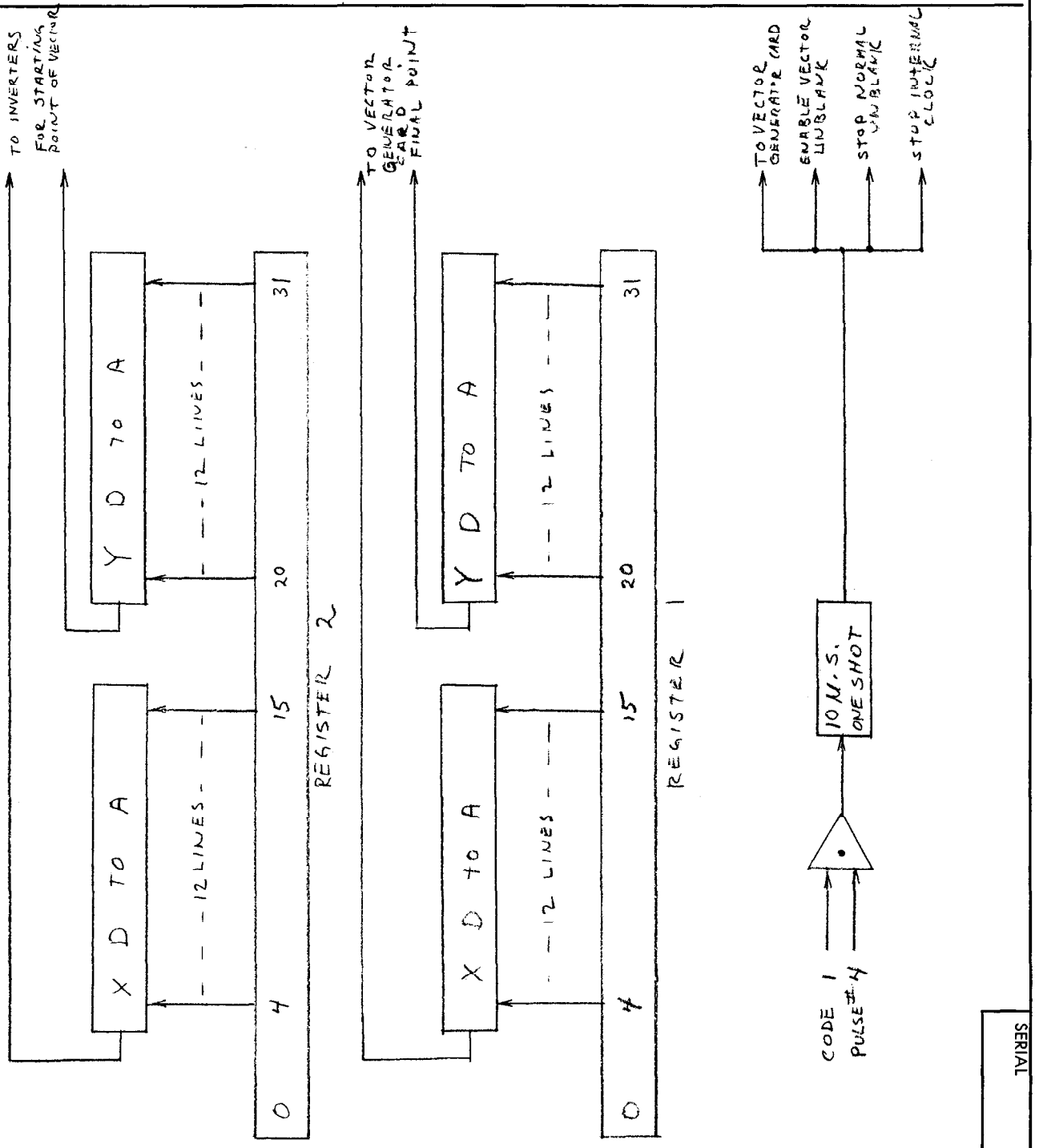
PROJECT—JOB 22½ DISPLAY CONSOLE			
TITLE FIGURE 10 -- VECTOR GENERATOR			



SERIAL

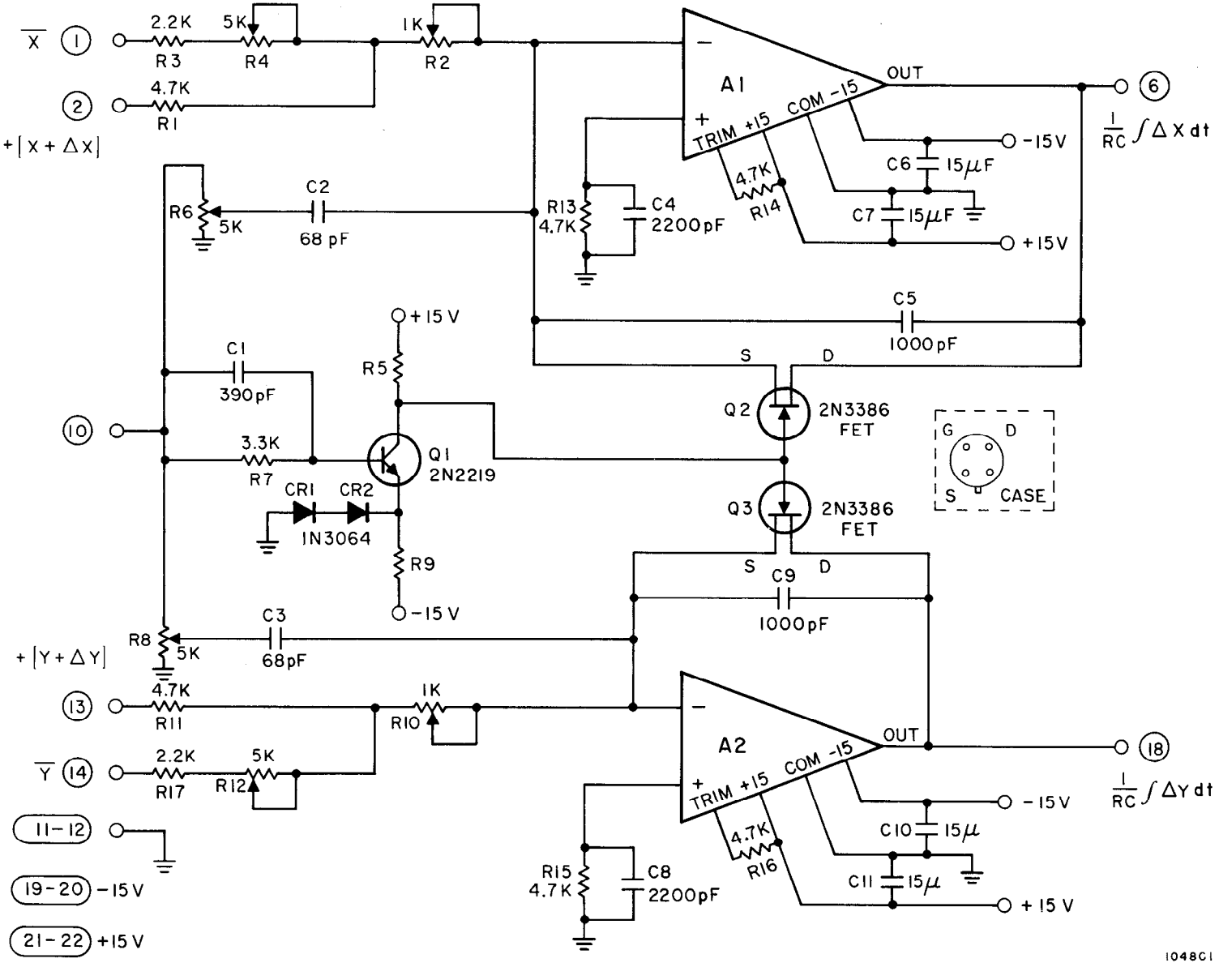


FIG. 11--22$\frac{1}{2}$ VECTOR GENERATOR

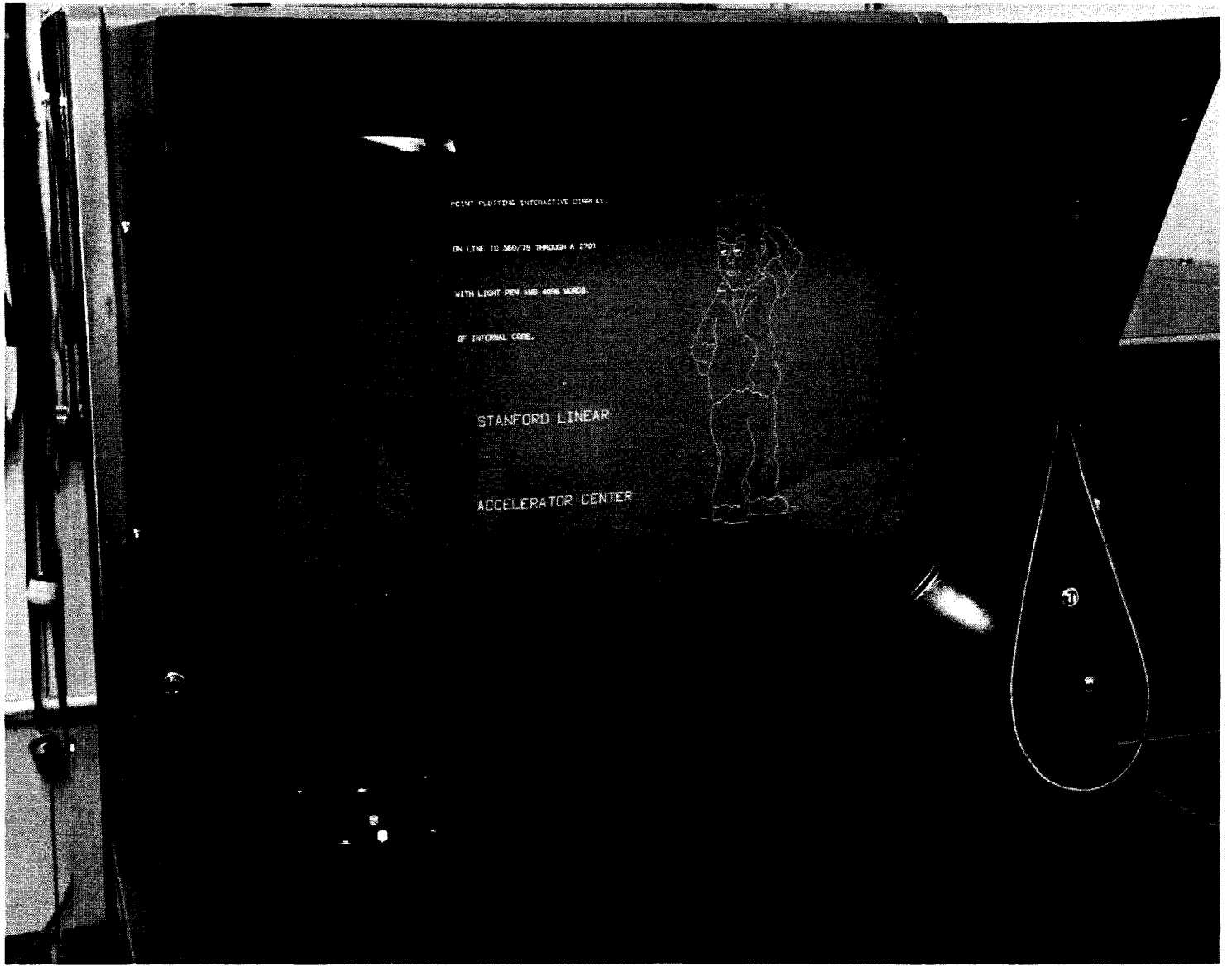


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FIG. 12--22$\frac{1}{2}$ DISPLAY CONSOLE, SHOWING FUNCTION KEYS AND LIGHT PEN

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