DEVELOPMENT OF DIGITAL LOW LEVEL RADIO FREQUENCY CONTROLLER AT SSRF

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Abstract

Digital low level radio frequency technology has been adopted in the storage ring of SSRF and a controller based on commercial FPGA and DSP board has been developed and operated successfully which helps SSRF to satisfy its specification with beam high to 300mA. The second generation controller has been fabricated in house and used with 240mA beam current at beginning of this year. The stability of amplitude and phase reaches 0.076% (RMS) and 0.053 degree (RMS) respectively. The recent progress on digital LLRF for FEL will be also reported such as the development activities and test results on the local oscillation generation board and down converter board.

INTRODUCTION

SSRF (Shanghai Synchrotron Radiation Facility) is the third generation light source, It includes the 150MeV Linac, the booster in which the beam energy is ramped from 150MeV to 3.5GeV, and storage ring which the energy is 3.5GeV.

RF system of storage ring includes three RF stations. Each has one superconducting cavity (SC) , one klystron and one set of LLRF control system. The first generation digital LLRF [1] based on commercial board has been used in 2007, and the second generation digital LLRF in house was fabricated and tested in 2013. Now it has been used into the RF system of storage ring.

The digital LLRF control system includes two basic feedback loops: the field control loop (relative to the traditional amplitude and phase feedback loop) to regulate the amplitude and phase of RF field and the tuning feedback loop to compensate for the transient beam loading, the ripples of the high voltage power supply, the temperature variations and helium pressure, etc. It requires controlling the amplitude and the phase within ±1% and ±1 degree in SSRF storage ring respectively. The frequency adjusting range is within ±10 Hz.

XFEL will be built in SINAP. The Linac is limited to be less than 300m. The linac energy is 6.5GeV. RF system include two S-band and one C-band accelerator structure.

THE FIRST GENERATION LLRF

In 2005, we start developing the digital LLRF control based on the commercial boards. Those boards include DDS board, Clock distribution board and DSP board which are integrated the digital part. The coaxial elements were used to build the RF receiver part. It has been finished and used in 2007.the picture of controller is showed in figure 1:

Figure 1: The first generation LLRF controller.

The GUI of LLRF divided into two part, The LabView software were used in the local interface and remote interface was built based on the EPICS. The data between local and remote interface were communicated through the share-memory.

The LLRF controller runs more than six years, the stability of amplitude and phase achieved 0.15% (RMS) and 0.06 degree (RMS) when storage ring operated in top-up mode with beam current 200 mA [2].

THE SECOND GENERATION LLRF

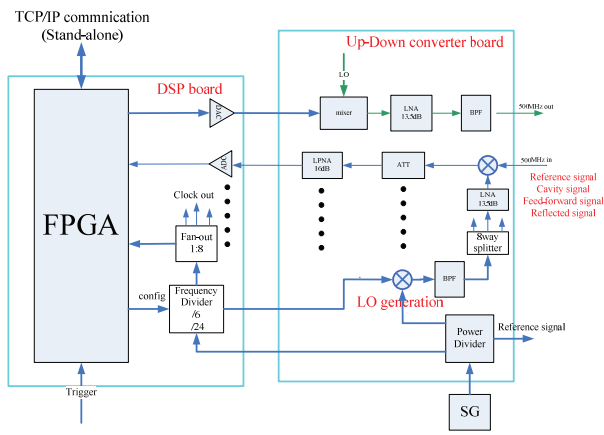

Figure 2: Function block of new LLRF.

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The first generation LLRF based on commercial boards have some defects. The structure of LLRF controller are complicate which bring some instability of signal transferred among hardware and difficulty of searching breakdown. So we develop the hardware of LLRF in house.

The layout of new LLRF is showed in figure 2. The clock signal was generated by frequency divider, the sample frequency is about 83MHz from which the main frequency of 500MHz divide 6. The LO signal is from the mixer between main frequency and one middle signal from which 500MHz divide 24 in the same frequency divider. Other parts are same as the first generation LLRF.

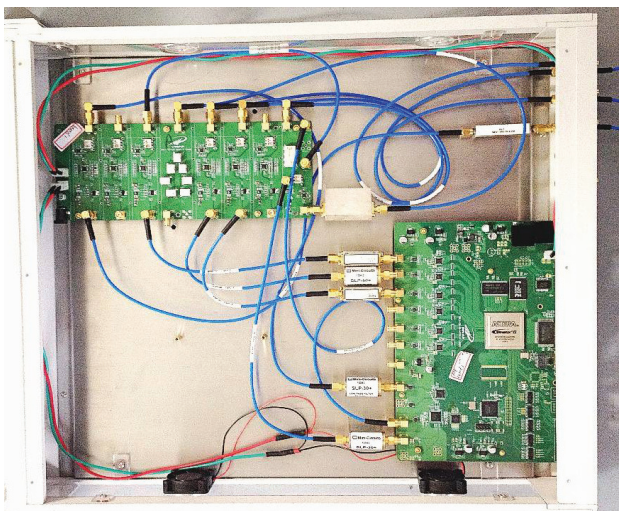

Figure 3: The second generation LLRF controller.

The second generation LLRF controller box is showed in figure 3. It include two boards, RF receiver board and DSP board. RF receiver board change 500MHz to 20MHz and verse visa. It has five down-converted channels and one up-converted channel. The channel crosstalk is less than 75dBc. The dynamic range is from -60dBm to 10dBm. Each channel gain is about 10dB. The DSP board includes six channels ADC of 125MSPS, two channels DAC of 275MSPS and Altera ep2s60 FPGA. The peripheries of controller include CPU reset button, the JTAG interface, 26 pins connector for tuner system.

The LLRF controller have been tested for six months in lab, the amplitude stability and phase stability achieved better than 0.025% (RMS) and 0.014°(RMS) without klystron and cavity respectively. After that, we tested the controller on line. The amplitude stability and phase stability achieved better than 0.076% (RMS) and 0.053 degree (RMS) with top-up of 240mA@3.5GeV beam current respectively.

The new LLRF GUI based on the EPICS have been developed simultaneously. It is showed in figure 4. There is only one interface that does not distinguish the local and remote compare with old one. The parameters and read back data are the same as the old one.

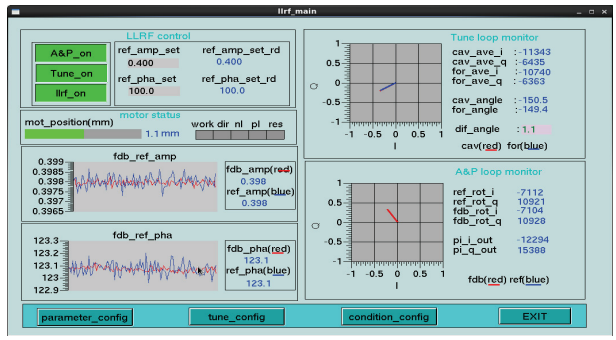

Figure 4: The EPICS GUI of new LLRF.

HARDWARE DEVELOPENT OF XFEL LLRF

RF frequency of XFEL will adopt two frequency[3]: 2856MHz and 5712MHz, some wide band chips which cover those two frequency will be used. The hardware board will be divided three parts: LO and clock signal generation board, RF receiver board and DSP board. The function block of XFEL LLRF is show in figure 5.

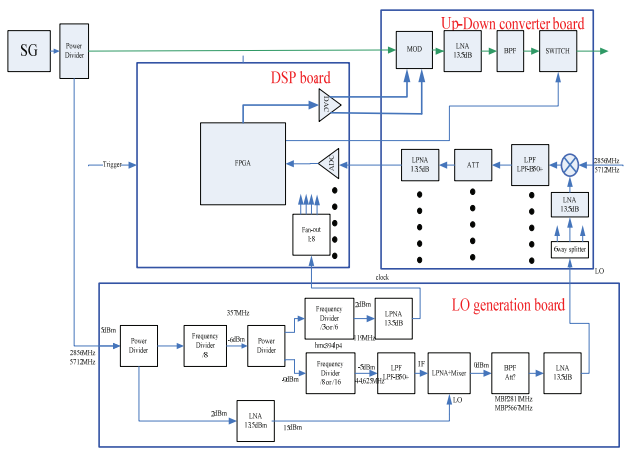

Figure 5: The function block of XFEL LLRF.

So far, we test the phase noise of clock signal and IF signal. The RMS jitter are 365fs and 788fs respectively. The measurement of result is showed in figure 6:

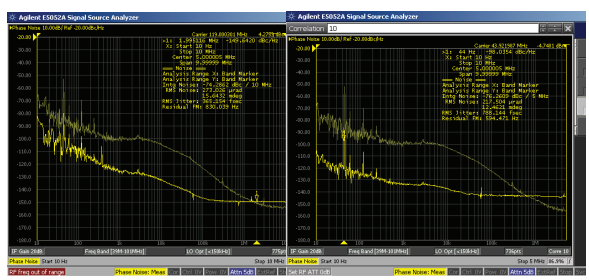

Figure 6: Phase noise of clock and IF from XFEL LLRF.

FUTURE PLAN

The second generation LLRF will be package into CPCI board and will be used in booster in SSRF at end of this year. The hardware development of XFEL LLRF will be continued.

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