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Improved Tapped-Delay-Line Time-to-Digital Converter with Time-over-Threshold measurement for a new generation of Resistive Plate Chamber detectors

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To exploit the timing performance of a new generation of Resistive Plate Chamber (RPC) detectors, we propose a TDC using a signal-reshaping approach to minimize bubble length (bits of uncertain data) and thus to improve the time measurement resolution. It includes two encoders to detect independently the signal's leading/trailing edges in a 64-bit window, instead of taking the whole delay line's length over hundreds of bits. This saves implementation resources. Our proposed TDC has been implemented on a FPGA (Cyclone V GT device, 5CGT–D9-C7N) in 65 channels in parallel. Test results give evaluated precision of measurements in RMS values: 10.0ps for leading edge, 14.1ps for trailing edge and 18.1ps for ToT respectively. The TDC can operate at a minimum pulse width of 2ns for its input pulsed signal.

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1. Introduction

As one of the CMS (Compact Muon Solenoid) muon upgrade projects, the RPC (Resistive Plate Chamber) upgrade aims to equip the high η muon stations for High-Luminosity Large Hadron Collider (HL-LHC) with a new generation of detectors. For this purpose, a new double-gap RPC with high-rate capability and improved spatial and timing resolution is proposed. This has led us to develop two prototypes (small size and full size respectively) with associated readout electronics (including Cyclone II FPGAs to implement a TDC to fully exploit the RPC fast timing capability [5]) [1]. Although the operations of both systems have been successfully tested at CERN, their integrated TDC did not fully meet the system requirements: more than 32-channel/module and a capability of measuring signal's pulse width (PW) down to a few ns.

For the latter requirement, it is needed to improve the time-over-threshold (ToT) measurement with sufficient PW resolution for measuring the signal charge. We have thus targeted the implementation of a TDC with less than 45ps for leading and trailing edges for PW determination, and a dead time of less than 10ns.

This paper presents the implementation of such a TDC based on a 28-nm low-end Cyclone V-GT FPGA, which allows ToT measurement using one single tapped-delay-line TDC channel. Our proposed tapped-delay-line TDC is based on the one suggested in 2003 [2], which mainly consists of a coarse-time counter and a fine interpolator. The coarse-time counter is driven by a clock to give out a coarse timestamp, while the fine time interpolator uses a tapped delay line to yield a sub-clock period resolution called fine timestamp. However, the suggested TDC is only suitable for using FPGA with a very few bits of bubble (i.e. bits of uncertain data, or noise). There has been an improved implementation by using Kintex-7 FPGA from Xilinx [3], but the number of bits of bubble remains limited to below 10. As new FPGAs provide higher speed, the bubble issue becomes more serious [4]. To deal with this problem, our implementation includes the use of some techniques such as signal reshaping and encoding only a small segment of signal around edge. Our paper is organized as follows. Section 2 presents our proposed TDC architecture as well as signal-reshaping and encoding techniques. In Section 3, the characteristics of the TDC will be analysed and discussed. Finally, in Section 4 we draw our conclusion.

2. TDC implementation

2.1 Architecture

Fig. 1 shows the architecture of our proposed tapped-delay-line TDC. It needs two clocks for its operation: a fast clock and a slow one (with a frequency division by 2). The TDC has two inputs, one for calibration (with data recording in a Look Up Table (LUT)), and the other for receiving signal from the detector. In the detection process (after calibration), via a multiplexer, a selected input signal goes through the reshaping module before entering into a tapped delay line built with a fast carry-chain of FPGA. The delay line status is then latched by the fast clock and sent to both leading-edge and trailing-edge encoder blocks. The two encoder blocks respectively detect the signal's leading and trailing edges within two fast clock's periods. They trigger the register module to record the value of free-running coarse-time-counter as corresponding coarse timestamp. Meanwhile, they count the number of delay elements of the selected signal reached on the delay line for a given slow clock's duration. Their output number corresponds to the time interval between the detected signal edge and the rising edge of the fast clock. Due to a non-linear

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relationship between an encoder output number and the time interval, it is necessary to employ a LUT for fine time measurement. The LUT data are previously set in calibration process.

As the two encoders operate simultaneously and independently, this allows ToT measurement for a signal's PW even below one fast clock's period (2ns). In addition, the dead time is equal to one slow clock's period (4ns).

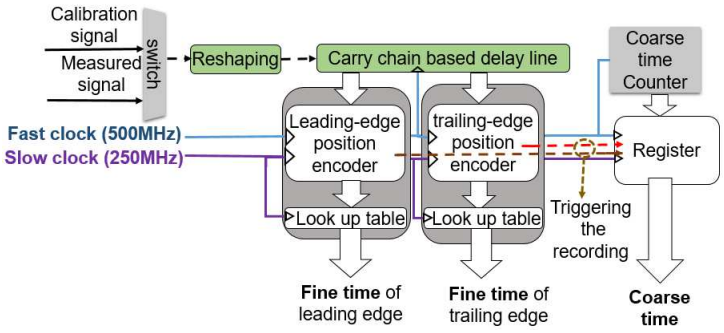

Figure 1: The proposed tapped-delay-line TDC architecture.

2.2 Reshaping module

The reshaping module is proposed to tackle the bubble issue, which is typically observed when input signal is fed directly on the delay line: there are a number of bubble bits after the first fast-clock cycle, and will not disappear until the second or third cycle. This phenomenon may result from the following factors: 1) increased transition time due to logic elements and/or interconnect network; 2) loop-back noise due to state transition of employed flip-flops, which induces fluctuations to the input of delay line via LAB (logic array blocks) interconnect network.

To reduce the transition time of the input signal, it is passed through a dedicated reshaping circuit based on a XOR and a flip-flop logic in loop. In addition, the circuit has an optimized output layout with a short link to the delay line. It gives an output signal with a transition edge of about 115ps. Accordingly, the bubble is reduced to 23 bits. This also improves the resolution of fine time measurement from 32ps to 10ps.

2.3 Encoders' operation

A typical encoder's operation consists in converting the thermometer code (ultra-wide input vector) into one-hot code (i.e. only one bit of '1' indicating the signal-edge position), and then extracting the position of bit '1' [2, 3, 4]. However, this mothed is suitable only for a bubble length limited to a few bits. As our case has a bubble length over twenty bits, we propose to implement an approach combining transition area determination and encoding. It operates as follows: 1) dividing the signal vector in the latched tapped-delay-line into several segments of 32-bits; 2) down sampling each segment by a factor of 8, and applying an OR/AND logic function to generate a bit as segment indicator, followed by concatenating all the segment indicator bits for leading/trailing edge detection; 3) determining the transition segments of the signal vector by leading/trailing edge detection ("01" for leading edge and "10" for trailing edge);4) detecting in each transition segment the first transition bit, from MSB (most significant bit) to LSB (least significant bit), as well as transforming the position of the first transition bit into a binary code.

The final step 4 can be performed in two slow clock's periods (for the saving of FPGA resources).

2.4 Multi-channel TDC implementation

For our application, we have implemented 65 TDCs in parallel (64 channels for signal measurements and an extra channel for system reset) on a FPGA (Cyclone V GT device, 5CGT–D9-C7N). Each TDC has a delay line of 380 bits. Our implementation makes use of about 86% logic cell resources. The FPGA is incorporated in a commercialized development board (DK-DEV-5CGTD9N), which we have used for the testing.

3. Test and results

3.1 Setup

We have carried out the test on two adjacent channels, which allows differentiation of measured parameters between channels. The same input testing signal is injected in both channels. It is a periodic pulse signal generated from Keysight (model 81150A) and applied to the circuit under test via a SMA (SubMiniature version A) connector. The input signal has no correlation with the TDCs' clocks. It triggers each TDC to record both coarse and fine timestamps, which are then transmitted to a signal acquisition PC via a serial data link.

3.2 Analysis

The time resolution of the implemented TDC has been evaluated by analysing the precision of measurements on leading and trailing edges as well as ToT.

For measuring leading and trailing edges, the same input stimulus has been applied on both TDCs under test to cancel jitter effect of the input signal, and the difference of their output responses has been registered. The statistical analysis of registered data determines the standard deviation (or RMS(root mean square)) of the measured edges for two TDCs. Dividing the RMS value by $\sqrt{2}$ gives the precision of the measured parameter (for one TDC).

ToT measurement has been carried out on one single TDC. For each input pulse, the PW of the output response has been registered. The statistical analysis gives RMS value, corresponding to the precision of measured PW. It is noted that the obtained RMS value includes contribution from the jitter of the input signal. The precision of measured PW without jitter contribution can be deduced by making root sum squared of the leading and trailing edges' RMS values. Thus input jitter effect can be estimated by comparing results from these two different approaches.

3.3 Results and discuss

Figure 2 shows statistical distributions of the measured parameters (using 5-ns PW of input pulsed stimulus): leading edge difference of the two TDCs (Fig. 2a), trailing edge difference of the on two TDCs (Fig. 2b) and ToT (with input jitter contribution) (Fig. 2c). The evaluated RMS values are respectively 14,2ps for leading edge, 20.0ps for trailing edge and 18.1ps for ToT. For one TDC, the calculated RMS values for leading and trailing edges are 10,0ps and 14,1ps respectively. For ToT without input jitter effect, the estimated RMS is 17.4ps. Thus, the jitter contribution is not significant.

Changing input signal's PW from 2 to 100ns gives stable RMS around 19ps over this measured range (see Fig. 3). This means that the implemented TDC can operate at a minimum PW of 2ns.

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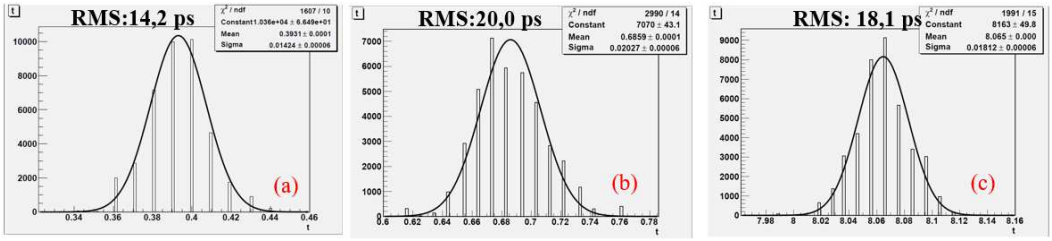

Figure 2: Statistical distributions of the measured parameters: a) leading edge difference of two TDCs; b) trailing edge difference of two TDCs; c) ToT with input jitter contribution.

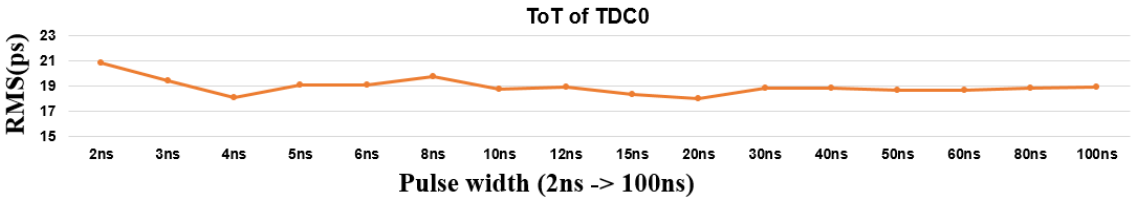

Figure 3: RMS values of ToT versus input signal's PW.

4. Conclusion

Our proposed TDC by adopting several performance-improving approaches has been implemented on a FPGA (Cyclone V GT device, 5CGT–D9-C7N) in 65 channels in parallel. It has been tested to validate its operation and to evaluate its characteristics. We have thus obtained the precision of measurements (in RMS values) as follows: 10,0ps for leading edge, 14.1ps for trailing edge and 18.1ps for ToT respectively. The TDC can operate at a minimum PW of 2ns for its input pulsed signal.

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