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Study of prototypes of LFoundry active CMOS pixels sensors for the ATLAS detector

L. Vigani[a,1] **D. Bortoletto,**[a] **L. Ambroz,**[a] **R. Plackett,**[a] **T. Hemperek,**[b] **P. Rymaszewski,**[b] **T. Wang,**[b] **H. Krueger,**[b] **T. Hirono,**[b] **I. Caicedo Sierra,**[b] **N. Wermes,**[b] **M. Barbero,**[c] **S. Bhat,**[c] **P. Breugnon,**[c] **Z. Chen,**[c] **S. Godiot,**[c] **P. Pangaud**[c] **and A. Rozanov**[c]

[a] *University of Oxford,*
Denys Wilkinson Building, OX1 3RH, Oxford, United Kingdom
[b] *University of Bonn,*
Nussallee 12, Bonn, Germany
[c] *Centre de physique des particules de Marseille,*
163 Avenue de Luminy, Marseille, France

E-mail: luigi.vigani@physics.ox.ac.uk

Abstract: Current high energy particle physics experiments at the LHC use hybrid silicon detectors, in both pixel and strip configurations, for their inner trackers. These detectors have proven to be very reliable and performant. Nevertheless, there is great interest in depleted CMOS silicon detectors, which could achieve a similar performance at lower cost of production. We present recent developments of this technology in the framework of the ATLAS CMOS demonstrator project. In particular, studies of two active sensors from LFoundry, CCPD_LF and LFCPIX, are shown.

Keywords: Particle tracking detectors; Radiation-hard detectors; Solid state detectors

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[1]Corresponding Author

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1 The ATLAS upgrade

1.1 The ATLAS experiment

ATLAS (A Large Toroidal LHC ApparatuS) is a large multi-purpose high energy particle physics experiment at the Large Hadron Collider (LHC) at CERN [1]. It consists of several detector elements, nested around the interaction point, measuring the properties of the particles produced in the LHC collisions. The main goals of the ATLAS physics program are precision studies of the Standard Model physics, including the recently found Higgs Boson, and searches for physics beyond the standard model, including Supersymmetry.

1.2 Towards HL-LHC

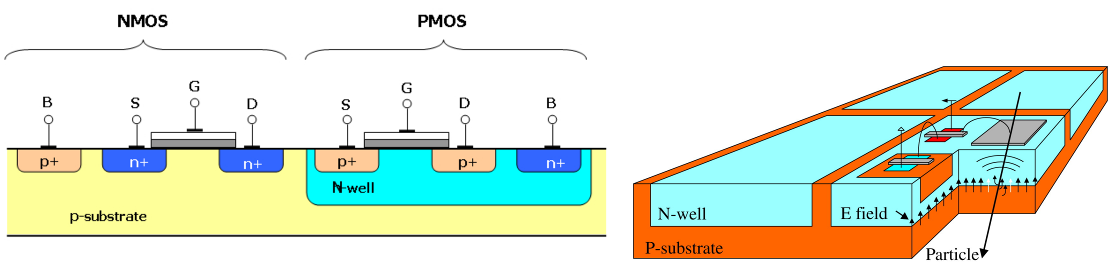
The Large Hadron Collider is currently taking data at 13 TeV and at a luminosity of $10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. It is expected that the center of mass energy of the machine will increase to 14 TeV for run 3. Then, the machine is scheduled to undergo an upgrade, denoted as the High Luminosity LHC or HL-LHC, that will increase the instantaneous luminosity to about $7 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ [2]. The HL-LHC phase will start in 2026 and will last about 10 years. In this period, the bunch crossing time will remain 25 ns, while the number of proton collisions per bunch crossing will be increased. The higher instantaneous luminosity imposes new requirements to the detectors in terms of speed, data acquisition rate and radiation resistance. In particular, the tracking system, which is the innermost part of the experiment, will be replaced with a new all-silicon tracker, the Inner Tracker or ITk. This is divided into two sub-subsystems, a Strip Detector surrounding a Pixel Detector. The devices presented in this paper are potential candidates for the 5th (last) layer of the pixel system, which will be located at about 30 cm from the interaction region. At that distance the fluence and the Total Ionization Dose (TID) are expected to be $1.5 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ and 80 Mrad respectively.

2 Introduction to CMOS detectors in ATLAS

Most current HEP experiments operating at the LHC have a pixel system based on silicon hybrid technologies at the center of their trackers. Silicon hybrid detectors are produced by connecting a high resistivity silicon diode to a front-end read-out chip. The connection is guaranteed by arrays of conductive bumps, one per pixel, generally made with solder material deposition of SnPb or indium. These detectors have achieved excellent performances providing a good signal response within 25 ns. They are also radiation hard up to $5 \cdot 10^{15}\ \mathrm{n_{eq}/cm^2}$.

CMOS technology provides a different detector concept, in which the read-out circuitry is inserted inside the silicon sensor itself. Therefore, sensors based on this technology are often called Monolithic Active Pixel Sensors, or MAPS. These sensors have been used in a variety of applications from industry to medical physics. A basic sketch of this technology is shown in figure 1(a). MAPS have been also used in particle physics experiments [3, 4] providing excellent performance due to their fine granularity (the pixel size can be about $20 \times 20\ \mu\mathrm{m}^2$) and low material. The use of MAPS for particle physics is also attractive since they are produced in large foundries at relatively low cost.

Standard MAPS detectors are not suitable for LHC and HL-LHC operation, since in these detectors the charge collection happens mainly trough thermal diffusion, which leads to a charge collection time that is too long for these challenging environments. In fact, charge collection via drift is favoured in silicon pixel sensors. This is achieved with the formation of a depleted region inside the silicon bulk. Since in diodes the depletion layer's depth is proportional to $\sqrt{\rho \cdot V_{\mathrm{bias}}}$, one must increase the resistivity (ρ) or the bias voltage (V_{bias}). Generally, sensors made with high resistivity wafers (higher than a few hundreds Ω·cm) are known as HR-CMOS, while sensors where high bias voltage can be applied (higher than a few tens of Volts) are named HV-CMOS. The devices described in this paper have both features, and are referred to as Depleted MAPS, or DMAPS. LFoundry provides high resistivity wafers as well as high voltage add-ons [5]. In order to obtain high voltage operation, the read-out circuitry is nested inside a deep n-well. This way, the depletion region is formed between the substrate and the deep N-well itself [6]. A sketch of these add-ons can be seen in figure 1(b).



(a) (b)

Figure 1. (Left) Standard CMOS sensor layout (from side). (Right) Layout of the CMOS modified process for high bias voltage. Reprinted from [6], Copyright (2007), with permission from Elsevier.

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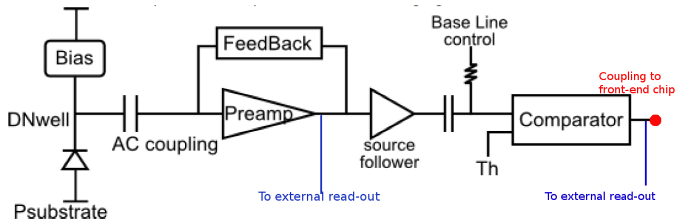

Figure 2. Single pixel cell schematics for the active CMOS sensors. One can read-out the preamplifier and comparator with a standalone board or glue it with capacitative glue to a front end chip.

3 LFoundry prototypes

In the past three years, a few prototypes of CMOS detectors have been designed and fabricated within the ATLAS CMOS pixel collaboration. In this paper we describe two devices produced in LFoundry technology: CCPD_LF and LF-CPIX. In addition to these devices, a fully monolithic device has been produced as well, the LF-MONOPIX, and its performance is currently under investigation [7].

CCPD_LF and LF-CPIX have a very similar in-pixel design: preamplifier, feedback resistance, source follower, baseline adjustment and comparator are implemented inside the deep n-well. For this reason they are referred to as active CMOS devices. In addition, both have different pre-amplifier transistors: PMOS, NMOS and CMOS (the last only for LF-CPIX) [8]. The basic read-out scheme is sketched in figure 2. Both devices can be capacitively glued to a FE-I4 chip or, alternatively, the preamp and comparator output of a single pixel can be read-out with a standalone board.

The main difference between the two devices is the pixel size, which is $33 \times 125\,\mu\mathrm{m}^2$ for CCPD_LF and $50 \times 250\,\mu\mathrm{m}^2$ for LF-CPIX, the latter being the same size as the FE-I4 [9] ATLAS pixel read-out chip.

4 Characterization and results

CCPD_LF and LF-CPIX have been extensively characterized in the laboratory and in test-beams before and after irradiation with different radiation sources at various doses.

4.1 Performances before irradiation

CCPD_LF was tested in a 3.2 GeV electron beam at the ELSA facility in Bonn (see figure 3). The collected charge spectra are compatible with a resistivity of 3 kΩ·cm [10].

This result has been confirmed by investigating the properties of charge collection with the edge-TCT, a technique that consists of shining very fast infra-red laser pulses on the edge of a sensor [11]. Once the laser is well focused, one can study the signal produced at different depth levels inside the silicon bulk and have a direct measurement of the depletion depth. Figure 4(a) shows the charge profiles obtained with this method at different bias voltages, confirming that the depletion region and therefore the signal increases with bias voltage as expected. The depletion depth is then calculated as the FWHM of this profile, and its value is plotted as a function of the bias voltage in figure 4(b). From an interpolation with a square root function it is possible to estimate the resistivity to be 3.3 ± 0.5 kΩ·cm, which confirms the result obtained with the electron beam.

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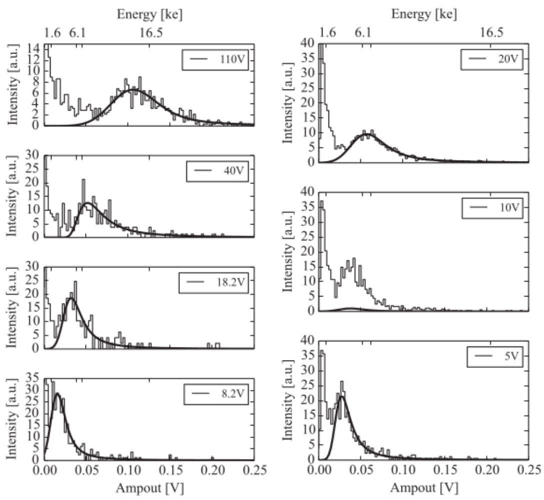
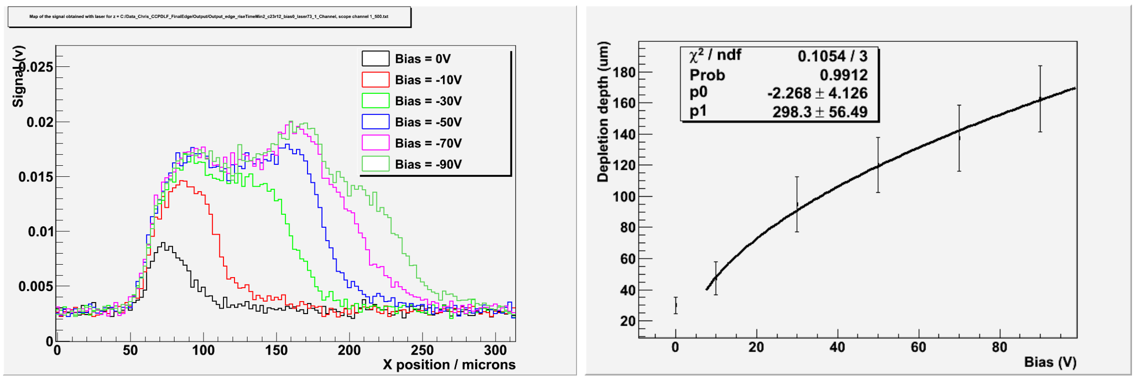


Figure 3. MIP spectra obtained with 3.2 GeV electron beam. Reprinted from [10], Copyright (2016), with permission from Elsevier.



(a) (b)

Figure 4. (a) Edge-TCT 1D scans of a CCPD_LF active pixel. Note that the chip surface starts at about 50 μm on the x axis and the depletion region extends from left to right. (b) FWHM of the signal profile vs bias.

The charge collection properties of LF-CPIX have also been investigated with the edge-TCT. Figure 5(a) shows the charge collection profile as a function of the laser depth for different bias voltages. From an interpolation with a square root function (figure 5(b)) it was possible to estimate the resistivity to be 4.2 ± 0.3 kΩ·cm.

4.2 Performances after irradiation

Some CCPD_LF prototypes have been irradiated with neutrons at the TRIGA reactor in Ljubljana [12] up to a fluence of $5 \cdot 10^{15}$ $n_{eq}cm^{-2}$ and then tested with the edge-TCT to evaluate the reduction in the depletion region due to bulk damage [13]. From the results of this study, shown in figure 6, it is clear that even after a fluence of $2 \cdot 10^{15}$ $n_{eq}cm^{-2}$ a depletion depth of more than 50 μm can be obtained, surpassing the requirements for operation in the outer pixel layers.

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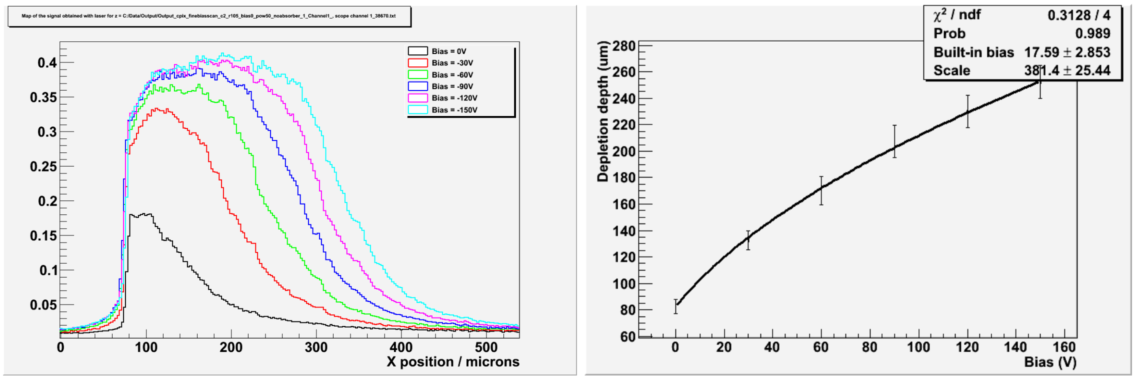

(a) (b)

Figure 5. (a) Edge-TCT 1D scans of an LF-CPIX active pixel. (b) FWHM of the signal profile vs bias.

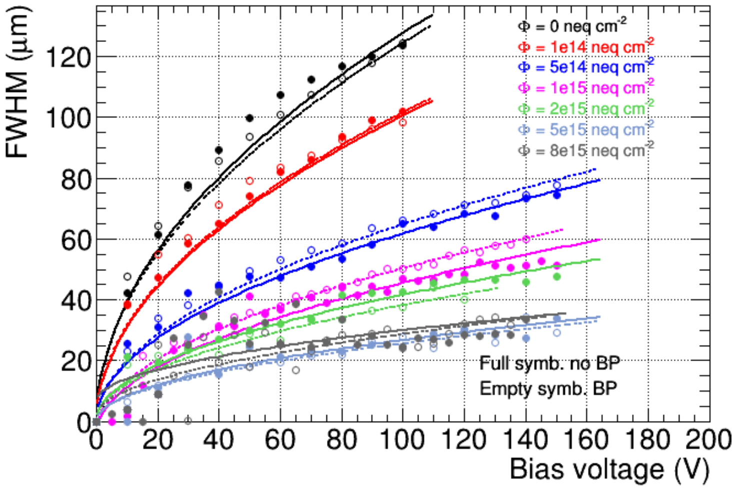

Figure 6. Depletion depth as a function of voltage obtained with CCPD_LF at different irradiation doses. Reproduced from [13]. © IOP Publishing Ltd. All rights reserved.

Some LF-CPIX samples have been irradiated with 27 MeV protons to a fluence of $1.0 \cdot 10^{15}\,\mathrm{n_{eq}cm^{-2}}$ at the Birmingham MC40 Cyclotron [14]. Afterwards, edge-TCT has been performed to check the effect of the irradiation on the charge collection. The results, shown in figures 7(a) and 7(b), prove that the device can be depleted to a depth of more than 70 μm after this dose.

In addition, the sample was exposed to X-rays from a ^{55}Fe source. The spectrum obtained from the preamplifier output of a single pixel (figure 8) shows the expected peak at 1640 e^-, demonstrating that the device is performing well.

5 Conclusion

The ATLAS upgrade demands very high standards on the performance of its new tracking system. A new concept of silicon detectors, based on CMOS technology, is under investigation as a candidate for the fifth pixel layer. The new technology brings great advantages including easier and lower

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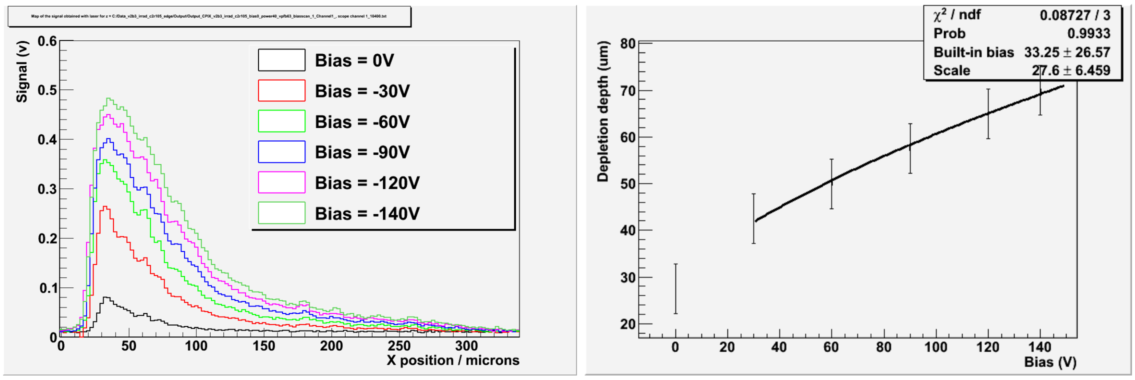

(a) (b)

Figure 7. (a) Edge-TCT 1D scans of an LF-CPIX active pixel after proton irradiation. (b) FWHM of the signal profile vs bias.

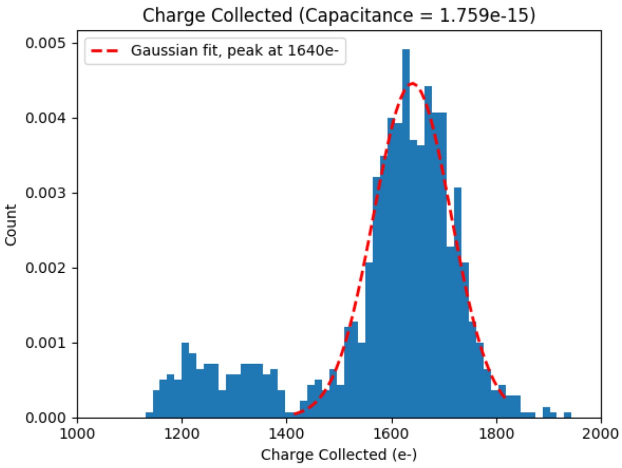

Figure 8. ^{55}Fe spectrum obtained with proton irradiated LF-CPIX.

cost of production of detector modules. The ATLAS demonstrator program is studying different prototypes and foundries to prove the feasibility of this technology for the ATLAS upgrade.

One of the foundries that have been investigated is LFoundry, which provides sensors with high resistivity and high voltage additions. These add-ons ensure a sufficiently high signal. Two active CMOS sensors, CCPD_LF and LF-CPIX, have been produced and studied in order to test the performance of this technology. Some tests have been conducted on these devices before and after irradiation with with neutrons and protons.

The tests performed so far indicate that these devices are capable of generating and collecting a signal even after being irradiated to $5 \cdot 10^{15}\ \mathrm{n_{eq}cm^{-2}}$. These studies provide an important reference for the next step of the ATLAS CMOS pixel project. In fact, a fully monolithic device has been already produced based on this technology. The final steps of this R&D requires the design and production of fully functional modules, in order to prove the feasibility of CMOS technology for the ATLAS upgrade.

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Acknowledgments

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