SLAC-TN-71-13
D. Porat/D. Ouimette
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8-BIT ADC WITH LINEAR GATE FOR CHARGE AND SUB-NANOSECOND TIME MEASUREMENTS

PART 1. Circuit Description and Performance

ABSTRACT

Short pulses are processed through a linear gate, an integrating circuit and a peak detector followed by an 8-bit ADC. The circuit can be used in two modes: (i) For amplitude measurement with a resolution of 5×10^{-11} volt-sec/count, and (ii) for time measurements with a resolution of $\approx$ 62 psec/count using a standard NIM logic input. Stability and linearity are $<$ 1%. The output is presented on a CAMAC bus.

1. INTRODUCTION

ADC's for nanosecond pulses have found a wide application in high-energy physics experiments. The circuit described here measures the time-integral of a gated pulse and can thus be used either for measurements of shower energies or for time-of-flight measurements when signal and gate are used in an overlap coincidence circuit. Nanosecond pulses are thus processed, digitized and then presented on data lines that interface easily with computer-controlled data-acquisition systems.

Forty ADC's, SLAC No. 114-121 were recently constructed under the coordination of HEEP. The purpose of this TN is to acquaint the experimenter with the operating characteristics of the circuit. A supplemental note, TN-71-14, contains information on adjustment and calibration procedures, and discusses systems utilization.

The ADC system utilizes two types of modules: (i) The ADC, SLAC No. 114-121 that accepts short pulses and measures either charge or time intervals, and

(ii) ADC CONTROL, SLAC No. 114-122, that provides control signals common to a maximum of ten ADC's in one chassis.

The CAMAC Format is used to facilitate data bussing and module address-selection.

Connector pin utilization follows the CAMAC code, as far as possible, with three exceptions: INHIBIT on pin 25, CLOCK on pin 27 and CLEAR on pin 29. (Note that these pins are allocated in the CAMAC system for WRITE operations on bits W24, W22 and W20, respectively. The likelihood of conflict in utilizing these pins is minimal at SLAC).

A circuit similar to that discussed in this note was described earlier.*

It is foreseen that some experiments may use ADC's of both kinds in a data acquisition system. The differences between these two circuits are discussed in section 5.

2. SPECIFICATIONS

2.1 Specifications of ADC, SLAC No. 114-121

Data Input: -220 pC, max. for linear output provided DATA amplitude does not exceed -1.1 volts (e.g., -1.1 volt into 50 ohms, 10 nsec duration).

Sensitivity: 0.99 pC/count, i.e., 62 psec/count for time measurements or 5×10^{-11} volt-sec for amplitude measurements. (Assume, for example, a rectangular pulse of 10 nsec duration. The sensitivity at this width is 5 mV/count.) Note: At maximum sensitivity, the total range available for time measurements is (62 psec/count) x (250 count) = 15.5 nsec. To extend the range insert an attenuator in the DATA path. The range, in nsec, will be proportional to the attenuation factor. (Sensitivity will, off course, decrease correspondingly.)

Gate Input: -0.8 V into 50 ohm, i.e., standard NIM logic ONE. Minimum duration 4 nsec.

Linearity: Better than 1%, integral.

* D. Porat and K. Hense: "Seven-bit Analog-to-Digital Converter for Nanosecond Pulses", Nucl. Instr. and Methods, vol. 67 (1969) 229-239; SLAC-PUB-442 (July 1968).

Resolution: 8 binary bits.

Analog Output (PHA): Delivers a negative pulse proportional to the time-integral of the input signal and matching input characteristics of pulse-height analyzers. Rise time (10 to 90%) = 0.5 μsec. Decay time constant (to 1/e) = 3.4 μsec;

Digital Outputs: (i) "SCALER". Delivers number of pulses (at 10 MHz rate) proportional to the time-integral of the input signal. Output is -0.4 V into 50 ohm, nominal.

(ii) On CAMAC bus. Delivers a TTL logic level requiring a pull-up resistor at the receiving end. Logic standards are in accordance with CAMAC specifications, EUR 4100 e: Voltages at output lines shall be +3.5 to +5.5 volts for logic "0", and 0 to + 0.5 volts for logic "1". The pull-up resistor at the receiving end should provide a current $6 \leq I_p \leq 9$ mA from a positive potential when the line is at +0.5 volts, and $I_p \geq 2.5$ mA from a positive potential when the line is at +3.5 volts.

Output Strobe: +3.5 to +5.5 volts. Load is 9 standard TTL gates. When OUTPUT STROBE is high, DATA are presented on CAMAC READ lines R1-R8.

Visual Indicators: (i) DATA pilot light shows when data are present on weights 2^2 through 2^7;

(ii) " $\geq 300_8$" pilot light indicates that counts exceed 300_8 (192_{10}).

2.2 Specifications of Control Module, SLAC No. 114-122

INPUT: -0.8 V into 50 ohm, i.e., standard NIM logic ONE. Minimum duration 4 nsec.

EXTERNAL CLEAR: 0 to +0.5 volts into one TTL load. CLEAR terminal shall be at +3.5 to +5.5 volts when not actuated.

Other modes of clearing the ADC are via (i) a push-button on the panel of the CONTROL module, or (ii) a self-clearing circuit in each ADC that is actuated by the trailing edge of the STROBE pulse interrogating the particular module (see section 3.1.4).

3. CIRCUIT DESCRIPTION

3.1 8-bit ADC

Refer to block diagram, Fig. 1, and the detailed schematics, Figs. 2 through 5. Component numbers appearing in the block diagram correspond to the respective components in the schematics.

The ADC is composed of the following circuits:

(i) Input stage, Q1.

(ii) Linear, balanced gate, D2-D5.

(iii) Integrator-amplifier, Q4-Q11.

(iv) Peak detector, Q13-Q17, A1, A2 and C45.

(v) ADC, Q19-Q23, A3-A5, A7-A8.

(vi) Output gates A10, A11.

3.1.1 Linear Gate and Integrator-Amplifier (Figs. 2 and 3)

An input pulse such as from a fast photomultiplier, applied to the grounded-base stage, Q1 (Fig. 2), will pass to the amplifier stages, provided it is coincident in time with a gate signal. The linear gate is of the matched-quad type and is driven from the gate amplifier Q2, Q3. Q4 through Q6 (Fig. 2) and Q9 through Q11 (Fig. 3) are used for quasi-integration and amplification of the signal. Q7 and Q8 are a feedback pair delivering a negative pulse (Fig. 8) whose characteristics match the input requirements of several commercially available pulse-height analyzers. This output facilitates monitoring selected channels during an experiment that involves a number of ADC's, and aids in adjusting the gate pedestal to null.

3.1.2 Peak Detector, (Fig. 4)

The peak detector consists of the differential pair Q13A, B, voltage followers A1, A2, constant current source Q16, Q17 and capacitor C45. Transistor Q18 clamps C45 to -100 mV in the interval between measurements to prevent accumulation of charge on C45 due to leakage currents. Q14 also acts as a clamp during the same time interval and prevents actuation of the current source, Q17. R58 and Q12 act as an efficient limiter to limit the input to the peak detector to +5 volts.

The arrival of an event pulse at the CONTROL module (see section 3.2) produces an UNCLAMPING signal, which resets CLAMP FF (A7 of Fig. 5) and

releases the clamps on Q14 and Q18. For a brief period Q13A and B conduct current equally due to the symmetrical design of the differential amplifier and its associated high impedance buffers, A1 and A2. The input pulse to the peak detector is positive, 5 volts maximum, having a rise time of 1.9 μsec (10 to 90%) and a decay time-constant of 6.4 μsec, see Fig. 9a. This signal turns on Q13A, keeping Q13B off as long as the input voltage to the peak-detector is higher than the voltage across C45. During this time interval Q17 is on and charges C45, the voltage V_{C45} rising with a linear slope dV/dt=3V/μsec. When $V_{C45} > V_{A1}$, charging of C45 ceases. Since the rise time of the pulse is longer than the charging time of C45, peak detection is attained with good accuracy.

Fig. 9b shows the resulting signal at C45: The steps at the leading edge are due to turn-on turn-off of the peak detector. This can also be observed at test points TP2 and TP3, see Figs. 17 and 18 of TN-71-14. The flat top is due to the time-constant C45·R75=5 msec. (Time constants of 100 ms and more are easily attainable and may be of interest in systems in which the individual ADC circuits are replaced by an analog multiplexer and a single ADC.) The trailing edge of Fig. 9b is due to the linear discharge of C45 in the process of analog-to-digital conversion, as described in the subsequent section.

3.1.3 Analog-to-Digital Converter, Fig. 5

A counter-ramp ADC is employed since ample time is available between accelerator pulses for slow A/D conversion. It is also the least expensive A/D circuit and exhibits very good differential and integral linearities. The ADC is composed of the comparator, A3, that senses the voltages across C45; an 8-bit counter A8, A9; a stabilized constant-current source Q19-Q23 (Fig. 4) which is controlled by the $I_{DISCHARGE}$ flip-flop, A7.

Analog-to-digital conversion starts 25μs after the input to Q1 (Fig. 2) to allow for the decay of the pulse at the peak-detector input. When A3 senses a voltage $V_{C45} > V_{REF}$ it delivers a positive gating pulse which allows 10 MHz CLOCK signals to pass to the input of binary counter A8. The leading edge of the gating pulse sets the $I_{DISCHARGE}$ flip-flop, which steers the current of the constant-current source through Q19, discharging C45 at a constant rate. This rate is variable within several percent through adjustment of R88 in Fig. 4.

Binary counter A8 receives CLOCK signals as long as $V_{C45} > V_{REF}$. Same signals are also buffered in Q24, Q25 and are available as a pulse train, -400 mV into 50 ohm at the front panel terminal labelled SCALER. This output

is convenient during adjustment of pulse amplitudes applied to the ADC, see Fig. 19 of TN-71-14.

When C45 is discharged, i.e. $V_{C45} < V_{REF}$, comparator A3 changes states, inhibiting further CLOCK pulses from being applied to the binary counter. The trailing edge of the comparator output actuates the CLAMP FF which inhibits the peak-detector (see section 3.1.2).

One pilot light, actuated by an OR gate, A12, of weights 2^2-2^7, indicates that DATA are available, the other provides a visual indication of a count $\geq 300_8$, showing that the pulse under measurement is in the upper 25 percent of the total range. These two visual indicators were chosen as a reasonable compromise to aid in setting-up procedures.

The maximum range of the ADC is 255_{10}, thus maximum conversion time is 25.5 μsec. It is advisable to adjust the maximum count to 245_{10} (see section 10.4 of TN-71-14) to avoid ambiguities due to counter overflow.

3.1.4 CLEAR Circuits

Clearing of bi-stable circuits can be accomplished in three ways:

(i) Push-button CLEAR at the front panel of the control module, see section 3.2.

(ii) External CLEAR, requiring a 0 V pulse, 70 nsec minimum, applied to P2-20 of the CONTROL module, the quiescent level being +4.0 V, nominal. This mode is most conveniently used in larger data acquisition systems under computer control.

(iii) Internal CLEAR. In this mode a 250 nsec clear pulse is produced by a monostable, A6 (Fig. 5) at the trailing edge of the STROBE pulse of $>$ 500 nsec duration. During external clear operation this monostable is inhibited via a level from the CONTROL module when switch S1, Fig. 7, is in the "INT. CLEAR" position.

In an experimental situation it is likely that some ADC channels did not receive data, though an event has been recorded which initiates the unclamping of C45. In such a case the ZERO state of the comparator A3 will inhibit any clock pulses from reaching the binary counter. The rising edge of the first clock pulse will set the CLAMP flip-flop, clamping C45 to a slightly negative voltage again.

3.2 Control Module

Refer to block diagram, Fig. 1, and the detailed schematics, Figs. 6 and 7. The CONTROL module generates a 10 MHz CLOCK pulse; an UNCLAMP for the peak-detector of Fig. 4; an INHIBIT level that is required when a CLEAR is generated internally (see section 3.1.4). It also supplies the manual and external CLEAR signals. All control signals originating in the CONTROL module can drive 10 ADC modules.

A description of the circuit follows: A NIM logic input of ≥ 4 nsec duration is amplified in Q1, Q2 and applied to the monostable Q3-Q5. The resultant 0.5 μsec signal removes the CLAMP to allow operation to the peak detector. The trailing edge of the 0.5 μsec pulse actuates delay monostable A2, which in turn starts a 30 μsec gate, generated by A3.

The crystal controlled 10 MHz CLOCK is generated in Q6 and amplified by Q7 and the subsequent gate (1/4 A5). Synchronization of the first CLOCK pulse is effected by D-flip-flop, A4, and the NAND gate following it. This synchronization ensures that the first CLOCK pulse is generated with full width, and improves the statistical accuracy of the A/D conversion by 1/2 bit. The CLOCK is transmitted to the CAMAC bus as long as A3 is ON. Thus no noise is generated in the chassis during the time-interval of integration, amplification and peak detection.

Toggle switch S1, located on the front panel, selects internal or external mode of operation for the CLEAR. Push-button S2 (also on the front panel) provides a MANUAL CLEAR.

4. PERFORMANCE

Fig. 10 shows the number of counts versus amplitude for pulses of 10 nsec duration. The maximum input amplitude for 1% linearity is -1.1 V; however the useful range is to -1.3 V at which point the sharp cut-off characteristics of the limiter (Q12) take over.

For measurement of subnanosecond time intervals, such as in time-of-flight analysis, one applies a signal of standard amplitude and duration to the DATA terminal of the instrument. This input stage together with its linear gate form an overlap-coincidence circuit, the output of which is then integrated and digitized. Fig. 11, Curve A, shows results obtained by moving the GATE signal with respect to the DATA input. A linear dependence from 8 counts to 232 counts is observed when the GATE precedes in time the DATA signal. This is the

preferred mode of operation. The slope is 16.2 counts, i.e., a time resolution of 62 psec/count. Curve B, with 6db attenuation in the DATA path, shows a slope of 7.9 counts/nsec in the linear region between 3 and 230 counts.

Integral linearity in amplitude and time measurements is better than 1%. Differential linearity has not been measured, but the counter-ramp type ADC utilized is compatible with the best differential linearities attainable in A/D conversion. Temperature stability has been measured on one instrument only. The worst TC observed over the range of 20^{o} to 45^{o}C was 0.1% per ^{o}C.

It should be noted that the instrument was developed in 1969 at SLAC, where the low-duty cycle favors ac-coupled design. Rate effects should be examined carefully when considering use of these ADC's on high duty accelerators or in storage rings.

5. SUMMARY OF ESSENTIAL DIFFERENCES BETWEEN THE 7-BIT AND THE 8-BIT ADC'S

HEEP has presently seventy 7-BIT ADC'S SLAC No. 135-009, and forty 8-BIT ADC'S. The respective circuits differ in several details that are summarized in Table 1. There is no difficulty utilizing both circuits in the same system, since a bin-controller is mandatory in any data acquisition system, and such controllers can generate the requisite interface levels. (The data-acquisition system of group G, for instance, has one simple solution to such a situation.) The 8-bit ADC, being of a later design, shows better performance at a lower cost ($\approx$ 30%) in components and labor.

6. ADDITIONAL INFORMATION

SLAC-TN-71-14 is a supplement to the present note and includes information that may be of use for calibration, adjustment, repair, and systems utilization. Documentation for production is available from SLAC Document Control.

Table 1. Summary of Essential Differences Between 8-Bit and 7-Bit ADC's.

	8-Bit ADC	7-Bit ADC
Mechanical packaging	CAMAC	NIM, plus daisy-chain for bussing of data and control signals
Resolution	8-Bits	better than 7-bits
Gate pedestal	One adjustment, better stability	Two adjustments
Voltage regulation for gate and amplifier	+20V, -20V. Temp coeff. over 15^{o} to 45^{o}: 2 x 10^{-3}%/^{o}C, typical.	None
Matched FET's	Not Used	Two sets required
Internal CLEAR	Derived from trailing edge of STROBE	All modules cleared simultaneously by subsequent event pulse.
Synchronization of first CLOCK pulse	Yes, improves statistical accuracy by 1/2 bit	N_0
Fan-out	Requires 11-fold F.O.	F.O. part of CONTROL module.
Outputs, DATA	Open collector, TTL. O to +0.5 V for logic "1", +3.5 to +5.5 V for logic "0", presented on CAMAC READ lines R1-R8	Saturated switch, capable of driving 100 Ohm loads. +4V nominal for logic "1"; OV for logic 0 (open collector)
Output, Scaler	-400 mV into 50 Ohms, dc coupled	-200 mV into 50 Ohms, ac coupled
Sensitivity	0.99 pC/count	1.2 pC/count
Time measurements (Standard NIM inputs)	16.2 counts/ns	12.6 counts/ns

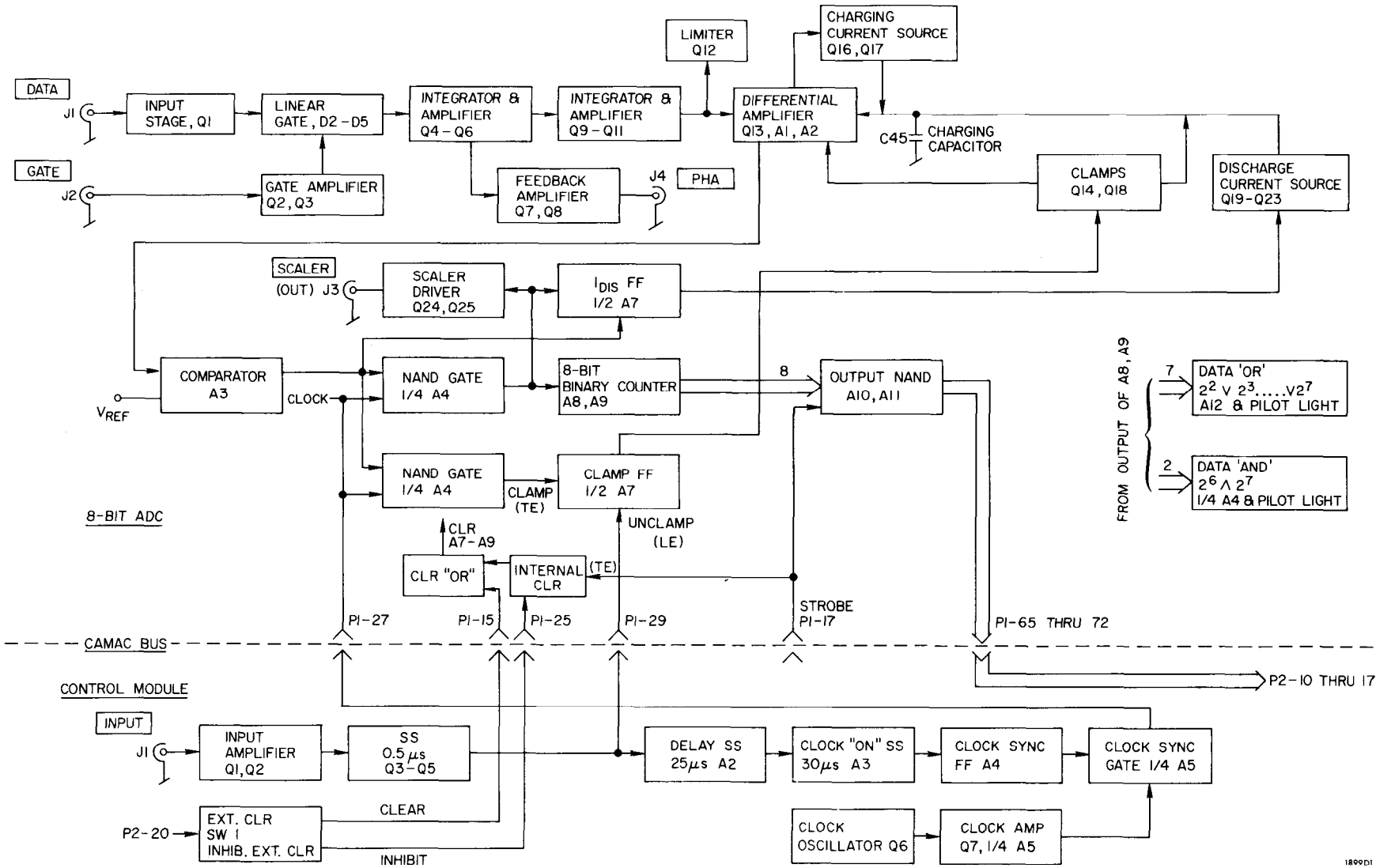

Fig. 1

8-bit ADC and CONTROL module. Block diagram.

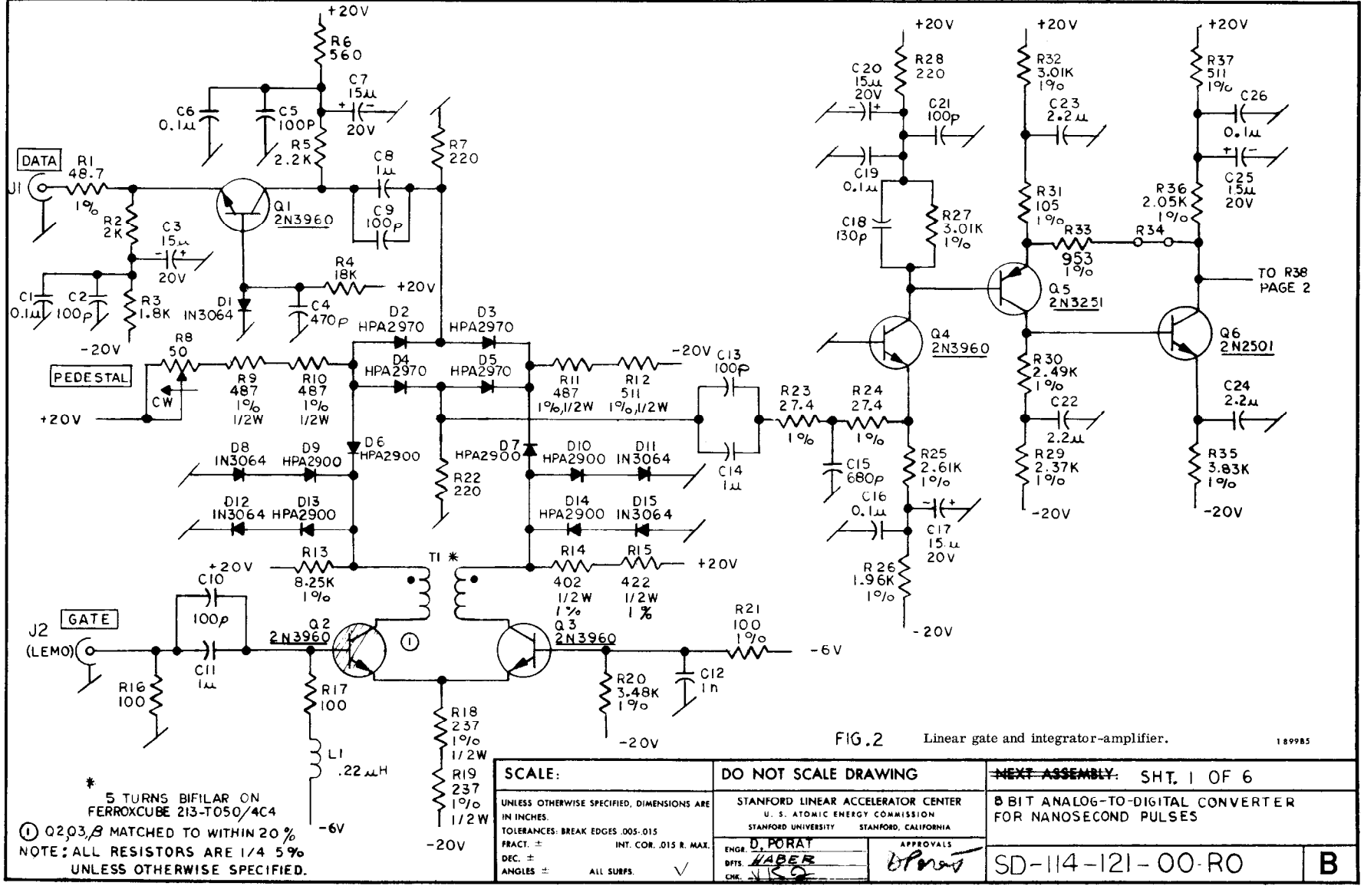

FIG. 2 Linear gate and integrator-amplifier.

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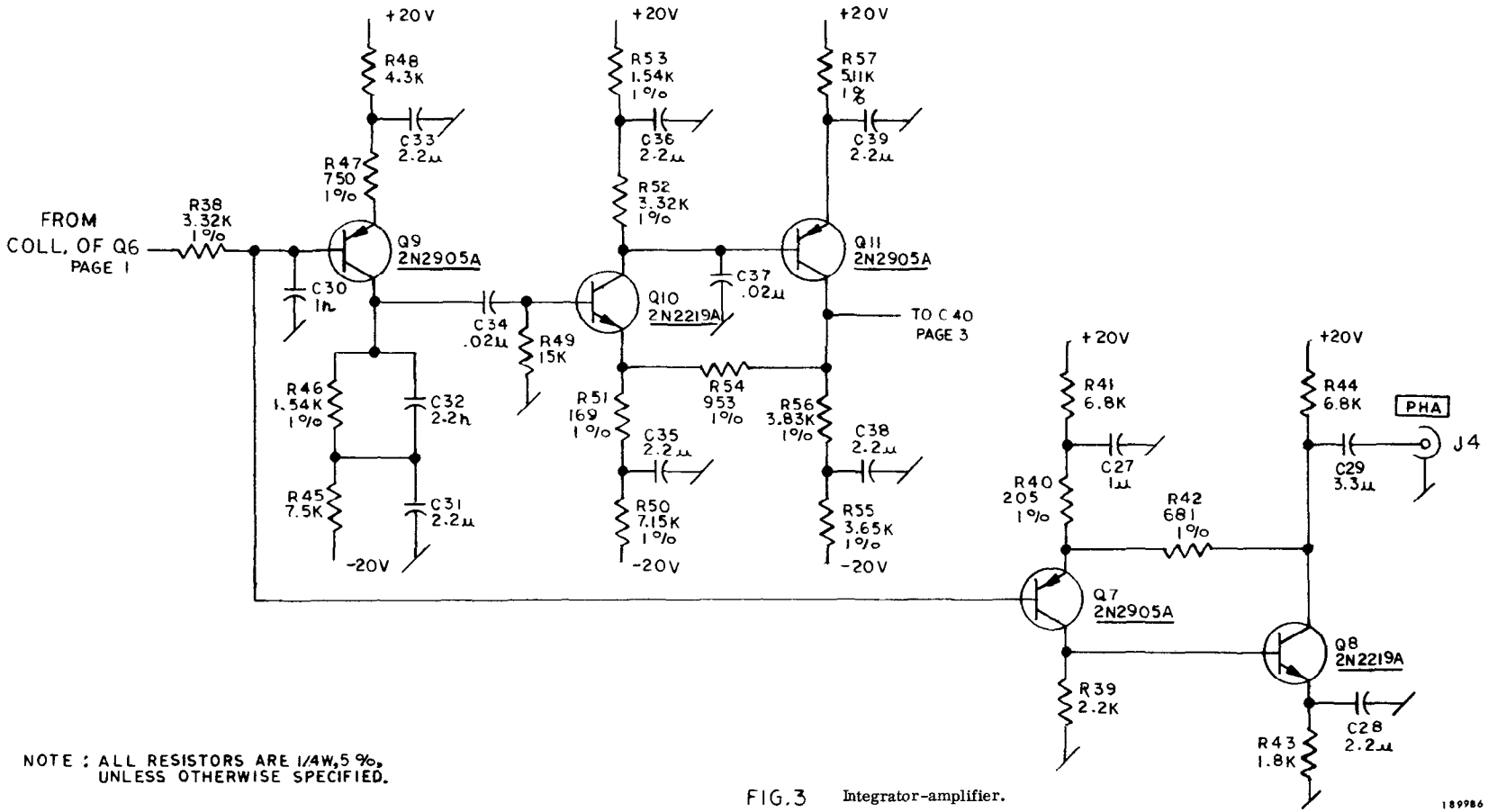

NOTE : ALL RESISTORS ARE 1/4W, 5 %, UNLESS OTHERWISE SPECIFIED.

FIG. 3 Integrator-amplifier.

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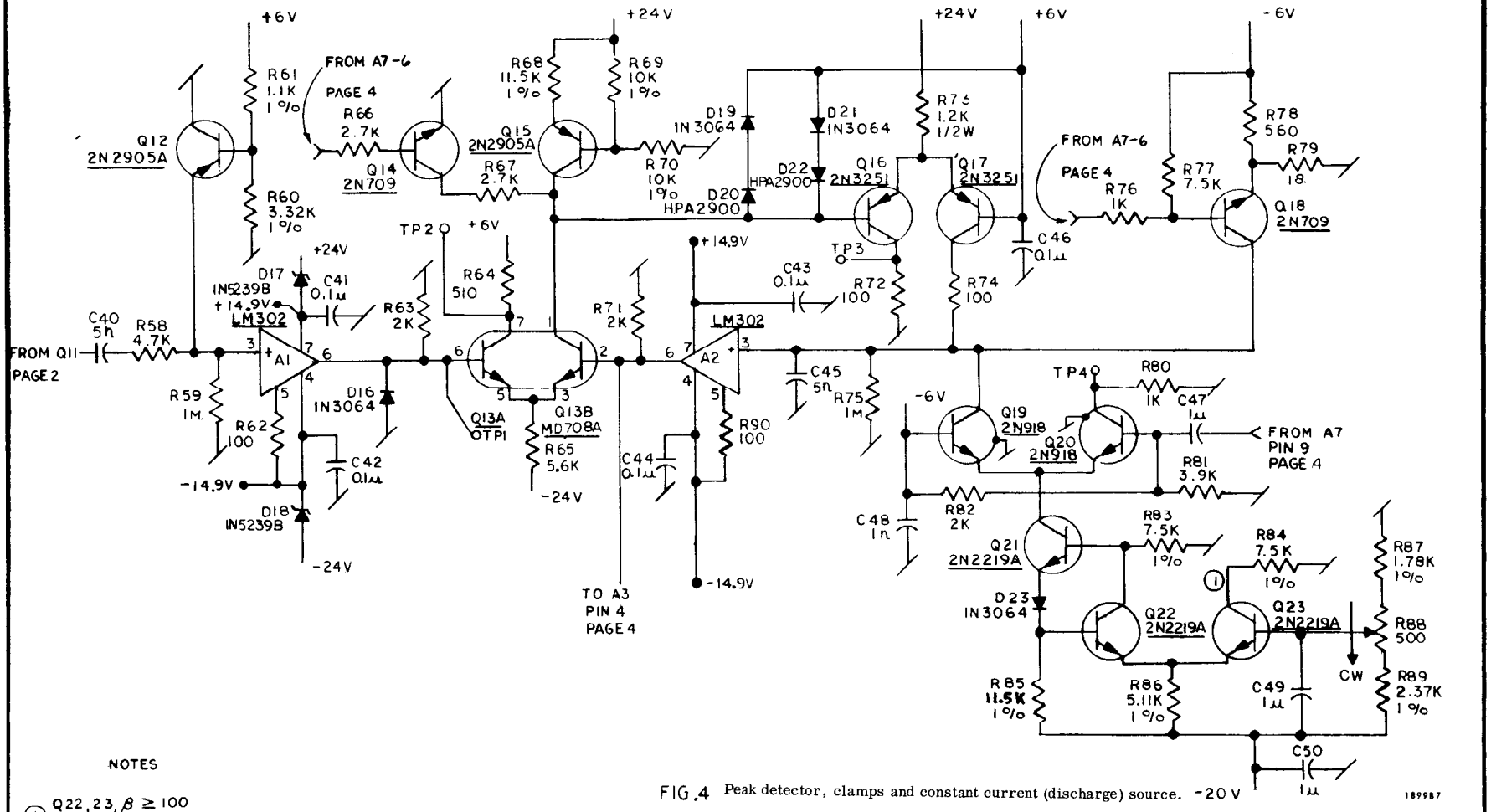

FIG. 4 Peak detector, clamps and constant current (discharge) source. -20 V

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NOTES

(1) Q22, 23, $\beta \geq 100$ MATCHED TO WITHIN 20 %

ALL RESISTORS ARE 1/4W, 5 %, UNLESS OTHERWISE SPECIFIED.

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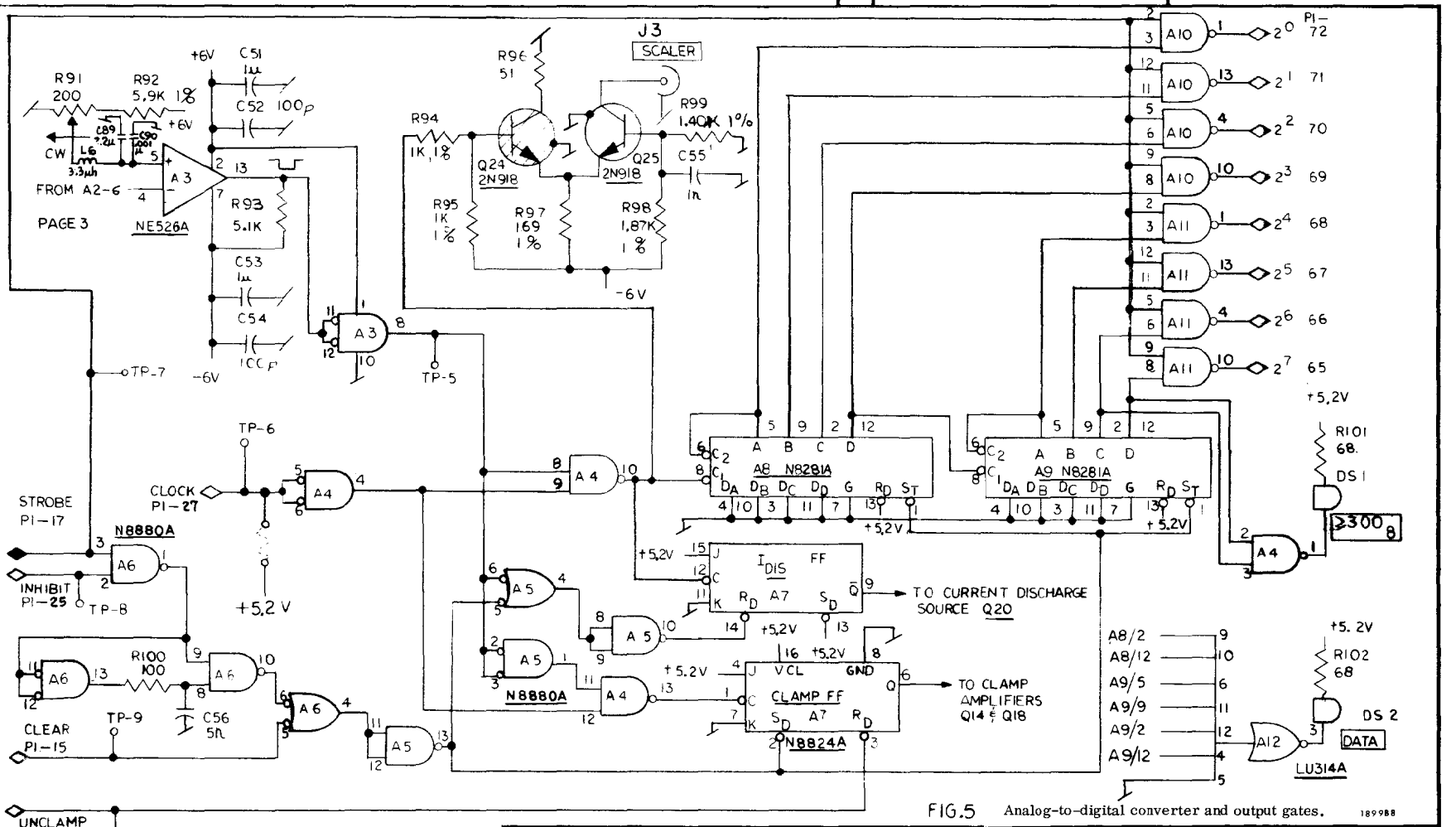

FIG.5 Analog-to-digital converter and output gates. 189988

NOTES:

1. A4 A5 AND A6 ARE N8880A.
2. A7 IS N8824B, A10 & A11 ARE N8881A
3. ALL RESISTORS ARE 1/4W, 5% UNLESS OTHERWISE SPECIFIED.
4. PIN 14 TO +5.2V ON ALL I.C.'S. PIN 7 TO GND EXCEPT A3 & A12.
5. A12 PIN 8 TO +5.2V. PIN 1 TO GND.

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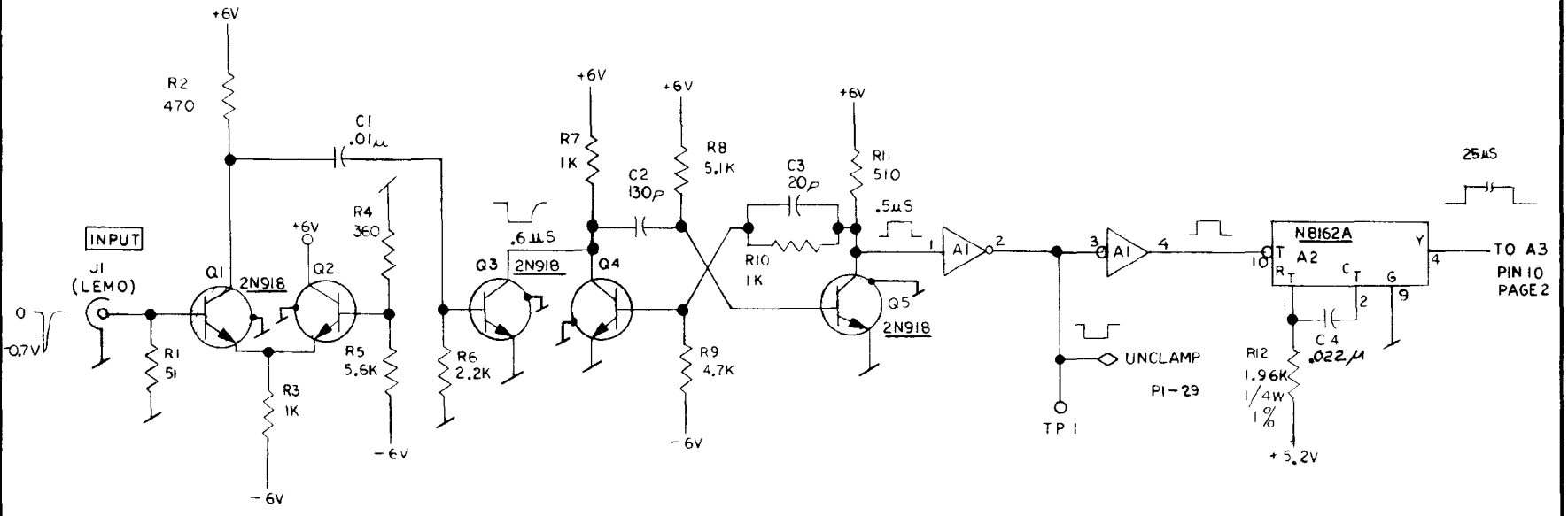

FIG. 6

CONTROL module. Input stage, stretcher and UNCLAMP.

NOTES:

1. A1 IS SN7404N, A5 IS N8880A
2. A2 & A3 ARE N8162A.
3. A4 IS N8828A.
4. PIN 14 TO +5.2V
   PIN 7 TO GND ON ALL IC'S.
5. ALL RESISTOR ARE 1/4 W, 5%, UNLESS OTHERWISE SPECIFIED.

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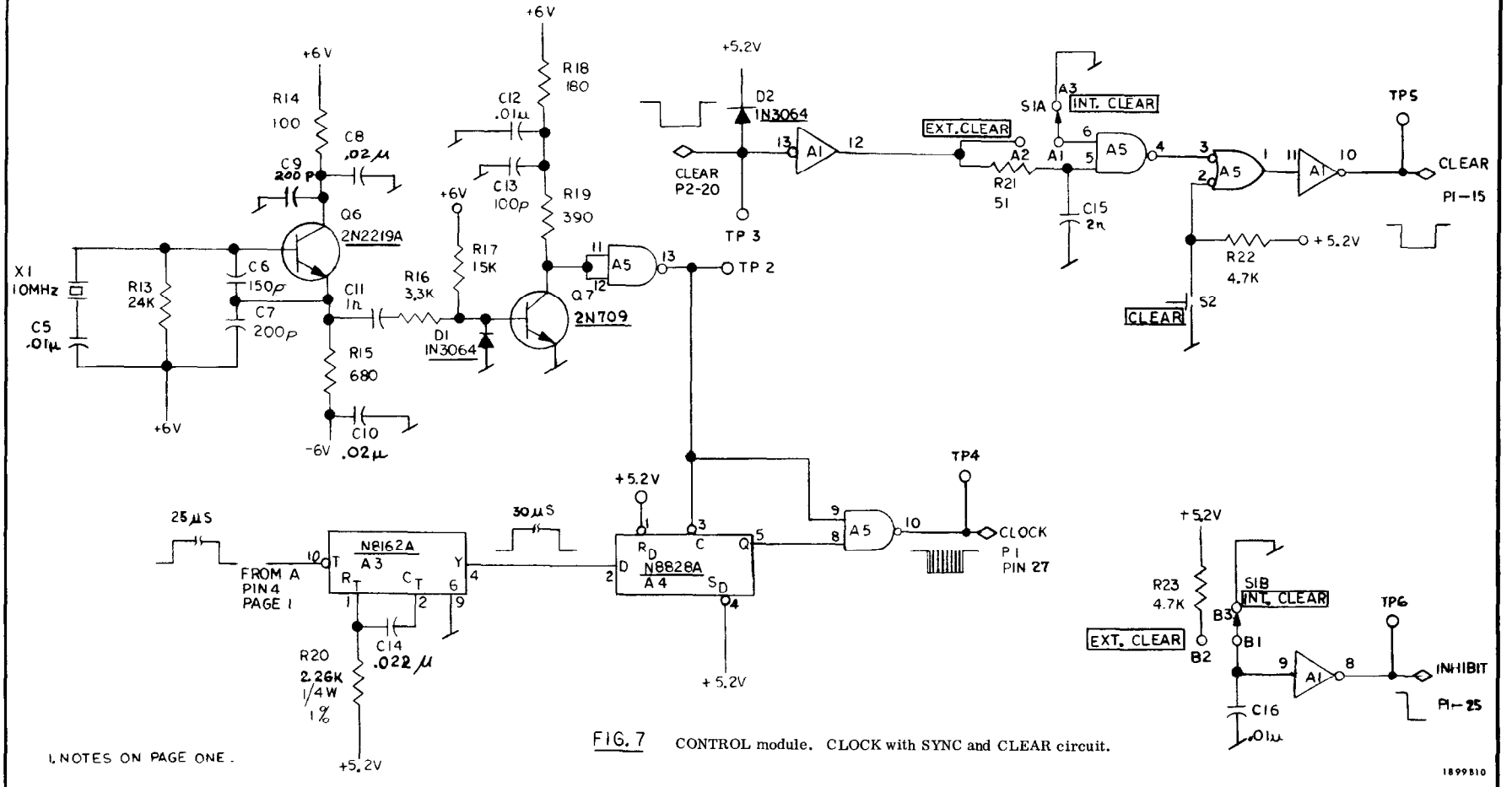

FIG. 7 CONTROL module. CLOCK with SYNC and CLEAR circuit.

1. NOTES ON PAGE ONE.

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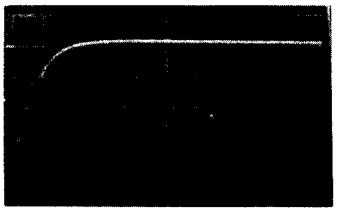
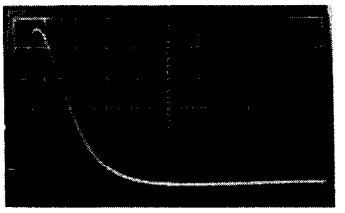


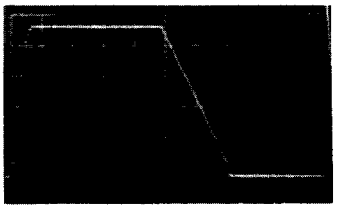
5 μsec/div.
0.5 V/div.

Fig. 8 Output at PHA terminal.
Hor.: 5 μsec/div
Vert.: 0.5V/div



5 μsec/div.
0.5 V/div.

Fig. 9a Input to peak-detector, test point TP-1.
Hor.: 5 μsec/div
Vert.: 0.5V/div



5 μsec/div.
0.5 V/div.

Fig. 9b

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Peak-detector output, V_{C45}.
Hor.: 5 μsec/div
Vert.: 0.5V/div

Flat top is due to peak-detector long time constant. Trailing ramp results from the linear discharge current source. Note the negative step at the end of the ramp caused by clamping action.

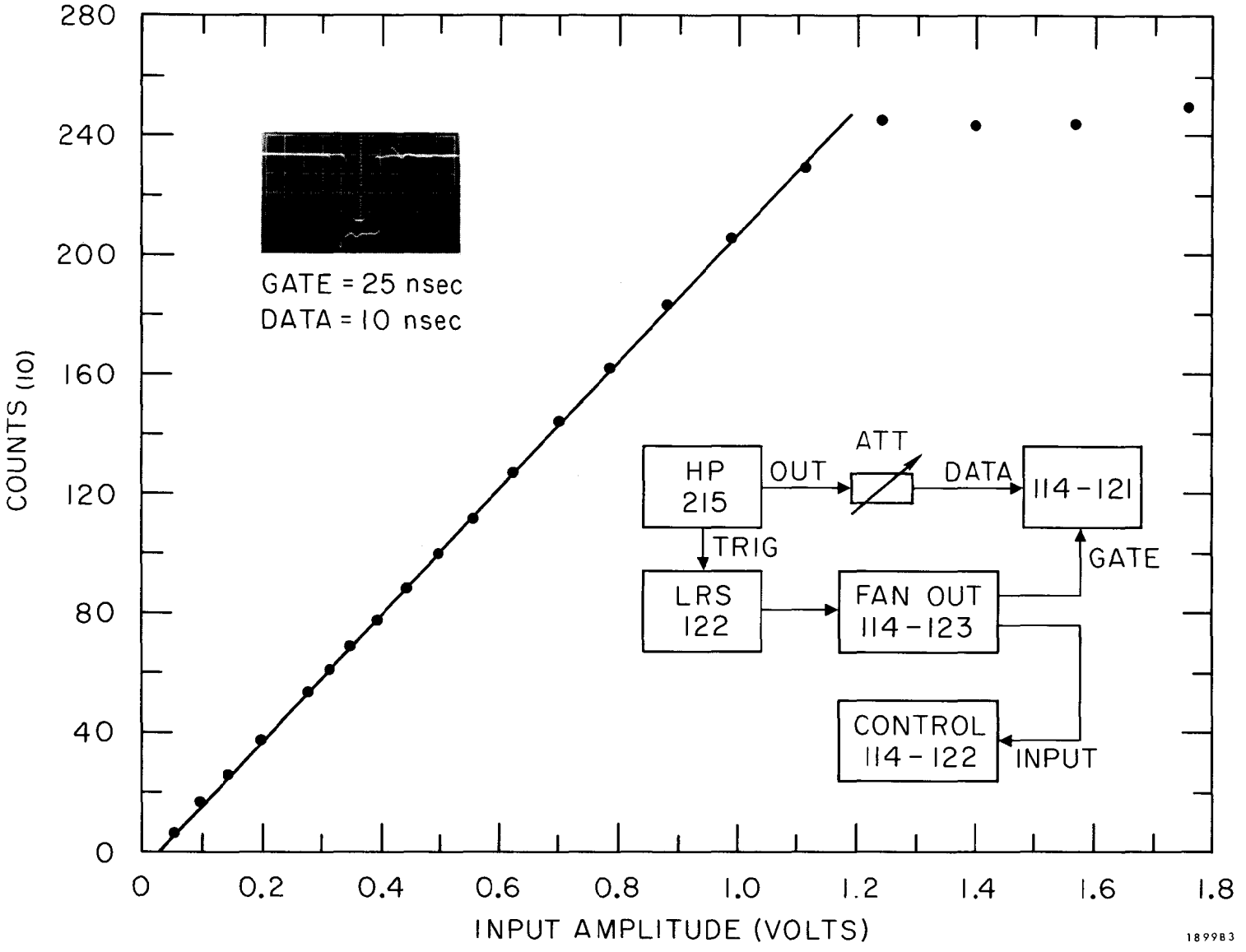

Fig. 10 Number of counts versus input amplitude of constant width. GATE = 25 nsec; DATA = 10 ns.

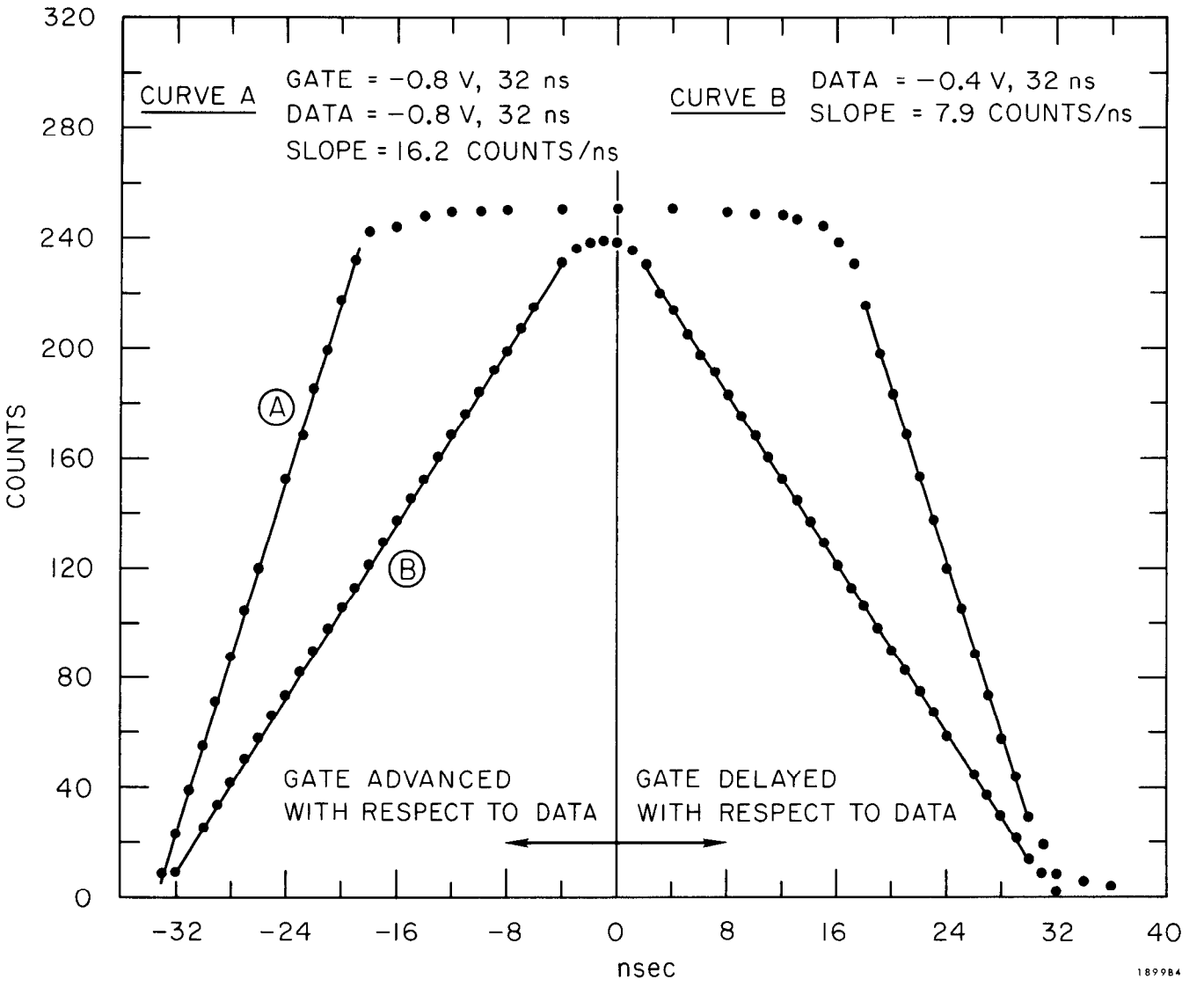

Fig. 11 Number of counts versus overlap-coincidence between GATE and DATA, each of 32 nsec duration.

Curve A: DATA = -0.8V, Slope = 16.2 counts/ns
Curve B: DATA = -0.4V, Slope = 7.9 counts/ns

Note: DATA delayed with respect to GATE is shown as negative time on the horizontal scale. This is the preferred mode of operation.