Final Acceptance of the DMILL Technology Stabilized at TEMIC/MHS.

M. Dentan, P. Abbon, P. Borgeaud, E. Delagnes, N. Fourches, D. Lachartre, F. Lugiez, B. Paul, M. Rouger; *CEA-DSM-DAPNIA Saclay, F-91191 Gif-sur-Yvette, France.*

R. Truche, J.P. Blanc, O. Faynot, C. Leroux, E. Delevoye-Orsier, JL. Pelloie, J. de Pontcharra; *CEA - Technologies Avancées - LETI, F-38054 Grenoble Cedex 09, France.*

O. Flament, JM. Guebhard, JL. Leray, J. Montaron, O. Musseau, A. Vitez; *CEA - Centre d'Etudes de Bruyères-le-Châtel, F-91680 Bruyères-le-Châtel, France.*

C. Le Mouellic, M. Carcaud, T. Corbière, A. Dantec, G. Festes, J. Martinez, K. Rodde *TEMIC / MHS S.A., La Chantrerie, B.P.70602, 44306 Nantes Cedex 03, France.*

Abstract

DMILL technology integrates mixed analog-digital very rad-hard (>10 Mrad and $>10^{14}$ neutron/cm^2) vertical bipolar, 0.8µm CMOS and 1.2 µm PJFET transistors on SOI substrate. In this paper, after recalling the DMILL program goal, we summarize the main milestones from the R&D to the industrial implementation, the main technological choices, and the main results obtained after stabilization of the final process-flow at MHS.

I. Goal of the DMILL program

The goal of the DMILL program is to provide the High Energy Physics (HEP) community, space industry, nuclear industry, and other applications, with an industrial very rad-hard mixed analog-digital microelectronics technology.

II. Main milestones from the R&D to the industry

The DMILL microelectronics technology was developed by the CEA (French Atomic Energy Agency) with the collaboration of IN2P3 (French Nuclear Physics and Particle Physics Institute) between 1990 and 1995 [1-10]. DMILL was presented to the CERN DRDC (Detector R&D Committee, the former LHC Electronics Board) in 1992, and was accepted by this Committee with two requests : 1/ open an access to DMILL for the HEP community as soon as possible, and 2/ transfer DMILL to the industry. Between 1993 and 1996, the CEA processed 7 DMILL « multi-project wafers » (MPW) batches open to all the laboratories participating in the LHC program, so that they could thus start the development of numerous circuits dedicated to ATLAS and CMS. In mid 1995, the DMILL process was stabilized at LETI (the CEA R&D laboratory, in Grenoble, France). In September 1995, the CEA and MHS signed a contract for the industrial transfer and fabrication of DMILL in the 6'' silicon foundry of MHS at Nantes. MHS, which is part of the TEMIC group, was initially held by Lagardère (France) and Daimler-Benz (Germany), and was purchased at the beginning of 1998 in totality by the US semiconductor manufacturer ATMEL. TEMIC/MHS is now the main center of expertise for ATMEL defence and space technologies. In spring 1997, DMILL was stabilized at 95% at the Nantes production plant [11-15] and MHS decided to open this technology to HEP laboratories so that they could continue and complete the development of their circuits before mass production. The last 5% of corrections were made during the period spring 97 - spring 98, leading to the final process-flow.

In spring 1998, MHS processed several batches using the final process-flow. Series of thorough characterizations made in summer 1998 by the CEA and MHS on these batches give fully satisfactory results. The compilation of the extensive measurements made on these batches together with those made on all the previous batches (43 DMILL batches were processed by MHS between spring 96 and summer 98) shows that all the parameters of DMILL technology stabilized at MHS now completely fulfil the specifications based on LHC requirements and previously obtained at LETI. These excellent results enabled the CEA to announce the official final acceptance of the industrial transfer of DMILL to MHS during the LEB 98 Workshop.

III. Recall of the technological choices

DMILL uses an SOI substrate which significantly reduces the sensitivity of the circuits to transient irradiation effects such as parasitic currents or memory cell upsets [17-19] induced by the passage of single ionizing particles.

The DMILL CMOS transistors are separated by a dielectric trench and by the buried oxide ; this dielectric

insulation definitively eliminates any possibility of latch-up (triggering of a parasitic thyristor structure constitued by the juxtaposition of two complementary MOS transistors ; this phenomenon, initiated in standard technologies by the passage of single ionizing particles, results in circuit malfunctions and, in some cases, in their definitive destruction).
The 0.8-µm CMOS and the vertical bipolar transistor of DMILL provide the advantages of present BiCMOS technologies. The PJFET transistor is used for a number of low-noise or low-temperature applications.
The CMOS structure was designed to obtain very high hardness to total ionizing dose (> 10 Mrad) and a low noise level. This type of transistor, which uses majority carriers, is naturally hardened to neutrons.
The bipolar transistor uses a vertical structure which provides both high neutron hardness (> 1E14 n/cm2) and high speed operation. Its structure was also carefully optimized to obtain high hardness to ionizing radiation (> 10 Mrad).
The PJFET transistor, which uses majority carriers and whose intrinsic operation does not involve oxides, has low sensitivity to ionizing radiations and to neutrons. Its structure was optimized to obtain an extremely high hardness to these radiation types (>> 10 Mrad and > 1E14 n/cm2).
For analog applications, DMILL integrates two capacitor and two resistor families, both radiation hardened.
DMILL also integrates rad-hard anti-ESD devices, specifically designed for protection of either analog or digital circuits.
The interconnections can be made with two metal layers whose minimum dimensions are those of a 0.6-µm technology, and with a low resistivity polysilicon layer.
The design rules for the components and their interconnections were optimized to obtain a high integration density, which is comparable to that of present 0.8-µm non rad-hard pure-CMOS technologies.

IV. Final acceptance of the industrial transfer

By mid 1997, the industrial transfer was completed and the process-flow was stabilized at 95%. The last corrections made between mid-97 and mid-98 to obtain the final process-flow are :

- Adjustment of the value of the high value resistor « RSRHV » ;
- Addition of a new rad-hard high value resistor « R_{ext} » (improved radiation hardness);
- Corrections to the bipolar transistor (improvement of the radiation hardness and of Vearly) ;
- Elimination of yield problems (which were due to polysilicon residues) ;
- Improvement of the final DMILL Design Kit.

The final acceptance of the industrial transfer is the last step foreseen in the contract signed by the CEA and MHS in 1995. This final acceptance is based on the results of extensive measurements made of several batches manufactured with the final process-flow, and on all the measurements made of all the previous MHS batches. The criterion used to analyse these results is the technical specification file, based on the complete set of measurements made on DMILL technology stabilized at LETI. The measurements and checking required to decide the final acceptance of the transfer are distributed in the 11 following steps :

1. Statistical Process Control (SPC);
2. Electrical parameters;
3. Radiation hardness;
4. Transistors and OTAs noise (pre-rad and post-rad);
5. Characterization and yield of demonstrator circuit ;
6. Characterization of anti-ESD devices ;
7. Electromigration tests ;
8. Hot carriers ageing tests ;
9. Oxide breakdown tests ;
10. Approval of the final process-flow ;
11. Approval of the final design kit.

In the following, all these measurements or checking steps are briefly described and the main results are summarized :

1. Statistical Process control.
SPC enables the verification and control of the critical technological parameters which govern the electrical, noise and radiation hardness characteristics. More than 120 parameters are measured during and after processing for each batch. All the SPC parameters obtained for batches made using the final process-flow are fully within the specifications.

2. Electrical parameters.
More than 90 electrical parameters are measured on several sites on each wafer, in each batch. All the parameters obtained for batches made using the final process-flow comply with the specifications. Figures 1 and 2 give an illustration of the stability of these parameters for successive batches, after initial adjustments made on the first batches.

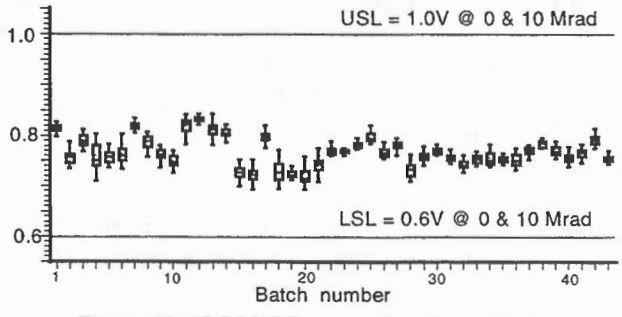

Fig.1 : NMOS Vt(V) versus batch number.

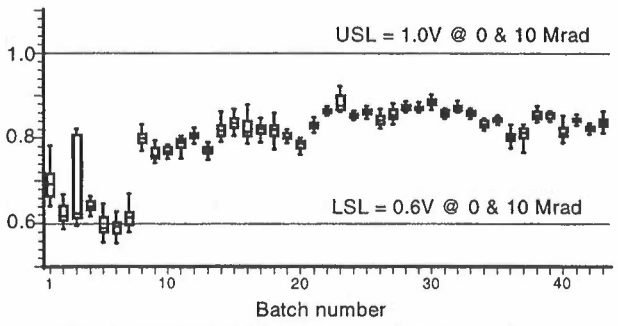

Fig.2 : PMOS IVtI (V) versus batch number.

LSL and USL are respectively the Lower Specified Limit and the Upper Specified Limit.

3. Radiation hardness.

The most sensitive static parameters of each active and passive device are measured before and after irradiation (10 Mrad, 1E14 n/cm2) ; values of the most significant of these for several batches are shown in figures 3 to 8 (arbitrary batch numbers are used in the X-axis).

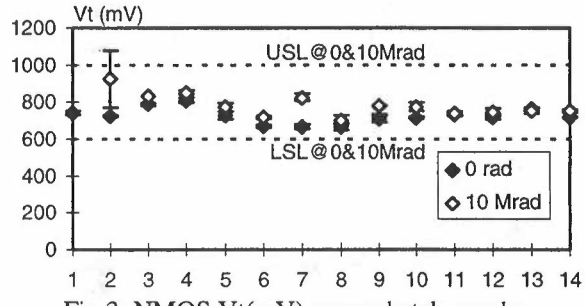

Fig.3. NMOS Vt(mV) versus batch number

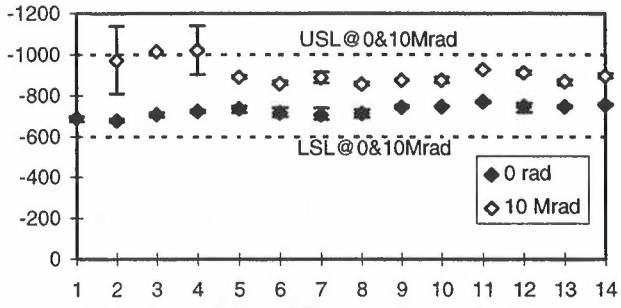

Fig.4 PMOS Vt(mV) versus batch number

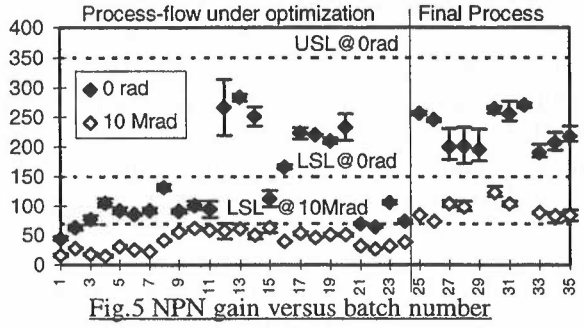

Fig.5 NPN gain versus batch number

For the bipolar transistor, to ensure that the final gain after 10 Mrad + 1E14 n/cm2 is sufficiently high, the specific minimum gain after 10 Mrad and before neutron irradiation is LSL@10Mrad = 70 (Ic = 10 µA). The left side of figure 6 corresponds to non optimized bipolars : the initial post-rad and pre-rad gains were below the specified values, respectively LSL@0rad and LSL@10Mrad. After several experiments, the difference between LETI and MHS equipment responsible for these insufficient gains was ascertained and the subsequent corrections gave the required pre-rad and post-rad gain, as shown in the right side of Fig.6 (final process-flow).

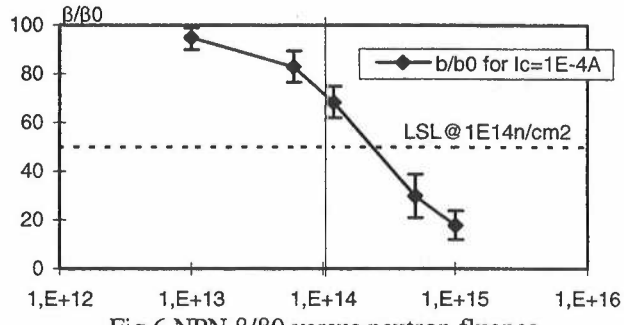

Fig.6 NPN β/β0 versus neutron fluence

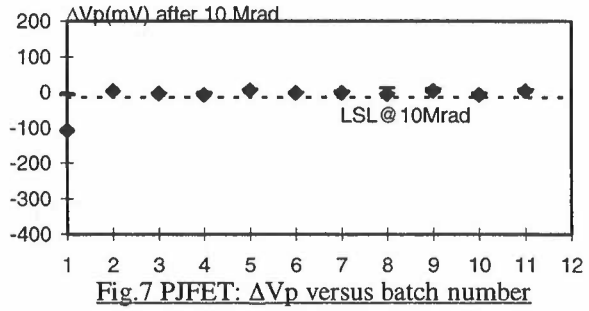

Fig.7 PJFET: ΔVp versus batch number

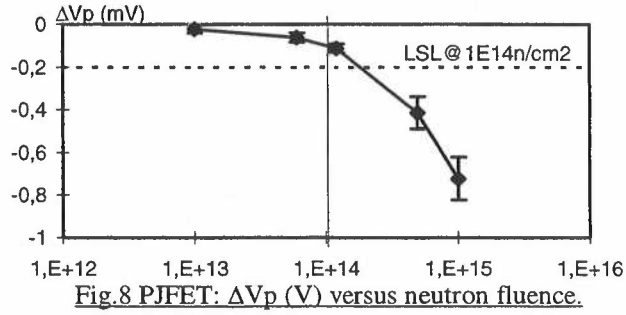

Fig.8 PJFET: ΔVp (V) versus neutron fluence.

The new high value resistor R_{ext} , which was made available to users in Summer 1998, was also measured before and after 10 Mrad. This resistor has a high radiation hardness: $\Delta R_{ext}/R_{ext}$ = +6.5% after 10 Mrad.

It is not possible to describe all the results obtained in radiation hardness tests in this paper. To summarize, here again all the values of the radiation hardness parameters measured on batches made using the final process-flow are within the specification limits.

4-a. Individual transistors noise.

Input noise spectral density is measured before and after irradiation on each type of transistor for various sizes and various biasing conditions [14]. Figures 9 to 16 show the pre-rad and post-rad noise spectral density ($nV/Hz^{1/2}$) versus Frequency (Hz) measured on the 4 types of DMILL transistors. The dotted lines correspond to the worst cases obtained with the stabilized DMILL-LETI process. The noise spectral density measured on batches made with the stabilized DMILL-MHS process-flow is consistent with that measured on batches issued from the stabilized DMILL-LETI process.

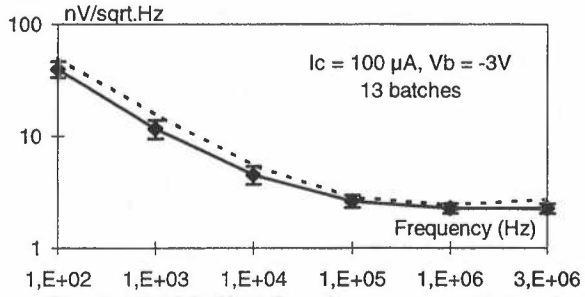

Fig. 9: NMOS 5000/3, noise spectrum @ 0 rad

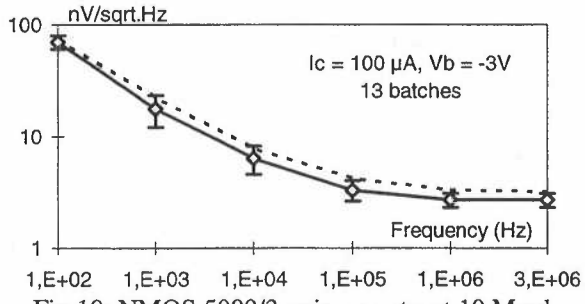

Fig.10: NMOS 5000/3 noise spectr. at 10 Mrad

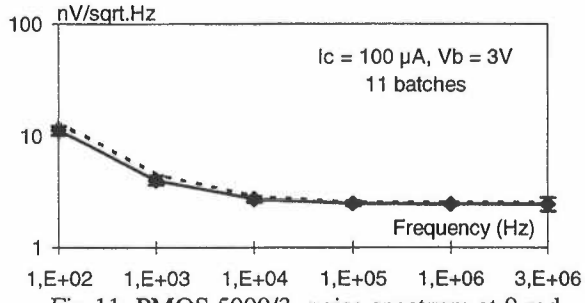

Fig.11: PMOS 5000/3, noise spectrum at 0 rad

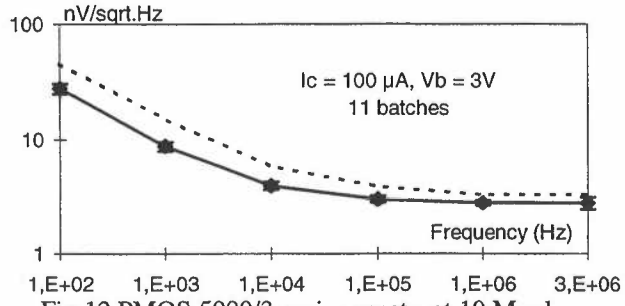

Fig.12 PMOS 5000/3, noise spectr. at 10 Mrad

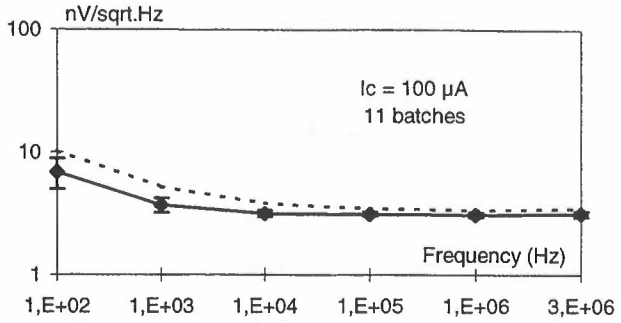

Fig.13 NPN 1.2x1.2 noise spectrum @ 0 rad

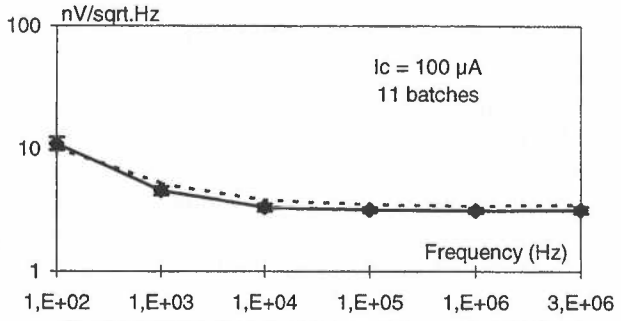

Fig.14 NPN 1.2x1.2 noise spectrum @ 10 Mrad

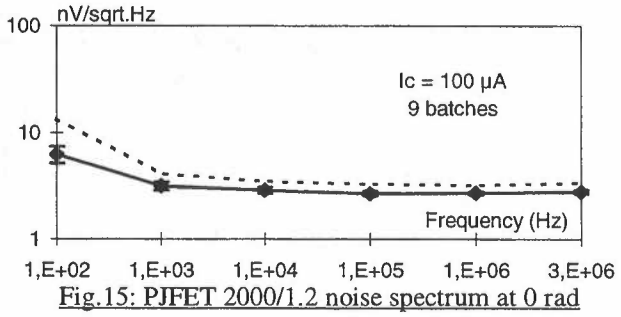

Fig.15: PJFET 2000/1.2 noise spectrum at 0 rad

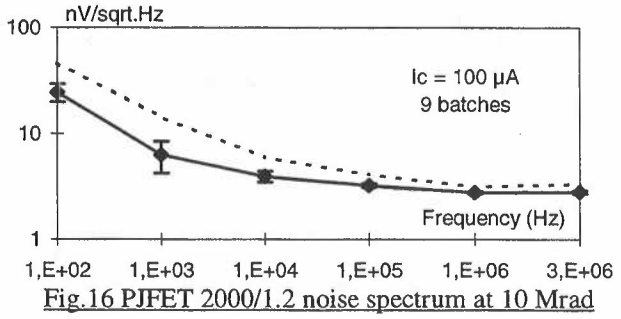

Fig.16 PJFET 2000/1.2 noise spectrum at 10 Mrad

4-b. Operational Transimpedance Amplifiers noise.

ENC is measured on several OTAs designed with various input transistors (NMOS, PMOS, NPN and PJFET). Results obtained for batches from the final DMILL-MHS process-flow are fully consistent with those obtained for DMILL-LETI batches and with individual transistors noise measurements.

5. Characterization and yield of demonstrator circuits.

The goal of this step is to validate the technology by electrical characterization and yield measurement on a

circuit as representative as possible of mixed analog-digital circuits developed for LHC applications. The demonstrator circuit DEMDSM (49,000 transistors, 28 mm2) [14] used for this validation is constructed around a high dynamic range switched capacitor analog memory HPSALM initially developed for ATLAS calorimetry. Some extra-logic has been added to make it self-testable. Table I shows that the main characteristics of this circuit, manufactured using the final DMILL-MHS process-flow, are very similar to those obtained for the reference circuit made in 1995 using the DMILL-LETI stabilized process-flow. The typical yield obtained with this circuit manufactured with the final DMILL-MHS process-flow is about 60%.

Technology	DMILL-LETI	DMILL-MHS	DMILL-MHS
Total dose	0 rad	0 rad	10 Mrad
Max. Freq.	65 MHz	60 MHz	55 MHz
Consumption @40MHz	460 mW	420 mW	310 mW
Droop rate	20 mV/s	40 mV/s	260 mV/s

Table I.

6. Anti-ESD (ElectroStatic Discharges) devices.
Three families of rad-hard anti-ESD devices are available in DMILL : one for digital input, one for digital output, and one for analog input. Measurements based on the Human Body Model (HBM) show that these devices efficiently protect input or output pads up to 4000V.

7. Electromigration tests.
The goal of these tests is to assess the reliability of metal interconnections stressed by high current density. Their results are in conformity with MHS standards.

8. Hot carriers ageing tests.
The goal of these tests is to measure accelerated ageing of CMOS devices. Their results are in conformity with MHS standards.

9. Oxide breakdown tests.
The goal of these tests is to assess the reliability of CMOS gate oxide under a high electrical field. Their results are in conformity with MHS standards.

10. Approval of the final process-flow.
The DMILL-MHS process-flow is an exact copy of the initial DMILL-LETI process-flow, except for a few adaptations made to take into account certain specific features of the equipment used by MHS. These adaptations were studied by MHS in collaboration with the LETI in order to preserve the structure and properties of all the DMILL components. After an in-depth analysis of the final DMILL-MHS process-flow, the LETI found it to be in conformity with the initial DMILL-LETI process-flow and has approved it.

11. Approval of the final design kit .
A new revision of the DMILL design kit (DDK) was completed by the CEA and MHS in summer 1998. It includes the following improvements :

- R_{ext} simulation parameters ;
- Extraction tools for R_{ext} ;
- Simulation parameters of the new NPN ;
- Extraction of buried oxide (BOX) capacitances ;
- Simulation of parasitic BOX capacitive couplings ;
- Guidelines for reducing the effects of these capacitive couplings;
- Device matching parameters.

Table 2 gives an excerpt of the matching parameters which illustrates the very good matching of the new R_{ext}. NPN and CMOS also exhibits good matching parameters. The values of sigma for the CMOS transistors are refered to transistors designed with a gate width W = 1 µm and a gate length L = 1 µm, and scale as $(WL)^{-1/2}$.

Device	**Dose**	**Parameter**	**unit**	**sigma**
R_{ext}	0 rad	resistance	%	0.24
R_{ext}	10 Mrad	resistance	%	0.22
NPN 1.2x10	0 rad	gain	%	4.0
NPN 1.2x10	0 rad	Vbe	mV	0.21
NMOS	0 rad	Vt	mV*µm	14.3
PMOS	0 rad	Vt	mV*µm	23.3

Table 2.

This new DDK is available immediately at MHS and will be available on CD-ROM via IMEC in November.

V. Qualification and Quality Assurance

An initial qualification of DMILL technology was made by MHS in October 1997 [16]. To take into account the corrections made in the process from mid-1997 to mid-1998, an additional qualification was carried out by MHS in june 1998. DMILL is today a fully qualified MHS process.

The quality assurance performed by MHS for DMILL includes three procedures [14]:

1. The standard quality assurance procedures applied to each DMILL batch. These procedures are mainly based on the Statistical Process Control (SPC) tools, on the Process Traceability tools, and on the Control of Process Changes rules. These tools and rules are common to all MHS technologies.

2. The radiation hardness monitoring was specifically studied [13, 14] and developed by the CEA for DMILL, and transfered to MHS. This monitoring consists in ionizing irradiation and measurements made of test structures up to 10 Mrads using a 10-keV RX ARACOR irradiation machine, and in neutron radiation-hardness tests made on test structures through electrical measurements. These tests made on each batch enable MHS to guarantee that each delivered wafer has a radiation hardness of 10 Mrad and 1E14 n/cm2.

3. The noise monitoring was also specifically studied and developed by the CEA for DMILL and transfered to MHS. This monitoring consists in noise spectral measurements made before irradiation and after 10 Mrads on elementary test structures for various sizes and various biasing conditions [14]. These measurements made on three batches per year enable MHS to maintain the noise characteristics within the specified limits.

VI. Summary

The DMILL rad-hard mixed analog-digital technology was developed between 1990 and 1995 by CEA with the collaboration of IN2P3, and transfered to TEMIC/MHS from 1996 to mid-1998. After stabilization of the process, series of thorough measurements made by the CEA and MHS show that all the parameters of DMILL stabilized at MHS completely fulfil the specifications. The compilation of these results together with those obtained for all the previous DMILL-MHS batches have enabled the CEA to certify officially the final acceptance of the industrial transfer and stabilization of DMILL at MHS.

DMILL is now a qualified process, manufactured and commercialized by MHS with a quality assurance, including radiation hardness and noise monitoring, which completely fulfils LHC requirements.

Numerous circuit developed since 1993 for the LHC by several laboratories with DMILL-LETI and then DMILL-MHS, give very satisfactory results which demonstrate the good adaptation of this technology to LHC applications [20-45]. Various circuits are also under development for the space, nuclear civilian industry, and other applications.

VIII. Acknowledgments

We wish to thank all the laboratories of the HEP community which have contributed to the development of this technology by their circuit developments, by the studies they have made of this technology, and by their very usefull technical discussion and suggestions.

We especially wish to thank the CERN for the development of the first DMILL digital library.

We also are very gratefull to the following for the valuable assistance they provided in carrying out the DMILL-LETI MPWs in 1996 :

- IN2P3-CNRS (France) ;
- University of Pavia (Italy) ;
- CERN (Switzerland) ;
- University of Basel (Switzerland) ;
- Paul Scherrer Institut - PSI (Switzerland).

IX. References

[1] "PJFET on SIMOX for Rad-Hard Analog Devices", E. Dupont-Nivet et al.,IEEE International Conference on SOS/SOI Technology, Key West, Florida, October 1990.

[2] "A Mixed Analog-Digital Radiation-Hard Technology for High Energy Physics Electronics: DMILL (Durci Mixte sur Isolant Logico-Linéaire)", M. Dentan et al., R. Truche et al., E.Dupont-Nivet et al., R&D Proposal, CERN/DRDC/92-32/P42, may 92.

[3] "A hardened technology on SOI for Analog Devices", E. Dupont-Nivet et al., IEEE TNS, Vol.39, N°3, June 1992.

[4] "DMILL (Durci Mixte sur Isolant Logico-Lineaire), a Mixed Analog-Digital Radiation Hard Technology for High Energy Physics Electronics", M. Dentan et al., R. Truche et al., O. Flament et al., Nuclear Physics B - (Proc. Suppl.) 32 (1993), North Holland, May 1993.

[5] "DMILL, A Mixed Analog-Digital Radiation-Hard Technology for High Energy Physics Electronics", M. Dentan et al., R. Truche et al., O. Flament et al., L. Blanquart et al., CERN/DRDC/93-45, DRDC/RD29 Status Report, 19 October 1993.

[6] "Study of a CMOS-JFET-Bipolar Radiation-Hard Analog-Digital Technology Suitable for High Energy Physics Electronics", M. Dentan et al., R. Truche et al., O. Flament et al., L. Blanquart et al., IEEE TNS vol.40, N°6, dec.1993.

[7] "Radiation Effects on SOI Analog Devices Parameters", O. Flament et al., IEEE Transaction on Nuclear Science Vol. 41, N°4, June. 1994.

[8] "Study of proton radiation effects on analog IC designed for High Energy Physics in a BiCMOS-JFET rad-hard technology", L. Blanquart et al., M. Dentan et al., R. Truche et al., O. Flament et al., IEEE TNS, Vol. 41, N°6, Dec. 1994, pp.2525-2529.

[9] "DMILL, A Mixed Analog-Digital Radiation-Hard Technology for High Energy Physics Electronics", M. Dentan et al., R. Truche et al., O. Flament et al., L. Blanquart et al., CERN/LERB/95-13/Project RD29 Status Report, march 1995.

[10] "DMILL, A Mixed Analog-Digital Radiation-Hard BiCMOS Technology for High Energy Physics Electronics", M. Dentan et al., R. Truche et al., O. Flament et al., L. Blanquart et al., CERN/LHCC/95-56/Proceedings of the 1st Workshop on Electronics for LHC Experiments, Lisbon, Oct. 1995.

[11] "DMILL, A Mixed Analog-Digital Radiation-Hard BiCMOS Technology for High Energy Physics Electronics", M. Dentan et al., R. Truche et al., O. Flament et al., IEEE Transaction on Nuclear Sciences, june 1996, vol.43, part.II, pp.1763-1767.

[12] "DMILL, a mixed Analog-Digital Rad Hard Technology", T. Corbiere, Proceedings of the 2nd Workshop on Electronics for LHC experiments, Balatonfüred, September 1996, pp.404-406.

[13] "Reevaluation of radiation hardness assurance methodology for qualification of electronics devoted to LHC applications", O. Flament et al., Proceedings of the 2nd Workshop on Electronics for LHC experiments, Balatonfüred, September 1996, pp.420-424.

[14] "DMILL, A Mixed Analog-Digital Radiation-Hard Technology for High Energy Physics Electronics", M. Dentan et al., R. Truche et al., O. Flament et al., L. Blanquart et al., M.Carcaud et al., CERN/LERB/97-15/Project RD29 Status Report, march 1997.

[15] "Results of the Industrial Transfer of DMILL, a Rad-Hard Mixed Analog-Digital Technology for High Energy Physics Applications", M. Dentan et al., R. Truche et al., O. Flament et al., C. Le Mouellic et al., Proceedings of the 3rd Workshop on Electronics for LHC experiments, London, October 1997, pp.134-138.

[16] DMILL QUALPACK revision zero (October 1997). MHS document available at the MHS Quality Department.

[17] "Heavy Ion Sensitivity of a SRAM in SOI Bulk-like Technology", V. Ferlet-Cavrois et al., Proceedings of the 2nd European RADECs Conference, Saint-Malo, France, Sept. 1993, 0-7803-1793-9/$4.00.1994IEEE.

[18] "Comparison of the Sensitivity to Heavy Ions of SRAM's in Different SIMOX Technologies", V. Ferlet-Cavrois et al., IEEE Electron Device Letters, Vol.15, NO.3, March 1994.

[19] "Dynamic single event effects in a CMOS/thick SOI shift register", F. Gardic et al., L. Blanquart, Proceedings of RADECs 1995 Conference (Arcachon, France), IEEE 95TH8147, p333.

[20] "Test Results for Prototype Pixel Chips for ATLAS in DMILL Rad-Hard Technology", L. Blanquart et al., CERN/LHCC/95-56/Proceedings of the 1st Workshop on Electronics for LHC Experiments, Lisbon, Oct. 1995.

[21] "Pixel analog cell prototypes for ATLAS in DMILL technology", L. Blanquart et al., Nucl. Instr. and Meth. A 395 (3) (1997) 313-317.

[22] "MAREBO, a pixel chip for ATLAS designed in DMILL technology", L. Blanquart et al., Nucl. Instr. and Meth. A, in preparation.

[23] "MAREBO, a Full Radhard Pixel Detector Prototype for ATLAS", L. Blanquart et al., Proceedings of the 4rd Workshop on Electronics for LHC Experiments, Rome, Sept. 1998.

[24] "MAREBO is born", "MAREBO works", L. Blanquart, http ://marpix1.in2p3.fr/Pixel/analog/PAPER/elecpaper.html.

[25] "Development of Front-End Electronics for Silicon Strip Detectors using the DMILL BiCMOS Rad-Hard Process", F. Anghinolfi et al., Proceedings of the 2nd Workshop on Electronics for LHC experiments, Balatonfüred, September 1996, pp.483-487.

[26] "SCTA - A Rad-Hard BiCMOS Analogue Readout ASIC for the ATLAS Semiconductor Tracker", F. Anghinolfi et al., IEEE Transactions on Nuclear Science, Vol. 44, NO. 3, June 97, pp. 298-302.

[27] "A Single chip Implementation of the Binary Readout Architecture for Silicon Strip Detectors in the ATLAS Silicon Tracker", W. Dabrowski et al., A. Grillo et al., Proceedings of the 3rd Workshop on Electronics for LHC Experiments, London, Oct. 1997 / CERN/LHCCL97-60.

[28] "Performance of the Binary Readout of Silicon Strip Detectors Using the Radiation Hard SCT128B Chip" , W. Dabrowski et al., IEEE Transactions on Nuclear Science, Vol. 45, NO. 3, June 98, pp. 310-314.

[29] "The ABCD Binary Readout Chip for Silicon Strip Detectors in the ATLAS Silicon Tracker", W. Dabrowski et al., Proceedings of the 4rd Workshop on Electronics for LHC Experiments, Rome, Sept. 1998.

[30] "DMILL Implementations of the analogue readout architecture for position sensitive detectors at LHC experiments", W. Dabrowski et al., Proceedings of the 4rd Workshop on Electronics for LHC Experiments, Rome, Sept. 1998.

[31] "The Front-end Board for the ATLAS Liquid Argon Calorimeters", E. Delagnes, D. Breton, W. Sippach, J. Pinfold et al., Proceedings of the 4rd Workshop on Electronics for LHC Experiments, Rome, Sept. 1998.

[32] "Pixel Detector at LHC", R. Horisberger et al., Nuclear Instruments and Methods A 384 (1996) pp. 185-191.

[33] "Design Requirements and first results of an LHC adequate analog block for the CMS pixel detector", R. Horisberger et al., Nuclear Instruments and Methods A 7005 (1997).

[34] "Front-End Electronics for the CMS Pixel Detector", R. Baur et al., Proceedings of the 4rd Workshop on Electronics for LHC Experiments, Rome, Sept. 1998.

[35] The Tracker Project Technical Design Report, CERN/LHCC 98-6, CMS TDR 5, 15 April 1998, Chapter 2.4, pp.27-63.

[36] "Design and Performances of a BiCMOS Transimpedance Amplifier for Microstrip Detector Readout Using DMILL Process", Y. Hu et al., Proceedings of the 2nd Workshop on Electronics for LHC experiments, Balatonfüred, September 1996, pp. 488-491.

[37] "Design and Performances of a Low-Noise, Low-Power Consumption CMOS Charge Amplifier for Capacitive Detectors", Y. Hu et al., IEEE Transaction on Nuclear Science, Vol.45, N°1, February 1998, pp.119-123.

[38] "Design of a High Performance, Low-noise Charge Preamplifier with DC Coupling to Silicon Detectors in CMOS Technology", Y .Hu et al., Proceedings of the 4rd Workshop on Electronics for LHC Experiments, Rome, Sept. 1998.

[39] "Design and Preliminary Results of APVD : a Fast, Low-Noise, Low-Power Rad-Hard CMOS Mixed Circuit for the CMS Silicon Tracker at LHC", R. Turchetta et al., P. Schmitt et al., S. Gardien et al., M. French et al., Proceedings of the SPIE's International Symposium on Optical Science, Engineering and Instrumentation, Conference. San-Diego, USA, July 1998.

[40] "APVD : a CMOS Mixed Analog-Digital Circuit for the Silicon Tracker in CMS", R. Turchetta et al., P. Schmitt et al., S. Gardien et al., M. French et al., Proceedings of the 3rd Workshop on Electronics for LHC Experiments, London, Oct. 1997 / CERN/LHCCL97-60.

[41] "APVD : Fast Low-Noise Low-Power Rad-Hard CMOS Mixed Analogue-Digital Circuit for the CMS Silicon Tracker at LHC, Design and Experimental Results", R. Turchetta et al., P. Schmitt et al., S. Gardien et al., M. French et al., Proceedings of the 4rd Workshop on Electronics for LHC Experiments, Rome, Sept. 1998.

[42] "FILTRES : a 128 Channels VLSI Mixed Front-End Readout electronic development for Microstrip Detectors", J. Michel et al., Nuclear Instruments and Methods in Physics Research, Section A 412 (1998), pp. 123-134.

[43] "Analog Signal Processing for the CMS Electromagnetic Calorimeter", J-P. Walder et al., Proceedings of the 4rd Workshop on Electronics for LHC Experiments, Rome, Sept. 1998.

[44] "A Radiation-Hard 80 MHz Clock and Data Recovery Circuit for LHC", T. Toifl et al., Proceedings of the 4rd Workshop on Electronics for LHC Experiments, Rome, Sept. 1998.

[45] "A 4-Channels Rad-Hard Delay Generator ASIC with 1 ns Minimum Time Step for LHC Experiments", T. Toifl et al., Proceedings of the 4rd Workshop on Electronics for LHC Experiments, Rome, Sept. 1998.